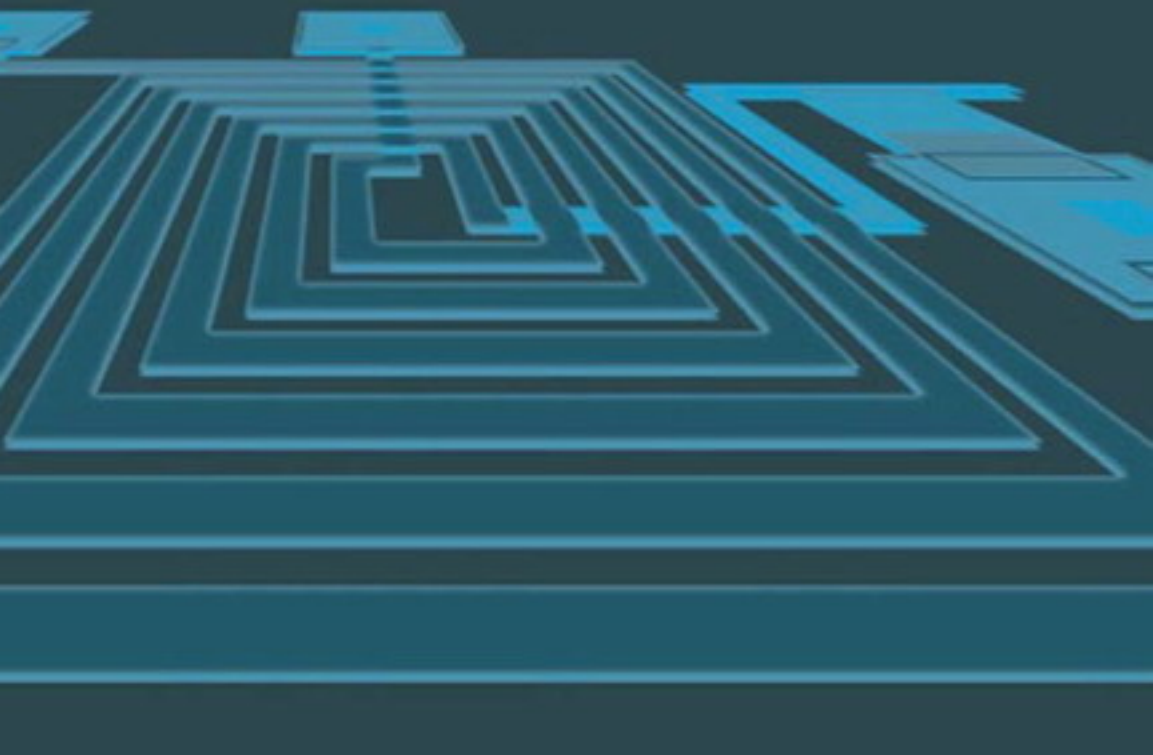
Inder Bahl

Lumped Elements for RF and Microwave Circuits



Lumped Elements for RF and Microwave Circuits

For a listing of recent titles in the *Artech House Microwave Library,*
turn to the back of this book.

Lumped Elements for RF and Microwave Circuits

Inder Bahl

Artech House
Boston • London
www.artechhouse.com

Library of Congress Cataloging-in-Publication Data
Bahl, I. J.
Lumped elements for RF and microwave circuits / Inder Bahl.
p. cm. — (Artech House microwave library)
Includes bibliographical references and index.
ISBN 1-58053-309-4 (alk. paper)
1. Lumped elements (Electronics) 2. Microwave integrated circuits. 3. Radio frequency integrated circuits. 4. Passive components. I. Title. II. Series.
TK7874.54.B34 2003
621.381'32—dc21 2003048102

British Library Cataloguing in Publication Data
Bahl, I. J. (Inder Jit)
Lumped elements for RF and microwave circuits. — (Artech House microwave library)
1. Radio circuits 2. Microwave circuits I. Title
621.3'8412

ISBN 1-58053-309-4

Cover design by Igor Valdman

685 Canton Street
Norwood, MA 02062

International Standard Book Number: 1-58053-309-4
Library of Congress Catalog Card Number: 2003048102

10 9 8 7 6 5 4 3 2 1

To my adorable grandsons, Karan and Rohan Kaushal, with whom I play, cry, and laugh, and who have provided me with the idea and inspiration to write this book

Contents

Preface

During the last decade, stimulated by unprecedented growth in the wireless communication application, outstanding progress has been made in the development of low-cost solutions for front-end RF and microwave systems. Lumped elements such as inductors, capacitors, and resistors have played a vital role in the development of such low-cost circuits. Numerous articles on the subject of lumped elements are scattered in a wide array of technical journals and conference proceedings; however, no comprehensive text dedicated to this topic exists. There is an urgent need for a book on this subject to fill the void.

This book deals with comprehensive treatment of RF and microwave circuit elements, including inductors, capacitors, resistors, transformers, via holes, airbridges, and crossovers. The topics discussed include materials, fabrication, analyses, design, modeling, and physical, electrical, and thermal practical considerations. The elements of the book are self-contained and cover practical aspects in detail, which generally are not readily available. This book also includes extensive design information in the form of equations, tables, and figures.

The unique features of this book include an in-depth study of lumped elements, extensive design equations and figures, the treatment of the practical aspect of lumped elements, and a description of fabrication technologies. The purpose of this book is to present a complete and up-to-date body of knowledge on lumped elements. The topics dealing with lumped elements are divided into 14 chapters.

The lumped elements are introduced in Chapter 1. This chapter describes the basic design of lumped elements and their modeling, fabrication, and applications. Chapter 2 deals with basics of inductors. It provides basic definitions, inductor configurations, inductor models, coupling between inductors, and electrical representations.

The printed inductors are covered in Chapter 3. The realization of inductors on several different substrates are treated. These include inductors on Si, GaAs, printed circuit board, and hybrid integrated circuit substrates. Wire inductors are the subject of Chapter 4. Analysis and design of wire-wound and bond wire inductors are discussed. A brief description of magnetic materials is also included.

Capacitors, including discrete, MIM, and interdigital, are described in Chapters 5, 6, and 7, respectively. The basic definition of capacitor parameters, chip capacitor types, the analysis of parallel plate capacitors, voltage and current ratings, and the electrical representation of capacitors are included in Chapter 5. Monolithic capacitors are treated in Chapter 6. Equivalent circuit models of capacitors, high-density capacitors, and capacitor shapes are discussed in this chapter. The treatment of interdigital capacitors is included in Chapter 7, describing its equivalent circuit models, design considerations, and applications.

Chapters 8, 9, and 10 deal with lumped resistors, via holes, and airbridge/dielectric crossovers, respectively. The basic definitions of resistor parameters, resistor types, high-power resistors, resistor equivalent circuit models, and resistor-circuit representations are included in Chapter 8. The effective conductivity of resistor materials and thermistor as an application of a resistor are discussed. Chapter 9 deals with via hole connection and via hole ground. The analysis and equivalent circuit models and design considerations, including coupling and layout of via holes, are described. Types of airbridge and crossover, analysis techniques, equivalent circuit models, and design consideration are discussed in Chapter 10.

The applications of lumped elements including transformers, baluns, and other passive circuits are treated in Chapters 11 and 12. The basic theory of transformers, wire wrapped, transmission line transformers, and ferrite transformers are discussed in Chapter 11. This chapter also describes parallel conductor transformers on Si substrate and spiral transformers on GaAs substrate. Passive lumped element circuits are discussed in Chapter 12. The circuit types include filters, hybrids, dividers, matching networks, biasing networks, switches, phase shifters, and attenuators.

Chapter 13 deals with fabrication technologies for lumped elements, including materials, salient features of fabrication, and examples. The fabrication technologies discussed are printed circuit board, microwave printed circuit, hybrid microwave integrated circuit, monolithic microwave integrated circuit, monolithic integrated CMOS, and micromachining.

The microstrip overview is given in Chapter 14 in order to make this book self-contained. The topics discussed are design equations, design considerations, thermal design, coupled lines, and discontinuities. The appendix is included to facilitate readers in their designs. I hope that the selection of topics and their presentation will meet the expectations of the readers.

Acknowledgments

As with any comprehensive treatment of a topic, one must draw upon the works of a large number of researchers and authors. I want to express my appreciation to their work and a number of publishing houses for copyright permissions for figures and other material from their work.

I am also indebted to Professor K. C. Gupta, who introduced me to the wonderful field of microwaves and antennas. He also critically reviewed the complete manuscript and made excellent suggestions to greatly enhance the text. Many friends and colleagues, at M/A-COM and elsewhere, have significantly contributed in the improvements of this book, through reading parts of the manuscript or the complete manuscript. I particularly want to thank Ken Puglia, Dr. Prakash Bhartia, Dr. Sanjay Raman, Dr. Arvind Sharma, Dr. Edward Griffin, Dr. Dain Miller, Chip Hudgins, and Sandy Martin for their support. I owe a special note of thanks to Linda Blankenship and Doris Cox for their support in expertly transforming my handwritten text into word-processing documents.

The preparation of this book has depended on my organization and a number of very supportive individuals. I would like to thank M/A-COM management for its support and encouragement.

The Artech House team did an excellent job on the final book. I would like to thank Mark Walsh, Barbara Lovenvirth, Judi Stone, and Rebecca Allendorf for their patience, support, and cooperation.

Finally, and most importantly, I want to express my deep appreciation to my wife, Subhash Bahl, for her encouragement, enduring unselfishness, and support. Her patience allowed me to work during many evenings, holidays, and weekends to complete this gigantic task. I especially wish to thank my daughter Preeti, son-in-law Ashutosh, son Puneet, and grandsons Karan and Rohan for their love, support, and patience.

1

Introduction

A lumped element in microwave circuits is defined as a passive component whose size across any dimension is much smaller than the operating wavelength so that there is no appreciable phase shift between the input and output terminals. Generally, keeping the maximum dimension less than $\lambda/20$ is a good approximation where λ is the guide wavelength. Lumped elements for use at RF and microwave frequencies are designed on the basis of this consideration. RF and microwave circuits use three basic lumped-element building blocks; capacitors, inductors and resistors. Lumped inductor transformers and baluns are also commonly used in many circuits.

1.1 History of Lumped Elements

Lumped elements (LEs) came into existence for possible use in *microwave integrated circuits* (MICs) almost four decades ago. The first usage of lumped elements was reported in 1965 [1]. During the late 1960s and early 1970s, several papers [2–9] describing the design, measurement, and application of LEs were published. During that time, the primary purpose was to reduce the size of MICs at the low end of the microwave frequency band. At L- and S-band frequencies, MIC technology using a distributed circuit approach (e.g., microstrip) occupies a lot of space. During the 1970s and early 1980s, tremendous progress was made using LEs for MICs at operating frequencies as high as 12 GHz [10–12]. During the advent of *monolithic microwave integrated circuits* (MMICs) in 1976, LEs became an integral part of microwave circuit design [13–28]. The emergence of wireless and mobile applications along with increased phased-array applications have provided additional incentives to use

LEs to develop compact and lower cost active and passive RF and microwave circuits [29]. Figure 1.1 shows the basic lumped elements used in MMICs. Also shown are via holes and dielectric crossovers, which are integral parts of these elements.

1.2 Why Use Lumped Elements for RF and Microwave Circuits?

Although lumped-element circuits typically exhibit a lower quality factor Q than distributed circuits due to smaller element dimensions and the multilevel fabrication process, they have the advantage of smaller size, lower cost, and wider bandwidth characteristics. These characteristics are especially suitable for monolithic MICs and for broadband hybrid MICs where small size requirements are of prime importance. Impedance transformations of the order of 20:1 can be accomplished easily using the lumped-element approach. Therefore, high-power devices with very low input and output impedance values can be matched to 50Ω easily with large impedance transformers using lumped elements. Because lumped elements are by definition much smaller than the wavelength, coupling effects between them when they are placed in proximity are smaller than those of distributed elements. In LE-based compact circuits, amplitude and phase variations are smaller due to smaller phase delays. This feature helps further in realizing high-performance compact circuits.

Currently MMIC technologies have reached a mature stage; lumped elements working at up to even 30 GHz are more suitable for low-cost circuit solutions. At frequencies below C-band, MMICs using lumped inductors and capacitors are an order of magnitude smaller than ICs using distributed elements fabricated in microstrip or *coplanar waveguide* (CPW). At RF and the low end of the microwave band, the use of lumped elements makes the chip size significantly smaller without affecting the RF performance, increases the number of chips per wafer, and gives improved visual and RF yields. All of these factors can reduce chip costs drastically.

Another advantage of using lumped elements in RF and microwave circuits lies in the fact that several design techniques used in circuits at lower RF frequencies, which are not practical at microwave frequencies using microstrip, coaxial, or waveguide transmission media, can now be successfully applied up to X-band frequencies. The circuit configurations include true lowpass and highpass filters; Gilbert-cell mixers; Colpitts, Pierce, Hartley, Clapp, and multivibrator-type oscillators; differential, push-pull, and feedback amplifiers; high-voltage and phase-splitting amplifiers; direct-coupled amplifiers; bridged T-coil amplifiers; and series and shunt gain peaked broadband amplifiers.

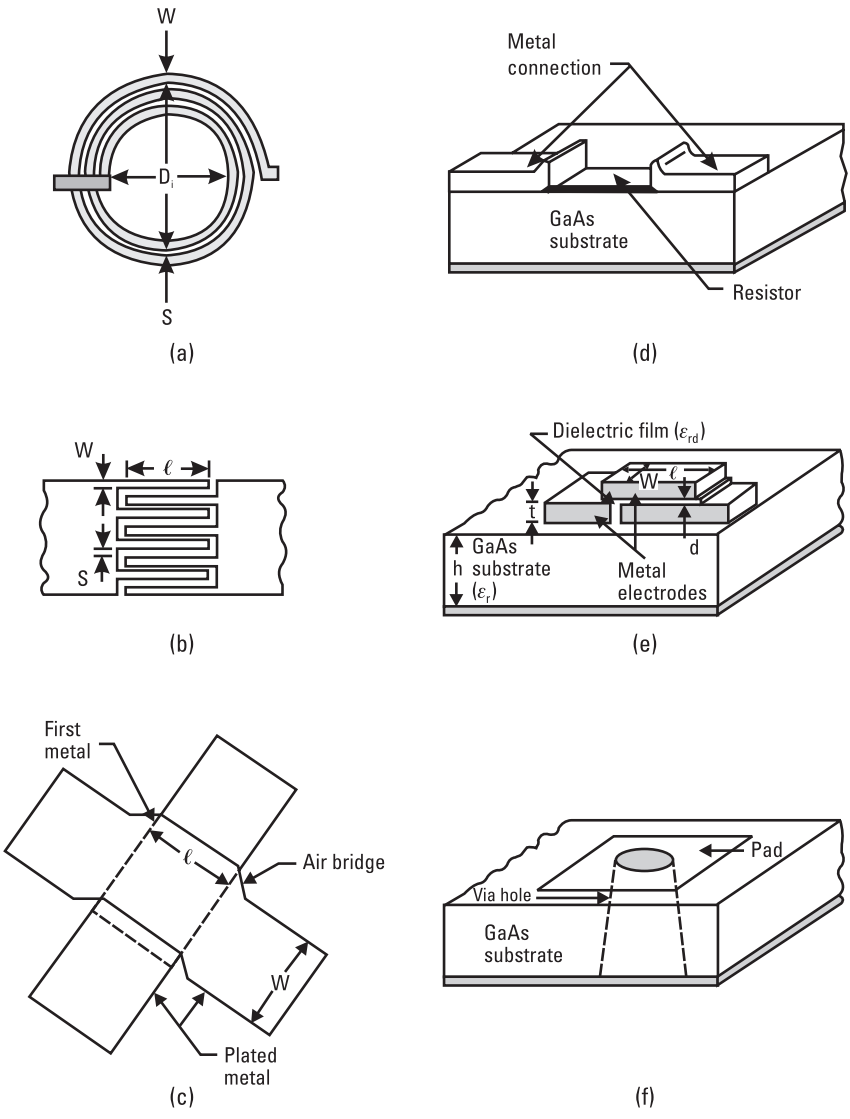


Figure 1.1 MMIC circuits use passive lumped elements: (a) spiral inductor, (b) interdigital capacitor, (c) airbridge crossover, (d) thin-film resistor, (e) MIM capacitor, and (f) via hole.

In broadband applications, lumped elements play a significant role in achieving the required circuit performance. To tune out the active device capacitance, one needs an inductance with the minimum possible parasitic capacitance. At microwave frequencies, one generally uses high-impedance lines, which are inductive in nature. However, these lines have associated shunt capacitance, which reduces the gain-bandwidth product of the circuit. For example, a 12-μm-wide microstrip conductor on a 75-μm-thick GaAs substrate requires a 1,160-μm-long line to realize an inductance value of 0.8 nH. The associated shunt capacitance value is about 0.13 pF. On the other hand, a lumped-element inductor with a 12-μm width and 2.5 turns will result in 0.8 nH of inductance and only 0.04 pF of shunt capacitance. Therefore, using lumped inductors with much lower parasitic capacitance will result in wider bandwidth circuits.

RF chokes using lumped inductors have a distinct advantage in terms of size and bandwidth in comparison to the $\lambda/4$ line transformers commonly used in microwave circuits to bring bias to active or passive solid-state devices. For example, a compact inductor having 5-nH value and a series resonant frequency above 20 GHz can be used as a RF choke from 5 to 20 GHz, whereas one needs two to three sections of $\lambda/4$ transformers to realize the same bandwidth.

In summary, LEs in comparison to conventional distributed elements have smaller size and lower cost, large impedance transformation ratio capability, smaller interaction effects between circuit elements, lower associated complementary reactance, and wider bandwidth capability.

1.3 *L, C, R* Circuit Elements

In this section brief descriptions of an inductor (L), a capacitor (C), and a resistor (R) and their basic functions are provided. Mathematical relations between the terminal voltage and current across these circuit elements as shown in Figure 1.2 are also included. In this discussion we will consider these elements as ideal; that is, *L, C, R* represent a pure and linear inductor, capacitor, and resistor, respectively.

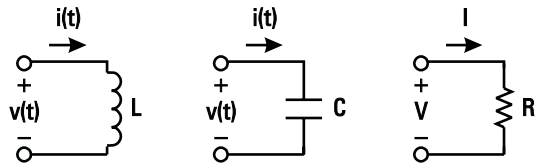


Figure 1.2 Two-terminal voltage and current representations of lumped inductor, capacitor and resistor.

An ideal inductor of inductance L stores or releases magnetic energy W_m, and does not store electric energy. This component also does not dissipate any power and the phase of the time-varying electric current $i(t)$ lags the phase of the voltage $v(t)$ across its terminals. Mathematically,

$$v(t) = L\frac{di(t)}{dt}, \qquad v = j\omega Li \tag{1.1a}$$

$$i(t) = \frac{1}{L}\int v(t)\ dt, \qquad i = \frac{v}{j\omega L} \tag{1.1b}$$

$$W_m = \frac{1}{2}Li_0^2 \tag{1.1c}$$

where the time dependence is assumed as $e^{j\omega t}$ and i_0 is the root mean square (rms) value of the current.

In an ideal capacitor of capacitance C, the stored or released energy is only of electric type W_e and such components do not dissipate any power. In a capacitor the phase of the electric current $i(t)$ leads the phase of the voltage $v(t)$ and the relationships between v and i are expressed as follows:

$$i(t) = C\frac{dv(t)}{dt}, \qquad i = j\omega Cv \tag{1.2a}$$

$$v(t) = \frac{1}{C}\int i(t)\ dt \tag{1.2b}$$

$$W_e = \frac{1}{2}Cv_0^2 \tag{1.2c}$$

where v_0 is the rms value of the voltage.

A lossy component, when its dimensions are much less than the operating wavelength, is considered a linear resistor. In such a component, the voltage and current across its terminals are in phase and the incident power is completely dissipated. If V and I are the rms voltage and current across a resistor of value R, then by Ohm's law

$$V = RI \tag{1.3}$$

The power dissipated P is given by

$$P = VI = RI^2 = \frac{V^2}{R} \tag{1.4}$$

1.4 Basic Design of Lumped Elements

Lumped elements at RF and microwave frequencies are designed based on small sections of TEM lines such as microstrip lines, which are much smaller than the operating wavelength. Consider a uniform transmission line with series resistance ($\overline{R}$), series inductance ($\overline{L}$), shunt conductance ($\overline{G}$), and shunt capacitance ($\overline{C}$), all defined per unit length of the line as shown in Figure 1.3. In this case the total length ℓ is divided into small sections of length $\Delta\ell << \lambda$. From transmission line theory, the driving point or input impedance Z_{in} of the line of length ℓ and terminated in an impedance Z_L at the output as shown in Figure 1.4, is given by

$$Z_{\text{in}} = Z_0 \frac{Z_L \cosh(\gamma\ell) + Z_0 \sinh(\gamma\ell)}{Z_0 \cosh(\gamma\ell) + Z_L \sinh(\gamma\ell)} \tag{1.5}$$

where Z_0 is known as the characteristic impedance and γ is the propagation constant of the transmission line. These quantities are expressed as

$$Z_0 = \sqrt{\frac{\overline{R} + j\omega\overline{L}}{\overline{G} + j\omega\overline{C}}} \tag{1.6}$$

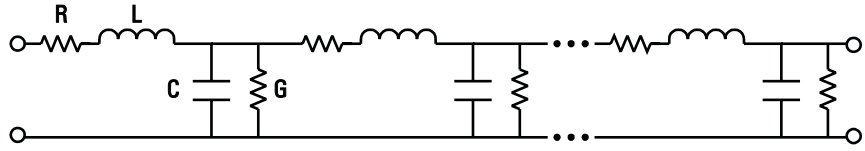


Figure 1.3 Lumped circuit representation of a transmission line.

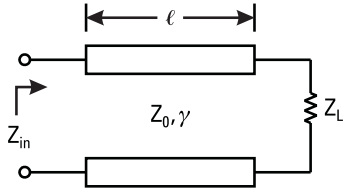


Figure 1.4 Input impedance of a transmission line terminated in load Z_L.

$$\gamma = \sqrt{\left(\overline{R} + j\omega\overline{L}\right)\left(\overline{G} + j\omega\overline{C}\right)} = \alpha + j\beta \tag{1.7}$$

where α and β are the attenuation and phase constants, respectively. When the line length is very small, $\gamma\ell << 1$, Z_{in} may be written as

$$Z_{\text{in}} = Z_0 \frac{Z_L + Z_0\,\gamma\ell}{Z_0 + Z_L\,\gamma\ell} \tag{1.8}$$

For a lossless case, $\overline{R} = \overline{G} = 0$

$$Z_0 = \sqrt{\frac{\overline{L}}{\overline{C}}} \text{ and } \gamma = j\beta = j\omega\sqrt{\overline{LC}} \tag{1.9}$$

Next we discuss the realization of various lumped elements using (1.5).

1.4.1 Capacitor

A lumped capacitor may be realized by using an open-circuited ($Z_L = \infty$) microstrip section. In this case (1.5) becomes

$$Z_{\text{in}} \cong \frac{Z_0}{\tanh(\gamma\ell)} \cong \frac{Z_0}{\gamma\ell - \frac{1}{3}(\gamma\ell)^3 + \ldots} \tag{1.10}$$

When $\gamma\ell << 1$,

$$Z_{\text{in}} \cong \frac{Z_0}{\gamma\ell} + \frac{Z_0\,\gamma\ell}{3} \tag{1.11}$$

From (1.6) and (1.7), and $\overline{G} << \omega\overline{C}$

$$Z_{\text{in}} \cong \frac{\overline{G}}{(\omega\overline{C})^2\ell} + \frac{\overline{R}\ell}{3} + \frac{1}{j\omega\overline{C}\ell} + \frac{j\omega\overline{L}\ell}{3} \tag{1.12}$$

Neglecting the inductor parasitic,

$$Z_{\text{in}} \cong \frac{G}{(\omega C)^2} + \frac{R}{3} + \frac{1}{j\omega C} \tag{1.13}$$

where *G, R, C* are the total conductance, resistance, and capacitance of the microstrip section. The equivalent circuit of the open-circuited stub is shown

in Figure 1.5, where $G/(\omega C)^2$ and $R/3$ represent the dielectric and conductor loss, respectively.

Equation (1.13) also provides another interesting conclusion: For any open-circuited line, the conductive resistance is only one-third of the total resistance measured between input and output. This is why in *metal semiconductor field-effect transistors* (MESFETs) or *high electron mobility transistors* (HEMTs), the RF gate resistance is taken as one-third of the end-to-end gate finger resistance.

1.4.2 Inductor

The input impedance of a small section ($\gamma\ell << 1$) short-circuited ($Z_L = 0$) line is expressed as

$$Z_{\text{in}} = Z_0 \tanh(\gamma\ell) \cong Z_0 \gamma\ell = R + j\omega L \tag{1.14}$$

Thus a small-length short-circuited transmission line behaves as an inductor in series with a resistor R as shown in Figure 1.6. The resistance R represents the conductor loss, which is negligible for short sections of copper or gold conductors.

1.4.3 Resistor

As discussed earlier, the short-circuited transmission line behaves as an inductor when the conductors have low resistance. However, when a section of good

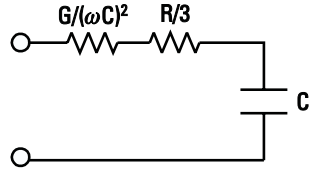


Figure 1.5 Capacitor-resistor representation of a short open-circuited transmission line section.

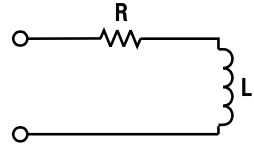


Figure 1.6 Inductor-resistor representation of a small-length short-circuited transmission line section.

conductor is replaced with thin lossy conductor such as NiCr (sheet resistance $\cong 20\Omega$/square compared to 0.005Ω/square for gold), the resistive part becomes dominant and the microstrip section behaves as a resistor with negligible parasitic inductive and capacitive reactances.

1.5 Lumped-Element Modeling

An ideal lumped element is not realizable even at lower microwave frequencies because of the associated parasitic reactances due to fringing fields. At RF and microwave frequencies, each component has associated electric and magnetic fields and finite dissipative loss. Thus, such components store or release electric and magnetic energies across them and their resistance accounts for the dissipated power. The relative values of the *C, L,* and *R* components in these elements depend on the intended use of the LE. To describe their electrical behavior, equivalent circuit models for such components are commonly used. Lumped-element *equivalent circuit* (EC) models consist of basic circuit elements (*L, C,* or *R*) with the associated parasitics denoted by subscripts. Accurate computer-aided design of MICs and MMICs requires a complete and accurate characterization of these components. This requires comprehensive models including the effect of ground plane, fringing fields, proximity effects, substrate material and thickness, conductor thickness, and associated mounting techniques and applications. Thus, an EC representation of a lumped element with its parasitics and their frequency-dependent characteristics is essential for accurate element modeling. An EC model consists of the circuit elements necessary to fully describe its response, including resonances, if any. Models can be developed using analytical, electromagnetic simulation, and measurement based methods.

The early models of lumped elements were developed using analytical semiempirical equations. In 1943, Terman [30] published an expression for the inductance of a thin metallic straight line that was later improved by Caulton et al. [3], who added the effect of metallization thickness. Wheeler [31] presented an approximate formula for the inductance of a circular spiral inductor with reasonably good accuracy at lower microwave frequencies. This formula has been extensively used in the design of microwave lumped circuits. Grover [32] has discussed inductance calculations for several geometries. The theoretical modeling of microstrip inductors for MICs has usually been based on two methods: the lumped-element approach and the coupled-line approach. The lumped-element approach uses formulas for free-space inductance with ground plane effects. These frequency-independent formulas are useful only when the total length of the inductor is a small fraction of the operating wavelength and when interturn capacitance can be ignored. In the coupled-line approach, an inductor is analyzed using multiconductor coupled microstrip lines. This

technique predicts the spiral inductor's performance reasonably well for two turns and up to about 18 GHz.

An earlier theory for the interdigital capacitor was published by Alley [4], and Joshi et al. [33] presented modified formulas for these capacitors. Mondal [34] reported a distributed model of the MIM capacitor based on the coupled-line approach. Pengelly et al. [35, 36] presented the first extensive results on different lumped elements on GaAs, including inductors and interdigital capacitors, with special emphasis on the Q-factor. Pettenpaul et al. [37] reported lumped-element models using numerical solutions along with basic microstrip theory and network analysis. In general, analytical models are good for estimating the electrical performance of lumped elements.

The realization of lumped *L, C, R* elements at microwave frequencies is possible by keeping the component size much smaller than the operating wavelength. However, when the component size becomes greater than $\lambda/10$, these components have undesirable associated parasitics such as resistance, capacitance, and inductance. At RF and higher frequencies, the reactances of the parasitics become more significant, with increasing frequency resulting in higher loss and spurious resonances. Thus, empirical expressions are not accurate enough to predict LE performance accurately. Once lumped elements are accurately characterized either by *electromagnetic* (EM) simulation or measurements, the parasitic reactances become an integral part of the component and their effects can be included in the design.

Recent advances in workstation computing power and user-friendly software make it possible to develop EM field simulators [38–43]. These simulators play a significant role in the simulation of single and multilayer passive circuit elements such as transmission lines and their discontinuities; patches; multilayer components, namely, inductors, capacitors, resistors, via holes, airbridges, inductor transformers, packages, and so on; and passive coupling between various circuit elements. Accurate evaluation of the effects of radiation, surface waves and interaction between components on the performance of densely packed MMICs can only be calculated using *three-dimensional* (3-D) EM simulators.

The most commonly used method of developing accurate models for lumped elements is by measuring dc resistance and S-parameter data. This modeling approach gives quick and accurate results, although the results are generally limited to just the devices measured. EC model parameters are extracted by computer optimization, which correlates the measured dc and S-parameter data (one- or two-port data) up to 26 or 40 GHz depending on the application. The accuracy of the model parameter values can be as good as the measurement accuracy by using recently developed on-wafer calibration standards and techniques [44]. The equivalent circuit models are valid mostly up to the first parallel resonant frequency f_{res}. However, when a design is involved with harmonics, for example, a power amplifier with second and third harmonic terminations at

the output, one requires either EM simulated data working up to the highest design frequency or a more complex model taking into account higher order resonances. If the operating frequency is lower than $f_{res}/3$, then the models discussed above are adequate.

At RF and microwave frequencies, the resistance of LEs is quite different from their dc values due to the skin effect. When an RF signal is applied across a LE, due to the finite conductivity of the conductor material, EM fields penetrate a conductor only a limited depth along its cross section. The distance in the conductor over which the fields decrease to $1/e$ (about 36.9%) of the values at the surface is called depth of penetration, or skin depth. This effect is a function of frequency with the penetration depth decreasing with increasing frequency. The flow of RF current is limited to the surface only, resulting in higher RF surface resistance than the dc value. This effect is taken into account during accurate modeling of the resistive loss in the component. Modeling of lumped elements is discussed in later chapters.

1.6 Fabrication

Various technologies are used to fabricate lumped elements, including printed circuit board, thin-film, thick-film, cofired ceramic, and MICs. At RF and microwave frequencies, printed circuit board technology is limited to inductors, whereas the other technologies can be used to make all lumped elements. In traditional MICs, active devices in addition to passive discrete components such as inductors, capacitors, and resistors are attached externally to an etched circuit on an alumina substrate. In contrast, in MMICs, all circuit components, active and passive, are fabricated simultaneously on a common semi-insulating semiconductor substrate. Therefore, by eliminating discrete components and bond wire interconnects, the monolithic technologies have the advantage of being well suited to high-volume production. Details of these technologies are given in Chapter 13. Discrete components are manufactured exclusively using thin- and thick-film techniques, whereas monolithic integrated components are commonly fabricated on GaAs and Si substrates. With the advent of new photolithographic techniques, the fabrication of lumped elements previously limited to X-band frequencies can now be extended to about 60 GHz.

Discrete lumped elements are produced on big sheets and then individually diced or cut. However, in MICs and MMICs the lumped elements are fabricated on dielectric substrates, such as alumina and GaAs. The main purpose of the substrate is to provide the needed physical support for these components and a fixed environment for accurate characterization. In this case the EM energy is confined to a very small area. Thus, the quality of the substrate material is not as critical as it is for distributed transmission lines. However, to keep the

dielectric loss due to fringing fields to a low value, substrate materials with small loss tangent values are preferred. For inductors, it is desirable to keep the resonant frequency high. For this purpose the interturn capacitance and the capacitance between the trace and ground plane may be kept to lower values by using low dielectric constant materials.

1.7 Applications

Lumped elements are widely used in RF and microwave circuits including couplers, filters, power dividers/combiners, impedance transformers, baluns, control circuits, mixers, multipliers, oscillators, and amplifiers. Most high-volume microwave applications are either served by MICs or MMICs or both used together. MMICs have significant benefits over MICs in terms of smaller size, lighter weight, improved performance, higher reliability, and, most importantly, lower cost in high-volume applications. The emergence of wireless and mobile applications along with increased phased-array applications is relentlessly driving efforts to reduce MMIC cost. LE-based circuit design using inductors, capacitors, and resistors is a key technique for reducing MMIC chip area, resulting in more chips per wafer and leading to lower costs.

Another application of spiral geometry is in printed antennas for wireless communication; such structures can result in a small, low-profile, conformal antenna [45]. Spiral antennas are very suitable for handsets for mobile communication due to their ultrasmall size compared to patch antennas.

Depending on the frequency of operation, passive components for RF, microwave, and millimeter wave applications may be realized using a combination of solid-state devices, lumped elements, distributed elements, and quasioptical elements. Unless there is a need for special requirements for circuit realization in a particular band, commonly used circuit elements in the RF through millimeter wave frequency spectrum are shown in Figure 1.7.

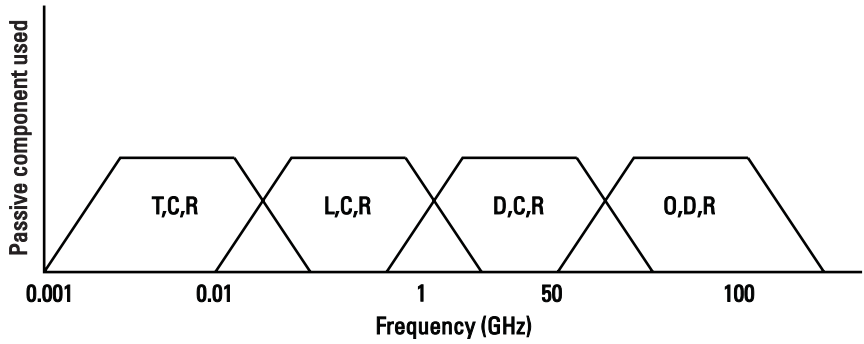


Figure 1.7 Realization of passive components using transistors (*T*), lumped elements (*L, C, R*), distributed elements (*D*), and quasioptical elements (*O*).

References

[1] Vincent, B. T., "Microwave Transistor Amplifier Design," *IEEE Microwave Symp. Dig.,* 1965, p. 815.

[2] Daly, D. A., et al., "Lumped Elements in Microwave Integrated Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-15, December 1967, pp. 713–721.

[3] Caulton, M., S. P. Knight, and D. A. Daly, "Hybrid Integrated Lumped-Element Microwave Amplifiers," *IEEE Trans. Electron Devices,* Vol. ED-15, July 1968, pp. 459–466.

[4] Alley, G. D., "Interdigital Capacitors and Their Application to Lumped-Element Microwave Integrated Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-18, December 1970, pp. 1028–1033.

[5] Caulton, M., et al., "Status of Lumped Elements in Microwave Integrated Circuits—Present and Future," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-19, July 1971, pp. 588–599.

[6] Coulton, M., "Film Technology in Microwave Integrated Circuits," *Proc. IEEE,* Vol. 59, Oct. 1971, pp. 1481–1489.

[7] Aitchison, C. S., et al., "Lumped Circuit Elements at Microwave Frequencies," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-19, Dec. 1971, pp. 928–937.

[8] Caulton, M., "Lumped Elements in Microwave Integrated Circuits," *Advances in Microwaves,* Vol. 8, L. Young and H. Sobol, (Eds.), New York: Academic Press, 1974.

[9] Chaddock, R. E., " The Application of Lumped Element Techniques to High Frequency Hybrid Integrated Circuits," *Radio Electron. Eng.,* Vol. 44, 1974, pp. 414–420.

[10] Gupta, K. C., "Lumped Elements for MICs," *Microwave Integrated Circuits,* K. C. Gupta and A. Singh, (Eds.), New Delhi, India: Wiley Eastern, 1974, Chap. 6.

[11] Gupta, K. C., *Microwaves,* New Delhi: Wiley Eastern, 1979, Chap. 11.

[12] Gupta, K. C., R. Garg, and R. Chadha, *Computer-Aided Design of Microwave Circuits,* Dedham, MA: Artech House, 1981, Chap. 7.

[13] Pengelly, R. S., and J. S. Turner, "Monolithic Broadband GaAs FET Amplifiers," *Electron. Lett.,* Vol. 12, May 1976, pp. 251–252.

[14] Pucel, R. A., "Design Considerations for Monolithic Microwave Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-29, June 1981, pp. 513–534.

[15] Esfandiari, R., D. Maki, and M. Siracusa, "Design of Interdigitated Capacitors and Their Application to GaAs Filters," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-31, January 1983, pp. 57–64.

[16] Podell, A., et al., "GaAs Real Estate Making the Most Efficient Use of Semiconductor Surface Area," *Microwave J.,* Vol. 30, November 1987, pp. 208–212.

[17] Bahl, I. J., and P. Bhartia, *Microwave Solid State Circuit Design,* New York: John Wiley, 1988; also 2nd ed., 2003.

[18] Goyal, R. (Ed.), *Monolithic Microwave Integrated Circuits: Technology and Design,* Norwood, MA: Artech House, 1989.

[19] Wadell, B. C., *Transmission Line Design Handbook,* Norwood, MA: Artech House, 1991.

[20] Fisher, D., and I. Bahl, *Gallium Arsenide IC Applications Handbook,* San Diego, CA: Academic Press, 1995.

[21] Goyal, R., *High-Frequency Analog Integrated Circuit Design,* New York: John Wiley, 1995.

[22] Gupta, K. C., et al., *Microstrip Lines and Slotlines,* 2nd ed., Norwood, MA: Artech House, 1996.

[23] Pozar, D. M., *Microwave Engineering,* 2nd ed., New York: John Wiley, 1998.

[24] Mongia, R., I. Bahl and P. Bhartia, *RF and Microwave Coupled-Line Circuits,* Norwood, MA: Artech House, 1999.

[25] Abrie, P. D., *Design of RF and Microwave Amplifiers and Oscillators,* Norwood, MA: Artech House, 1999.

[26] Weber, R. J., *Introduction to Microwave Circuits,* New York: IEEE Press, 2001.

[27] Chang, K., I. Bahl, and V. Nair, *RF and Microwave Circuit and Component Design for Wireless Systems,* New York: John Wiley, 2002.

[28] Kangaslahti, P., P. Alinikula, and V. Perra, "Miniature Artifical Transmission-Line Monolithic Millimeter-Wave Frequency Doubler," *IEEE Trans. Microwave Theory Tech.,* Vol. 48, April 2000, pp. 510–517.

[29] Lin, Y. H., and Y. J. Chan, "2.4 GHz Single-Balanced Diode Mixer Fabricated on Al2O3 Substrate by Thin-Film Technology," *Microwave Optical Tech. Lett.,* Vol. 25, April 2000, pp. 83–86.

[30] Terman, F. E., *Radio Engineers Handbook,* New York: McGraw-Hill, 1943, p. 51.

[31] Wheeler, H. A., " Simple Inductance Formulas for Radio Coils," *Proc. IRE,* Vol. 16, 1928, pp. 1398–1400.

[32] Grover, F. W., *Inductance Calculations: Working Formulas and Tables,* Princeton, NJ: Van Nostrand, 1946; reprinted by Dover Publications, 1962, pp. 17–47.

[33] Joshi, J. S., J. R. Cockrill, and J. A. Turner, "Monolithic Microwave Gallium Arsenide FET Oscillators," *IEEE Trans. Electron Devices,* Vol. ED-28, Feb. 1981, pp. 158–162.

[34] Mondal, J. P., "An Experimental Verification of a Simple Distributed Model of MIM Capacitors for MMIC Applications," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT 35, April 1987, pp. 403–407.

[35] Pengelly, R. S., and D. C. Rickard, "Measurement and Application of Lumped Elements Up to J-Band," *Proc. 7th European Microwave Conf.,* Copenhagen, 1977, pp. 460–464.

[36] Pengelly, R. S., "Monolithic GaAs IC's Tackle Analog Tasks," *Microwaves,* Vol. 18, July 1979, p. 56.

[37] Pettenpaul, E., et al., "CAD Models of Lumped Elements on GaAs Up to 18 GHz," *IEEE Trans. Microwave Theory Tech.,* Vol. 36, Feb. 1988, pp. 294–304.

[38] EM, Liverpool, NY: Sonnet Software.

[39] HFSS, Pittsburgh: ANSOFT Corp.

[40] High-Frequency Structure Simulator, Santa Rose, CA: Agilent.

[41] LIMMIC + Analysis Program, Ratingen, Germany: Jansen Microwave.

[42] MSC/EMAS, Milwaukee, WI: MacNeal Schwendler.

[43] IE3D, San Francisco: Zeland Software.

[44] Sadhir, V., I. Bahl, and D. Willems, "CAD Comparable Accurate Models for Microwave Passive Lumped Elements for MMIC Applications," *Int. J. Microwave and Millimeter Wave Computer-Aided Engineering,* Vol. 4, April 1994, pp. 148–162.

[45] Kan, H. K., and R. B. Waterhouse, "Shorted Spiral-Like Printed Antennas," *IEEE Trans. Antennas Propagation,* Vol. 50, March 2002, pp. 396–397.

2

Inductors

2.1 Introduction

Lumped-element design using inductors, capacitors, and resistors is a key technique for reducing MMIC chip area resulting in more chips per wafer and thus lower cost. Inductors used as circuit components, matching networks, and biasing chokes play a significant role in the realization of compact integrated chips. Below C-band frequencies, MMICs using lumped inductors are an order of magnitude smaller than ICs using distributed matching elements such as microstrip lines or coplanar waveguides.

Inductors can take the form of single or multiple bond wires, wire-bound chip inductors, or lumped inductors made using hybrid and MIC fabrication technologies. In the low-microwave-frequency monolithic approach, low-loss inductors are essential to develop compact low-cost, low-noise amplifiers and high-power-added-efficiency amplifiers. Chip inductors are invariably used as RF chokes at RF and low microwave frequencies.

Inductors in MICs are fabricated using standard integrated circuit processing without any additional process steps. The innermost turn of the inductor is connected to other circuitry using a wire bond connection in conventional hybrid MICs, or through a conductor that passes under airbridges in multilayer MIC and MMIC technologies. The width and thickness of the conductor determines the current-carrying capacity of the inductor. In MMICs the bottom conductor's thickness is typically 0.5 to 1.0 μm, and the airbridge separates it from the upper conductors by 1.5 to 3.0 μm. In a dielectric crossover technology, the separation between the conductor layers may be anywhere between 0.5 and 3.0 μm. Typical inductance values for MMICs working above L-band are in

the range of 0.5 to 20 nH, whereas chip inductors are presently available up to 400 nH.

Three chapters are devoted to inductors; this chapter deals with general information on inductors, analytical equations, methods of analysis, measurement techniques for modeling, and coupling between inductors. Chapters 3 and 4 deal with printed/monolithic and wire inductors, respectively.

2.2 Basic Definitions

First of all we define several terms that we come across in the design and usage of inductors [1–8].

2.2.1 Inductance

In electrical circuits, the effect of magnetic energy storage is represented by an inductance L, which is defined in terms of magnetic flux ψ by

$$L = \frac{1}{I}\oint_S B \cdot ds = \frac{\Psi}{I}$$

$$= \mu_0 \mu_r \frac{1}{I}\oint_\ell H \cdot dl \tag{2.1}$$

where

I = the current flowing through the conductor in amperes,

B = magnetic flux density expressed in tesla (T) or weber/m^2 = $\mu_0 \mu_r H$, where the magnetic field, H is expressed in amp/m,

S = surface area enclosed by the loop of wire of length ℓ.

For perfect conductors $\mu_r = 1$. Free-space permeability is $\mu_0 = 4\pi \times 10^{-7}$ H/m.

The current I produces magnetic flux in the area S bound by the loop as shown in Figure 2.1. In this case, L is also known as *self-inductance.* Figure 2.2 shows the magnetic flux lines in a coil.

2.2.2 Magnetic Energy

In an inductor, the magnetic energy is stored as long as the current keeps flowing through it and is given by

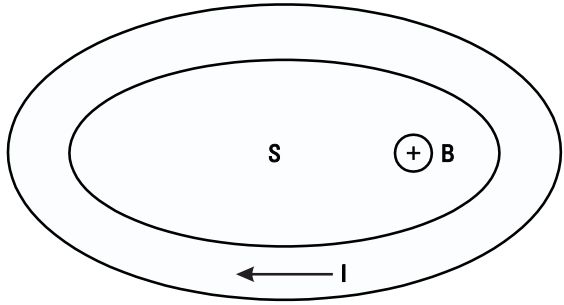


Figure 2.1 Loop wire configuration showing flux area *S*, current *I*, and magnetic flux *B*.

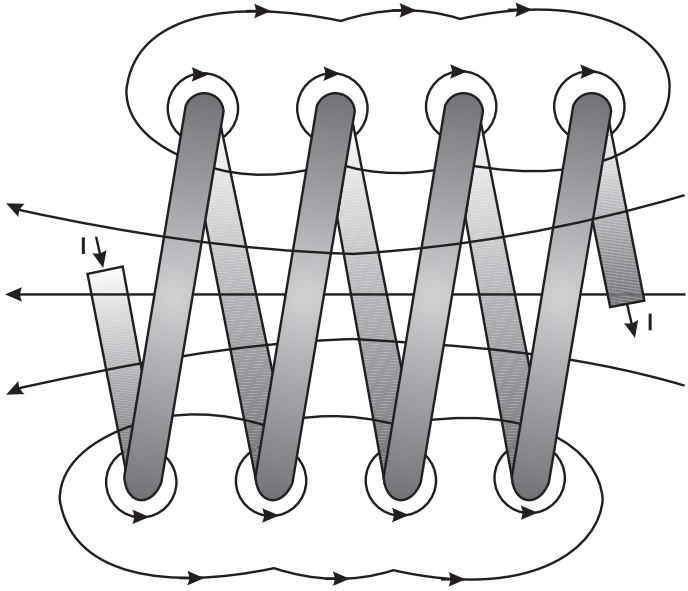


Figure 2.2 Magnetic flux lines in a coil.

$$W_m = \frac{LI^2}{2} \tag{2.2}$$

where:

W_m = magnetic energy expressed in Joules (W · s = J), W and s designate watt and second, respectively;

L = inductance in henrys (H);

I = current in amperes (A).

2.2.3 Mutual Inductance

When two conductors carrying current are in proximity, their magnetic flux lines interact with each other. If the currents flow in opposite directions, the inductance of each conductor is reduced. Currents flowing in the same direction increase each conductor's inductance. The change in an isolated conductor's inductance when in proximity to another conductor is known as their *mutual inductance*. Consider two conductors in parallel; the mutual inductance is defined by

$$M = L_m = \frac{L_a - L_o}{2} \tag{2.3}$$

where

$M = L_m$ = mutual inductance in henrys (H);

L_a = total inductance of the two conductors when the currents flow in the same direction;

L_o = total inductance of the two conductors when the currents flow in the opposite direction.

If L is the self-inductance of each conductor in the isolated case, then the total inductance of each conductor is given by

$$\begin{aligned} L_t &= L + M \quad \text{(currents flow in the same direction)} \\ &= L - M \quad \text{(currents flow in the opposite direction)} \end{aligned} \tag{2.4}$$

2.2.4 Effective Inductance

For chip inductors, the nominal inductance value is measured at low frequencies; however, the operating frequency range is much higher. Because the inductor has associated parasitic capacitance (due to interturn and ground plane effects) in parallel with its inductance as shown in Figure 2.3(a), the impedance of the inductor (neglecting series resistance) can be written as

$$Z_i = \frac{j\omega L \times \dfrac{1}{j\omega C_p}}{j\omega L + \dfrac{1}{j\omega C_p}} = \frac{j\omega L}{1 - \omega^2 L C_p} \tag{2.5a}$$

or

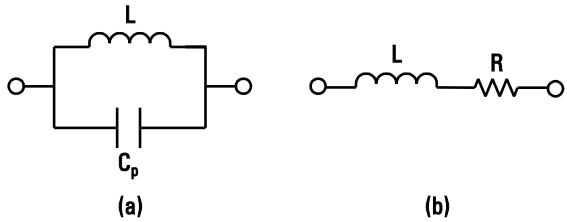


Figure 2.3 (a) Self-inductance in parallel with parasitic capacitance. (b) Series inductance-resistance representation.

$$Z_i = j\omega L_e \tag{2.5b}$$

where

$$L_e = \frac{L}{1 - (\omega/\omega_p)^2} \tag{2.5c}$$

Here $\omega_p \left(= 1/\sqrt{LC_p}\right)$ is the parallel resonant frequency. The equivalent inductance L_e is known as *effective inductance,* and below the first resonance its value is generally greater than the nominal specified value.

2.2.5 Impedance

The impedance of an inductor is defined as

$$Z_L = \frac{V}{I} = j\omega L \tag{2.6}$$

where $\omega = 2\pi f$ and f is the operating frequency in hertz (Hz). The preceding equation shows that the sinusoidal current in a perfect inductor lags the voltage by 90°.

2.2.6 Time Constant

When a dc voltage is applied across a series inductor-resistor combination as shown in Figure 2.3(b), the time required to charge the inductor to the applied voltage is known as the time constant τ and is given as

$$\tau = \frac{L}{R} \tag{2.7}$$

where τ, L, and R are expressed in seconds, henries, and ohms, respectively.

2.2.7 Quality Factor

Several different definitions of Q-factors for inductors have been used in the literature [9–18]. The most general definition of Q is based on ratio of energy stored, W_S, to power dissipated, P_D, in the inductor per cycle; that is

$$Q = \frac{\omega W_S}{P_D} \tag{2.8}$$

At low frequencies an inductor's primary reactance is inductive and

$$Q = \frac{\omega \frac{1}{2} L i_0^2}{\frac{1}{2} R i_0^2} = \frac{\omega L}{R} \tag{2.9}$$

where i_0 is the rms value of the current. When the inductor is used as a resonant component close to its *self-resonance frequency* (SRF) f_{res}, a more appropriate definition of the Q-factor is in terms of its 3-dB bandwidth (BW) is given by

$$Q = \frac{f_{\text{res}}}{\text{BW}} \tag{2.10}$$

A third definition of Q-factor, which has been used for distributed resonators, is evaluated from the rate of change of input reactance with frequency [19, 20]:

$$Q = \frac{f_{\text{res}}}{2R} \left[\frac{dX_{\text{in}}}{df} \right] \tag{2.11}$$

where X_{in} is the input reactance of the inductor and dX_{in}/df is determined at f_{res}.

In microwave circuits where the inductors are used far below the self-resonance frequency, the degree at which the inductor deviates from an ideal component is described by the effective quality factor Q_{eff}, expressed as [18]:

$$Q_{\text{eff}} = \frac{\text{Im}[Z_{\text{in}}]}{\text{Re}[Z_{\text{in}}]} = \frac{X}{R} = \frac{\omega L_e}{R} \tag{2.12}$$

where $\text{Re}[Z_{\text{in}}]$ and $\text{Im}[Z_{\text{in}}]$ are the real and imaginary parts of the input impedance of the inductor, respectively. This definition leads to the unusual

condition that Q_{eff} becomes zero at resonance. Since in RF and microwave circuits, for series applications of inductors, the operating frequencies are well below the self-resonance frequency, the preceding definition is traditionally accepted.

2.2.8 Self-Resonant Frequency

The self-resonant frequency (f_{res}) of an inductor is determined when $\text{Im}[Z_{\text{in}}] = 0$; that is, the inductive reactance and the parasitic capacitive reactance become equal and opposite in sign. At this point, $\text{Re}[Z_{\text{in}}]$ is maximum due to parallel resonance and the angle of Z_{in} changes sign. The inductor's first resonant frequency is of the parallel resonance type. Beyond the resonant frequency, the inductor becomes capacitive.

2.2.9 Maximum Current Rating

The maximum dc current an inductor can withstand without being destroyed (fusing or electromigration) or overheating due to its finite resistance is known as the *maximum current rating.* This maximum current limit depends on the conductor material, shape, core material used, surrounding environment, and temperature.

2.2.10 Maximum Power Rating

The maximum RF power that can be applied safely to an inductor without changing its characteristics or destroying it due to heat generated is known as the *maximum power rating.* The maximum power limit depends on the inductor's Q, area/volume, core material used, surrounding environment, and temperature. Printed inductors have higher maximum power ratings than air coil inductors.

2.2.11 Other Parameters

The reader must consider several other inductor parameters per design requirements. These parameters are as follows:

Operating temperature range. This is the specified temperature limit within which the inductor can be operated safely. Above the specified limits, the inductor's maximum current rating is reduced due to thermal effects as well as reliability concerns.

Temperature coefficient of inductance. This is the amount the inductance changes with temperature and is expressed in parts per million per degree Celsius (ppm/°C).

Saturated RF power limit. Inductors with magnetic cores have a maximum RF power level above which they get saturated, resulting in a nonlinear response.

2.3 Inductor Configurations

Inductors can be realized in one of the following three forms: a small section of a strip conductor or a wire [Figure 2.4(a)], a single loop [Figure 2.4(b)], or a spiral [Figure 2.4(c)]. The printed microstrip section inductor is used for low inductance values, typically less than 2 nH and often meandered to reduce the component's size. Printed circuit single-loop inductors are not as popular as their coil versions due to their limited inductance per unit area. However, in MICs, single-loop wire inductors are often used in RF and microwave circuits. The spiral/coil type are the most popular type of inductors. The coil inductors may be printed or wire wound. Both can take a rectangular or circular shape. The circular geometry is superior in electrical performance, whereas the rectangu-

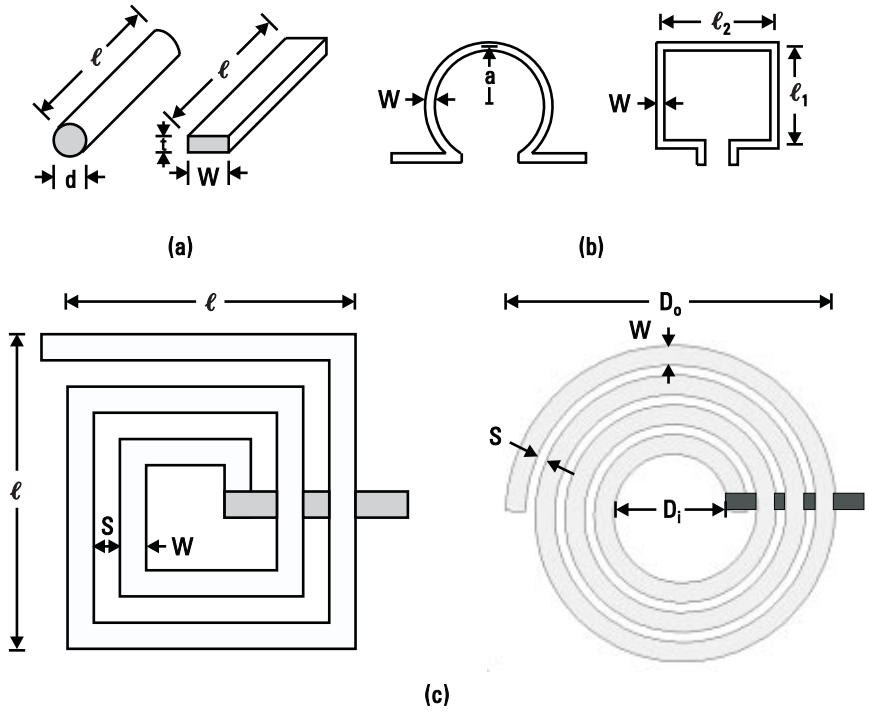


Figure 2.4 Inductor configurations: (a) bond wire and strip sections, (b) circular and rectangular loops, and (c) rectangular and circular spirals.

lar shapes are easier to lay out. Printed inductors are fabricated by using thin- or thick-film fabrication processes or using monolithic Si and GaAs-based IC technologies. The inner connection is pulled out to connect with other circuitry through a gold wire or by using a multilevel crossover metal strip.

2.4 Inductor Models

Numerous papers have been published in the literature describing lumped inductor models. Models can be developed using analytical, physics and EM, and measurement-based methods. The analytical/semiempirical models are based on three approaches: the lumped-element method [1, 21–26], the microstrip coupled-line method, and the mutual inductance method [27]. The lumped-element approach uses frequency-independent formulas for free-space inductance with ground plane effects. These formulas are useful only when the total length of the inductor is a small fraction of the operating wavelength and when the interturn capacitance can be ignored. In the coupled-line approach [28, 29], an inductor is analyzed using multiconductor coupled microstrip lines. This technique predicts the spiral inductor's performance reasonably well for up to two turns and frequencies up to 18 GHz. For more than three turns, we need to analyze three or more parallel coupled lines. The analytical semiempirical models are good for approximating the electrical performance of inductors. Accurate characterization of inductors including the effects of radiation, surface waves, and interaction between components on the performance of densely packed inductors in MMICs can only be calculated using 3-D EM simulators [30–35].

The most commonly used method of developing models for lumped inductors is by measuring dc resistance and S-parameters [18, 36–40]. This modeling approach gives quick and accurate results although they are generally limited to just the devices measured. Equivalent circuit model parameters are extracted by computer optimization, which correlates the measured dc resistance and S-parameter data (one- or two-port data) and are valid up to 26 or 40 GHz depending on the application. The accuracy of the model parameter values can be as good as the measurement accuracy if recently developed on-wafer calibration standards and techniques [41] are used. These methods are discussed next.

2.4.1 Analytical Models

Lumped-element EC models of printed inductors are shown in Figure 2.5. Approximate expressions for inductance L, resistance R_s, and parasitic capacitances for microstrip sections, circular loops, and circular coils are given next [42].

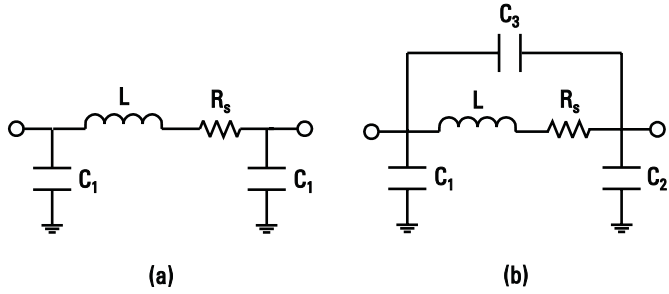


Figure 2.5 EC models: (a) microstrip section and loop and (b) coil.

2.4.1.1 Microstrip Section

$$L(\text{nH}) = 2 \times 10^{-4} \ell \left[\ln\left(\frac{\ell}{W+t}\right) + 1.193 + \frac{W+t}{3\ell} \right] \cdot K_g \quad (2.13a)$$

$$R_s(\Omega) = \frac{KR_{sh}\ell}{2(W+t)} \quad (2.13b)$$

$$C_1(\text{pF}) = 16.67 \times 10^{-4} \ell \sqrt{\epsilon_{re}}/Z_0 \quad (2.13c)$$

where all dimensions are in microns and

$$K_g = 0.57 - 0.145 \ln \frac{W}{h}, \frac{W}{h} > 0.05 \quad (2.14)$$

$$K = 1.4 + 0.217 \ln\left(\frac{W}{5t}\right), 5 < \frac{W}{t} < 100 \quad \text{for a ribbon} \quad (2.15a)$$

$$K = 1 + 0.333\left(1 + \frac{S}{W}\right) \quad \text{for a spiral} \quad (2.15b)$$

The term K_g accounts for the presence of a ground plane and decreases as the ground plane is brought nearer. Another term K is a correction factor that takes into account the crowding of the current at the corners of the conductor. The terms W, t, h, ℓ, and R_{sh} are the line width, line thickness, substrate thickness, length of the section, and sheet resistance per square of the conductor, respectively. The calculation of microstrip parameters Z_0 and ϵ_{re} are presented in Chapter 14.

2.4.1.2 Circular Loop

$$L\ (\text{nH}) = 1.257 \times 10^{-3} a \left[\ln\left(\frac{a}{W+t}\right) + 0.078 \right] \cdot K_g \tag{2.16a}$$

$$R_s\ (\Omega) = \frac{KR_{sh}}{W+t}\,\pi a \tag{2.16b}$$

$$C_1 = 33.33 \times 10^{-4}\,\pi a \sqrt{\epsilon_{re}}/Z_0 \tag{2.16c}$$

where a is the mean radius of the loop.

2.4.1.3 Circular Spiral

$$L\ (\text{nH}) = 0.03937 \frac{a^2 n^2}{8a + 11c} \cdot K_g \tag{2.17a}$$

$$a = \frac{D_o + D_i}{4},\ c = \frac{D_o - D_i}{2}$$

$$R_s\ (\Omega) = \frac{K\pi a n R_{sh}}{W} \tag{2.17b}$$

$$C_3\ (\text{pF}) = 3.5 \times 10^{-5} D_o + 0.06 \tag{2.17c}$$

where n is the number of turns, D_i is the inductor's inside diameter, D_o is the inductor's outside diameter, and S is the spacing between the turns. The effect of ground plane on the inductance value can be reduced by keeping $S < W$ and $S << h$.

A more general expression for inductance of arbitrary shape has been reported in the literature [43, 44] and reproduced as follows:

$$L = \frac{\mu_0 n^2 D_{\text{av}} c_1}{2} \left[\ln(c_2/\rho) + c_3\rho + c_4\rho^2\right] \tag{2.18}$$

where coefficients c_i for various geometries are given in Table 2.1, ρ is the fill ratio, and D_{av} is the average diameter of the inductor. Their expressions are given here:

$$\rho = \frac{D_o - D_i}{D_o + D_i} \tag{2.19a}$$

Table 2.1
Coefficients for General Inductance Expression [43]

Inductor Geometry	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

$$D_{\text{av}} = \frac{1}{2}(D_o + D_i) \tag{2.19b}$$

2.4.2 Coupled-Line Approach

A 2-turn spiral microstrip inductor with opposite sides appropriately connected as shown in Figure 2.6 may be treated as a coupled-line section. This figure shows 2-turn circular and rectangular spiral inductors and 1.75-turn rectangular spiral inductor with connecting single line section and the feed lines represented between nodes 1 and 2 and between nodes 4 and 5. In the 2-turn case, the parallel coupled line section, which has a total line length equivalent to the spiral length between nodes 2 and 4, is represented between nodes 2, 3, and 4 and constitutes the intrinsic inductor. The length is taken as the average of the outer and inner turn lengths. In the 1.75-turn inductor, an additional single line between nodes 3 and 4 is connected, whereas the coupled line is between nodes 2 and 3.

The electrical equivalent coupled-line model shown in Figure 2.6 does not include the crossover capacitance or the right-angle bend discontinuity effects. Figure 2.7 shows a modified equivalent circuit of a 1.75-turn rectangular spiral inductor that also includes the crossover capacitance. This figure also shows the physical and electrical parameters of the inductor. Figure 2.8 shows a further subdivision of the inductor, which is required to evaluate its performance more accurately. In this case the inductor is split into three sections representing elements 1, 2, and 3. The performance of these inductors can be calculated by using either commercial CAD tools or by solving cascaded ABCD or *S*-parameter matrices for these elements. Improved versions of these inductors include chamfered bends.

The electrical characteristics of the intrinsic 2-turn inductor can be derived from the general four-port network of a coupled-line section as shown in Figure 2.9 where the current and voltage relationships of the pair of lines can be described by the admittance matrix equation as follows:

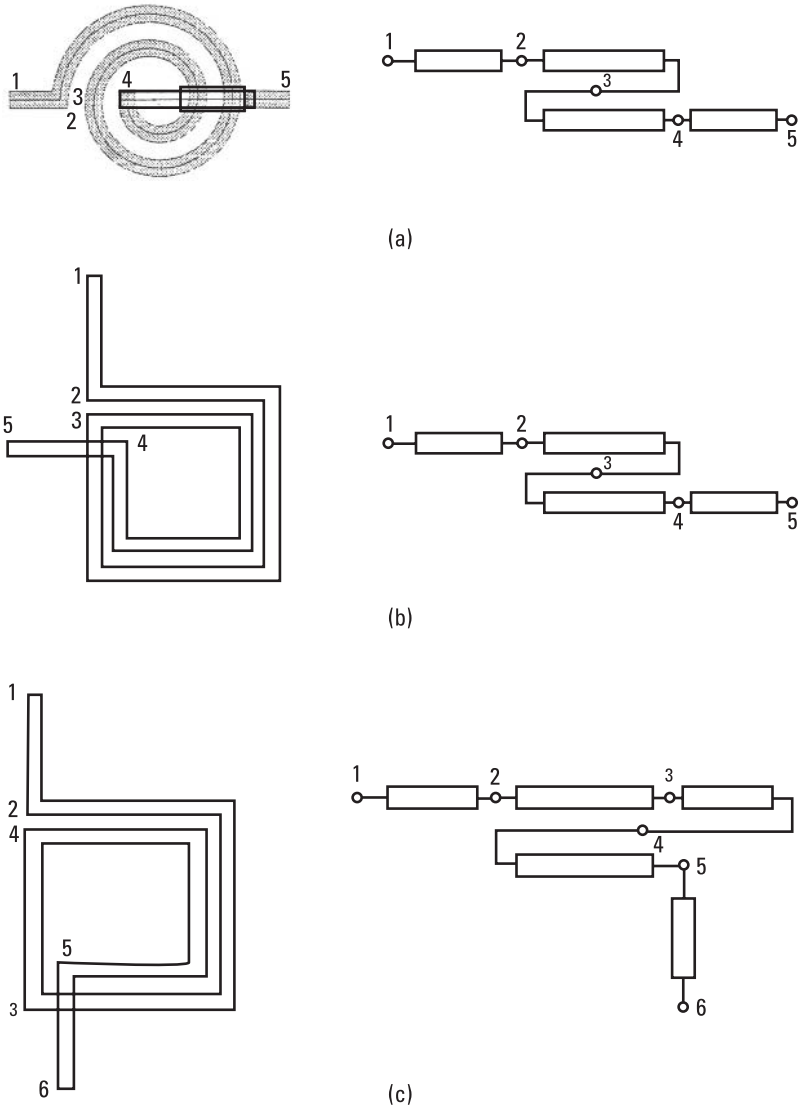
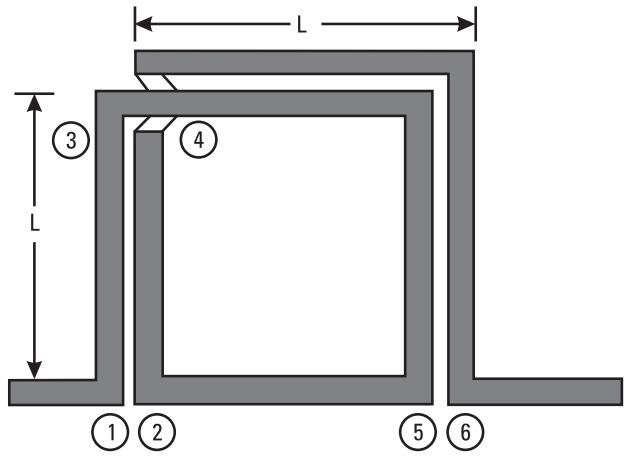


Figure 2.6 Spiral inductors and their coupled-line EC models: (a) circular 2 turns, (b) rectangular 2 turns, and (c) rectangular 1.75 turns.

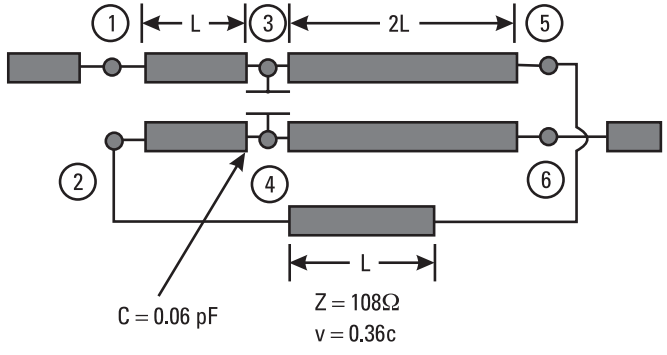
$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \tag{2.20}$$



10 micron Wide lines
10 micron Space
175 micron Above ground plane

(a)

$Z_{0e} = 165\Omega$
$Z_{0o} = 42\Omega$
$v_e = 0.35c$
$v_o = 0.365c$



L = 0.006 inches in 2–6 GHz CAD model

(b)

Figure 2.7 Rectangular 1.75-turn spiral inductor: (a) physical layout and (b) coupled-line EC model.

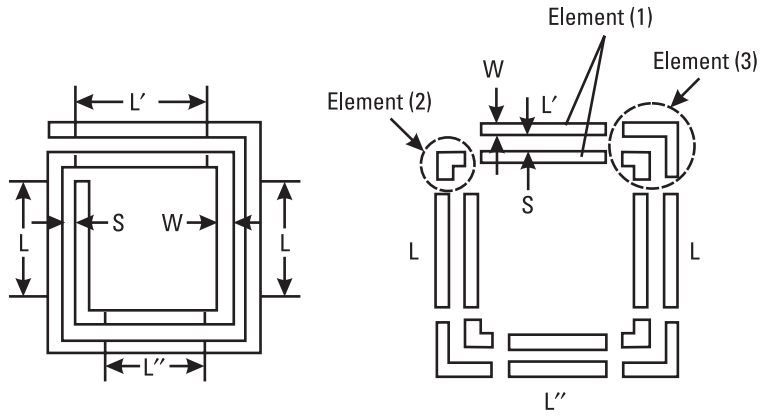


Figure 2.8 The network model for calculating the inductance of a planar rectangular spiral inductor.

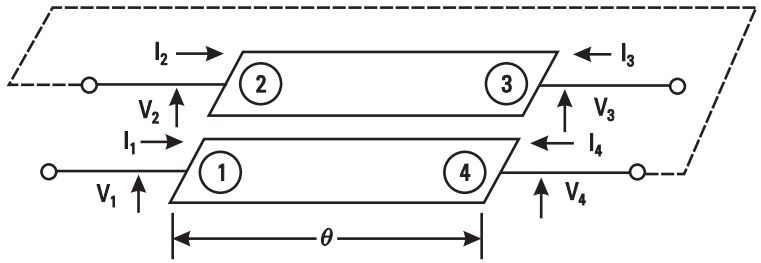


Figure 2.9 A four-port representation of the coupled-line section of an inductor.

This matrix can be reduced to two ports by applying the boundary condition that ports 2 and 4 are connected together:

$$V_2 = V_4 \tag{2.21a}$$

$$I_2 = -I_4 \tag{2.21b}$$

By rearranging the matrix elements, the two-port matrix can be written as follows:

$$\begin{bmatrix} I_1 \\ I_3 \end{bmatrix} = \begin{bmatrix} Y'_{11} & Y'_{13} \\ Y'_{31} & Y'_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_3 \end{bmatrix} \tag{2.22}$$

where

$$Y'_{11} = Y_{11} - \frac{(Y_{12} + Y_{14})(Y_{21} + Y_{41})}{Y_{22} + Y_{24} + Y_{42} + Y_{44}} \tag{2.23}$$

$$Y'_{13} = Y_{13} - \frac{(Y_{12} + Y_{14})(Y_{23} + Y_{43})}{Y_{22} + Y_{24} + Y_{42} + Y_{44}} \tag{2.24}$$

and

$$Y'_{33} = Y'_{11} \tag{2.25}$$

$$Y'_{31} = Y'_{13} \tag{2.26}$$

due to symmetry.

The admittance parameters for a coupled microstrip line are given by [45]

$$Y_{11} = Y_{22} = Y_{33} = Y_{44} = -j[Y_{0e} \cot \theta_e + Y_{0o} \cot \theta_o]/2 \tag{2.27a}$$

$$Y_{12} = Y_{21} = Y_{34} = Y_{43} = -j[Y_{0e} \cot \theta_e - Y_{0o} \cot \theta_o]/2 \tag{2.27b}$$

$$Y_{13} = Y_{31} = Y_{24} = Y_{42} = j[Y_{0e} \csc \theta_e - Y_{0o} \csc \theta_o]/2 \tag{2.27c}$$

$$Y_{14} = Y_{41} = Y_{23} = Y_{32} = j[Y_{0e} \csc \theta_e + Y_{0o} \csc \theta_o]/2 \tag{2.27d}$$

where e and o designate the even mode and the odd mode, respectively.

An equivalent "pi" representation of a two-port network is shown in Figure 2.10 where

$$Y_A = -Y'_{13} \tag{2.28}$$

$$Y_B = Y'_{11} + Y'_{13} \tag{2.29}$$

and

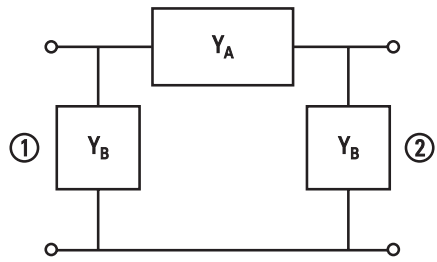


Figure 2.10 Pi EC representation of the inductor.

$$Y_A = -j\frac{1}{2}\left\{ Y_{0e}\cot\theta_e + Y_{0o}\cot\theta_o + \frac{\left[Y_{0e}\left(\frac{1-\cos\theta_e}{\sin\theta_e}\right) + Y_{0o}\left(\frac{1+\cos\theta_o}{\sin\theta_o}\right)\right]}{2\left[Y_{0e}\left(\frac{1-\cos\theta_e}{\sin\theta_e}\right) - Y_{0o}\left(\frac{1+\cos\theta_o}{\sin\theta_o}\right)\right]}\right\} \tag{2.30}$$

$$Y_B = \frac{2jY_{0e}Y_{0o}(1-\cos\theta_e)(1+\cos\theta_o)}{[Y_{0o}\sin\theta_e(1+\cos\theta_o) - Y_{0e}\sin\theta_o(1-\cos\theta_e)]} \tag{2.31}$$

Because the physical length of the inductor is much less than $\lambda/4$, $\sin\theta_{e,o} \cong \theta_{e,o}$ and $\cos\theta_{e,o} \cong 1 - \theta_{e,o}^2/2$. Also $Y_{0o} > Y_{0e}$; therefore, (2.30) and (2.31) are approximated as follows:

$$Y_A \cong -j\frac{Y_{0e}}{2\theta_e} \tag{2.32}$$

$$Y_B \cong jY_{0e}\theta_e \tag{2.33}$$

which are independent of the odd mode. Thus the "pi" EC consists of shunt capacitance C and series inductance L as shown in Figure 2.11. The expressions for L and C can be written as follows:

$$Y_A = \frac{1}{j\omega L} = -j\frac{Y_{0e}}{2\theta_e} \tag{2.34}$$

or

$$L = \frac{2\theta_e}{\omega Y_{0e}} \tag{2.35}$$

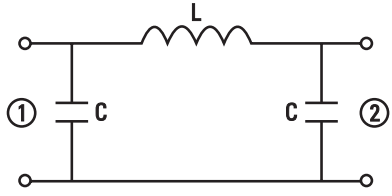


Figure 2.11 Equivalent LC circuit representation of the inductor.

and

$$Y_B = j\omega C = jY_{0e}\,\theta_e \tag{2.36}$$

or

$$C = \frac{Y_{0e}\,\theta_e}{\omega} \tag{2.37}$$

If ℓ is the average length of the conductor, then

$$\theta_e = \frac{\omega \ell}{c}\sqrt{\epsilon_{ree}} \tag{2.38}$$

where c is the velocity of light in free-space and ϵ_{ree} is the effective dielectric constant for the even mode. When $Z_{0e} = 1/Y_{0e}$, from (2.35) and (2.37),

$$L = \frac{2\ell Z_{0e}\sqrt{\epsilon_{ree}}}{c} \tag{2.39}$$

$$C = \frac{\ell\sqrt{\epsilon_{ree}}}{Z_{0e}\,c} \tag{2.40}$$

In a loosely coupled inductor, $Z_{0e} \cong Z_0$ and $\epsilon_{ree} = \epsilon_{re}$ for the single conductor microstrip line. The above equations can be used to evaluate approximately the inductor's performance.

2.4.3 Mutual Inductance Approach

Greenhouse [27] has provided expressions for inductance for both rectangular and circular geometries based on self-inductance of inductor sections and mutual inductances between sections. These relations are also known as *Greenhouse formulas* for spiral inductors. Consider a 10-section rectangular inductor like the one shown in Figure 2.12(a). Let all sections have line width W, separation between sections S, mean distance between conductors d, and thickness t. The total inductance of the coil is the sum of self-inductance of all 10 sections or segments and the mutual inductance between sections, assuming the total length is much less than the operating wavelength so that the magnitude and phase of the currents across the length of the inductor are constant. Two sections carrying currents in the same direction have positive mutual inductance, whereas the inductance is negative for currents flowing in opposite directions. Figure

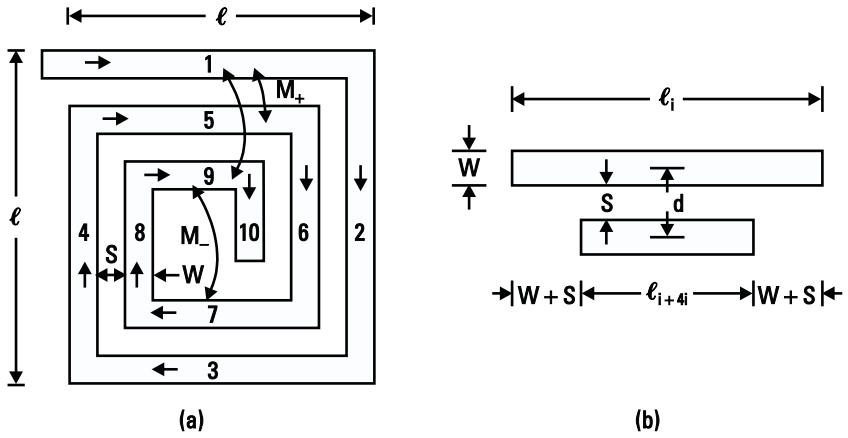


Figure 2.12 (a) Ten-section rectangular spiral inductor showing positive and negative mutual inductance paths. (b) Lengths for an adjacent sections pair.

2.13 shows the magnetic flux lines for positive and negative mutual inductance. Because the magnitude and phase of the currents are assumed identical in all sections, the mutual inductance between sections a and b is $M_{a,b} = M_{b,a}$. The total inductance of 10 sections and a 2.5-turn inductor can be written:

$$\begin{aligned} L = {} & L_1 + L_2 + \ldots + L_{10} \\ & \text{(self inductance)} \\ & + 2(M_{1,5} + M_{2,6} + M_{3,7} + M_{4,8} + M_{5,9} + M_{6,10} + M_{1,9} + M_{2,10}) \\ & \text{(positive mutual inductance)} \\ & - 2(M_{1,7} + M_{1,3} + M_{2,8} + M_{2,4} + M_{3,9} + M_{3,5} + M_{4,10} + M_{4,6} \\ & + M_{5,7} + M_{6,8} + M_{7,9} + M_{8,10}) \\ & \text{(negative mutual inductance)} \end{aligned} \tag{2.41}$$

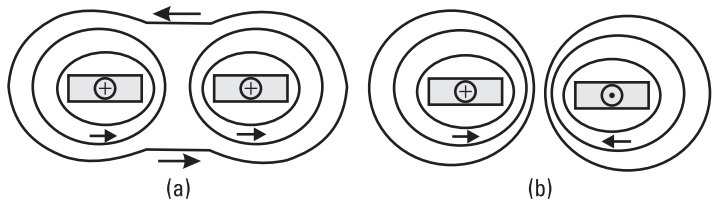


Figure 2.13 Magnetic flux lines: (a) positive mutual inductance case and (b) negative mutual inductance case.

The preceding equation is generalized as follows:

$$L = \sum_{i=1}^{m} L_i + 2\left[\sum_{j=1}^{n}\left(\sum_{i=1}^{m-4} M_{i,i+4j} - \sum_{i=1}^{m-2} M_{i,i+2j}\right)\right] \tag{2.42}$$

where m is the number of sections, n is the number of complete turns, and a maximum value of $i + 4n$ is m. For example, for a 2.5-turn inductor, $n = 2$, $m = 10$, and the total positive and negative mutual inductance terms are 16 and 24, respectively. The total of positive mutual inductance terms M_+ is given by

$$M_+ = 4[n(n-1)] + 2n[m-4n] \tag{2.43a}$$

Similarly, for total negative mutual inductance terms M_- the expression is

$$M_- = 4n^2 + 2n(m-4n) + (m-4n-2)(m-4n-1)[(m-4n)/3] \tag{2.43b}$$

Although M_- is larger than M_+, their contribution to the total inductance value is much less due to much larger spacing. As a first-order approximation, only mutual inductances between adjacent sections may be included.

Next, the self- and mutual inductances can be calculated from the inductor geometry. The self-inductance of each section of straight length ℓ_i can be calculated by using (2.13a), where $K_g = 1$. The mutual inductance is calculated approximately using

$$M_{a,b} = 2 \times 10^{-4}\ell_e\left[\ln\left\{\frac{\ell_e}{d} + \left(1 + \frac{\ell_e^2}{d^2}\right)^{1/2}\right\} - \left(1 + \frac{d^2}{\ell_e^2}\right)^{1/2} + \frac{d}{\ell_e}\right] \tag{2.44}$$

where ℓ_e is the effective length of the two sections between which the mutual inductance is being calculated. Dimensions of ℓ_e and d are in microns and $M_{a,b}$ is in nanohenries. As an approximation ℓ_e can be considered an average length for the two sections shown in Figure 2.12(b).

2.4.4 Numerical Approach

The analytical methods just described provide a quick way to determine the inductor dimensions required for a particular design. However, inductor charac-

terization at high frequencies is generally not adequate to design a circuit accurately. Numerical methods, implemented in EM simulators, on the other hand, simulate inductors adequately and also provide additional flexibility in terms of layout, complexity (i.e., 2-D or 3-D configuration) and versatility. EM simulations automatically incorporate junction discontinuities, airbridge or crossover effects, substrate effects (thickness and dielectric constant), strip thickness, and dispersion and higher order modes effects. Several different field solver methods have been used to analyze inductors as described in the literature [46, 47]. The most commonly used technique for planar structures is the *method of moments* (MoM), and for 3-D structures, the *finite element method* (FEM) is usually used. Both of these techniques perform EM analysis in the frequency domain. FEM can analyze more complex structures than can MoM, but requires much more memory and longer computation time. There are also several time-domain analysis techniques; among them are the *transmission-line matrix method* (TLM) and the *finite-difference time-domain* (FDTD) method. Fast Fourier transformation is used to convert time-domain data into frequency-domain results. Typically, a single time-domain analysis yields *S*-parameters over a wide frequency range. An overview of commercially available EM simulators is given in Table 2.2. More comprehensive information on these tools can be found in recent publications [48, 49].

Table 2.2
An Overview of Some Electromagnetic Simulators Being Used for MMICs

Company	Software Name	Type of Structure	Method of Analysis	Domain of Analysis
Agilent	Momentum HFSS	3-D planar 3-D arbitrary	FEM	Frequency
Sonnet Software	Em	3-D planar	MoM	Frequency
Jansen Microwave	Unisim SFMIC	3-D planar 3-D planar	Spectral domain MoM	Frequency
Ansoft Corporation	Maxwell-Strata Maxwell SI Eminence	3-D planar 3-D arbitrary	MoM FEM	Frequency
MacNeal-Schwendler Corp.	MSC/EMAS	3-D arbitrary	FEM	Frequency
Zeland Software	IE3-D	3-D arbitrary	MoM	Frequency
Kimberly Communications Consultants	Micro-Stripes	3-D arbitrary	TLM	Time
Remco	XFDTD	3-D Arbitrary	FDTD	Time

In EM simulators, Maxwell's equations are solved in terms of electric and magnetic fields or current densities, which are in the form of integrodifferential equations, by applying boundary conditions. Once the structure is analyzed and laid out, the input ports are excited by known sources (fields or currents), and the EM simulator solves numerically the integrodifferential equations to determine unknown fields or induced current densities. The numerical methods involve discretizing (meshing) the unknown fields or currents. Using FEMs, six field components (three electric and three magnetic) in an enclosed 3-D space are determined while MoMs give the current distribution on the surface of metallic structures.

All EM simulators are designed to solve arbitrarily shaped strip conductor structures and provide simulated data in the form of single or multiport *S*-parameters that can be read into a circuit simulator. To perform an EM simulation, the structure to be simulated is defined in terms of dielectric and metal layers and their thicknesses and material properties. After creating the complete circuit/structure, ports are defined and the layout file is saved as an input file for EM simulations. Then the EM simulation engine is used to perform an electromagnetic analysis. After the simulation is complete, the field or current information is converted into S-parameters and saved to be used with other CAD tools.

EM simulators, although widely used, still cannot handle complex structures such as an inductor efficiently due to its narrow conductor dimensions, large size, and 3-D geometry. One has to compromise among size, speed, and accuracy. Simulators lead to accurate calculation of inductance and resonant frequencies but not the *Q*-factor.

2.4.5 Measurement-Based Model

The advantages of a measurement-based model include accuracy and the ease with which it can be integrated into RF circuit simulators to perform linear simulation in the frequency domain. The accuracy of measurement-based models depends on the accuracy of the measurement system, calibration techniques, and calibration standards. On-wafer measurements using high-frequency probes provide accurate, quick, nondestructive, and repeatable results up to millimeter-wave frequencies. Various vector network analyzer calibration techniques are being used to determine a two-port error model that de-embeds the device *S*-parameters. The conventional *short, open, load, and through* (SOLT) calibration technique has been proven unsatisfactory because the open and short reference planes cannot be precisely defined. Unfortunately, another calibration technique, *through-short-delay* (TSD) also relies on either a short or open standard. The reference plane uncertainties for the perfect short limit the accuracy of these techniques. However, these techniques work fine for low frequencies.

The *line-reflect-match* (LRM) calibration technique requires a perfect match on each port. The *thru-reflect-line* (TRL) calibration method is based on transmission-line calibration standards which include a nonzero length thru, a reflect (open or short), and delay line standards (one or more dictated by the frequency range over which the calibration is performed). The advantage of TRL calibration lies in the fact that it uses simple standards that can be placed on the same substrate as the components to be measured, thus ensuring a common transmission medium. This calibration technique accurately locates the reference planes and minimizes radiative crosstalk effects between the two probes since they are sufficiently far apart during the calibration procedure.

The TRL calibration technique accurately de-embeds passive circuit elements by measuring the *S*-parameters at the reference planes as shown in Figure 2.14. Typically, passive circuit elements are embedded in 50-Ω lines (88 μm wide) on a 125-μm-thick GaAs substrate 500 μm long. These microstrip lines have 50Ω grounded coplanar waveguide transitions at each end for on-wafer probing as shown in Figure 2.14. Figure 2.15 illustrates the calibration standards on a 125-μm-thick substrate for de-embedding the two-port elements. The reference plane in the thru line is located at the center. The length of the thru line (1,000 μm) is chosen to be as short as possible but long enough to avoid interaction between the probes. The electrical length of the delay line chosen is approximately 20° of insertion phase at the lowest frequency and less than 160° at the highest frequency. Measurement uncertainties increase significantly when the insertion phase of the delay line nears 0 degrees or an integer multiple of 180°. A via hole short is used as the "reflect" standard. Because one delay standard covers an 8:1 frequency span, two delay line standards are included on the wafer to cover the 1.5- to 26-GHz frequency range. The two delay lines are 10,600 and 1,460 μm long with an associated time delay of about 102.0 ps (at 2.5 GHz) and 14.1 ps (at 18 GHz), respectively. These time delay values include frequency dispersion effects.

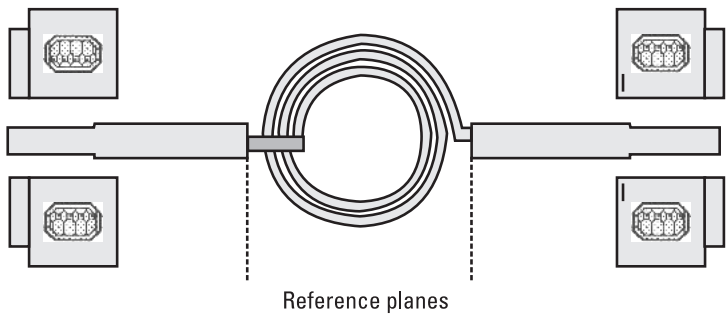


Figure 2.14 The TRL calibration accurately de-embeds the inductor at the reference planes.

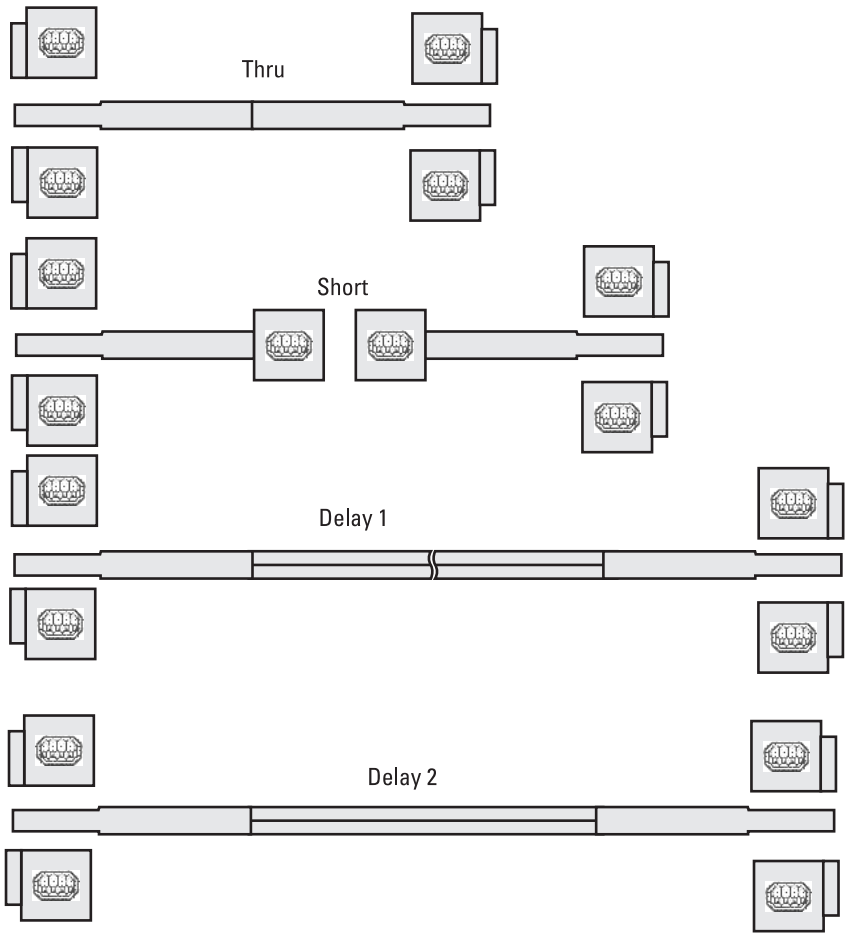


Figure 2.15 On-wafer TRL calibration standards include a thru, reflect provided by a via hole and delay lines.

Many components have low impedances, so their accurate characterization is difficult by measuring their *S*-parameters in a 50-Ω system. In such cases, TRL standards and de-embedding lines must have a much lower characteristic impedance than 50Ω. Gross and Weller [50] used 3-Ω and 7-Ω TRL de-embedding system impedances to determine an air core inductor's low series resistance. The RF probable TRL standards in a 3Ω system are shown in Figure 2.16(a). Because the measurement system and RF probes have 50Ω impedance, the TRL standards employ broadband taper line transformers between the probe launcher and the thru, reflect, and delay lines, which have 3Ω characteristic impedance. Figure 2.16(b) shows a taper line transformer and half thru line

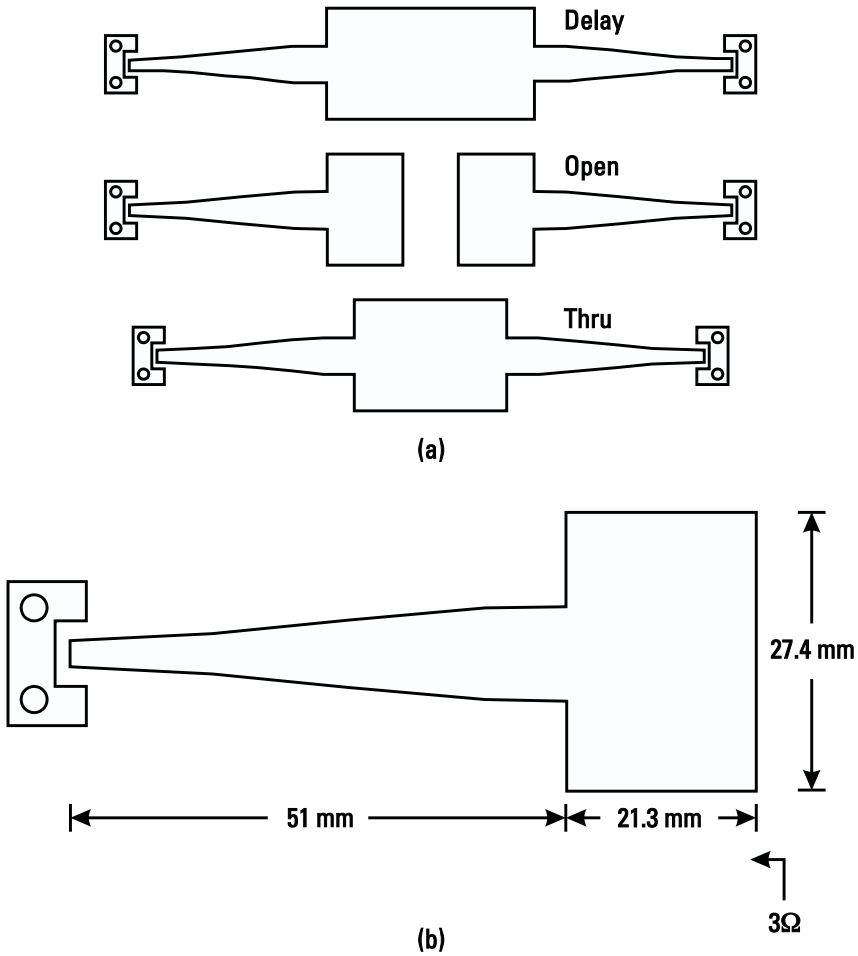


Figure 2.16 (a) TRL calibration standards for the 3-Ω reference impedance system. (b) Microstrip line geometry to match 3-Ω impedance to 50-Ω probe impedance, where $\epsilon_r = 10.2$ and $h = 0.635$ mm.

with dimensions on copper clad Arlon substrate with $\epsilon_r = 10.2$ and $h = 0.635$ mm.

To extract device model parameters, one can use either the direct method or the indirect method, as discussed next.

2.4.5.1 Direct Method

An accurate model of an inductor can be developed by making *S*-parameter measurements in a series configuration as shown in Figure 2.17(a). The

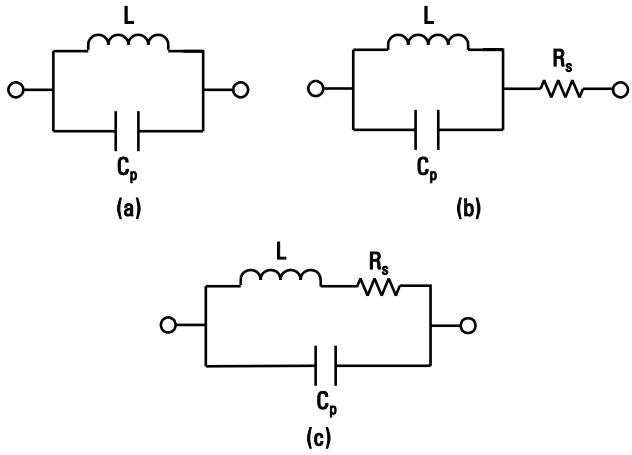


Figure 2.17 (a–c) Three simplified EC models of an inductor.

S-parameter measurements are made in a 50Ω microstrip system. The inductors are printed between 50Ω TRL microstrip lines (Figure 2.14) and the substrate could be alumina, low-temperature cofired ceramic (LTCC), FR-4, GaAs, or Si depending on the technology being used. In case of chip inductors, they are mounted across 50Ω microstrip lines. The device's *S*-parameter data are de-embedded using TRL standards on the same substrate. The maximum frequency of measurement must be well beyond the first resonance. A simplified equivalent circuit to predict accurately the inductance, *Q* and the first resonance frequency is shown in Figure 2.17(b).

The *S*-matrix of Figure 2.17(b) is given by

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{Z + 2Z_0} \begin{bmatrix} Z & 2Z_0 \\ 2Z_0 & Z_0 \end{bmatrix} \tag{2.45}$$

Here,

$$S_{11} = \frac{Z}{Z + 2Z_0} \tag{2.46a}$$

$$S_{21} = \frac{2Z_0}{Z + 2Z_0} \tag{2.46b}$$

$$Z = R_s + \frac{j\omega L}{[1 - (\omega/\omega_p)^2]} \tag{2.46c}$$

where

$$\omega_p^2 = 1/LC_p \tag{2.46d}$$

If S_{21r} and S_{21i} are the real and imaginary parts of S_{21}, then by equating real and real parts of (2.46b),

$$R_s = 2Z_0\left[\frac{S_{21r}}{S_{21r}^2 + S_{21i}^2} - 1\right] \tag{2.47a}$$

$$L = \frac{2Z_0 S_{21i}}{S_{21r}^2 + S_{21i}^2}\,\frac{1 - (\omega/\omega_p)^2}{\omega} \tag{2.47b}$$

The value of C_p is determined using (2.46d) from the first resonance frequency. At first resonance ω_p, the angle of $S_{21} = 0$. Thus, the inductor EC model parameters are determined from (2.46) and (2.47) or they may be extracted by computer optimization. Normally, the computer optimization technique is used because it also helps to fit more complex EC models for devices that will also predict higher order resonances. Such models are discussed in the next chapter.

2.4.5.2 Indirect Method

The inductance value and Q-factor of an inductor can be determined by connecting externally a known capacitor to the inductor and measuring the first resonant frequency of the LC resonator. In this method, one can use the *device under test* (DUT) in series or in parallel as shown in Figure 2.18. In this method the Q of the externally added capacitor at the resonant frequency is much larger than the Q of the DUT. These capacitors have negligible parasitics (or they are accounted for) and their values are selected so that the first resonant frequency of the LC network is several times lower than the estimated first self-resonant frequency of the inductor. Devices are then characterized by making one-port S-parameter measurements at the input of the DUT.

2.4.5.3 Series Capacitor

In this case, the capacitor's bottom plate is grounded and the inductor is connected in series with the top plate. The EC model for a series resonator is shown in Figure 2.18(a). When $C_1 >> C_p$, at the first series resonance,

$$L = 1/(C_1\omega_1^2) \tag{2.48}$$

where $\omega_1 = 2\pi f_1$. From the 3-dB bandwidth BW, Q is calculated:

$$Q = \frac{f_1}{\text{BW}} = \frac{\omega_1 L}{R_s} \tag{2.49a}$$

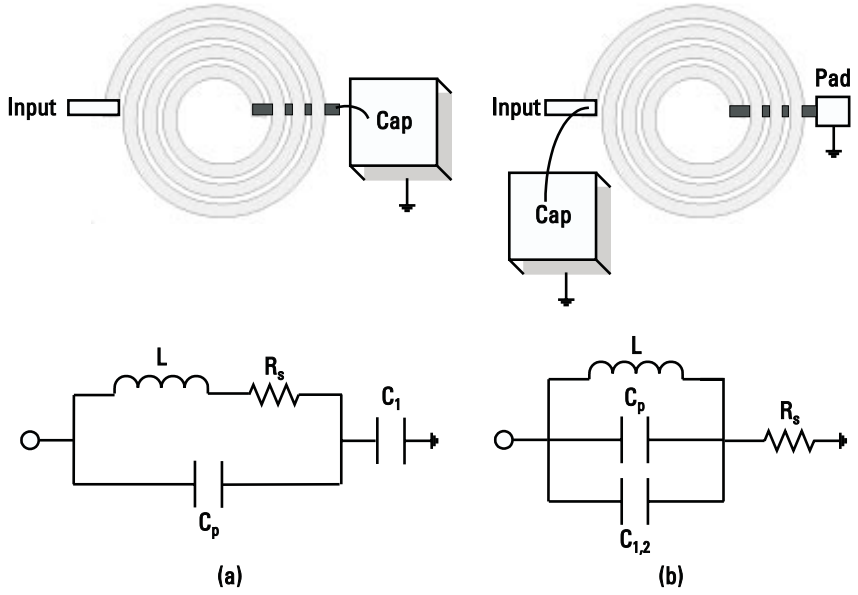


Figure 2.18 One-port LC resonator schematics and EC models: (a) series and (b) parallel.

or

$$R_s = \frac{\omega_1 L}{Q} \tag{2.49b}$$

2.4.5.4 Parallel Capacitor

In the parallel resonator case, two capacitors C_1 and C_2 are used [51]. The capacitance values are within about 25% of each other. The EC model is shown in Figure 2.18(b). With each capacitor, the input return loss of the LC combination is measured. The input impedance can be written as

$$Z_{\text{in}} = R_{\text{in}} + jX_{\text{in}} = \frac{R + j\omega L(1 - \omega^2 LC_t) - jR^2\omega C_t}{[1 - \omega^2 LC_t]^2 + [R\omega C_t]^2} \tag{2.50}$$

where $C_t = C_p + C_{1,2}$. At resonance $X_{\text{in}} = 0$ and the resonant frequencies are given by

$$f_{1,2}^2 = \frac{1}{(2\pi L)^2}\left(\frac{L}{C_{t1,2}} - R_s^2\right) \tag{2.51}$$

where $C_{t1,2} = C_p + C_{1,2}$. From (2.51)

$$L = \frac{1}{4(C_1 - C_2)\pi^2}\left[\frac{1}{f_1^2} - \frac{1}{f_2^2}\right] \tag{2.52}$$

Ignoring the effect of R_s, as $\omega L >> R_s$

$$C_p = \frac{1}{8\pi^2 L}\left[\frac{1}{f_1^2} - \frac{1}{f_2^2}\right] - \frac{1}{2}(C_1 + C_2) \tag{2.53}$$

From (2.51) an average value of R_s is given by

$$R_s = 0.5\left[\frac{L}{C_{t1}} - (2\pi L)^2 f_1^2\right]^{1/2} + 0.5\left[\frac{L}{C_{t2}} - (2\pi L)^2 f_2^2\right]^{1/2} \tag{2.54}$$

2.5 Coupling Between Inductors

When two inductors are placed in proximity to each other, their EM fields interact and a fraction of the power present on the primary or main inductor is coupled to the secondary inductor. In this case, the coupling between the electromagnetic fields is known as *parasitic coupling*. Parasitic coupling affects the electrical performance of the circuit in several ways. It may change the frequency response in terms of frequency range and bandwidth, and it may degrade the gain/insertion loss and its flatness, input and output VSWR, and many other characteristics including output power, power added efficiency, and noise figure depending on the type of circuit. The coupling can also result in instability of an amplifier circuit or create feedback that results in a peak or a dip in the measured gain response or make a substantial change in the response of a phase shifter. In general, this parasitic coupling is undesirable and is an impediment to obtaining an optimum solution in a circuit design. However, this coupling can be taken into account in the design phase by using empirical equations, by performing EM simulations, or by reducing it to an acceptable level by maintaining a large separation between the inductors.

The coupling between two closely placed inductors depends on several factors, including separation between the inductors, size of each inductor and its orientation, resistivity of the substrate on which they are printed, substrate thickness, and the frequency of operation [52–55].

2.5.1 Low-Resistivity Substrates

Figure 2.19(a) shows the measured S_{21} response representing the coupling between two inductors as a function of distance D between them. Each inductor has an inside diameter of 60 μm, outside diameter of about 275 μm, 8 turns,

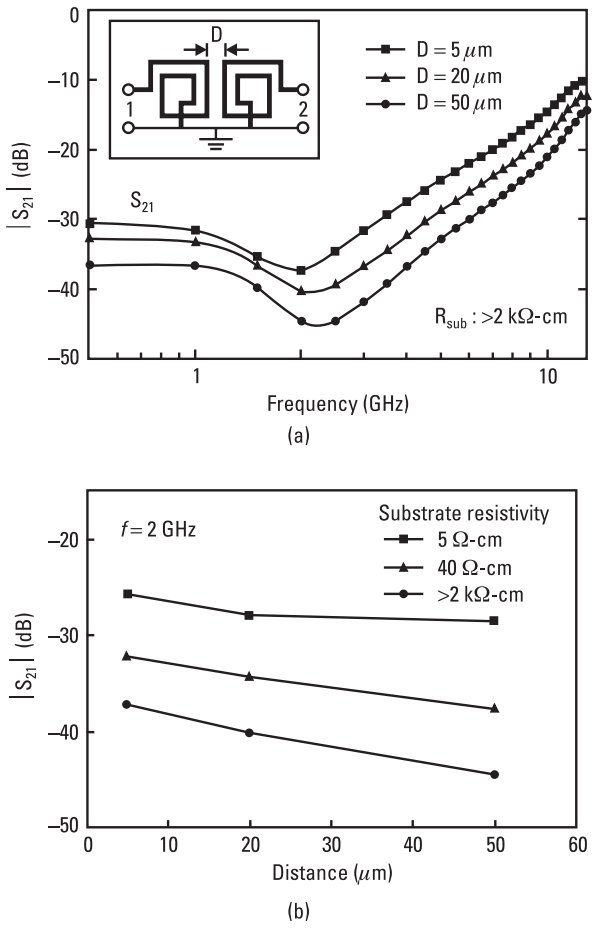


Figure 2.19 (a) Measured S_{21} response for two adjacent inductors versus frequency for three different separations. (b) Measured S_{21} response for two adjacent inductors versus distance between them for three values of Si resistivity.

and total inductance of 13 nH. Both inductors were printed on 2 kΩ-cm resistivity Si substrate with a thickness of about 650 μm. Increasing the separation from 5 to 50 μm reduces the coupling by about 10 dB. Figure 2.19(b) shows S_{21} as a function of substrate D at 2 GHz, for three values of substrate resistivity. As the resistivity is reduced, the substrate conductivity increases, resulting in larger coupling between the inductors.

2.5.2 High-Resistivity Substrates

Coupling effects between two coplanar inductors as shown in Figure 2.20 were also investigated for three different orientations using the FDTD method. Each

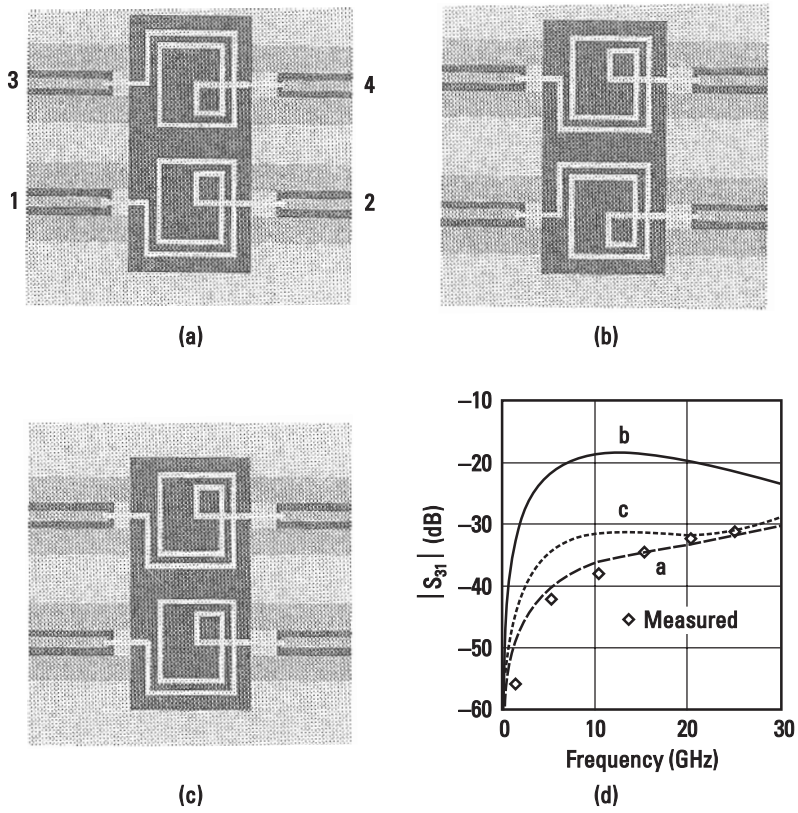


Figure 2.20 (a–c) Three different orientations of rectangular inductors in proximity. (d) Simulated and measured coupling coefficient versus frequency. (*From:* [52]. © 1997 IEEE. Reprinted with permission.)

square spiral inductor has a 10-μm conductor width, 10-μm spacing between conductors, 3-μm-thick conductors, and about a 200-μm outer diameter. The spacing between the inductors was 60 μm and they were fabricated on a GaAs substrate. The inductor conductor patterns were elevated above the GaAs substrate using airbridges to reduce the parasitic capacitance. (See Chapter 10 for more detail on this subject.). The ground planes in the coplanar waveguide feedlines were connected using airbridges to suppress the coupled slotline mode. Figure 2.20(a–c) shows the three possible configurations, and Figure 2.20(d) shows the simulated coupling between ports 3 and 1, while the other two ports were terminated in 50Ω. As reported by Werthen et al. [52], coupling between ports 3 and 1 is slightly higher than between ports 4 and 1. Measured coupling in the case of configuration (a) is also shown in this figure for comparison.

Coupling between inductors on a 75-μm-thick GaAs substrate has been described by Bahl [55]. For a given inductance value and distance between two

spiral inductors, the coupling between the circular spirals shown in Figure 2.21(a) is lower than for the rectangular spirals shown in Figure 2.21(b), because of the larger average coupling distance. Figure 2.22 shows the coupling coefficient between ports 3 and 1 as a function of frequency for 0.8-nH circular and rectangular inductors placed 20 μm apart. Dimensions for the circular inductors are as follows: line width $W = 12$ μm, line spacing $S = 8$ μm, inner diameter $D_i = 50$ μm, and number of turns $n = 2.5$. The rectangular inductor has the same dimensions, except it has 11 sections. Here all ports are terminated in 50Ω. The coupling between ports 3 and 1 is slightly higher than between ports 4 and 1.

Coupling effects between two circular spiral inductors in three different possible orientations, shown in Figure 2.21, were also investigated [55]. Each inductor has a 12-μm conductor width, 8-μm spacing, 4.5-μm-thick conductors, and 50-μm inner diameter. The separation between the inductors varied from 20 to 200 μm. Figure 2.23 shows the simulated coupling between ports 3 and 1, when the other two ports were terminated in 50Ω, for 20-μm spacing as a function of frequency. Among all three configurations, coupling between ports 3 and 1 is slightly higher than between ports 4 and 1. The configurations shown in Figure 2.21(c, d) result in the largest and smallest coupling, respectively. The difference between these two configurations is about 10 dB. Thus, the

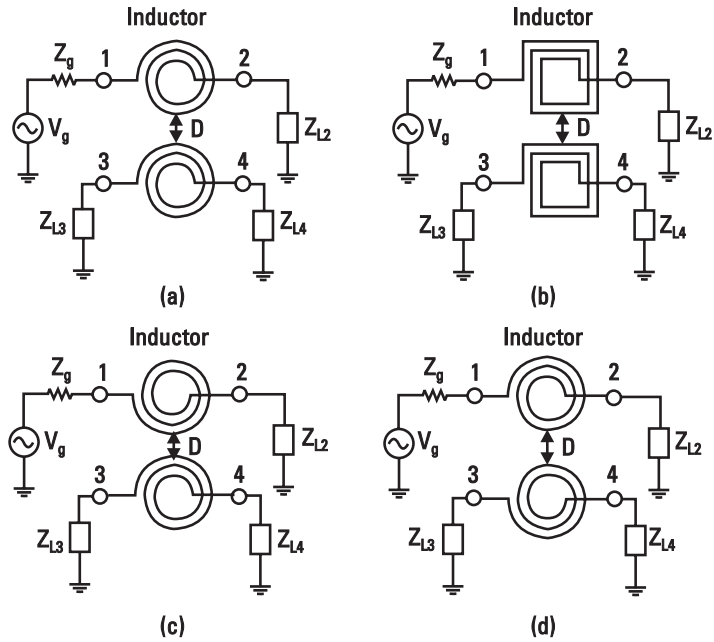


Figure 2.21 (a–d) Several configurations of inductors in proximity.

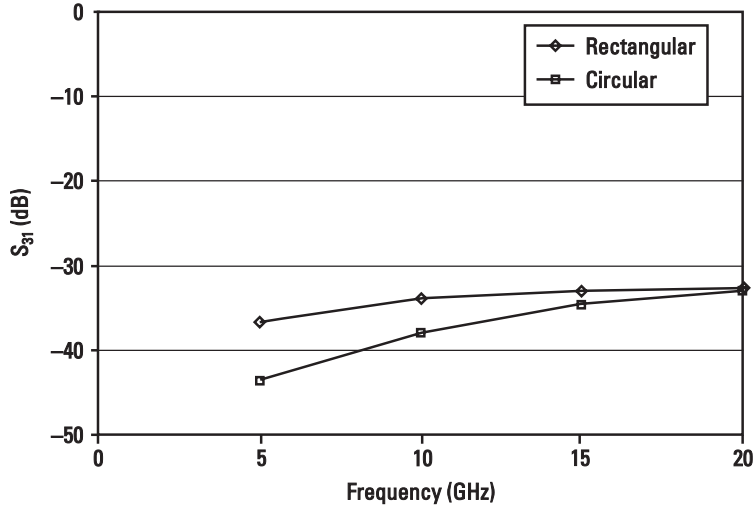


Figure 2.22 Comparison of coupling coefficient versus frequency for circular and rectangular 0.8-nH spiral inductors having similar areas, with $D = 20$ μm.

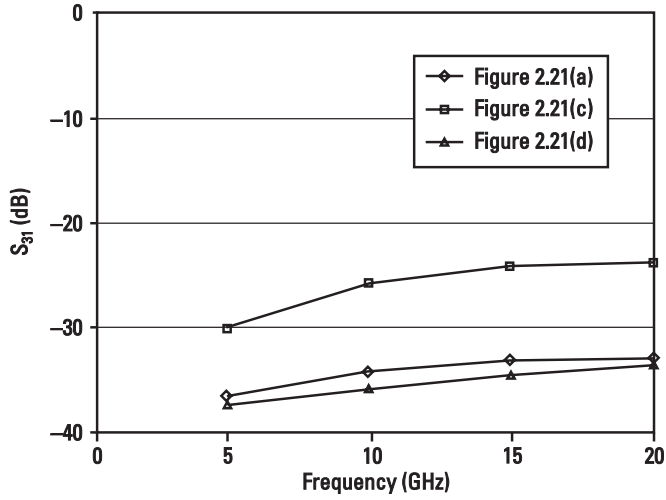


Figure 2.23 Coupling between circular inductors for the three different orientations shown in Figure 2.21, with $D = 20$ μm.

orientations of the inductor coils significantly affect the parasitic coupling between the two. Similar results have been reported for rectangular spiral inductors [52] as discussed earlier. Therefore, in the layout of such inductors, extra care must be exercised to minimize the parasitic coupling. Figure 2.24 shows

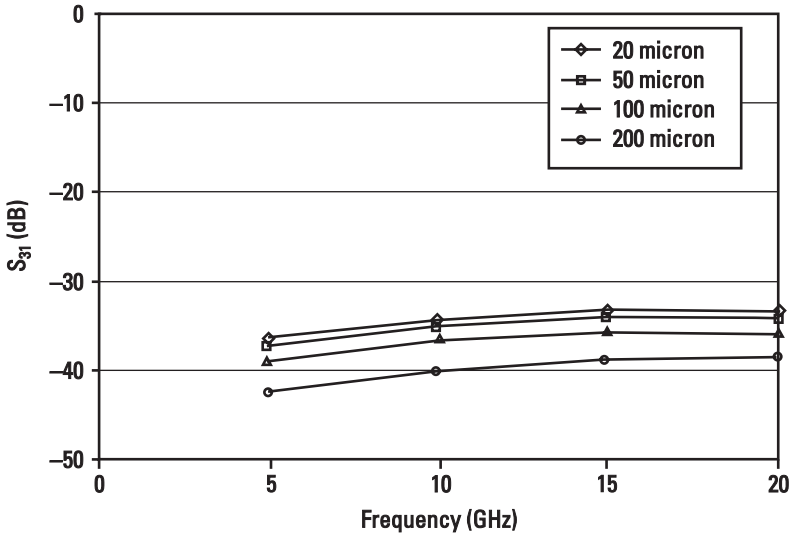


Figure 2.24 Coupling between inductors shown in Figure 2.21(a) for various separations.

the coupling at 10 GHz as a function of separation between the inductors. As distance increases, the coupling decreases monotonically. Table 2.3 summarizes the effect of inductor B on the input impedance of inductor A. The coupling effect is less than 1% for inductors having reactance of about 50Ω and separated by 20 μm on a 75-μm-thick GaAs substrate.

2.6 Electrical Representations

2.6.1 Series and Parallel Representations

When n inductors (having inductance values $L_1, L_2, \ldots, L_n$) are connected in parallel, the total inductance L_T is given by

Table 2.3
Percentage Change in Input Impedance (Z_{in}) of Inductor Due to Another Inductor's Proximity, with $D = 20$ μm

	Re[ΔZ_{in}] Ω (%)		Im[ΔZ_{in}] Ω (%)	
Inductor Conf.	**@ 10 GHz**	**@ 20 GHz**	**@ 10 GHz**	**@ 20 GHz**
Figure 2.21(a)	0.9	2.7	–0.02	0.6
Figure 2.21(c)	14.6	17.6	–0.06	–0.65
Figure 2.21(d)	0.4	2.7	–0.06	0.62

$$L_T = \frac{1}{1/L_1 + 1/L_2 + \ldots 1/L_n} \tag{2.55}$$

and its value is always less than the value of the smallest inductor. To increase the inductance value, the inductors are connected in series. In this case, the total inductance is written as

$$L_T = L_1 + L_2 + \ldots L_n \tag{2.56}$$

where L_T is larger than the largest value of the inductor. Impedance, admittance, and transmission phase angle formulas for various combinations of inductors are given in Table 2.4.

2.6.2 Network Representations

At RF and the lower end of the microwave frequency band, the inductor can be represented by its inductance value L. If Z_0 is the characteristic impedance of the lines across which the inductor is connected, the *ABCD, S*-parameter, *Y*- and *Z*-matrices for an inductor L connected in series and shunt configurations are given in Table 2.5, where ω is the operating frequency in radians per second. When resistance and parasitic capacitances are included in the inductor model, as shown in Figure 2.17(b, c), the results in Table 2.5 can be used by replacing $j\omega L$ with Z_L for series configuration and $\frac{1}{j\omega L}$ by Y_L in shunt configuration. Z_L and Y_L are impedance and admittance for the model in Figure 2.17(b, c).

The discussion on inductors is continued in Chapters 3 and 4, where printed and wire inductors are described, respectively.

Table 2.4
Impedance, Admittance, and Transmission Phase Angle Representations of Inductors, with $R = 0$

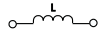
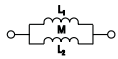
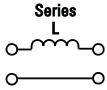
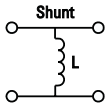
Inductor Configuration	Impedance $Z = R + jX$	Admittance $Y = 1/Z$	Phase Angle $\phi = \tan^{-1}(X/R)$
	$j\omega L$	$-j/\omega L$	$+\pi/2$
	$j\omega(L_1 + L_2 \pm 2M)$	$-j/\omega(L_1 + L_2 \pm 2M)$	$+\pi/2$
	$j\omega\left(\frac{L_1L_2 - M^2}{L_1 + L_2 \mp 2M}\right)$	$-(j/\omega)\left(\frac{L_1 + L_2 \mp 2M}{L_1L_2 - M^2}\right)$	$+\pi/2$

Table 2.5
ABCD, S-Parameter, *Y*- and *Z*-Matrices for Ideal Lumped Inductors

	***ABCD* Matrix**	***S*-Parameter Matrix**	***Y*-Matrix**	***Z*-Matrix**
	$\begin{bmatrix} 1 & j\omega L \\ 0 & 1 \end{bmatrix}$	$\frac{1}{j\omega L + 2Z_0}\begin{bmatrix} j\omega L & 2Z_0 \\ 2Z_0 & j\omega L \end{bmatrix}$	$\frac{j}{\omega L}\begin{bmatrix} -1 & 1 \\ 1 & -1 \end{bmatrix}$	
	$\begin{bmatrix} 1 & 0 \\ \frac{-j}{\omega L} & 1 \end{bmatrix}$	$\frac{1}{Z_0 + 2j\omega L}\begin{bmatrix} -Z_0 & 2j\omega L \\ 2j\omega L & -Z_0 \end{bmatrix}$		$\begin{bmatrix} j\omega L & j\omega L \\ j\omega L & j\omega L \end{bmatrix}$

References

[1] Terman, F. E., *Radio Engineer's Handbook,* New York: McGraw-Hill, 1943, p. 51.

[2] Durney, C. H., and C. C. Johnson, *Introduction to Modern Electromagnetics,* New York: McGraw-Hill, 1969.

[3] Zahn, M., *Electromagnetic Field Theory,* New York: John Wiley, 1979.

[4] Ramo, S., J. R. Whinnery, and T. Van Duzer, *Fields and Waves in Communication Electronics,* 2nd ed., New York: John Wiley, 1984.

[5] Walker, C. S., *Capacitance, Inductance and Crosstalk Analysis,* Norwood, MA: Artech House, 1990.

[6] Ballou, G., "Capacitors and Inductors," *Electrical Engineering Handbook,* R. C. Dorf, (Ed.), Boca Raton, FL: CRC Press, 1997.

[7] Inductor Product Catalog, Cary, IL: Coilcraft.

[8] Inductor Product Catalog, Gowanda, NY: Gowanda Electronics.

[9] Long, J. R., and M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF ICs," *IEEE J. Solid-State Circuits,* Vol. 32, March 1997, pp. 357–369.

[10] Zhao, J., et al., "S Parameter-Based Experimental Modeling of High Q MCM Inductor with Exponential Gradient Learning Algorithm," *IEEE Trans. Comp. Packing Man. Tech–Part B,* Vol. 20, August 1997, pp. 202–210.

[11] Niknejad, A. M., and R. G. Meyer, "Analysis, Design and Optimization of Spiral Inductors and Transformers for Si RF ICs," *IEEE J. Solid-State Circuits,* Vol. 33, October 1998, pp. 1470–1481.

[12] Park, J. Y., and M. G. Allen, "Packaging-Compatible High Q Microinductors and Microfilters for Wireless Applications," *IEEE Trans. Advanced Packaging,* Vol. 22, May 1999, pp. 207–213.

[13] Lutz, R. D., et al., "Modeling and Analysis of Multilevel Spiral Inductors for RFICs," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1999, pp. 43–46.

[14] Nam, C., and Y.-S. Kwon, "High-Performance Planar, Inductor on Thick Oxidized Porous Silicon (OPS) Substrate," *IEEE Microwave Guided Wave Lett.,* Vol. 7, August 1997, pp. 236–238.

[15] Zu, L., et al., "High Q-Factor Inductors Integrated on MCM Si Substrates," *IEEE Trans. Comps. Packaging Manufacturing Tech.–Part B,* Vol. 19, August 1996, pp. 635–642.

[16] Groves, R., D. L. Harame, and D. Jadus, "Temperature Dependence of Q and Inductance in Spiral Inductors Fabricated in a Silicon-Germanium/Bi CMOS Technology," *IEEE J. Solid-State Circuits,* Vol. 32, September 1997, pp. 1455–1459.

[17] Niknejad, A. M., and R. G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RFICs," *IEEE J. Solid-State Circuits,* Vol. 33, October 1998, pp. 1470–1481.

[18] Bahl, I. J., "High Performance Inductors," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, April 2001, pp. 654–664.

[19] Matthaei, G. L., L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks and Coupling Structures,* New York: McGraw-Hill, 1964, p. 214.

[20] Chang, K. (Ed.), *Handbook of Microwave and Optical Components,* Vol. 1, New York: John Wiley, 1989, p. 195.

[21] Caulton, M., S. P. Knight, and D. A. Daly, "Hybrid Integrated Lumped Element Microwave Amplifiers," *IEEE Trans. Electron Devices,* Vol. ED-15, 1968, pp. 459–466.

[22] Wheeler, H. A., "Simple Inductance Formulas for Radio Coils," *Proc. IRE,* Vol. 16, Oct. 1928, pp. 1398–1400.

[23] Grover, F. W., *Inductance Calculations,* Princeton, NJ: Van Nostrand, 1946; reprinted by Dover Publications, 1962, pp. 17–47.

[24] Daly, D. A., et al., "Lumped Elements in Microwave Integrated Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-15, December 1967, pp. 713–721.

[25] Caulton, M., et al., "Status of Lumped Elements in Microwave Integrated Circuits—Present and Future," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-19, July 1971, pp. 588–599.

[26] Pettenpaul, E., et al., "CAD Models of Lumped Elements on GaAs Up to 18 GHz," *IEEE Trans. Microwave Theory Tech.,* Vol. 36, February 1988, pp. 294–304.

[27] Greenhouse, H. M., "Design of Planar Rectangular Microelectronic Inductors," *IEEE Trans. Parts, Hybrids, Packaging,* Vol. PHP-10, June 1974, pp. 101–109.

[28] Camp Jr., W. O., S. Tiwari, and D. Parson, "2–6 GHz Monolithic Microwave Amplifier," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1983, pp. 46–49.

[29] Cahana, D., "A New Transmission Line Approach for Designing Spiral Microstrip Inductors for Microwave Integrated Circuits," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1983, pp. 245–247.

[30] EM, Liverpool, NY: Sonnet Software.

[31] Maxwell SV, Pittsburgh: Ansoft.

[32] High Frequency Structure Simulator, Santa Rosa, CA: Agilent.

[33] LIMMIC + Analysis Program, Ratngen, Germany: Jansen Microwave.

[34] EM Wave Tracer, Acton, MA: Wavetracker.

[35] MSC/EMAS, Milwaukee, WI: MacNeal Schwendler.

[36] Shih, Y. C., C. K. Pao, and T. Itoh, "A Broadband Parameter Extraction Technique for the Equivalent Circuit of Planar Inductors," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1992, pp. 1345–1348.

[37] Sadhir, V. K., I. J. Bahl, and D. A. Willems, "CAD Compatible Accurate Models of Microwave Passive Lumped Elements for MMIC Applications," *Int. J. Microwave and Millimeter-Wave Computer Aided Engineering,* Vol. 4, April 1994, pp. 148–162.

[38] Bahl, I. J., "Improved Quality Factor Spiral Inductors on GaAs Substrates," *IEEE Microwave and Guided Wave Lett.,* Vol. 9, October 1999, pp. 398–400.

[39] Bahl, I. J., "High Current Capacity Multilayer Inductors for RF and Microwave Circuits," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 10, March 2000, pp. 139–146.

[40] Bahl, I. J., "High Performance Inductors," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, April 2001, pp. 654–664.

[41] Bahl, I., G. Lewis, and J. Jorgenson, "Automatic Testing of MMIC Wafers," *Int. J. Microwave and Millimeter-Wave Computer-Aided Engineering,* Vol. 1, January 1991, pp. 77–89.

[42] Bahl, I., and P. Bhartia, *Microwave Solid State Circuit Design,* 2nd ed., New York: John Wiley, 2003, Chap. 2.

[43] Mohan, S. S., et al., "Simple Accurate Expressions for Planar Spiral Inductances," *IEEE J. Solid-State Circuits,* Vol. 34, October 1999, pp. 1419–1424.

[44] Bunch, R. L., D. I. Sanderson, and S. Raman, "Quality Factor and Inductance in Differential IC Implementations," *IEEE Microwave Magazine,* Vol. 3, June 2002, pp. 82–92.

[45] Zysman, G. I., and A. K. Johnson, "Coupled Transmission Line Networks in an Inhomogeneous Dielectric Medium," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-17, Oct. 1969, pp. 753–759.

[46] Itoh, T., (Ed.), *Numerical Techniques for Microwave and Millimeter-Wave Passive Structures,* New York: John Wiley, 1989.

[47] Sorrentino, R., (Ed.), *Numerical Methods for Passive Microwave Millimeter-Wave Structures,* New York: John Wiley, 1989.

[48] Special Issue on Engineering Applications of Electromagnetic Field Solvers, *Int. J. Microwave and Millimeter-Wave Computer-Aided Engineering,* Vol. 5, September 1995.

[49] Special Issue on Automated Circuit Design Using Electromagnetic Simulators, *IEEE Trans. Microwave Theory Tech.,* Vol. 45, Part II, May 1997.

[50] Gross, S., and T. Weller, "Determining the RF Resistance and Q-Factor of Air-Core Inductors," *Microwave Optical Tech. Lett.,* Vol. 29, April 2001, pp. 89–93.

[51] Dayal, H., and Q. Le, "Printed Inductors on Alumina Substrates," *IEEE Microwave Magazine,* Vol. 2, June 2001, pp. 78–86.

[52] Werthen, M., et al., "Investigation of MMIC Inductor Coupling Effects," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1997, pp. 1793–1796.

[53] Paek, S. W., and K. S. Seo, "Air-Gap Stacked Spiral Inductors," *IEEE Microwave and Guided Wave Lett.,* Vol. 7, October 1997, pp. 329–331.

[54] Kim, C. S., et al., "Design Guide of Coupling Between Inductors and Its Effect on Reverse Isolation of a CMOS LNA," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2000, pp. 225–228.

[55] Bahl, I. J., "Coupling Effects Between Lumped Elements," *IEEE Microwave Magazine,* Vol. 2, September 2001, pp. 73–79.

3

Printed Inductors

Planar inductors can be classified into two-dimensional and three-dimensional structures. Two-dimensional inductors are further grouped into four categories based on their shape, that is, meander, rectangular, hexagonal, or octagonal and circular as shown in Figure 3.1. Table 3.1 summarizes the major advantages and disadvantages of each shape. The circular geometry has the best electrical performance, whereas meander line inductors are seldom used. Three-dimensional inductor topologies are shown in Figure 3.2 and their major advantages and disadvantages are summarized in Table 3.2.

In this chapter we discuss planar inductors on semiconductor substrates such as Si and GaAs, on printed circuit boards, and on hybrid integrated circuit substrates. Silicon is a potential candidate for RFICs, and GaAs is widely used for MMICs. Standard silicon substrates have low resistivity and Si-based technologies use thin metallization layers that give rise to high substrate and conductor losses. In comparison, GaAs substrates are semi-insulating (having very high resistivity), and GaAs-based technologies use thick electroplated gold interconnects. GaAs passive components have low capacitive and conductor losses. Several different techniques in both these technologies are employed to reduce losses in order to enhance the quality factor of inductors.

Low-cost wireless applications require integration of more circuit components using *multichip modules* (MCMs). At RF, organic substrate-based MCM technology using a standard FR-4 board is another viable approach to develop low-cost integrated solutions by printing inductors on the same substrate. Several hybrid integrated technologies are being pursued to integrate inductors along with other passive components into a MCM substrate. These include thin film, thick film, and LTCC; and are suitable for high-quality, low-cost, and compact, high-performance inductors, respectively.

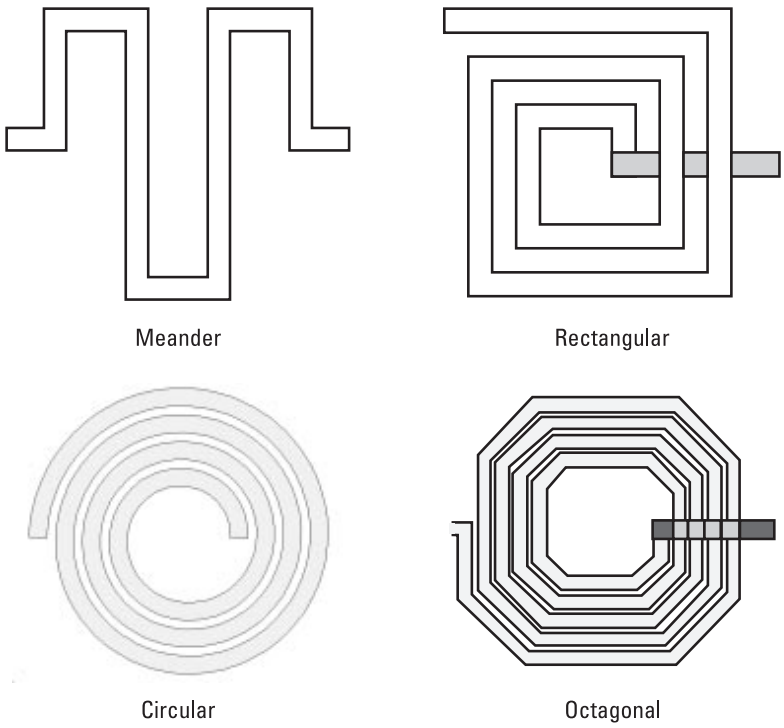


Figure 3.1 Two-dimensional inductor types: (a) meander, (b) rectangular, (c) circular, and (d) octagonal.

Table 3.1
Two-Dimensional Inductor Configurations and Their Features

Configuration	Advantage	Disadvantage
Meander line	Lower eddy current resistance	Lowest inductance and SRF
Rectangular	Easy layout	Lower SRF
Octagonal	Higher SRF	Difficult layout
Circular	Highest SRF	Difficult layout

3.1 Inductors on Si Substrate

RF monolithic ICs are being developed using Si employing CMOS, BiCMOS, and SiGe-HBT technologies in order to take advantage of mature Si processes and low-cost potential. One of the major disadvantages of standard Si technologies is the high substrate losses due to much lower substrate resistivity (less than 10^3 Ω-cm) compared to GaAs substrate (10^7 Ω-cm). High-density CMOS

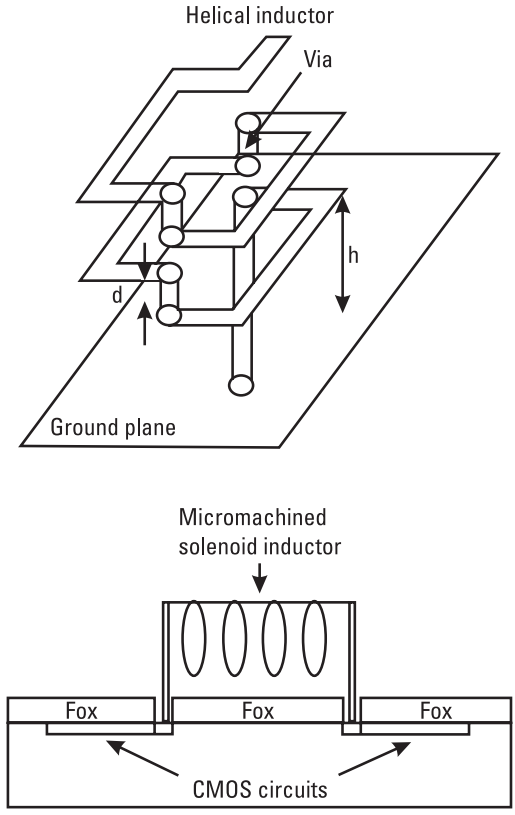


Figure 3.2 Three-dimensional inductor types.

Table 3.2
Three-Dimensional Inductor Topologies and Their Features

Configuration	Advantage	Disadvantage
Rectangular and circular	Higher inductance	Lower SRF
Solenoidal or lateral	Lower eddy current resistance	Lower inductance
Helical	Higher SRF	Lower inductance

technology uses highly doped substrates with resistivity of the order of 0.01 Ω-cm, while in the case of BiCMOS, the nominal resistivity value is about 10 Ω-cm. Thus, spiral inductors and transmission-line sections fabricated on Si substrates have much lower Q-values than their counterparts on GaAs substrates. In this section, we discuss the characteristics of Si-based inductors

including Q-enhancement techniques, stacked inductors, and other various configurations.

Extensive work on Si-based inductors was conducted during the 1990s and a partial list of references is provided here [1–60]. Because Si technologies use a large variety of Si substrate resistivity values (i.e., 0.01–100 Ω-cm), the design of coil inductors becomes quite complex. The selection of physical dimensions, such as the number of turns (n), the trace width (W), the trace thickness (t), line spacing (S), and the inner diameter (D_i) as shown in Figure 3.3(a), determines the excitation of eddy currents responsible for extra loss in the conductor as well as in the Si substrate. It is important to discuss first the excitation of eddy currents and then describe the design of inductors on Si substrates. The loss in an inductor can be divided into two components; conductor loss and substrate loss. These losses are discussed next.

3.1.1 Conductor Loss

The conductor loss in an inductor is proportional to its series resistance. At low frequencies, the series resistance can be calculated from the conductor sheet resistance multiplied by the number of squares of the conductor. However, at microwave frequencies, the series resistance becomes a complex function due to the skin effect and magnetically induced currents (eddy currents). The series resistance increases significantly at higher frequencies due to eddy currents. Eddy currents produce nonuniform current flow in the inner portion of spiral inductors, with much higher current density on the inner side of the conductor than on the outer side. These two components of conductor loss are briefly discussed in the following sections.

3.1.1.1 Sheet Resistance

The dc sheet resistance of a spiral coil can be reduced by using a thicker metallization. Several available thin metal layers can be connected or shunted together through via holes to realize a thick metal layer or a thicker plated conductor can be used. Alternatively, high-conductivity conductors such as copper or gold can be used instead of the aluminum commonly used in Si technologies. Advanced Si technologies (both Si CMOS and SiGe BiCMOS) now have a very thick (at least several microns thick) copper interconnect layer as the last metal. Inductor Qs approaching those typically found on semi-insulating substrates have been achieved. Use of inductors in the copper metal layer have replaced the use of "strapping" multiple thin aluminum layers together to synthesize effectively thicker metal in RFICs.

At low frequencies, the total dc resistance of the coil is given by

$$R_{\text{dc}} = \frac{\ell}{Wt\sigma} \tag{3.1}$$

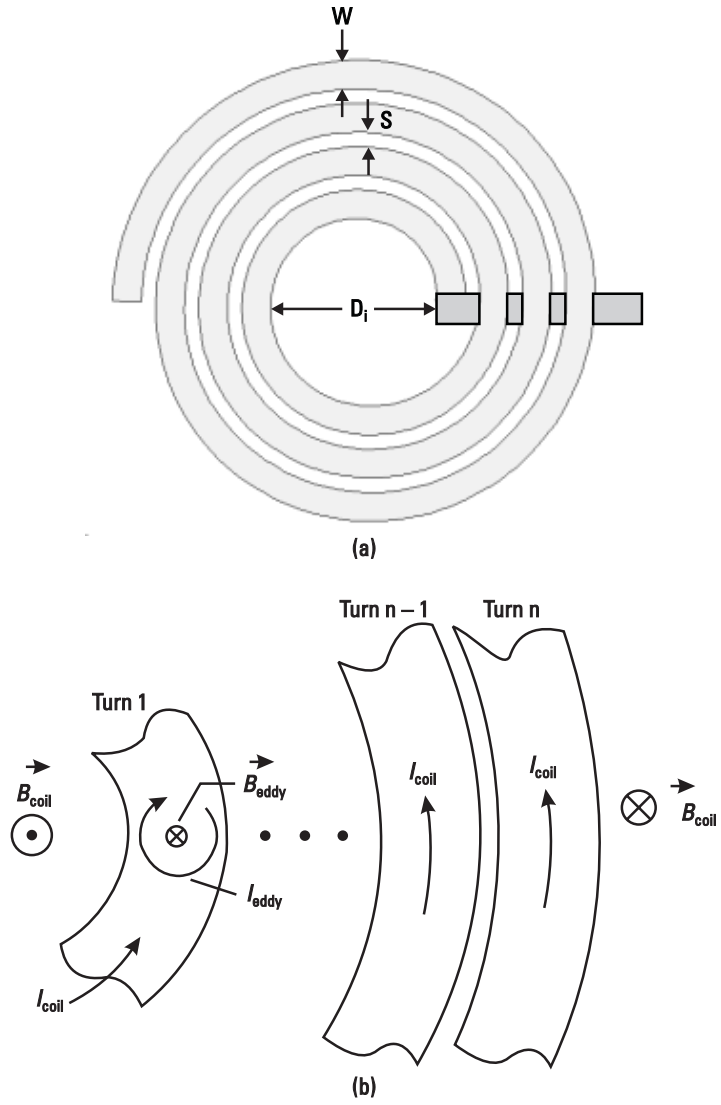


Figure 3.3 (a) A 3.5-turn circular inductor with dimensions. (b) Excitation and eddy currents, and fields in a coil. I_{coil} is the excitation current.

where W is the width, t is the thickness, ℓ is the total length of the conductor strip in the coil, and σ is the conductivity of the conductor material. At high frequencies, the above equation is modified and given as

$$R_{rf} = \frac{\ell}{W\sigma\delta(1 - e^{-t/\delta})} \tag{3.2}$$

where δ is the skin depth given by

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{3.3}$$

where μ is the magnetic permeability of the material. Because Si technologies use thin conductors $\cong$ 1 to 2 μm thick, at RF frequencies, $t/\delta < 1$, $R_{rf} \cong R_{dc}$. Table 3.3 compares conductivities and skin depth of various metals used. Silver has the maximum conductivity.

3.1.1.2 Eddy Current Resistance

The eddy current resistance in the inductor trace is a result of current crowding, that is, increasing current density along a part of the trace width. Consider a sector of an n-turn circular spiral inductor as shown in Figure 3.3(b). The inductor carries a current I_{coil} and the associated magnetic flux is B_{coil}. The magnetic flux lines enter the page plane at the far end of the turn n and come out of the page plane in the center of the coil, where they have maximum intensity. When there is not enough hollow space in the center of the coil, a large part of the magnetic flux also goes through the inner turns. According to Faraday-Lenz's law, when a conductor is moved into a magnetic field or a conductor is placed in a time-varying magnetic field, eddy currents are induced in the conductor in the direction where their self-flux is opposite to the applied magnetic field. Thus, as shown in Figure 3.3(b), circular eddy currents I_{eddy} are generated due to magnetic fields that go through the inner turns, and an opposing magnetic field B_{eddy} due to eddy currents is established.

The eddy current loops produced within the trace width cause nonuniform current flow in the inner coil turns. They add to the excitation current I_{coil} on the inside edge and subtract from the excitation current I_{coil} on the outside edge. Therefore, the inside edges of the coil carry current densities much larger than the outside edges, giving rise to a larger effective resistance compared to the case of uniform current flow throughout the trace width. Because the eddy

Table 3.3
Conductivity, Resistivity, and Skin Depth Values of Commonly Used Metals

Metal	Conductivity (10^5 s/cm)	Resistivity (10^{-6} Ω-cm)	Skin Depth (μm) @ 1 GHz	Skin Depth (μm) @ 10 GHz
Aluminum (Al)	3.8	2.6	2.57	0.81
Gold (Au)	4.1	2.4	2.50	0.79
Copper (Cu)	5.8	1.7	2.09	0.66
Silver (Ag)	6.2	1.6	2.02	0.64

currents are induced due to time-varying magnetic fields, their values are a strong function of frequency. The critical frequency f_c at which the current crowding begins to become significant is given by [40]

$$f_c = \frac{3.1(W+S)}{2\pi\mu_0 W^2} R_{sh} \tag{3.4}$$

where μ_0 is the free-space permeability and R_{sh} is the sheet resistance of the trace. An approximate expression for the series resistance is given by [40]

$$R_s = R_{dc}[1 + 0.1(f/f_c)^2] \tag{3.5}$$

The excitation of eddy currents can be minimized by cutting longitudinal slits in the inner turns' conductors or making the inner turns narrower and the outer turns wider. Because the contribution of the inner turns to the inductor's inductance is low because of its small area, removing them altogether or using a "hollow" coil reduces the effect of eddy currents.

An inductor's loss depends on the geometry of the inductor, metal conductivity, substrate resistivity, and frequency of operation. Metal losses dominate at low frequencies, whereas substrate losses are critical at high frequencies and are discussed next.

3.1.2 Substrate Loss

A major drawback of inductors on Si substrates (intrinsic or heavily doped) is the extra substrate resistive losses due to low resistivity of the substrates. The substrate loss consists of two parts: finite resistance due to electrically induced conductive and displacement currents, and magnetically induced eddy current resistance. These losses are known as capacitive and magnetic, respectively.

3.1.2.1 Capacitive Loss

When a coil is excited, a voltage difference occurs between the conductor and the grounded substrate that gives rise to capacitive coupling between the conductors. If the substrate is an insulator (i.e., very high resistivity) with a very low loss tangent value, the ohmic loss in the dielectric is negligible. When the substrate has finite resistivity, the penetration of the electric field into the substrate is limited (very low for a low-resistivity substrate). In this case, finite ohmic loss takes place, depending on the resistivity of the substrate. In low-resistivity substrates, such as in CMOS technology, the skin depth becomes on the order of the substrate thickness, giving rise to higher ohmic losses. Because this loss is coupled through the shunt capacitance, it is also commonly referred to as *capacitive* or *electric substrate loss.*

Finite resistivity loss can be minimized by either using very high resistivity substrates or by placing a shield between the oxide layer and the substrate.

3.1.2.3 Magnetic Loss

In heavily doped Si substrates, currents induced by the penetration of the magnetic fields of the inductor into the substrate cause extra resistive loss. Consider Figure 3.4, which shows magnetic field flux lines associated with the coil excitation current. The flux lines uniformly surround the inductor and penetrate into the substrate. As discussed in Section 3.1.1, due to the Faraday-Lenz law, loops of eddy currents I_{sub} flow in the low-resistivity substrate underneath the coil, with higher current density closer to the coil. The direction of I_{sub} is opposite to the direction of I_{coil}, giving rise to extra substrate loss. Because this loss is associated with magnetic fields, it is commonly referred to as *magnetic* or *inductive substrate loss.* Substrates with high resistivity have negligible magnetic loss.

In summary, by using narrow conductors that meet skin effect requirements ($W \cong 3\delta$) in the inner turns, using a hollow coil design, and using compact area coils, one can keep the substrate loss to a minimum. Because the magnetic field in a small coil penetrates less deeply into the substrate, eddy current loss is not severe as for large coils. Therefore, an optimum solution, in terms of inside dimensions and coil area for a given substrate, can be found. These losses are again discussed in detail in Section 3.1.5.

3.1.3 Layout Considerations

For a given inductance value, one would like to have the highest possible values of Q and SRF in the smallest possible area of an inductor using standard process

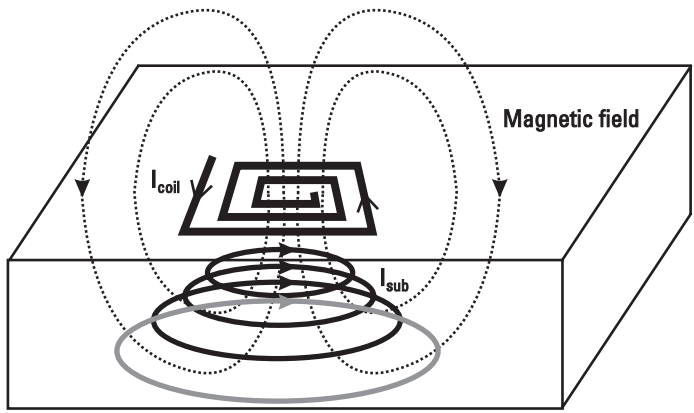


Figure 3.4 Currents and fields in a coil printed on a lossy Si substrate.

techniques. For the most part, the cost of the integrated chip dictates the inductor area, but the high-Q requirement may also be a deciding factor in low-noise and power amplifiers.

The operation of inductors on Si substrates can be classified into three regimes: inductor mode, resonator mode, and eddy current mode as described by Burghartz and Rejaei [60]. These three modes are determined by the resistivity of the Si wafers. Figure 3.5 shows the variations of $Q_{\max}$, the frequency at which the value of Q is maximum, $f(Q_{\max})$, SRF, and inductance at maximum quality factor, $L(Q_{\max})$, of a 2-nH inductor as a function of silicon resistivity. The value of maximum Q-factor of a 2-nH inductor on a 3.5-Ω-cm resistivity substrate varies from 5.5 to 7.5 when realized using various different values of n, W, S, and inner radius. The dimensions for the results in Figure 3.5 are based on average Q-value.

Both $Q_{\max}$ and $f(Q_{\max})$ increase with substrate resistivity in the inductor mode regime. In the resonator mode domain, both the $Q_{\max}$ and SRF drop drastically due to increased capacitive loss in the substrate. In this regime, after $Q_{\max}$ drops it increases slightly due to decreased capacitive loss with further reduction in the resistivity. Further decrease in the resistivity leads to the eddy current regime, where magnetic loss is greater than the capacitive loss and $Q_{\max}$ decreases further. From Figure 3.5 it is evident that the substrate resistivity should be greater than 30 and 0.3 Ω-cm to prevent the contributions of substrate's capacitive and magnetic losses, respectively. These numbers will vary slightly with the inductor's geometry. Figure 3.6 shows the values for inductance and the Q-factor for various combinations of the inductor's dimensions (width, spacing, inside diameter, and number of turns).

3.1.4 Inductor Model

The EC model for inductors discussed in Section 2.4 of Chapter 2 is based on the assumption that the substrate is lossless. However, a Si substrate is lossy; several different models for inductors on Si substrate have been reported in the literature to account accurately for the effect of a dielectric layer between the inductor coil and the Si substrate, and for capacitive and inductive losses in the substrate. The main difference in the models relates to the capacitive and inductive losses in the low-resistivity Si substrate.

Figure 3.7 shows various EC models that can be used to describe the characteristics of an inductor on a Si substrate. Various model parameters are described as follows:

R_s = series resistance of the inductor metal;

L = total inductance;

C_p = fringing capacitance between the inductor turns;

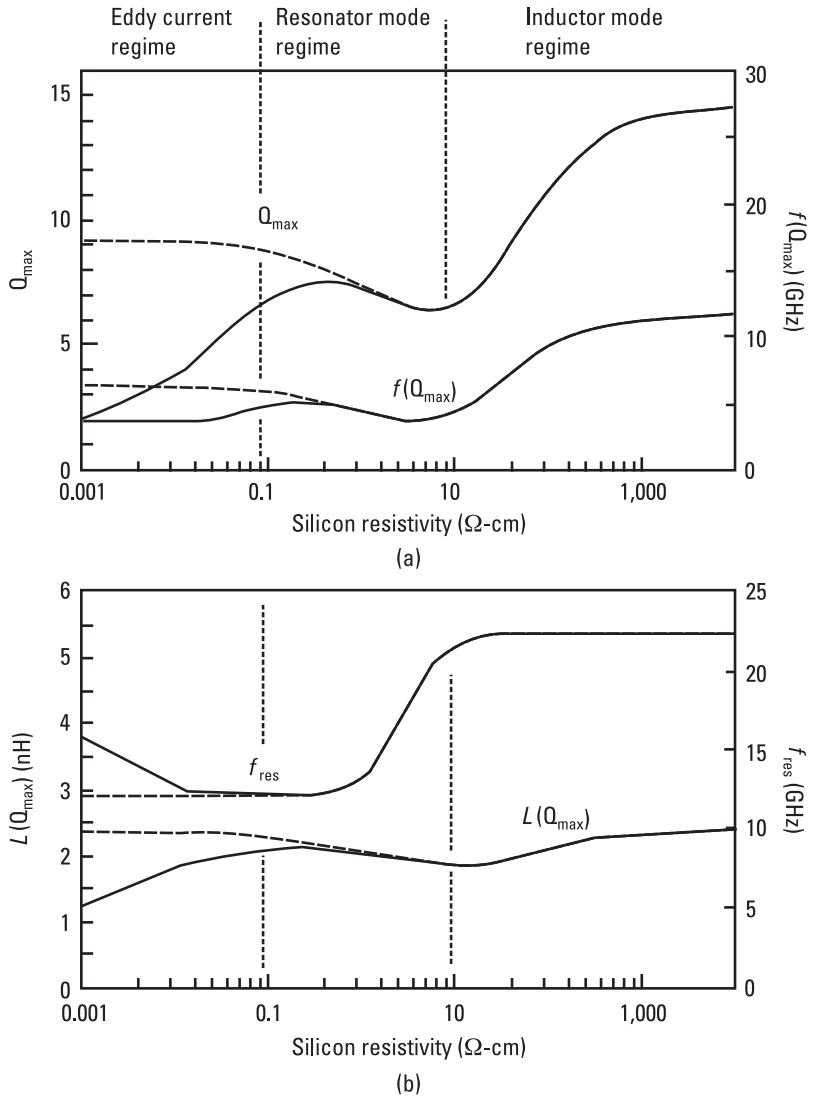


Figure 3.5 Dependence of the maximum quality factor (Q_{max}); the frequency at Q_{max}, $f(Q_{max})$; the inductance at Q_{max}, $L(Q_{max})$; and the self-resonance frequency (f_{res}) on the substrate resistivity (ρ_{Si}) with (solid lines) and without (dotted lines) consideration of eddy current in the substrate. The three regimes, in inductor mode (resonance through C_p) at >10 Ω-cm, in resonator mode (resonance through C_{0x}) at 0.1 to 10 Ω-cm, and with considerable eddy current at <0.1 Ω-cm are indicated. (*From:* [60]. © 2003 IEEE. Reprinted with permission.)

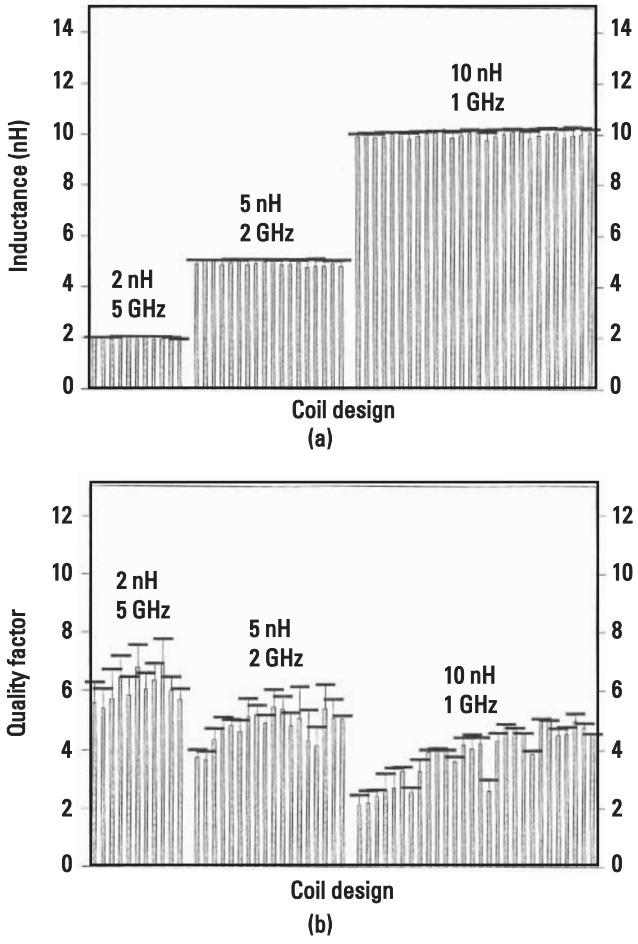


Figure 3.6 Comparison of measured (vertical bars) and simulated (small horizontal bars) values of (a) inductances and (b) quality factors (Q) of 57 circular spiral coils (T_{M4} = 1 μm; T_{0x} = 4 μm; ρ_{Si} = 2.5–3.5 Ω-cm) having optimum metal widths (W = 4–23 μm) and spaces (S = 3–16 μm) for given radius (R = 60–220 μm) and numbers of turns (n = 2–8). (*From:* [60]. © 2003 IEEE. Reprinted with permission.)

$C_{ox1,2}$ = shunt capacitances of the oxide layer;

$C_{sb1,2}$ = total shunt capacitance of the dielectric layers and substrate;

$R_{sb1,2}$ = shunt resistance due to substrate losses;

R_{se} = parallel resistance due to eddy current loss in the substrate.

Figure 3.7(a, b) describes commonly used EC models. These models are electrically identical when the shunt series arrangement is converted into a

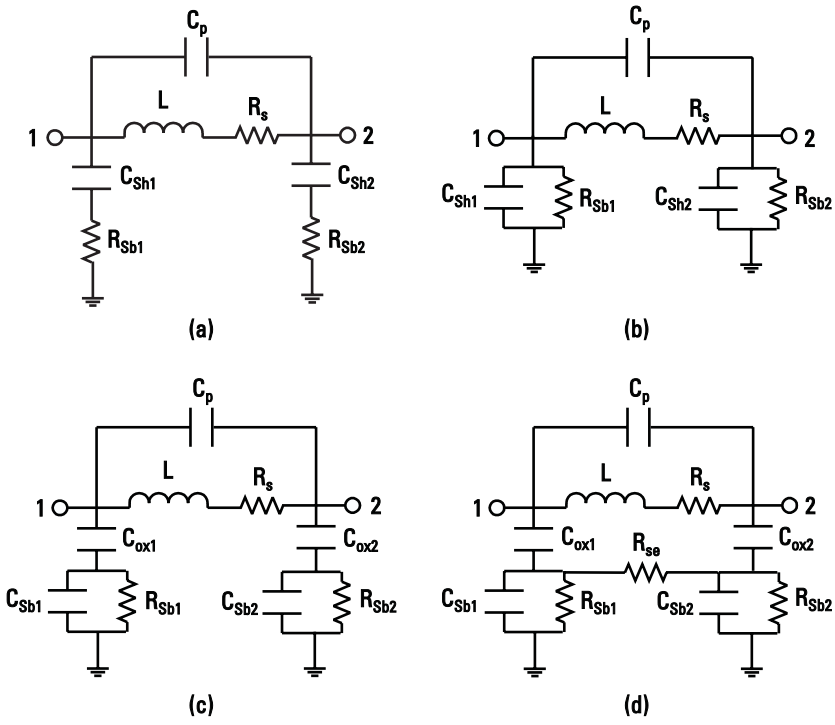


Figure 3.7 (a–d) Equivalent circuit models used for characterizing coil inductors on Si substrate.

parallel combination. Here the oxide layer capacitance is absorbed into the substrate capacitance. Figure 3.7(c) shows a more detailed version of the above model in which another capacitor C_{sb} has been added that accounts for capacitive coupling to the lossy substrate. The above-mentioned models predict reasonably well the behavior of an inductor on a Si substrate. A more accurate model includes substrate resistance, R_{se}, as shown in Figure 3.7(d), and accounts for the magnetic coupling between the spiral and low-resistivity CMOS Si substrate. The magnetic field generated by the current on the spiral induces current in the Si substrate, which has the opposite polarity, giving rise to R_{se} resistance. In a simple way, if the R_{se} term is not used in the model it becomes a part of R_{sb}.

Thus, series element values depend on the properties and dimensions of the inductor conductor trace, whereas the shunt element values are determined by the dielectric parameters between the inductor and the substrate, substrate doping, and thickness and substrate parameters. Shunt values at ports 1 and 2 are not the same due to asymmetry in the inductor trace and the connections

between the inductor and ports. As a first-order approximation, shunt values for ports 1 and 2 can be assumed identical.

3.1.5 *Q*-Enhancement Techniques

One of the important characteristics of an inductor on a Si substrate is its quality factor Q. Techniques used to enhance the Q-factor of inductors on a Si substrate can be grouped into four categories as shown in Figure 3.8. These are based on trace layout, trace metal parameters, the use of a high resistivity substrate, and the use of a substrate shield. These are discussed in this section.

3.1.5.1 Trace Layout

For a given set of inductor conductor and substrate materials, one can optimize the inductor's Q by properly selecting the physical layout of the inductor trace to minimize the resistive, capacitive, and inductive losses. Several techniques discussed in the literature include variable line width [21, 38], differential configuration [22, 57], and vertical inductor.

Variable Line Width

The effect of eddy currents can be minimized by making the line widths of the inner turns of the inductor narrower than the outer turns [21, 38]. Narrower line widths have higher dc resistance; however, this is compensated by using wider line widths in the outer turns. This structure is shown in Figure 3.9(a). In this structure the improvement in Q-value is more pronounced at higher than lower frequencies, because the effect of eddy currents is more severe at high frequencies.

For inductors having variable line width on a conducting Si substrate, no substantial improvement in Q is possible, because of excessive capacitive losses

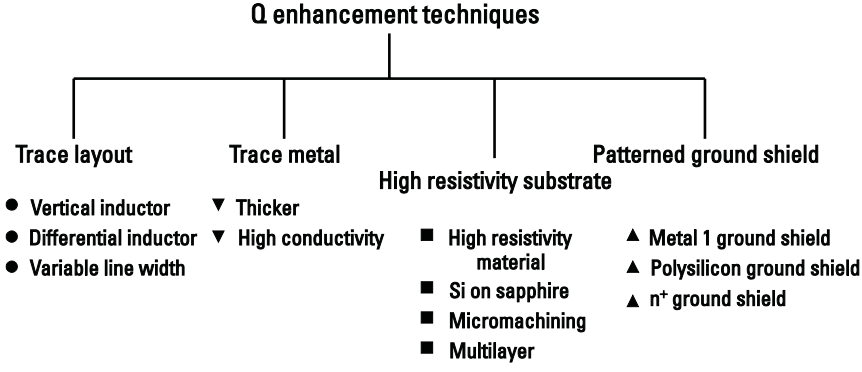


Figure 3.8 *Q*-Enhancement techniques for inductors on Si substrate.

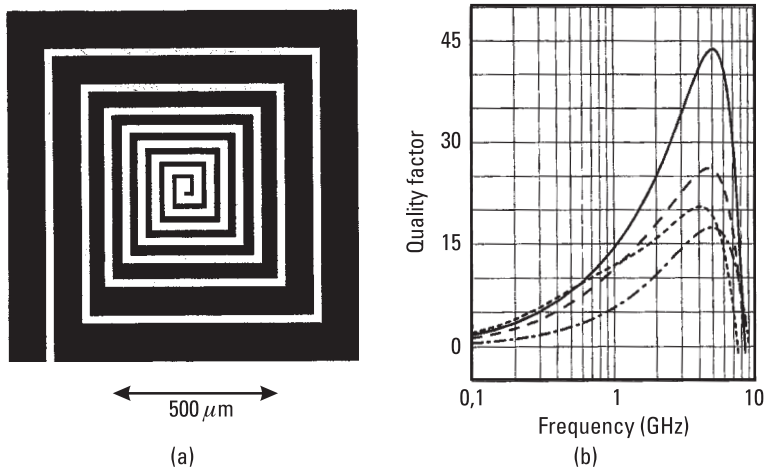


Figure 3.9 (a) Variable width layout of an inductor. (b) Simulated Q-factor of 20-nH inductors for several line widths. Optimum layout (———), 25 μm (— — —), 40 μm (– – – –), and 10 μm (— · — · —). (*From:* [38]. © 2000 IEEE. Reprinted with permission.)

through the substrate. However, improvement can be achieved by reducing the capacitive losses by using a multilayer dielectric Si technology or micromachining technology as discussed later in this section.

Figure 3.9(b) shows simulated results for four different 20-nH inductors using eight turns optimized for operation at 3.5 GHz. Three inductors have constant line widths of 10, 25, and 40 μm, whereas the optimized layout inductor has inner and outer segments line width of 10 and 130 μm, respectively. The spacing between the turns was 30 μm. In all four inductors, the Si substrate below the inductor pattern was removed using micromachining techniques. The maximum Q-value for the optimized layout inductor was about 43 compared to 26 obtained for the 25-μm constant line width inductor, which had the largest simulated Q of all the three cases.

Differential Excitation

The Q-enhancement of planar inductors can also be achieved by using the differential excitation technique [22, 57]. Differential circuit topologies are used at RF frequencies because they are less susceptible to supply noise present in on-chip bias lines, offer common-mode rejection, and minimize even-order mixing products [57]. Commonly used ICs that employ these inductors are differential VCOs, double-balanced mixers, Gilbert cell mixers, and differential amplifiers. Spiral inductors excited differentially play an important role in these circuits. The Q-factor of such inductors is enhanced because of smaller substrate loss and is maintained over a broader bandwidth [22] compared to the single-ended configuration.

Five-turn conventional and differential inductors having 8-nH inductance fabricated on a 15-ohm-cm silicon substrate were characterized. The differential test structure is shown in Figure 3.10(a). The line width, spacing, and inner and outer dimensions were 8, 2.8, 150, and 250 μm, respectively. The measured and simulated Q-values for both single-ended and differential inductors are compared in Figure 3.10(b). The differential configuration has higher peak Q-values and a wider operating bandwidth.

Vertical Inductors

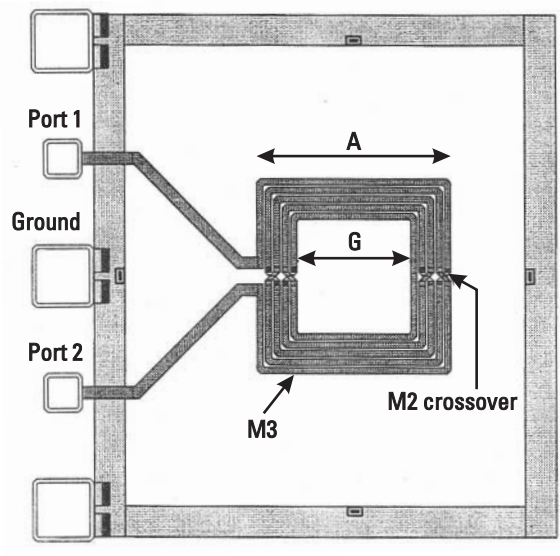
A vertical inductor, popularly known as a solenoid inductor, has higher Q than a planar inductor because of lower capacitive and magnetic losses from the lossy Si substrate. Solenoid inductors on a Si substrate were fabricated using micromachining techniques [43]. In this example a thick photoresistive epoxy mold was used and the Cu-electroplated solenoid coil was built on top of the 50-μm-thick epoxy mold above the CMOS Si substrate. Figure 3.11 shows a 6-turn micromachined solenoid inductor. The spacing between the coil and the substrate results in lower substrate capacitive and magnetic losses and higher Q-factor and SRF. The Cu trace was 20 μm wide and 20 μm thick with an 80-μm turn-to-turn pitch. The measured values for the inductance and peak Q of a 6-turn inductor at 4.5 GHz were 2.6 nH and 21, respectively.

3.1.5.2 High-Resistivity Substrates

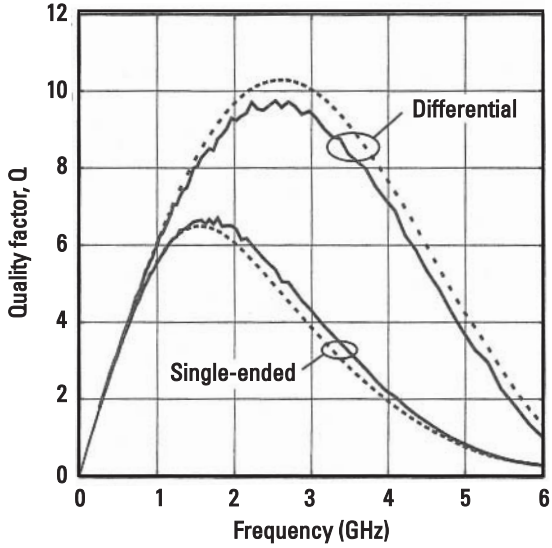
Many techniques have been used to improve the Q-factor of inductors by reducing substrate loss, especially capacitive loss. These include using high-resistivity silicon substrates [5], silicon on sapphire [9, 18] or glass or quartz, using an oxidized porous silicon substrate [15, 25], removing the silicon underneath the inductor by micromachining techniques [39], and building inductors on a multilayer structure using low dielectric constant materials between the trace and the Si substrate [20, 23, 32, 54, 58]. The primary objective in all of these techniques is to either put the inductor trace on an insulator or to increase the distance between the trace and the lossy substrate.

Multilayer Techniques

Figure 3.12(a) shows a schematic cross-sectional view of an inductor fabricated on a multilayer substrate (polyimide–SiO_2–Si). The line width, spacing, and outer dimensions were 16, 16, and 432×448 μm, respectively [23]. SiO_2 and Si MOSFET substrate thicknesses were 0.5 and 450 μm, respectively. The measured inductance and dc resistance of a 6-turn gold-conductor inductor were 10 nH and 1.3Ω, respectively. Figure 3.12(c) shows the measured Q-factor and SRF as a function of polyimide thickness. As a benchmark, the Q-value of a similar inductor on a GaAs substrate is also shown. For a polyimide thickness of 60 μm, the Q-value is about 14 and the resonant frequency is about 9 GHz.



(a)



(b)

Figure 3.10 (a) Five-turn spiral inductor in differential configuration. (b) Simulated (dashed line) and measured (solid line) Q-factor values of single-ended and differential inductor configurations. (*From:* [22]. © 1998 IEEE. Reprinted with permission.)

Figure 3.11 Photograph of a micromachined 6-turn solenoid inductor. (*From:* [43]. © 2001 IEEE. Reprinted with permission.)

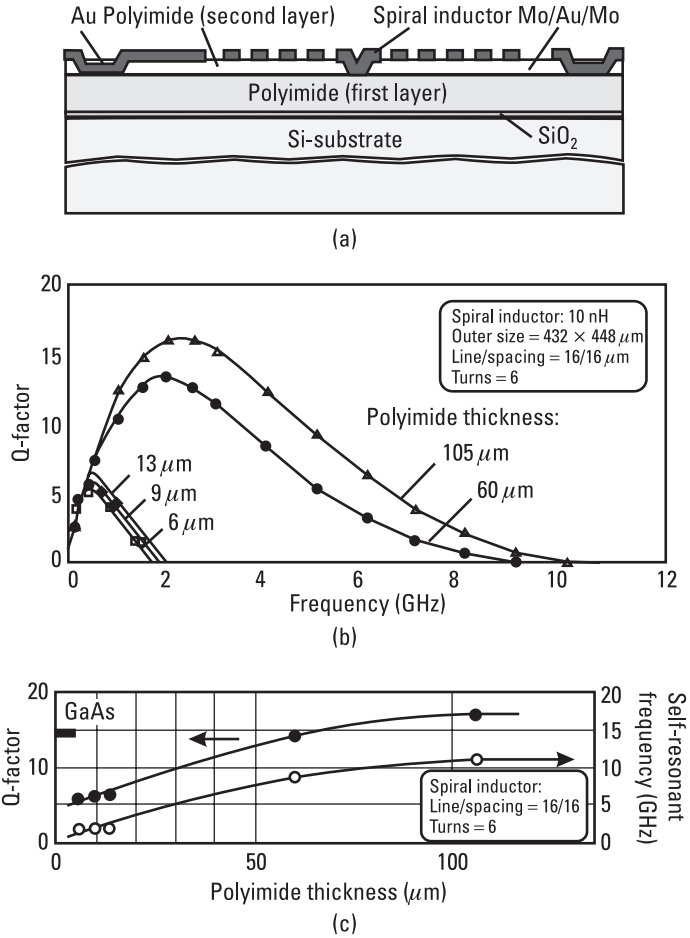


Figure 3.12 (a) Cross-sectional view of a spiral inductor fabricated on a polyimide–SiO_2–Si substrate. (b) Measured Q-factor versus frequency of 10-nH inductors on Si substrate for different polyimide thicknesses. (c) Measured Q-and SRF versus polyimide thickness of 10-nH inductors. (*From:* [23]. © 1998 IEEE. Reprinted with permission.)

The Q of an inductor can be further enhanced by reducing the conductor resistance using thick Cu metal [54]. The test data obtained for various inductors on a CMOS-grade p-type silicon substrate with a resistivity of 20 Ω-cm is summarized in Table 3.4. The maximum Q-value for several inductance values is at 2 GHz.

Micromachined Inductors

The quality factor of inductors on a Si substrate has been improved using micromachining techniques [4, 33, 39, 61–63] as described in Chapter 13. In this method the Si substrate is removed underneath the planar inductor pattern by a chemical etching process, which results in much lower capacitive loss and increased self-resonant frequency due to the reduction of interturn and substrate parasitic capacitances.

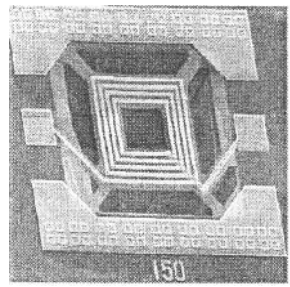
Inductors were realized by placing crossover connections on a Si_3N_4 membrane using 0.6-μm-thick metal 1 and the inductor pattern on SiO_2 using 1.4-μm-thick metal 2. The p-type Si substrate had a resistivity value of 3.5 Ω-cm. A photograph of a 4.25-turn inductor is shown in Figure 3.13(a). Measured and simulated inductance and Q-values [61] for several inductors are shown in Figure 3.13(b, c). As shown, the Q-values for suspended inductors, because of negligible substrate loss, are much higher than typically obtained Q-values of 4 to 6 for similar inductors when directly printed on Si substrates [2, 3]. Normally, metal layers used in Si technology are of aluminum and have thicknesses on the order of one skin depth. The Q-values of suspended inductors are further enhanced by using thick Cu metal layers.

In silicon technology, copper interconnects have been introduced to improve the Q-factors of passive components including inductors and capacitors.

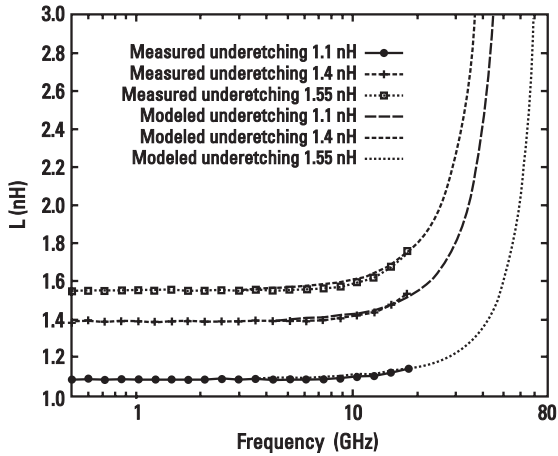
Table 3.4
Summary of Q-Values for Various Conductor and Multilayer Dielectric Thicknesses

Inductance (nH)	Metal Thickness (μm)	BCB Thickness (μm)	Max Q-Value*
1.0	0.8	6.0	6.5
1.0	1.2	6.0	10.8
1.0	3.2	6.0	16.1
1.0	15.0	6.0	25.4
3.2	6.0	6.0	23.0
5.2	6.0	6.0	20.0
1.0	6.0	6.0	25.0
1.0	6.0	12.0	28.0

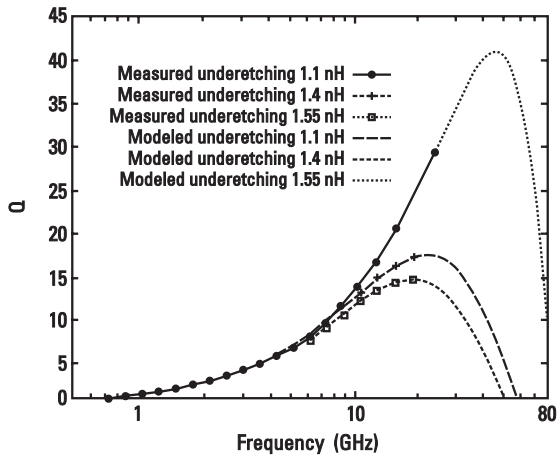
*Maximum Q-value is at about 2 GHz.



(a)



(b)



(c)

Figure 3.13 (a) Micromachined 4.25-turn inductor configuration. (b) Simulated and measured inductance versus frequency of a 4.25-turn micromachined inductor. (c) Simulated and measured Q-value versus frequency. (*From:* [61]. © 1996 IEEE. Reprinted with permission.)

Table 3.5 compares conventional and micromachined inductor measured data for 4-turn spiral inductors fabricated with 0.18-μm Si CMOS technology using a 6-level copper interconnect and low-K dielectrics. The line width and spacing were 20 and 10 μm, respectively. In Table 3.5, "Q_{max} conv." and "Q_{max} LC" were calculated using (2.12) and (2.11), respectively. For the smaller diameter inductor, the maximum Q and f_{res} values for a micromachined inductor are 12.5 and 14.0 GHz as compared to 4.39 and 10.1 GHz for conventional inductors on Si substrate.

To provide an electromagnetic shield and to reduce the crosstalk between circuits in a MMIC, a cavity backed suspended inductor can be used [62]. In this configuration, the etched cavity (both bottom surface and sidewalls) is metallized with copper as shown in Figure 3.14(a). The spiral inductor consists of electroless plated copper on polysilicon. It has been reported that this topology can withstand high shock and vibration requirements. Figure 3.14(b) shows the top view of a 2.5-turn rectangular spiral inductor and Table 3.6 summarizes various parameters. Here, n is the number of turns, W is the width of the inductor, S is the spacing between turns, d is the inner diameter, t_s is the thickness of the polysilicon conductor, W_o is the width of the overpass conductor, d_c is the depth of the cavity, t is the thickness of the copper deposited, and d_e is the separation between the spiral and the cavity wall. The inductor model is represented by a parallel combination of a capacitor C_p and an inductor L in series with a resistor R_s as shown in Figure 2.17(b) in Chapter 2, and the values measured at 1 GHz along with Q_{max} values are given in Table 3.6. The variations of self-inductance L and parasitic capacitance C_p as a function of cavity depth are shown in Figure 3.14(c, d), respectively, and the data show that a cavity depth of 40 to 50 μm is sufficient to achieve the minimum value of C_p. The self-resonant frequency f_{res} of an inductor is estimated by using

Table 3.5
Summary of Conventional and Micromachined Four-Turn Inductor Measured Parameters on Si Substrate

Parameter	Conventional	Micromachined	Conventional	Micromachined
L_m (nH)	3.16	3.19	4.61	4.69
Q_{max} conv.	4.39	12.5	3.64	7.61
@ f (GHz)	1.75	7.75	1.25	4.75
R_{dc} (Ω)	3.45	3.32	5.28	5.21
Q_{max} LC	4.43	25.7	3.50	10.3
@ f (GHz)	2.05	13.7	1.45	6.80
f_{res} (GHz)	10.1	14.0	6.65	11.38
Diameter (μm)	300	300	365	365

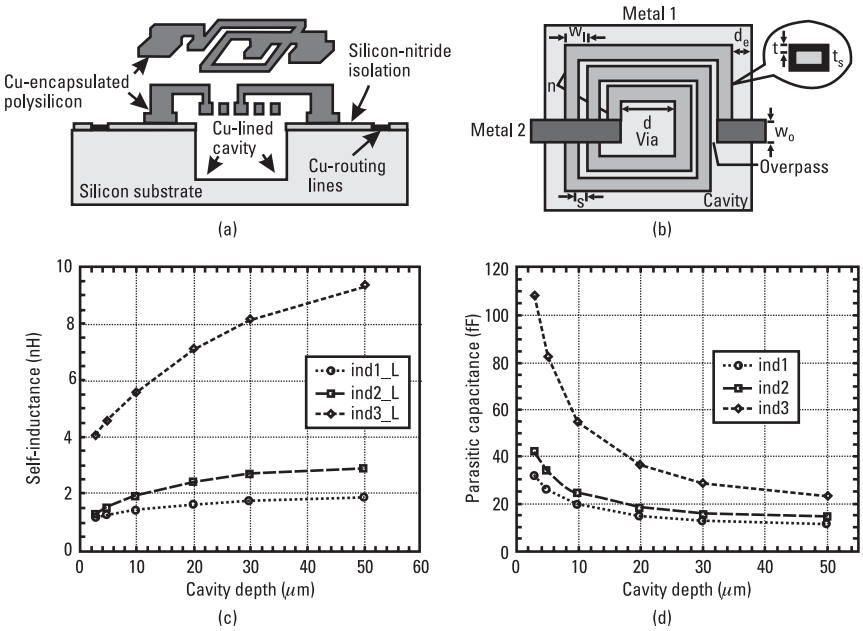


Figure 3.14 (a) Cavity-backed membrane suspended inductor; (b) top view of a 2.5-turn inductor, with dimensions; and (c, d) inductance and capacitance versus cavity depth, respectively. (*From:* [62]. © 2000 IEEE. Reprinted with permission.)

Table 3.6
Summary of Cavity-Backed Three Inductor Parameters and Measured Data

Parameters	Ind1	Ind2	Ind3
n	3	5	7
W (μm)	3	5	6
S (μm)	3	3	4
d (μm)	125	75	125
t_s (μm)	1.5	1.5	1.5
W_o (μm)	18	18	18
d_c (μm)	30	30	30
t (μm)	0.75	0.75	0.75
d_e (μm)	30	30	30
$L\|_{1GHz}$ (nH)	1.8	2.7	8.2
C_p (fF)	13.1	16.0	28.9
$R_{s\|1GHz}$ (Ω)	2.7	3.7	8.4
Q_{max}	23	36	30

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{LC_p}} \tag{3.6}$$

For $L = 8$ nH and $C_p = 0.03$ pF, the SRF is 10.27 GHz.

3.1.5.3 Patterned Ground Shield

Several techniques have been discussed in the literature to reduce substrate loss by placing an EM shield between the trace and substrate. These include *metal ground shield* (MGS), *polysilicon ground shield* (PGS), and n^+ *ground shield* (NGS). Solid ground shields result in very large capacitances between the trace and the ground plane, lower inductance, and SRF. Therefore, solid shields are not used; instead, patterned ground shields are preferred in which slots are cut perpendicular to the traces of the inductor or the flow of eddy currents. Such slots block the eddy current flow and reduce the magnetic loss. They also allow partial passing of the electric field, lowering the capacitive loss without increasing the parasitic capacitance appreciably. The effectiveness of a patterned ground shield on the improvement of Q depends on several factors including the resistivity of the Si substrate and ground shield metal, the thickness of the shield metal, the shield pattern type, the oxide layer's dielectric constant and thickness, the inductor layout and the frequency of operation. Among MGS, PGS, and NGS techniques, NGS is considered to be the most robust. Figure 3.15 shows a rectangular spiral inductor with a patterned n^+ ground shield underneath [44].

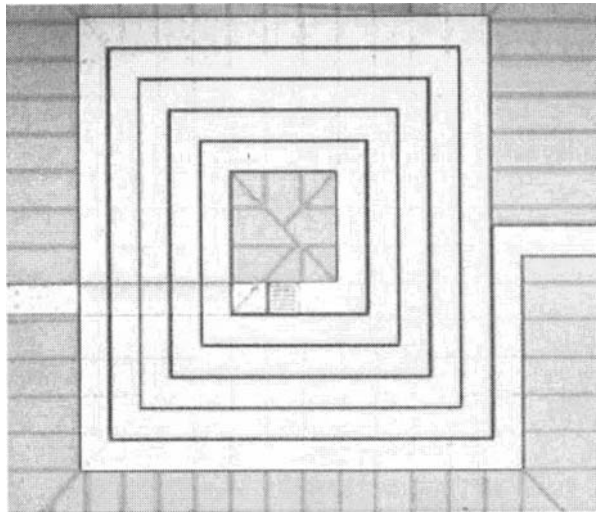


Figure 3.15 Spiral inductor with a patterned ground shield underneath on a Si substrate. (*From:* [44]. © 2001 IEEE. Reprinted with permission.)

The contribution of resistive, inductive, and capacitive losses in the Q-calculations of the PGS inductor can be analyzed by simplifying the EC shown in Figure 3.7(c) to one port, that is, port 2 grounded. In this case a simplified EC is shown in Figure 3.16, where

$$R_p = \frac{1}{\omega^2 C_{ox1}^2 R_{sb1}} + \frac{R_{sb1}(C_{ox1} + C_{sb1})^2}{C_{ox1}^2} \tag{3.7}$$

$$C_{cp} = C_{ox1} \cdot \frac{1 + \omega^2 (C_{ox1} + C_{sb1}) C_{sb1} R_{sb1}^2}{1 + \omega^2 (C_{ox1} + C_{sb1})^2 R_{sb1}^2} \tag{3.8}$$

From (2.12),

$$Q = \frac{\omega L}{R_s} \cdot \frac{R_p}{R_p + \left[\left(\frac{\omega L}{R_s}\right)^2 + 1\right] R_s} \cdot \left[1 - \frac{R_s^2 (C_{cp} + C_p)}{L} - \omega^2 L (C_{cp} + C_p)\right]$$

$$= \frac{\omega L}{R_s} \cdot \text{resistor load factor} \cdot \text{capacitor loss factor} \tag{3.9}$$

Here both the resistor and capacitor loss factors are less than unity. Thus, the Q-value can be enhanced by making both loss factors close to unity. From (3.9) it is evident that the resistor loss factor becomes unity when the value of R_p from (3.7) is very large; that is, R_{sb1} is very small (when ground shields provide a low-resistance ground path) or R_{sb1} is very large (replacing the substrate with an insulator). All of the patterned ground shields reduce R_{sb1} or improve the resistive loss factor. However, they also introduce additional parasitic capacitance to C_{ox1} and C_{sb1}, which can degrade both loss factors. Due to the short distance between the spiral and ground, the MGS and PGS configurations increase these capacitances much more than the NGS topology. This means

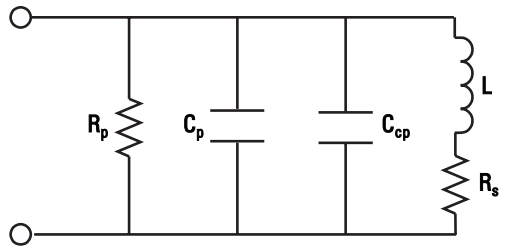


Figure 3.16 Simplified one-port inductor model.

that NGS is the most robust technique to enhance the Q-factor by about 20% to 30% [44].

One of the undesirable features of the ground shield technique is lower and more pronounced SRF due to higher substrate capacitance and lower substrate loss, respectively.

3.1.6 Stacked-Coil Inductor

To realize very large inductances per unit area, the stacked or multilevel inductor configuration is used. In this case, as shown in Figure 3.17(a), two inductor layers are placed on top of each other and connected in series. Because two-level inductor conductors are connected in such a way that the RF current flows in the same direction through both of the inductor traces, the magnetic flux lines add in phase and result in higher mutual inductance. A simplified EC of a stacked inductor is shown in Figure 3.17(b) and total inductance (L_t) is given by

$$L_t = L_1 + L_2 + 2M \tag{3.10}$$

where L_1 and L_2 are the self-inductances of spirals 1 and 2 and M is the mutual inductance between them. The dots in Figure 3.17(b) represent the current flowing in the same direction through the spirals. If k is the coupling between the spirals, M can be written

$$M = k\sqrt{L_1 L_2} \tag{3.11a}$$

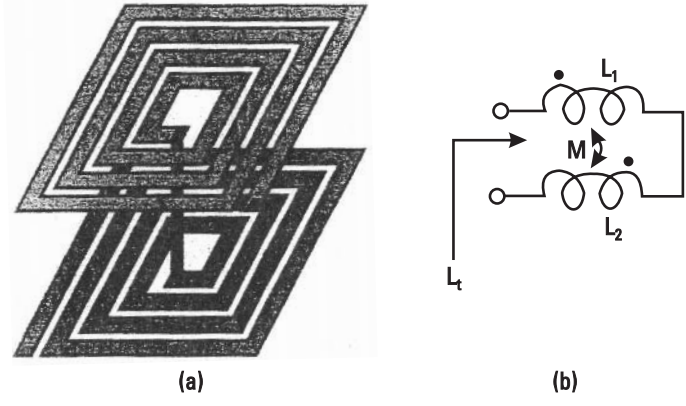


Figure 3.17 (a) Two-level inductor configuration. (b) Simplified two-port EC.

When both spirals are identical (i.e., $L_1 = L_2 = L$) and tightly coupled ($k \cong 1$), the total inductance becomes

$$L_t \cong 4L \cong 2^2 L \tag{3.11b}$$

Thus the maximum inductance value by stacking two spirals can be increased by a factor of 4. Similarly, for n stacked spirals, the total inductance of the structure is n^2 times that of one spiral; that is, inductance can be increased quadratically with the number of layers and therefore, very compact inductors can be realized.

In silicon technology, stacked inductors can be realized by using multilevel interconnects [8, 42, 48, 60]. Thus, very compact inductors can be realized using the four to five metal layers typically available in CMOS technologies. In these technologies, the top layer thickness is about 2 μm, whereas other metal layers are about 1 μm thick and the oxide layers are about 1 to 1.5 μm thick. The Si substrate resistivity is about 0.01 Ω-cm. Because the metal layers are very close to each other, the coupling coefficient k is close to unity and results in large parasitic capacitances between the metal layers. This leads to reduced SRF. The SRF is also affected by the maximum thickness of the oxide layer that can be deposited. The oxide thickness affects the SRF much more than it affects the Q- and L-values because the vertical dimensions are much smaller than the lateral dimensions and the substrate loss remains unchanged. Therefore, one can select various metal layers to realize the required inductance with the highest possible SRF by keeping a larger spacing between the spiral levels.

Figure 3.18 shows two configurations for a two-layer inductor. The SRF of a two-layer inductor using M_5 and M_3 is higher than the inductor using M_5 and M_4 because of reduced interlayer capacitance. For a typical CMOS technology with five metal layers, the parasitic capacitance between metal layers, bottom metal and substrate, and C_{eq} are given in Table 3.7. Here for two-layer and multilayer structures, the expressions for C_{eq} are given by [42]

$$C_{\text{eq}} = \frac{1}{12}(4C_1 + C_2) \qquad \text{two-layer} \tag{3.12a}$$

$$= \frac{1}{3n^2}\left(4\sum_{i=1}^{n-1} C_i + C_n\right) \qquad n\text{-layer} \tag{3.12b}$$

The resonant frequency is given by

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_t C_{\text{eq}}}} \tag{3.13}$$

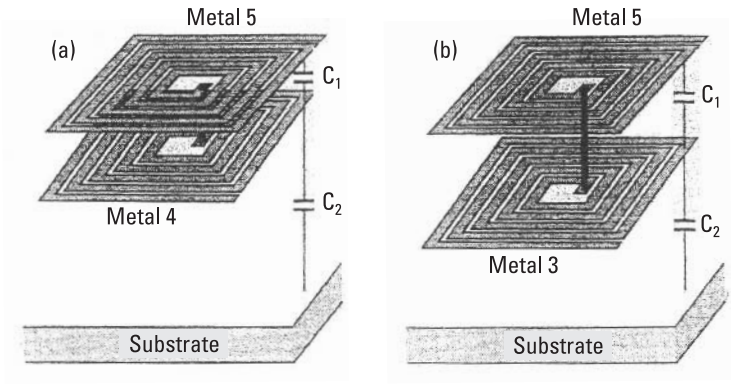


Figure 3.18 Two-level inductor fabricated using (a) metal 5 and metal 4 and (b) metal 5 and metal 3 layers. (*From:* [42]. © 2001 IEEE. Reprinted with permission.)

Table 3.7
Approximate Parasitic Capacitance Between Metal Layers and Metal and Si Substrate

Metal A	Metal B	C_1 (pF/μm^2) Metal A–Metal B	C_2 (pF/μm^2) Metal B–Substrate	C_{eq} (pF/μm^2)
M_5	M_4	40	6	14
M_5	M_3	14	9	5.4
M_5	M_2	9	12	4.0

M_i designates the metal i layer.

where L_t is the total inductance of the stacked inductor. From Table 3.7 it is obvious that the SRF of a two-layer inductor using M_5 and M_2 is about twice that of the inductor using M_5 and M_4 layers. Also (3.12a) and (3.12b) suggest that the effect of interlayer capacitance C_1 is about four times more than the bottom-layer capacitance C_2. Figure 3.19(a) shows a three-layer inductor.

Table 3.8 summarizes the measured performance of nine inductors characterized using 0.25-μm CMOS technology. Assuming a single-layer inductance of about 13 nH (45 nH divided by about 3.5) in 240 μm^2 square area, a five-layer inductor has about 20 times more inductance compared to the conventional inductor of the same physical area, using the same conductor dimensions and spacings.

An alternative approach for a multilevel inductor having about four times lower C_{eq} has been reported [48]. Figure 3.19(b) shows the four-layer inductor wiring diagram with current flow. Due to slightly lower inductance value, this configuration has a SRF that is approximately 34% higher than the conventional stacked inductor.

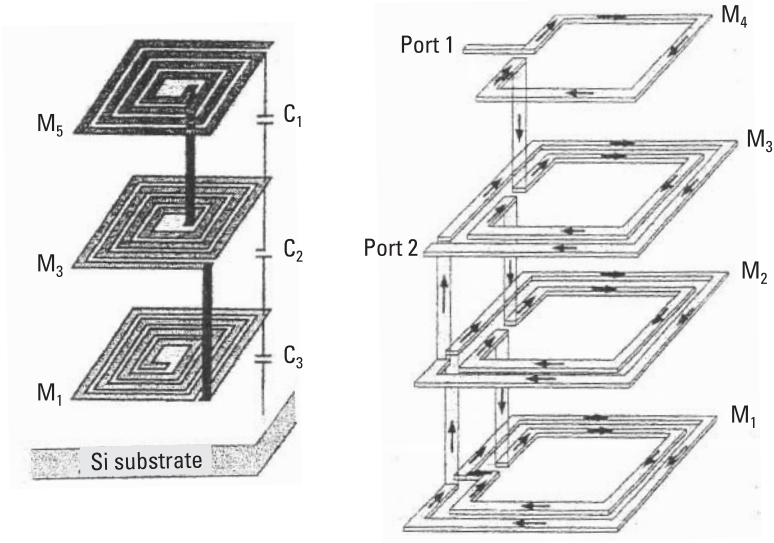


Figure 3.19 (a) Conventional three-level inductor using metals 5, 3, and 1 on a Si substrate. (b) Improved SRF four-level stacked inductor with current flow path. (*From:* [48]. © 2002 IEEE. Reprinted with permission.)

Table 3.8
Summary of Measured Performance of Stacked Inductors Fabricated in 0.25-μm CMOS Technology*

Inductor	Metal Layers	Number of Turns	L (nH)	Measured f_{res} (GHz)
L_1 (240 μm)^2	5,4	7	45	0.92
L_2 (240 μm)^2	5,3	7	45	1.5
L_3 (240 μm)^2	5,2	7	45	1.8
L_4 (240 μm)^2	5,4,3	7	100	0.7
L_5 (240 μm)^2	5,3,1	7	100	1.0
L_6 (200 μm)^2	5,2,1	5	50	1.5
L_7 (200 μm)^2	5,2,1	5	48	1.5
L_8 (240 μm)^2	5,4,3,2	7	180	0.55
L_9 (240 μm)^2	5,4,3,2,1	7	266	0.47

*Line width = 9 μm; line spacing = 0.72 μm.

3.1.7 Temperature Dependence

Spiral inductors on a Si substrate were also characterized [16] over temperature range −55°C to +125°C. Figure 3.20 shows the top and side views of a 6-turn inductor studied for this purpose. The line width and spacing were 16 and

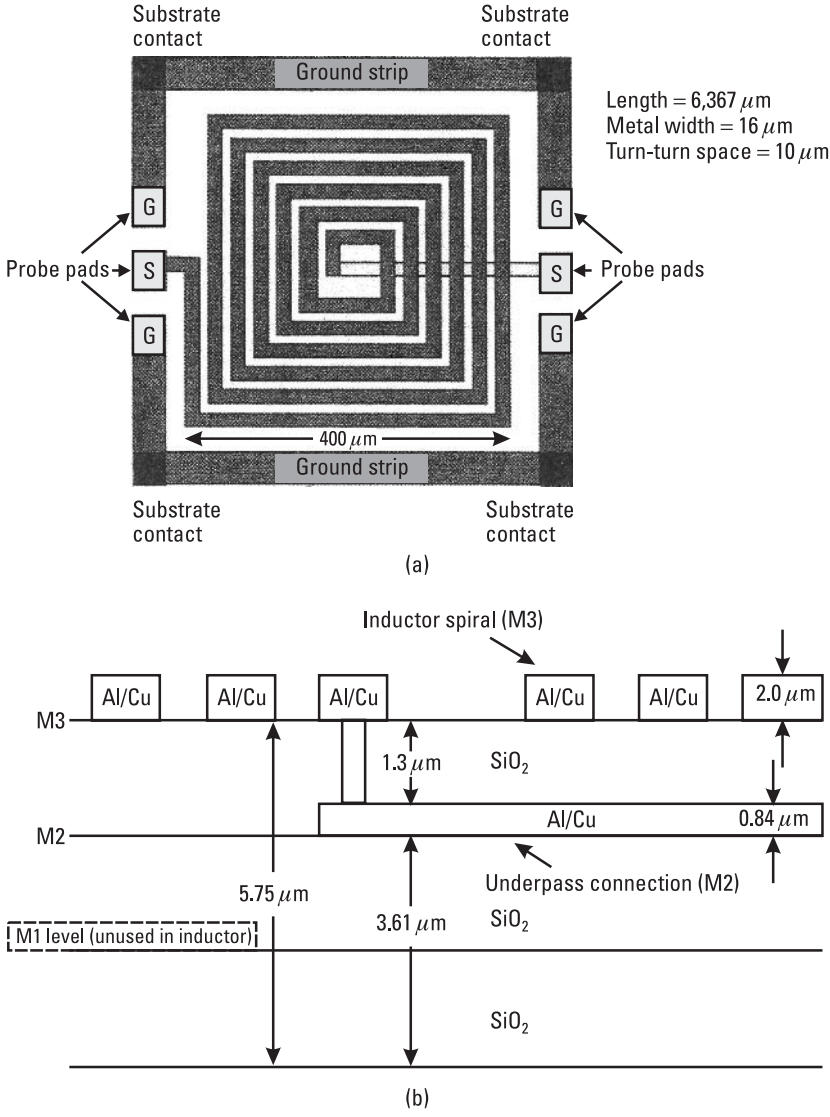


Figure 3.20 (a) Top view of a 6-turn inductor on a Si substrate with ground signal ground pads for RF probe. (b) Cross-sectional view of the inductor with various dimensions. (*From:* [16]. © 1997 IEEE. Reprinted with permission.)

10 μm, respectively. Top and underpass connection metallizations were of aluminum. The inductance, Q, and f_{res} values at 25°C were 10.5 nH and 5.8 at 1 GHz and 4 GHz, respectively.

The inductor's S-parameters were measured using RF probes over the temperature range from −55°C to +125°C. The modeled value of inductance was almost constant with temperature below f_{res}. Figure 3.21 shows the variation of inductance, Q, normalized metal resistance, and substrate resistance and capacitance. Both resistance values doubled from −55°C to 125°C. The Q-value decreases with increasing temperature below 2 GHz and increases with increasing temperature above 2 GHz. At low frequencies (below 2 GHz in this case), the primary loss in the inductor is due to the series resistance of the conductor. However, at higher frequencies (above 2 GHz), the capacitive reactance decreases and more currents start flowing through the substrate and thus more power is dissipated in the substrate. Figure 3.21(b) indicates that below 2 GHz, the variation of Q is dominated by the conductor loss, whereas above 2 GHz, substrate loss becomes more pronounced. The decreased value of capacitance with temperature results in lower substrate loss above 2 GHz.

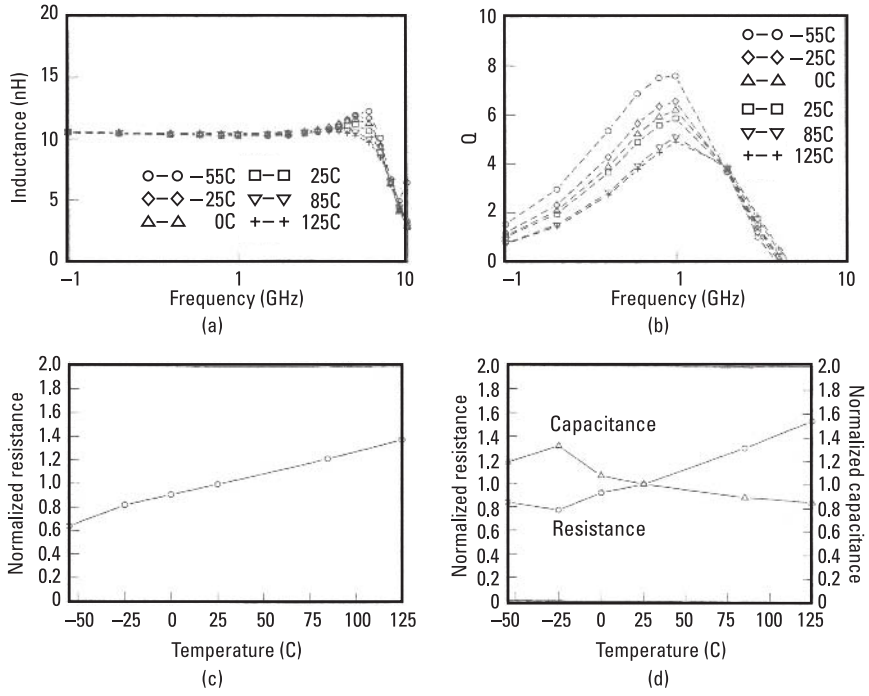


Figure 3.21 Measured 6-turn inductor's parameters with temperature: (a) inductance, (b) Q, (c) normalized conductor resistance, and (d) normalized substrate resistance and capacitance. (*From:* [16]. © 1997 IEEE. Reprinted with permission.)

3.2 Inductors on GaAs Substrate

This section describes spiral inductors on a GaAs substrate. Because GaAs is an insulator compared to Si, substrate losses are negligible and the inductor's EC becomes simpler. Q-values of inductors made using GaAs MMIC technologies are four to five times higher than Si-based technologies due to thicker high-conductivity metals and the insulating property of the GaAs substrate. Because high-Q inductors improve IC performance in terms of gain, insertion loss, noise figure, phase noise, power output, and power added efficiency, several schemes similar to Si-based inductors to improve further the Q-factor of GaAs inductors have been used. Improved Q is also a very desirable feature in oscillators to lower the phase noise. (The phase noise of an oscillator is inversely proportional to Q^2. Thus, a 20% increase in Q-factor will improve the phase noise by about 40%.) Because compact inductors are essential to develop low-cost MMICs, the 3-D MMIC process employing multiple layers of polyimide or BCB dielectric films and metallization to fabricate compact multilayer/stacked inductors is becoming a standard IC process. Multilayers of thick high conductivity metallization are capable of producing compact, high-current-capacity, high-performance inductors.

Spiral (rectangular or circular) inductors on a GaAs substrate are used as RF chokes, matching elements, impedance transformers, and reactive terminations, and they can also be found in filters, couplers, dividers and combiners, baluns, and resonant circuits [64–83]. Inductors in MMICs are fabricated using standard integrated circuit processing with no additional process steps. The innermost turn of the inductor is connected to other circuitry by using a conductor that passes under airbridges in monolithic MIC technology. The width and thickness of the conductor determines the current-carrying capacity of the inductor. Typically the thickness is 0.5 to 1.0 μm and the airbridge separates it from the upper conductors by 1.5 to 3.0 μm. In dielectric crossover technology, the separation between the crossover conductors can be anywhere between 0.5 and 3 μm. Typical inductance values for monolithic microwave integrated circuits working above the S-band fall in the range of 0.5 to 10 nH.

Both square and circular spiral inductors are being used in MICs and MMICs. It has been reported [13, 76] that the circular geometry has about 10% to 20% higher Q-values and f_{res} values than the square configuration. The design of spiral inductors as discussed in Chapter 2 can be based on analytical expressions or EM simulations or measurement-derived EC models. Usually, inductors for MMIC applications are designed either using EM simulators or measurement-based EC models. Bahl [81] reported extensive measured data for circular spiral inductors fabricated on GaAs substrates using a monolithic multilayer process. Various factors such as high inductance, high Q, high current handling capacity, and compactness were studied. Several configurations for

inductors were investigated to optimize the inductor geometry such as line width, spacing between turns, conductor thickness, and inner diameter. The measured effects of various parameters on inductor performance were included, such as line width, spacing, inner diameter, metal thickness, underlying dielectric, and dielectric thickness as discussed in Section 3.2.3.

3.2.1 Inductor Models

Various methods for modeling and characterization of GaAs spiral inductors have been described in the literature [69–82]. An inductor is characterized by its inductance value, the unloaded quality factor Q, and its resonant frequency f_{res}. Figure 3.22 shows various EC models used to describe the characteristics of GaAs inductors. Figure 3.22(a) represents the simplest model, whereas a comprehensive model for larger inductance values is shown in Figure 3.22(d). A commonly used EC model is shown in Figure 3.22(b) and an accurate account of substrate loss is represented in a model shown in Figure 3.22(c). In all of these models, the series inductance is represented by L, R_s accounts for the total loss in the inductor, C_p is the fringing capacitance between inductor turns, and $C_{ga,b}$ represents shunt capacitances between the trace and the substrate.

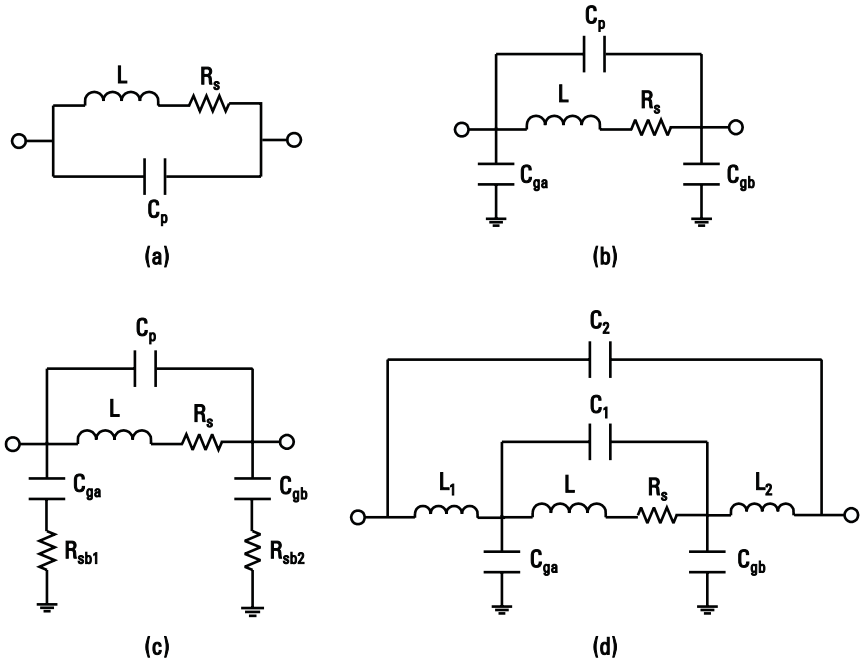


Figure 3.22 (a–d) Lumped-element EC models of the inductor on GaAs substrate.

The two-port lumped-element EC model used to characterize GaAs inductors in this section is shown in Figure 3.22(d). The series resistance R_s used to model the dissipative loss is given by

$$R_s = R_{\text{dc}} + R_{\text{ac}}\sqrt{f} + R_d f \tag{3.14}$$

where R_{dc} represents dc resistance of the trace, and R_{ac} and R_d model resistances due to skin effect, eddy current excitation, and dielectric loss in the substrate. In the model L_t ($L + L_1 + L_2$), R_s and the C's represent the total inductance, series resistance, and parasitic capacitances of the inductor, respectively. The frequency f is expressed in gigahertz.

In microwave circuits, the quality of an inductor is represented by its effective quality factor Q_{eff} and calculated using (2.12) from Chapter 2. The Q_{eff} values were obtained by converting two-port S-parameters data into one-port S-parameters by placing a perfect short at the output port. In this case, the following relationships are used to calculate the quality factor and f_{res}:

$$\Gamma_{\text{in}} = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}} \tag{3.15}$$

$$Z_{\text{in}} = 50\,\frac{1 - \Gamma_{\text{in}}}{1 + \Gamma_{\text{in}}} = R + jX\ (\Omega) \tag{3.16}$$

The self-resonant frequency (f_{res}) of an inductor is calculated by setting $\text{Im}[Z_{\text{in}}] = 0$; that is, the inductive reactance and the parasitic capacitive reactance become equal. At this point, $\text{Re}[Z_{\text{in}}]$ is maximum and the angle of Z_{in} changes sign. The inductor's first resonance frequency is of the parallel resonance type. Beyond the resonant frequency, the inductor becomes capacitive.

3.2.2 Figure of Merit

For a given inductance value, one would like to have the highest possible Q_{eff} and f_{res} in the smallest possible area. In an inductor, changing W, S, and the inner diameter affects its area and so it is difficult to make a good comparison. Here we define a unique *figure of merit of an inductor* (FMI) as follows [81]:

$$\text{FMI} = Q_{\text{res}} \cdot f_{\text{res}}/\text{inductor area} \tag{3.17}$$

Thus, the highest FMI value is desirable.

3.2.3 Comprehensive Inductor Data

Several types of circular spiral inductors having different dimensions, such as line width, spacing between the turns, and inner diameter, have been designed,

fabricated, and modeled [81]. These inductors as shown in Figure 3.23 were fabricated using both a standard and a multilayer MMIC process, with different conductor thicknesses. A summary of these inductors is given in Table 3.9, including the dimensions [Figure 3.23(a) and Figure 3.24] and current handling capability of several inductors. In the inductor column, the first three characters show the number of turns (e.g., 2.5), the fourth character (I) designates that the coil inductor has circular geometry, the fifth character is a numeric designator that represents the inductor's dimensions (W, S, W', D_i) and the last character signifies its fabrication scheme using polyimide layers and multilevel conductors: standard S, inductor conductor on 3-μm polyimide—A and B; conductors on 10-μm polyimide and multilevel plating—M; and conductors on 10-μm

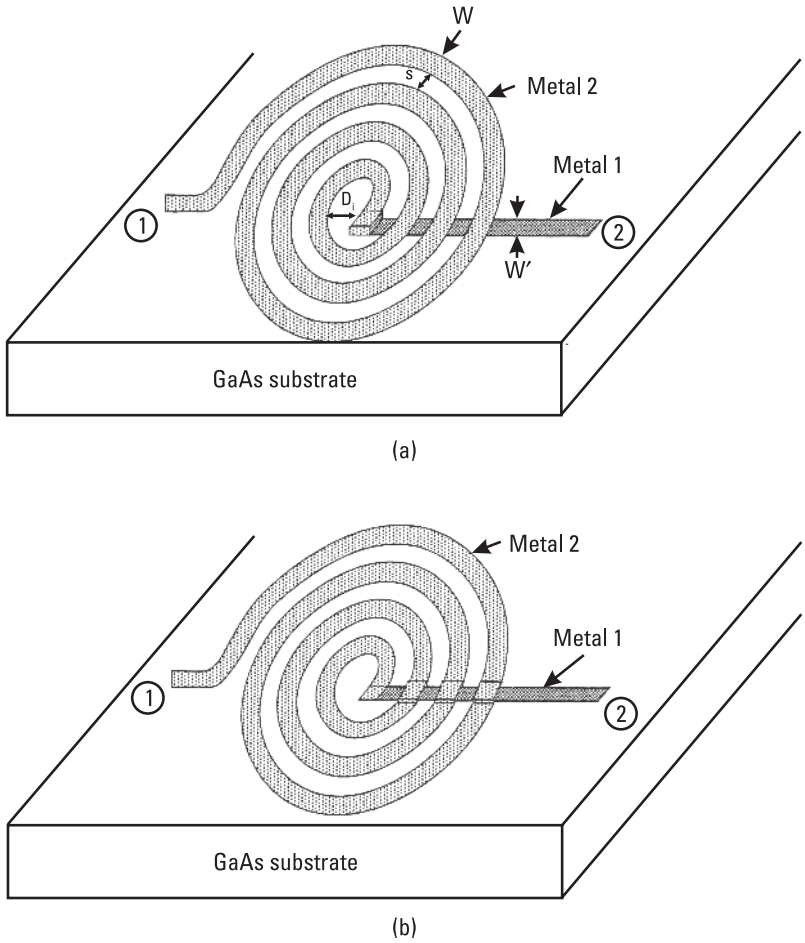


Figure 3.23 Circular spiral inductors: (a) multilayer and (b) standard.

Table 3.9
Summary of Various Inductors with Dimensions and Current-Handling Capacity*

Inductor Number	Number of Turns n	Dimensions (μm)								Current Handling** (mA)
		W	S	D_i	W'	t_1	t_2	d_1	d_2	
1.5I1S	1.5	20	8	108	20	0.6	4.5	0	3	40
1.5I1A	1.5	20	8	108	20	1.5	4.5	0	3	100
1.5I1B	1.5	20	8	108	40	1.5	4.5	0	3	200
1.5I1M	1.5	20	8	108	20	4.5	4.5	3	7	300
1.5I1T	1.5	20	8	108	40	4.5	9.0	3	7	600
2.5I1S	2.5	16	10	108	16	0.6	4.5	0	3	32
2.5I1A	2.5	16	10	108	16	1.5	4.5	0	3	80
2.5I1B	2.5	16	10	108	32	1.5	4.5	0	3	160
2.5I1M	2.5	16	10	108	16	4.5	4.5	3	7	240
2.5I1T	2.5	16	10	108	32	4.5	9.0	3	7	480
3.5I1S	3.5	12	14	108	12	0.6	4.5	0	3	24
3.5I1A	3.5	12	14	108	12	1.5	4.5	0	3	60
3.5I1B	3.5	12	14	108	24	1.5	4.5	0	3	120
3.5I1M	3.5	12	14	108	12	4.5	4.5	3	7	180
3.5I1T	3.5	12	14	108	24	4.5	9.0	3	7	360
3.5I5S	3.5	8	8	50	8	0.6	4.5	0	3	16
3.5I5A	3.5	8	8	50	8	1.5	4.5	0	3	40
3.5I5B	3.5	8	8	50	16	1.5	4.5	0	3	80
3.5I5M	3.5	8	8	50	8	4.5	4.5	3	7	120
3.5I5T	3.5	8	8	50	16	4.5	9.0	3	7	240

*For dimensional labels refer to Figures 3.23 and 3.24.
**Based on 3.3×10^5 amp/cm^2 current density.

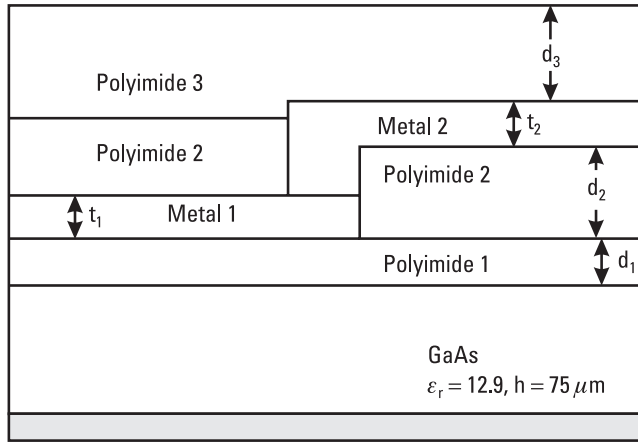


Figure 3.24 Cross-sectional view of the multilayer inductor. For multilayer process, $t_1 = t_2 =$ 4.5 μm and $d_1 = 3$ μm, and $d_2 = d_3 = 7$ μm.

polyimide and thick multilevel plating—T. In all the inductors, the underpass metal 1 is directly on the GaAs substrate. Using the multilayer process, two types of inductors were studied: high Q and high current. The first type of inductor is designed using a single level of plating. In this case, as shown in Figure 3.23(a), the inductor pattern with thick plated metallization 2 is placed on a 3-μm-thick polyimide layer (not shown) backed by a 75-μm-thick GaAs substrate. The innermost turn of the conductor is connected to the output line through a via in the 3-μm-thick polyimide layer and metal 1. Metal 1 is about 1.5 μm thick and placed directly on the GaAs substrate. Parameters for these inductors are listed in Table 3.10.

Figure 3.25 shows the layouts of some of the 2.5-turn inductors described here. All inductor patterns are drawn to the same scale. In the second type of inductor, two levels of plating are used. The first conductor layer is placed on top of 3-μm-thick polyimide and connects the innermost turn of the inductor to the output line through the via. The second conductor layer is placed on an additional 7-μm-thick polyimide layer and forms the inductor pattern. The total polyimide thickness underneath the inductor pattern is about 10 μm. Both metallizations are 4.5 μm thick and are connected by a via through the 7-μm-thick polyimide. Figure 3.24 shows the multilayer structure used for multilayer inductors.

Several compact inductors having various numbers of turns (1.5, 2.5, 3.5, 4.5, and 5.5) were also studied. All of these inductors have an inner mean radius of 50 μm, an 8-μm line width, and 8-μm spacing between the turns. Metal 1, which is placed directly on the GaAs substrate, has a thickness of 1.5 μm, whereas metal 2 has a thickness of 4.5 μm and is placed on top of

Table 3.10
Model Parameter Values for Type A Inductors

Inductor Number	Inductor Type	Number of Turns	Dimensions (μm) W	S	D_i	R_{dc} (Ω)	R_{ac} (Ω)	R_d (Ω)	L_1 (nH)	L_2 (nH)	L (nH)	C_{ga} (pF)	C_{gb} (pF)	C_1 (pF)	C_2 (pF)	f_{res} (GHz)	Peak Q_{eff}
1.5I0A	X0	1.5	20	8	50	0.1	0.167	0.001	0.0001	0.0001	0.378	0.019	0.020	0.0001	0.00001	>40	49
1.5I1A	X1	1.5	20	8	108	0.18	0.15	0.009	0.0001	0.0001	0.563	0.028	0.027	0.0001	0.00001	37.6	52
1.5I2A	X2	1.5	20	8	158	0.23	0.16	0.018	0.0001	0.0001	0.760	0.038	0.036	0.0001	0.00001	27.2	48
1.5I3A	X3	1.5	20	8	210	0.24	0.24	0.02	0.092	0.077	0.85	0.048	0.046	0.0001	0.00001	22.3	40.5
1.5I4A	X4	1.5	12	8	50	0.10	0.19	0.0001	0.0001	0.0001	0.342	0.014	0.011	0.0001	0.00001	>40	41.5
1.5I5A	X5	1.5	8	8	50	0.20	0.155	0.01	0.0001	0.0001	0.32	0.010	0.008	0.00002	0.00001	>40	35
2.5I0A	X0	2.5	16	10	50	0.20	0.3	0.03	0.18	0.30	0.42	0.020	0.033	0.002	0.0096	28.7	37
2.5I1A	X5	2.5	16	10	108	0.30	0.25	0.06	0.16	0.10	1.10	0.039	0.037	0.0016	0.0043	21.00	39
2.5I2A	X2	2.5	16	10	158	0.35	0.27	0.1	0.21	0.23	1.45	0.048	0.054	0.0045	0.0045	16.2	38
2.5I3A	X3	2.5	16	10	210	0.38	0.3	0.15	0.24	0.26	1.91	0.059	0.065	0.0023	0.0052	13.15	35.5
2.5I4A	X4	2.5	12	8	50	0.25	0.33	0.021	0.028	0.029	0.751	0.022	0.021	0.00002	0.00001	34.2	35
2.5I5A	X5	2.5	8	8	50	0.25	0.40	0.02	0.033	0.032	0.696	0.019	0.015	0.00003	0.00005	38.1	30.0
3.5I0A	X0	3.5	12	14	50	0.38	0.55	0.06	0.32	0.32	1.18	0.036	0.039	0.0048	0.0075	18.7	30.0
3.5I1A	X1	3.5	12	14	108	0.45	0.52	0.13	0.26	0.29	2.08	0.047	0.053	0.0001	0.006	14.0	31.5
3.5I2A	X2	3.5	12	14	158	0.6	0.7	0.17	0.30	0.33	3.00	0.061	0.071	0.0001	0.0025	10.6	29.5
3.5I3A	X3	3.5	12	14	210	0.7	0.80	0.25	0.37	0.48	3.74	0.073	0.082	0.0003	0.0032	8.75	27.5
3.5I4A	X4	3.5	12	8	50	0.3	0.55	0.06	0.033	0.44	1.12	0.022	0.037	0.016	0.0001	20.5	30.0
3.5I5A	X5	3.5	8	8	50	0.3	0.60	0.07	0.036	0.034	1.407	0.023	0.023	0.001	0.0018	25.0	27.5
4.5I0A	X0	4.5	12	14	50	0.46	0.66	0.12	0.33	0.34	2.36	0.053	0.066	0.002	0.008	11.9	30.0
4.5I5A	X5	4.5	8	8	50	0.4	0.8	0.16	0.044	0.036	2.421	0.029	0.033	0.0023	0.002	17.5	25.5
5.5I5A	X5	5.5	8	8	50	0.5	1.0	0.21	0.047	0.038	3.64	0.044	0.054	0.0029	0.002	11.8	25.0

Note: The EC model used is shown in Figure 3.22(d), where R is given by (3.14).

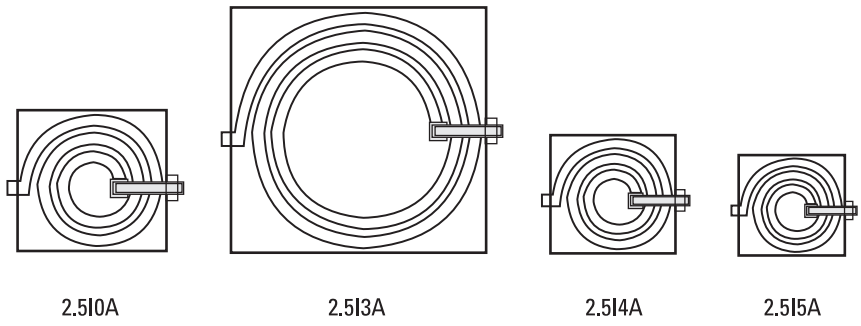


Figure 3.25 Four different types of 2.5-turn inductors. 2.5I0A: $W = 16$, $S = 10$, $D_i = 50$; 2.5I3A: $W = 16$, $S = 10$, $D_i = 210$; 2.5I4A: $W = 12$, $S = 8$, $D_i = 50$; and 2.5I5A: $W = S = 8$, $D_i = 50$. All dimensions are in microns.

3-μm-thick polyimide. These inductors are types A and B, with the only difference being that in type A inductors $W' = W$ [Figure 3.23(a)] and in type B inductors $W' = 2W$.

Inductors fabricated using two levels of plating can be designed for much higher current capacity than is possible if one wiring layer must be thin, as is the case if only one layer of plating is available. Along with increased current capability, the Q-factor is enhanced due to lower resistance. The current-handling capability of a conductor is limited by the onset of electromigration. The conductor thickness and line width determine the current-carrying capacity of the inductor. A safe value of maximum current density of gold conductors on a flat surface is $3.3 \times 10^5 \text{A/cm}^2$. For example, for 4.5-$\mu$m-thick conductors, the calculated maximum current-handling capacity is 15 mA per micron of line width. Table 3.9 provides the calculated value of maximum current for several inductors investigated in this study.

Inductors were tested for two-port S-parameters up to 40 GHz using RF probes. Measured data were taken using an on-wafer TRL de-embedding technique. The TRL calibration standards were placed directly on the same GaAs substrate as the inductor structures, so that the same calibration standards can be used for all the multilayer inductors. From the de-embedded S-parameter data, the model element values were derived and Q_{eff} and f_{res} were obtained as described in Section 3.2.1. The Q_{eff} values are obtained at the maximum Q_{eff} frequency, which is experimentally observed at about $0.5f_{\text{res}}$. Table 3.10 summarizes typical model parameter values for various circular spiral inductors tested on a 75-μm-thick GaAs substrate. The inductors are classified into six groups, depending on the $W + S$ dimension and the inner diameter. Figure 3.26 shows total inductance as a function of inductor area for an inductor of type A. Higher inductance and area for a given inductor type means a larger

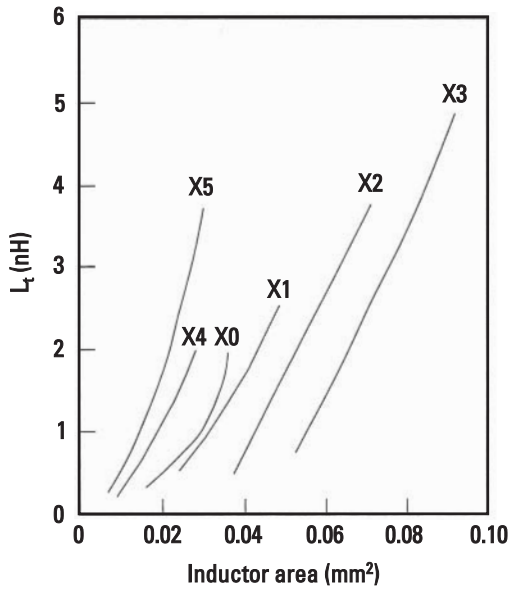


Figure 3.26 Variations of measured total inductance versus area for different inductors of type A.

number of turns. Six groups of inductors are described next, with all dimensions given in microns:

X0: $D_i = 50$ and $n = 1.5$, $W = 20$, $S = 8$; $n = 2.5$, $W = 16$, $S = 10$; $n = 3.5$, $W = 12$, $S = 14$; $n = 4.5$, $W = 12$, $S = 14$;

X1: $D_i = 108$ and $n = 1.5$, $W = 20$, $S = 8$; $n = 2.5$, $W = 16$, $S = 10$; $n = 3.5$, $W = 12$, $S = 14$;

X2: $D_i = 158$ and $n = 1.5$, $W = 20$, $S = 8$; $n = 2.5$, $W = 16$, $S = 10$; $n = 3.5$, $W = 12$, $S = 14$;

X3: $D_i = 210$ and $n = 1.5$, $W = 20$, $S = 8$; $n = 2.5$, $W = 16$, $S = 10$; $n = 3.5$, $W = 12$, $S = 14$;

X4: $D_i = 50$, $W = 12$, $S = 8$, and $n = 1.5, 2.5, 3.5$;

X5: $D_i = 50$, $W = 8$, $S = 8$, and $n = 1.5, 2.5, 3.5, 4.5, 5.5$.

For a 1-nH inductance value, the X5-type inductors have about 0.25 of the area of X3-type inductors, whereas for larger inductance values, X5 inductors are about one-third of the area of X3 inductors. Figure 3.27 shows Q_{eff} as a function of inductor area. The broken lines indicate Q_{eff} values for 1- and 2-nH inductance values. Note that for an inductor having about a 1-nH value,

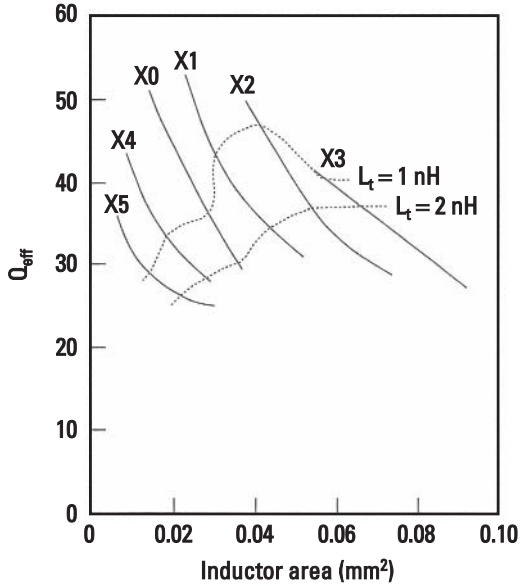


Figure 3.27 Variations of measured Q_{eff} versus area for different inductors of type A.

X2-type inductors provide the maximum Q_{eff}, whereas for a 2-nH value, the X2 and X3 types have similar Q_{eff} values, while X3-type inductors have about a 25% larger area. Figure 3.28 shows the self-resonant frequency of these inductors as a function of area. The broken lines indicate the resonant frequency values for 1- and 2-nH inductance values. In general, the larger the area, the lower the resonant frequency, and X3-type inductors have the lowest and X5 type the highest resonant frequencies.

3.2.3.1 Line Width

The line width is the most critical variable in the design of coils. In general, Q_{eff} increases due to lower dc resistance and f_{res} decreases due to higher parasitic capacitance with the increase in the line width. Figures 3.29 and 3.30 show the variations of Q_{eff}, f_{res}, and inductor area for 1- and 2-nH inductance values, respectively, for $W = 8\ \mu$m, $S = 8\ \mu$m, $D_i = 50\ \mu$m, and the number of turns is selected for the desired L value. For $W = 12\ \mu$m; S, D_i, and n are desirable variables for achieving the desired inductance value. For $W = 16\ \mu$m, $S = 10\ \mu$m and D_i and are desirable variables, whereas for $W = 20\ \mu$m, $S = 8\ \mu$m and D_i and number of turns are desirable variables. For the 1-nH inductor, the increase in Q_{eff} value is not significant when the line width increases from 16 to 20 μm, while the increase in area is about 80%. For higher inductance values, an optimum line width is about 16 μm for maximum Q_{eff}.

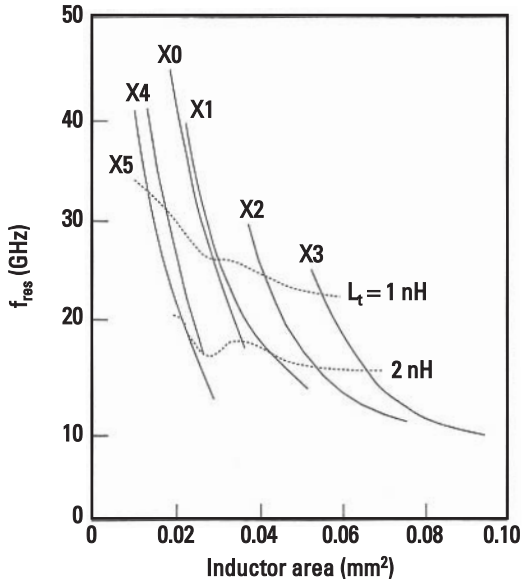


Figure 3.28 Variations of measured self-resonance frequency versus area for different inductors of type A.

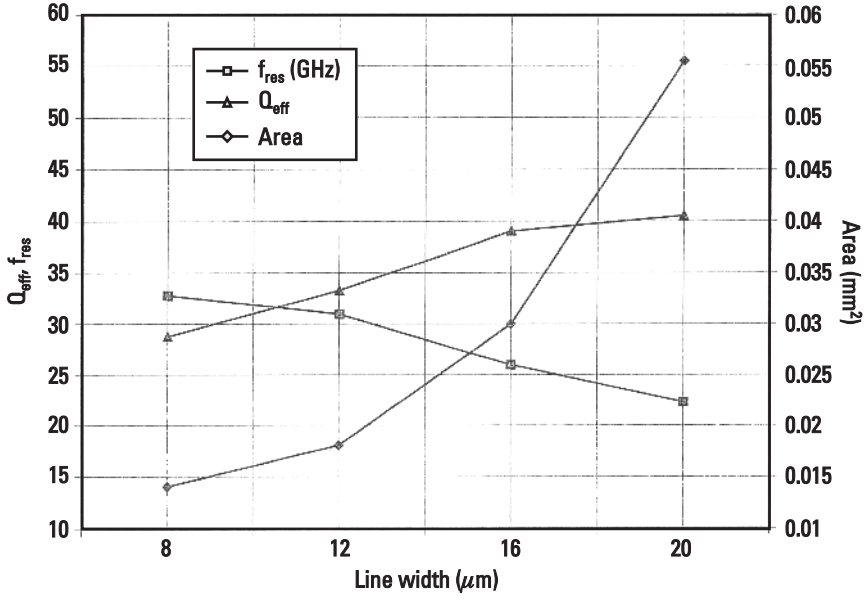


Figure 3.29 Inductor's Q_{eff}, f_{res}, and area as a function of line width for a 1-nH inductance value.

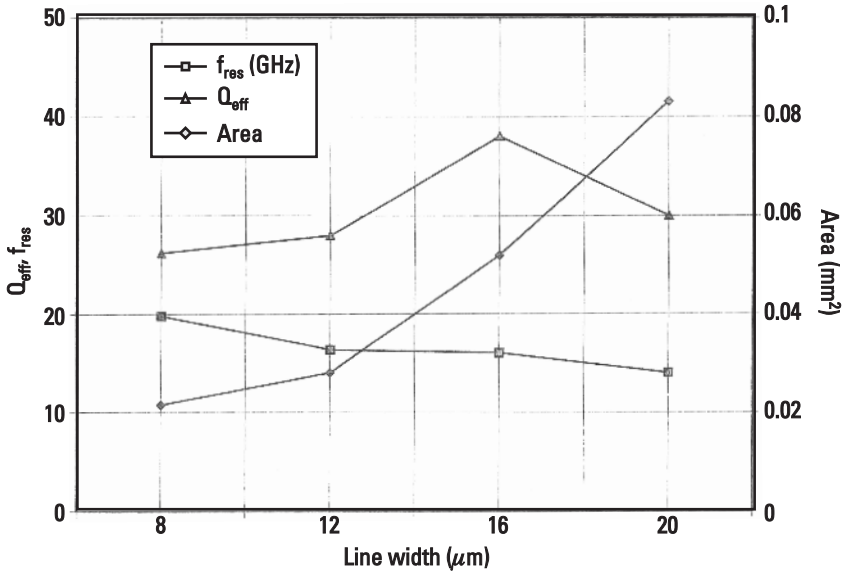


Figure 3.30 Inductor's Q_{eff}, f_{res}, and area as a function of line width for a 2-nH inductance value.

3.2.3.2 Spacing Between Turns

In general, Q_{eff} increases with the area of an inductor. However, small area inductors mandate small separation between the turns. Table 3.11 shows inductor parameters for 8- and 14-μm spacing. As expected a 3.5I0A inductor has

Table 3.11
Inductor Parameters for Several Inductors Fabricated Using a Multilevel MMIC Process on 75-μm-Thick GaAs Substrate

Inductor Number	Width (μm)	Spacing (μm)	L_t (nH)	f_{res} (GHz)	Peak Q_{eff}
1.5I4A	12	8	0.342	>40	41.5
2.5I4A	12	8	0.808	34.2	35
3.5I4A	12	8	1.593	20.5	30
3.7I4A*	12	8	1.82	18.0	29
3.5I0A	12	14	1.82	18.7	30
3.5I1A	12	14	2.63	14.0	31.5
3.5I2A	12	14	3.63	10.6	29.5
3.5I3A	12	14	4.59	8.75	27.5

*Extrapolated from Figures 3.26, 3.27, and 3.28.

a slightly higher inductance and lower f_{res} than the 3.5I4A one due to increased area. Because the 3.5I0A inductor has higher inductance and lower f_{res}, its Q_{eff} is expected to be higher than the 3.5I4A inductor's Q_{eff}. The data in Figures 3.26, 3.27, and 3.28 have been used to extrapolate f_{res} and Q_{eff} values for the inductance value of 1.82 nH. As expected, the 3.7I4A inductor has lower f_{res} and Q_{eff} values than the 3.5I0A inductor. For spiral coils, $W/S > 1$ is recommended.

3.2.3.3 Inner Diameter

Because the contribution of the innermost turn is small due to its very small inner diameter, enough empty space must be left in the center of a coil to allow the magnetic flux lines to pass through it in order to increase the stored energy per unit length. Inductors with four different inner diameters (50, 108, 158, and 210 μm) were studied. Figures 3.31 and 3.32 show the variations of L_t, Q_{eff}, and f_{res} as a function of inner diameter for $W = 20$ μm, $S = 8$ μm, $n = 1.5$, and $W = 12$ μm, $S = 14$ μm, $n = 3.5$, respectively. As expected, the inductance increases and f_{res} decreases with increasing inner diameter (D_i) due to increased inductor area. As can be seen, the maximum Q_{eff} occurs around $D_i = 100$ μm. Similar optimum D_i is obtained for other line widths and multilayer inductors.

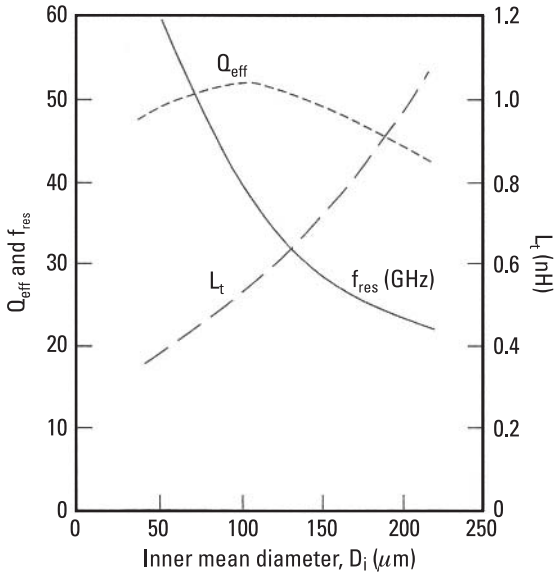


Figure 3.31 Inductor's L_t, Q_{eff}, and f_{res} versus inner mean diameter for 1.5-turn inductors.

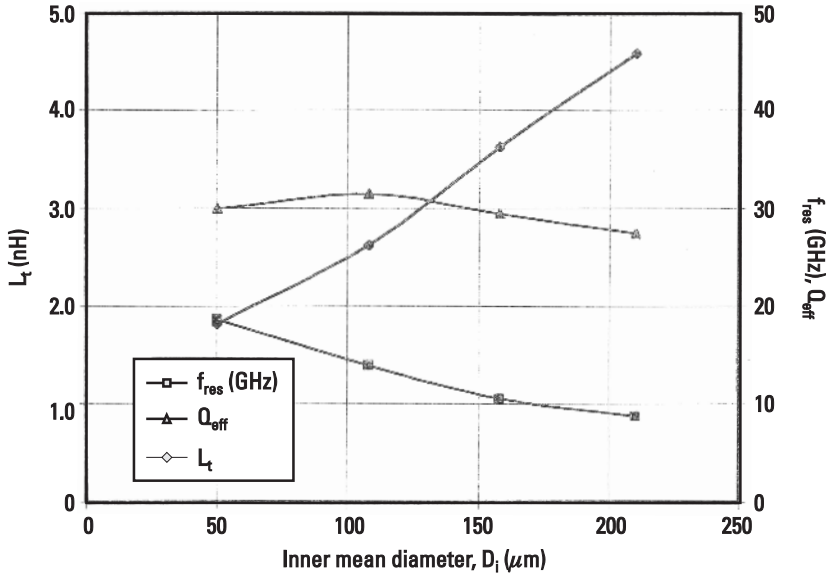


Figure 3.32 Inductor's L_t, Q_{eff}, and f_{res} versus inner mean diameter for 3.5-turn inductors.

3.2.3.4 Number of Turns

Multiturn inductors have higher inductance per unit area, but due to higher parasitic capacitances, have lower-self-resonance frequencies. Figure 3.33 shows the plots of L_t, Q_{eff}, and f_{res} versus number of turns for X5 inductors.

The decrease of Q_{eff} with an increasing number of turns is because of increased parasitic capacitance and increased RF resistance due to eddy currents. Figures 3.34 and 3.35 show typical variations of inductance and Q_{eff} as a function of frequency for 1.5-, 2.5-, 3.5-, 4.5-, and 5.5-turn inductors. Data are shown up to the first resonance. The maximum Q_{eff} point decreases with the increase in number of turns because of increased RF resistance due to eddy currents and the increase of parasitic capacitance. Below the maximum Q_{eff} point, the inductive reactance and Q_{eff} increase with frequency, while at frequencies above the maximum Q_{eff} point, the RF resistance increases faster than the inductive component. This results in a decrease in the Q_{eff} value with frequency, and Q_{eff} becomes zero at resonance of the inductor. As expected, the inductance increases approximately as n^2, where n is the number of turns. For X5-type inductors the value of total inductance (nH), Q_{eff} factor, and resonance frequency (GHz) can be calculated approximately using the following empirical equations:

$$L_t = 0.04 + 0.12n^2 \text{ (nH)} \tag{3.18}$$

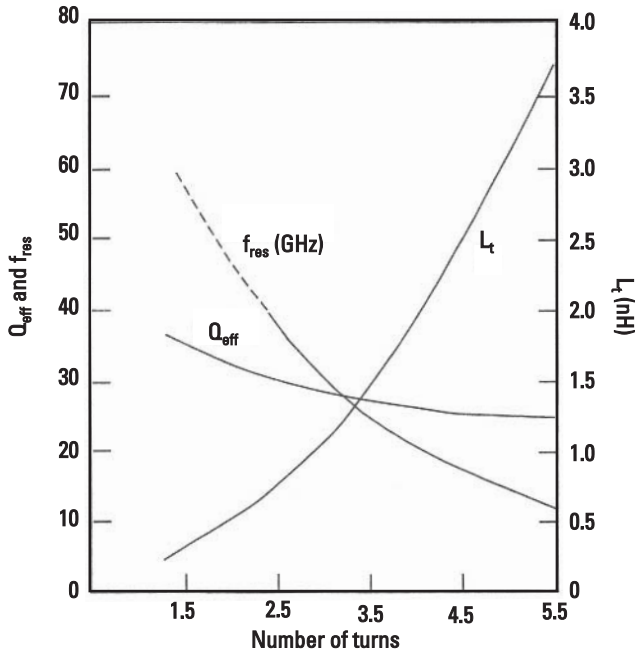


Figure 3.33 Variations of L_t, Q_{eff}, and f_{res} area as a function of number of turns for X5 inductors.

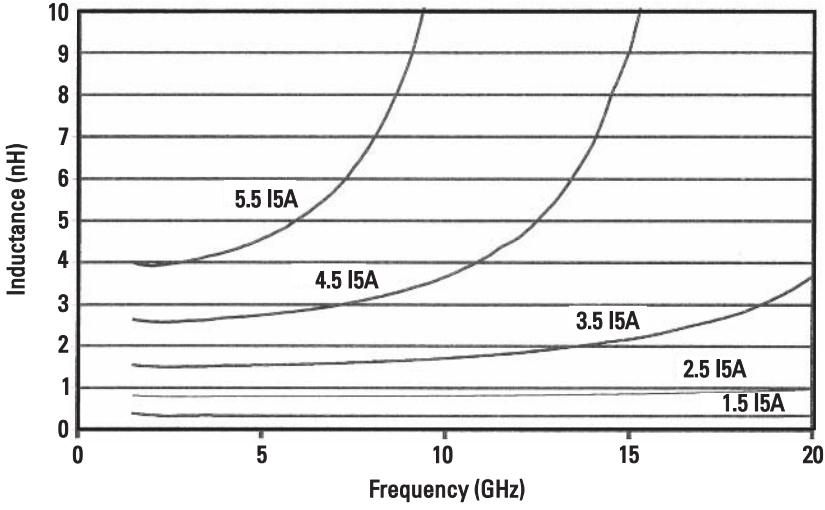


Figure 3.34 Typical variations of L_t versus frequency for different inductor turns.

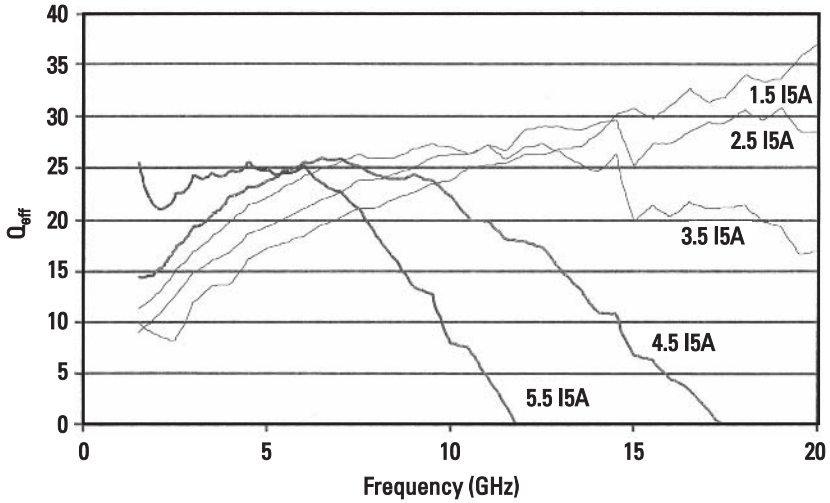


Figure 3.35 Typical variations of Q_{eff} factor versus frequency for different inductor turns.

$$Q_{\text{eff}} = \frac{38}{n^{0.25}} \tag{3.19}$$

$$f_{\text{res}} = \frac{36.52}{0.9432 + 0.01n^{3.15}} \text{ (GHz)} \quad \text{for } f_{\text{res}} < 30 \text{ GHz} \tag{3.20}$$

3.2.3.5 Multilayer Dielectric Inductors

Typical inductance values for MMIC applications on a GaAs substrate in the microwave frequency band fall in the range from 0.2 to 10 nH. On a thin GaAs substrate (3 mil or smaller), the use of high value inductors in the matching networks becomes difficult because of lower resonant frequencies due to larger interturn fringing capacitance and larger shunt capacitance to ground. These parasitic capacitances can be reduced significantly by using a multilayer configuration [83].

Several types of multilayer dielectric inductors have been tested and compared with standard inductors. Variations of L_t ($L + L_1 + L_2$), the quality factor Q_{eff}, and resonant frequency f_{res} for four inductor types (see Table 3.9 for designation) are shown in Figures 3.36, 3.37, and 3.38, respectively. Compared to standard inductors, inductors using the multilayer process have about 17% to 21% higher resonance frequencies and 65% to 73% higher Q_{eff} values. The thicker polyimide layer increases the values of Q_{eff} and the resonance frequency of the inductors due to reduced dissipative loss and lower parasitic capacitance, similar to the characteristics of multilayer microstrip lines [83].

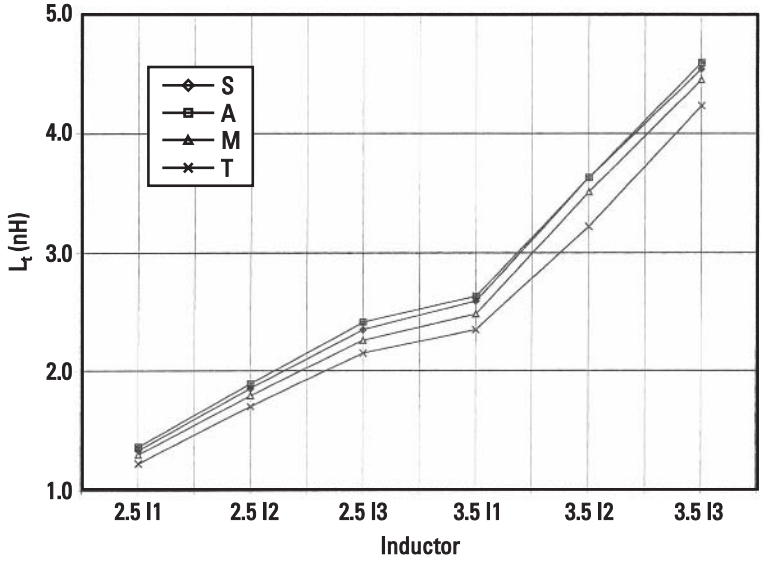


Figure 3.36 Comparison of L_t for various inductors types fabricated using standard (S), multilayer (A), multilayer and multilevel metallization (M), and multilayer and multilevel thick metallization (T) processes. For inductor parameters refer to Tables 3.9 and 3.10.

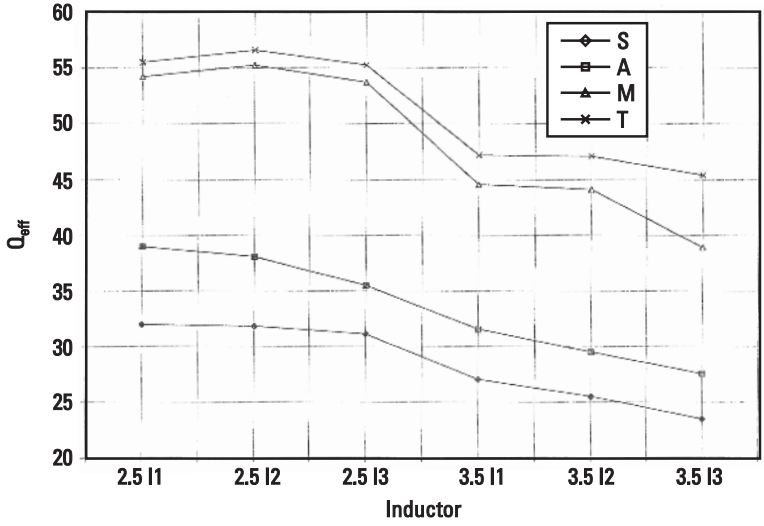


Figure 3.37 Comparison of Q_{eff} for various inductors types fabricated using standard (S), multilayer (A), multilayer and multilevel metallization (M), and multilayer and multilevel thick metallization (T) processes. For inductor parameters refer to Tables 3.9 and 3.10.

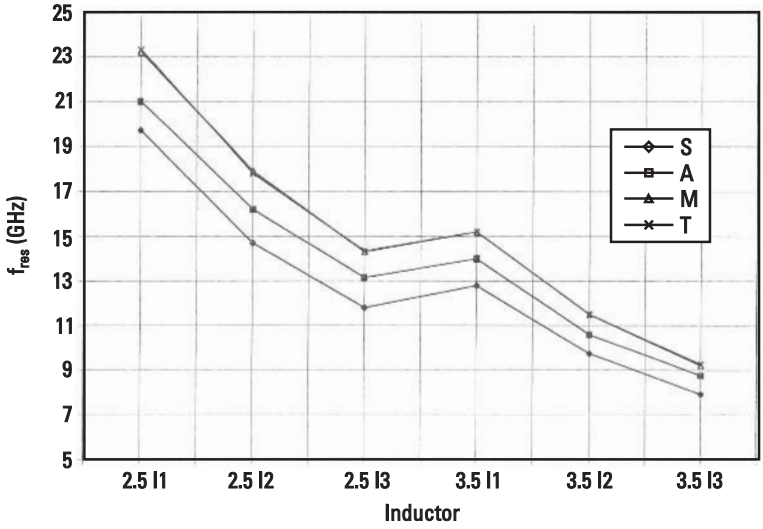


Figure 3.38 Comparison of f_{res} for various inductors types fabricated using standard (S), multilayer (A), multilayer and multilevel metallization (M), and multilayer and multilevel thick metallization (T) processes. For inductor parameters refer to Tables 3.9 and 3.10.

Similar improvements in the inductor's performance have also been observed by placing the inductor's conductor on thick oxidized porous silicon [15]. The total inductance value is more or less invariant.

The performance of these inductors can be improved further by using low dielectric constant ($\epsilon_{rd} = 2.7$) low-loss (tan $\delta = 0.0006$) *benzocyclo-butene* (BCB) as a multilayer dielectric. The thermal resistance of polyimide or BCB is about 200 times the thermal resistance of GaAs. To ensure reliable operation of these components for high-power applications, these components must be modeled thermally.

3.2.3.6 Thickness Effect

The effect of metal 2 (Figure 3.24) thickness on the inductors' characteristics was also investigated. The Q-factor of an inductor is increased by increasing the conductor thickness because this reduces the series resistance. For this study, the metal 2 thickness was increased from 4.5 to 9.0 μm. This increases the current handling by a factor of 2 when the width of metal 1 is twice the inductor's line width (Table 3.9). In the thick metallization case, the Q_{eff} value is further enhanced by about 3% to 17%, the inductance value is reduced by about 4% to 6%, and the resonant frequency does not change due to increased parasitic capacitance as shown in Figures 3.36, 3.37, and 3.38. Table 3.12

Table 3.12
Inductor Parameters for Several Values of Polyimide Thicknesses and Metallization Thicknesses

Polyimide Thickness (μm)	Inductor Number	L_t (nH)	Peak Q_{eff}	f_{res} (GHz)
0	2.5I3S	2.35	31.1	11.8
3	2.5I3A	2.41	35.5	13.15
10	2.5I3M	2.26	53.7	14.3
10	2.5I3T	2.15	55.2	14.35

summarizes the inductor model parameters for several 2.5-turn inductors. These inductors have up to 93% higher Q_{eff} factor values than the standard inductors.

3.2.3.7 Inductor Area

The Q-factor of a coil can be enhanced by increasing its area using either a larger inside diameter or wider line dimensions or by increasing the separation between the turns. In general, using a wider line dimension reduces the dc resistance of the coil. However, the parasitic capacitance of the inductor trace and the RF resistance due to eddy currents increase with the line width. This sets a maximum limit for the line width. For a micromachined inductor, this limit is about 20 μm [21], whereas for planar inductors on a 3-mil-thick GaAs substrate this limit is about 16 μm for larger inductance values.

However, for low-cost considerations one needs compact inductors. Figure 3.39 shows the figure of merit for several inductors of type A. The value of inductance selected is 1 nH, and the X5 structure has the best FMI because it has the smallest area and highest resonance frequency due to lower parasitic capacitances.

The data discussed earlier for circular spiral inductors are also compared with standard [81] and variable line width [80] square inductors in Figure 3.40. As expected, the square inductors have lower Q_{eff} than the circular inductors; however, for higher values of inductances, the Q_{eff} values for the circular inductor on a 3-μm-thick polyimide dielectric layer and the variable line width square inductors are comparable. The resonant frequencies for small inductance values are comparable; however, for high values of inductance the circular inductors have higher resonant frequencies primarily due to their small line widths.

3.2.4 *Q*-Enhancement Techniques

One of the most important FMIs is the quality factor (Q). Higher values of Q are needed to improve the microwave circuit's performance. Because an

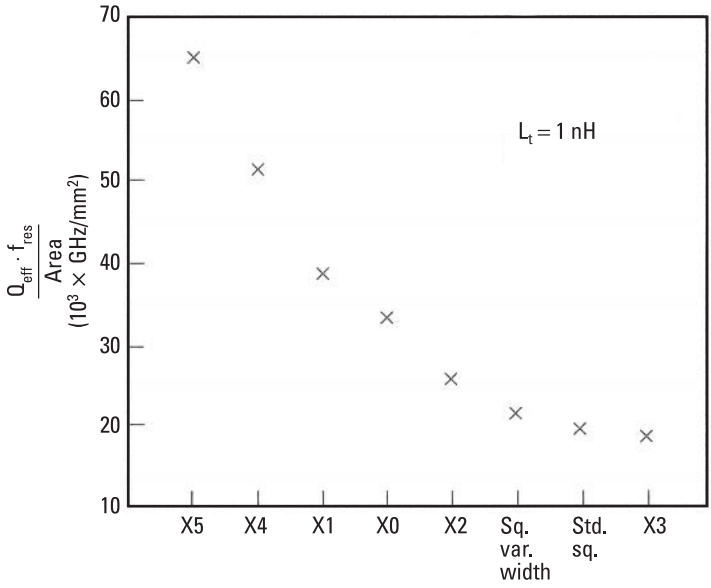


Figure 3.39 Comparison of FMI for various inductors.

inductor's Q is inversely proportional to the series resistance of its metal conductor trace, high conductivity and thick conductors are desirable. Other Q-enhancement techniques include using variable line width [21, 79], the differential excitation technique [22], and multilayer dielectric and metallization [80–82]. In the latter case, as discussed in the previous section, the improvement in Q is achieved by reducing both the dc resistance using thicker conductors and parasitic capacitance using a multilayer dielectric medium. More discussion on this subject for rectangular inductors is included in the next section. The Q-factor of a coil can be enhanced by increasing its area and reducing the dc resistance by using a wider line width. However, the parasitic capacitance of the inductor trace and the RF resistance due to eddy currents increase with line width; this sets a maximum limit for the line width.

It has been shown experimentally that the quality factor of spiral inductors can be increased by reducing magnetically induced currents in the trace width by narrowing the line width of the inner turns similar to a silicon micromachined inductor [21]. Several square spiral inductors using different trace line widths and number of segments were designed. A summary of these inductors is given in Table 3.13. Standard inductors 11S, 15S, 19S, and 23S, also tested for comparison, have a constant line width of 20 μm, whereas modified inductors 11SM, 15SM, 19SM, and 23SM have different line widths for each turn as given in Table 3.13. The first two numbers designate the number of segments.

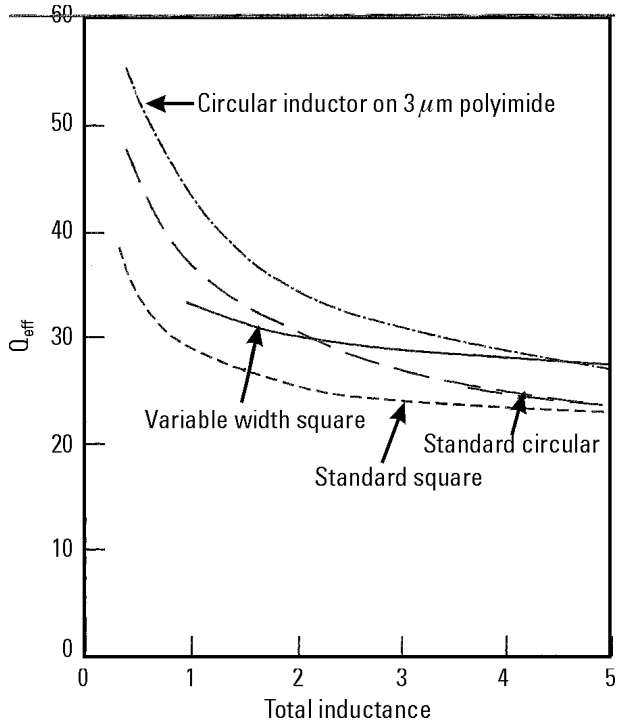


Figure 3.40 Comparison of Q_{eff} for type A, and standard circular, square, and variable width inductors.

All inductors have 12-μm spacing between the turns. Figure 3.41 shows typical physical layouts for standard and modified inductors using 23 segments. The area of the modified inductors is about 20% to 30% larger than for standard inductors.

The inductors were fabricated on a 75-μm-thick GaAs substrate using a MMIC process. The thicknesses of the interconnect (metal 1) and plated gold (metal 2) metallizations are about 1.5 and 4.5 μm, respectively. The inductors were tested for two-port S-parameters up to 40 GHz using RF probes. The measured data were taken by using an on-wafer TRL de-embedding technique. The two-port EC model used is shown in Figure 3.22(d).

Table 3.13 summarizes typical model values for various standard and variable width inductors. Figure 3.42 shows the variation of measured Q as a function of number of segments for standard and modified (to minimize eddy current) spiral inductors. The Q-values are obtained at about $0.5f_{res}$, which is also a maximum Q-point frequency. An increase of about 22% in the quality factor of modified inductors in comparison to standard inductors was observed. For a given number of segments, the number of squares of conductor is approxi-

Table 3.13
Square Inductor Model Parameters

Structure Number	Dimensions (μm) W	S	R_{dc} (Ω)	R_{ac} (Ω)	R_d (Ω)	L_1 (nH)	L_2 (nH)	L (nH)	C_{ga} (pF)	C_{gb} (pF)	C_1 (pF)	C_2 (pF)	f_{res} (GHz)	Q at $0.5f_{res}$
7S	20	12	0.30	0.04	0.032	0.009	0.009	0.384	0.03	0.022	0.00001	0.00001	>40	37
11S	20	12	0.5	0.2	0.07	0.011	0.011	1.053	0.048	0.048	0.0001	0.0001	20.85	29
15S	20	12	0.6	0.42	0.14	0.025	0.020	1.95	0.069	0.083	0.0075	0.001	12.5	25.5
19S	20	12	0.7	0.7	0.25	0.31	0.56	2.98	0.083	0.108	0.0007	0.019	8.1	23.8
23S	20	12	0.8	0.9	0.5	0.32	0.64	5.11	0.126	0.157	0.0011	0.0096	5.65	22.0
11SM	10, 20, 30	12	0.4	0.085	0.09	0.01	0.01	1.014	0.044	0.055	0.0048	0.0048	20.8	33
15SM	10, 20, 30, 40	12	0.5	0.2	0.14	0.025	0.021	1.75	0.067	0.117	0.021	0.003	12.55	31.2
19SM	10, 20, 30, 35, 40	12	0.6	0.12	0.35	0.21	0.50	2.63	0.099	0.18	0.0007	0.0033	7.55	28.7
23SM	10, 20, 25, 30, 35, 40	12	0.7	0.24	0.54	0.3	0.60	4.44	0.15	0.24	0.0011	0.024	5.35	27.0

Note: The EC model used is shown in Figure 3.22(d), where R is given by (3.14).

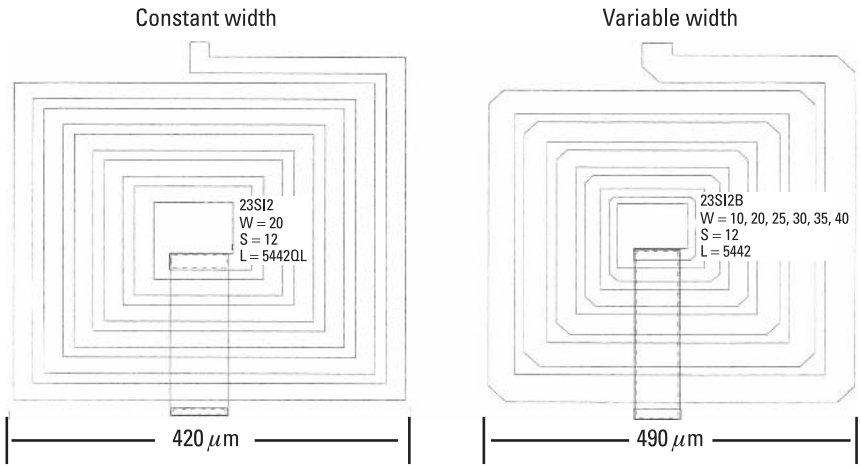


Figure 3.41 Physical layouts of constant line width and variable line width 23-segment inductors.

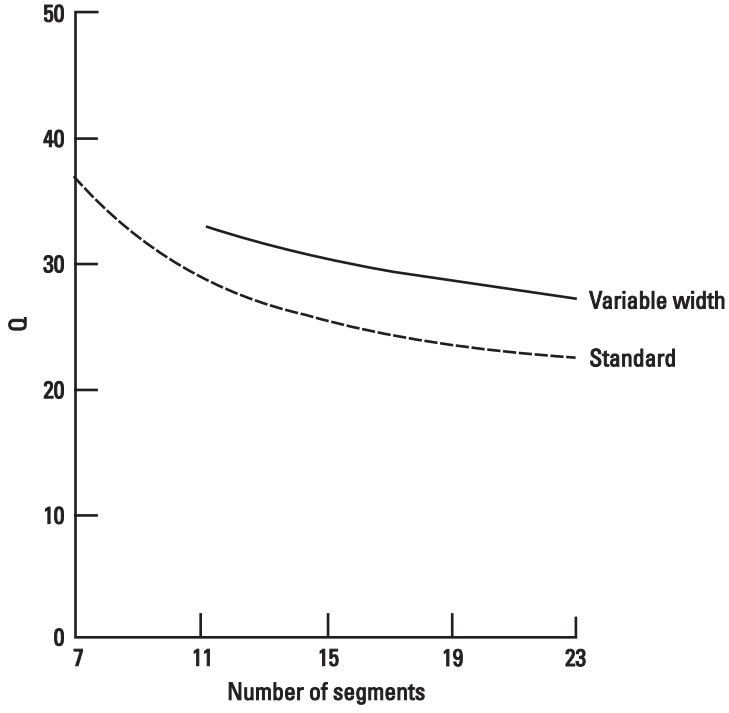


Figure 3.42 Variations of measured Q versus number of segments for constant and variable line width inductors.

mately the same. The extracted model parameters also suggest that the modified inductors have reduced R_s. Figure 3.43 shows the ratio of R_s/R_{dc} as a function of frequency for 15S, 15SM, 23S, and 23SM inductors.

The Q-factor of spiral inductors can be enhanced by using thicker metallization and placing inductors on a thick polyimide layer that is placed on top of the GaAs substrate. Using this technique, an improvement of 68% in the quality factor of spiral inductors as compared to standard spiral inductors, has been demonstrated [80]. Tables 3.14 and 3.15 summarize typical model parameter values for multilayer dielectric inductors. The inductors are rectangular spirals and their dimensions are the same as those given in Table 3.13 for standard inductors. The polyimide thickness was 10 μm and the substrate thickness was 75 μm. For Table 3.14, the inductor's metal 2 thickness was 4.5 μm, whereas for Table 3.15 it was 9 μm. In comparison to standard inductors the inductors using a multilayer dielectric process with 4.5-μm-thick metal 2 have about an 18% to 20% higher resonance frequency and 41% to 56% higher Q-values. The polyimide layer increased the values of Q and the resonant frequency.

The total inductance value (in nanohenries) of a multilayer dielectric inductor can be calculated using the following empirical equation:

$$L_t = 0.8\sqrt{A}\,(p/4)^{1.667} \tag{3.21}$$

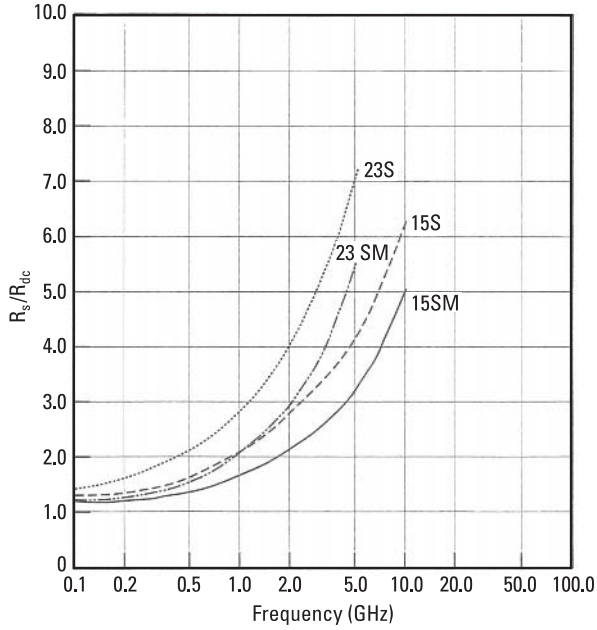


Figure 3.43 Normalized total resistance versus frequency for several inductors.

Table 3.14
Inductor Model Parameters for Multilayer Square Spiral Inductors, Metal 2 = 4.5 μm

Structure Number	R_{dc} (Ω)	R_{ac} (Ω)	R_d (Ω)	L_1 (nH)	L_2 (nH)	L (nH)	C_{ga} (pF)	C_{gb} (pF)	C_1 (pF)	C_2 (pF)	f_{res} (GHz)	Q at $0.5f_{res}$
11SIML2	0.4	0.12	0.05	0.06	0.106	0.900	0.036	0.047	0.0002	0.004	24.6	43.8
15SIML2	0.47	0.28	0.09	0.064	0.13	1.946	0.055	0.071	0.00001	0.0005	14.75	39.7
19SIML2	0.55	0.40	0.20	0.168	0.321	3.288	0.076	0.097	0.00001	0.00001	9.55	36.2
23SIML2	0.70	0.62	0.40	0.592	0.717	4.832	0.094	0.116	0.00001	0.0041	6.7	30.9

Note: The EC model used is shown in Figure 3.22(d), where R is given by (3.14).

Table 3.15
Inductor Model Parameters for Multilayer Square Spiral Inductors, Metal 2 = 9.0 μm

Structure Number	R_{dc} (Ω)	R_{ac} (Ω)	R_d (Ω)	L_1 (nH)	L_2 (nH)	L (nH)	C_{ga} (pF)	C_{gb} (pF)	C_1 (pF)	C_2 (pF)	f_{res} (GHz)	Q at $0.5f_{res}$
11SIML1	0.20	0.12	0.05	0.06	0.106	0.832	0.038	0.05	0.0003	0.0045	24.6	48.6
15SIML1	0.25	0.28	0.09	0.064	0.13	1.848	0.058	0.075	0.00001	0.0003	14.75	43.5
19SIML1	0.30	0.40	0.20	0.168	0.321	3.138	0.079	0.099	0.00008	0.00001	9.6	39.5
23SIML1	0.35	0.62	0.40	0.592	0.717	4.57	0.096	0.118	0.00029	0.0056	6.75	34.0

Note: The EC model used is shown in Figure 3.22(d), where R is given by (3.14).

where A is the area in square millimeters and p is the number of segments. When the metal 2 thickness was increased from 4.5 to 9.0 μm, the Q-value was enhanced by about 9% to 12%, the inductance value decreased by about 4% to 6.6%, and the resonant frequency did not change due to increased parasitic capacitance, respectively. These inductors have about 50% to 68% higher Q-factor values compared to standard inductors. The 10-μm-thick polyimide layer increased the values of the Q-factor and the resonance frequency of the inductors due to reduced dissipative loss and lower parasitic capacitance, respectively, similar to the characteristics observed in multilayer microstrip lines [83, 84]. The total inductance value is more or less invariant.

3.2.5 Compact Inductors

Compact inductors can be obtained by stacking several layers of inductor patterns. Such inductors are known as 3-D or *stacked inductors.* Potential problems in such inductors are lower Q because of higher series resistance of thin cross-under conductors, and lower self-resonant frequency due to higher interlayer capacitance. Bahl [80] reported on high-performance 3-D inductors using a multilayer process employing two levels of thick metallizations. A two-layer inductor with the first layer on 3-μm-thick polyimide and the second layer on 10-μm-thick polyimide was tested. Both inductor layers have 4.5-μm-thick metallizations and are connected by a via in 7-μm-thick polyimide. Because two-level inductor conductors are connected so that the RF current flows in the same direction through both of the inductor traces, the magnetic flux lines add in phase and result in a higher mutual inductance. Figure 3.44 shows two views of 15-segment inductors. The inductor parameters are the same as those given for the 15S inductor in Table 3.13; that is, a 20-μm line width and 12-μm line spacing.

The performance of a 3-D inductor is compared with rectangular spiral standard inductors (Table 3.13) and multilayer dielectric inductors (Table 3.14) in Figures 3.45, 3.46, and 3.47, which show total inductance, Q-factor, and f_{res}, respectively. For the 3-D inductor the inductance value is about 3.35 times higher compared to standard inductors having the same inductor area. The number of segments for each level of the 3-D inductor is 15, similar to 15S.

Table 3.16 summarizes figure of merit as defined in (3.17) for standard inductors, multilayer dielectric inductors using 9-μm-thick metal 2, and 3-D inductors. The value of inductance chosen is 6.7 nH. The 3-D structure has the best FMI because of the smallest area and has the lowest resonant frequency due to higher interlevel capacitances. The Q-factor for the 3-D inductor is about 23% higher than for the standard inductor, but about 16% lower than for the multilayer inductor using thick metallization.

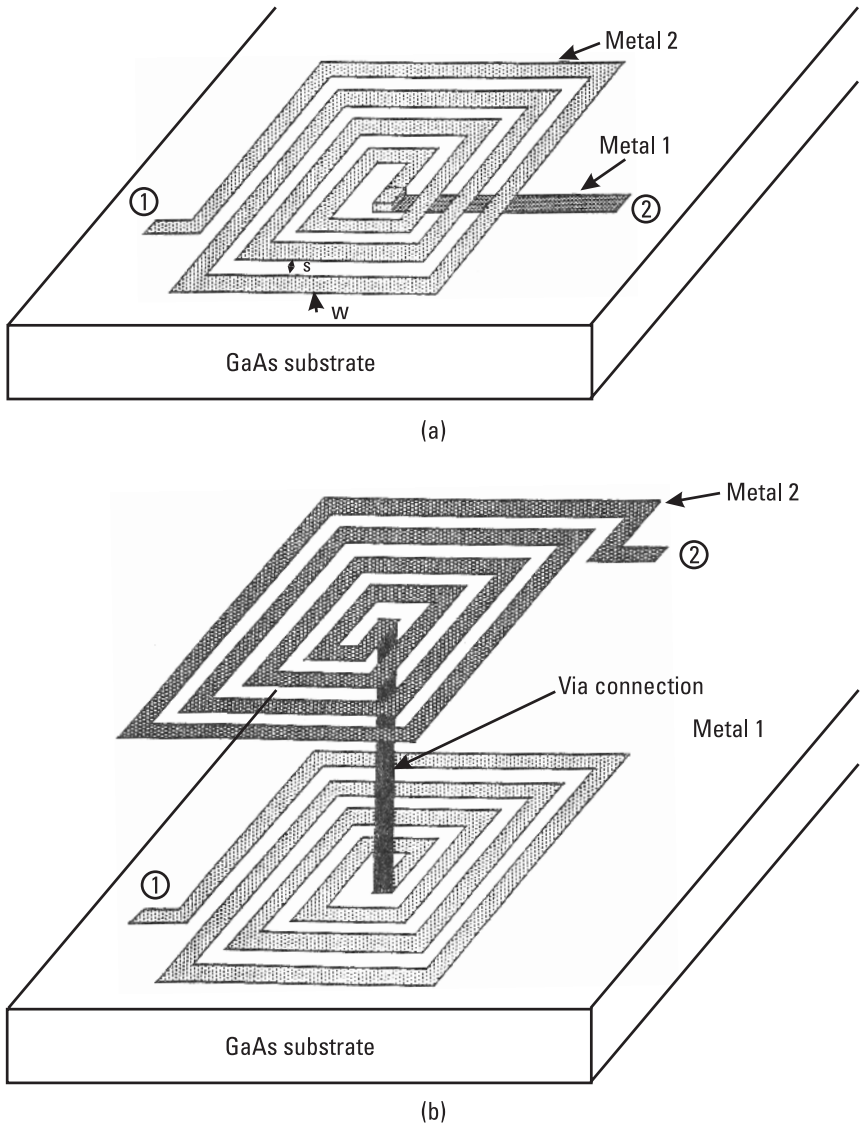


Figure 3.44 Rectangular spiral inductors: (a) multilayer and (b) multilevel.

The 3-D inductors have high current handling capacity, are compact in size, and have the highest figure of merit. The use of such inductors in passive and active MMICs will result in improved RF performance, smaller size, and lower cost. These inductors can also be used as RF chokes for biasing power amplifier circuits. The multilayer inductors also allow the use of thinner

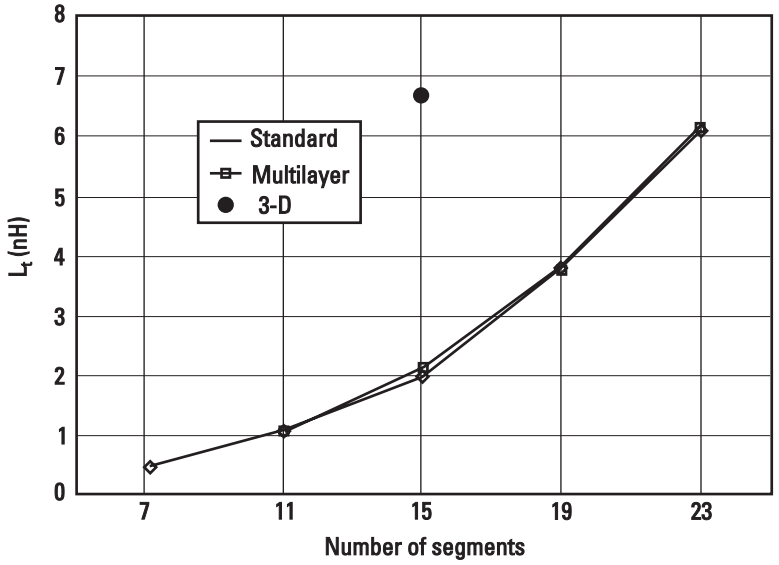


Figure 3.45 Variations of measured total inductance versus number of segments for standard, multilayer, and 3-D inductors.

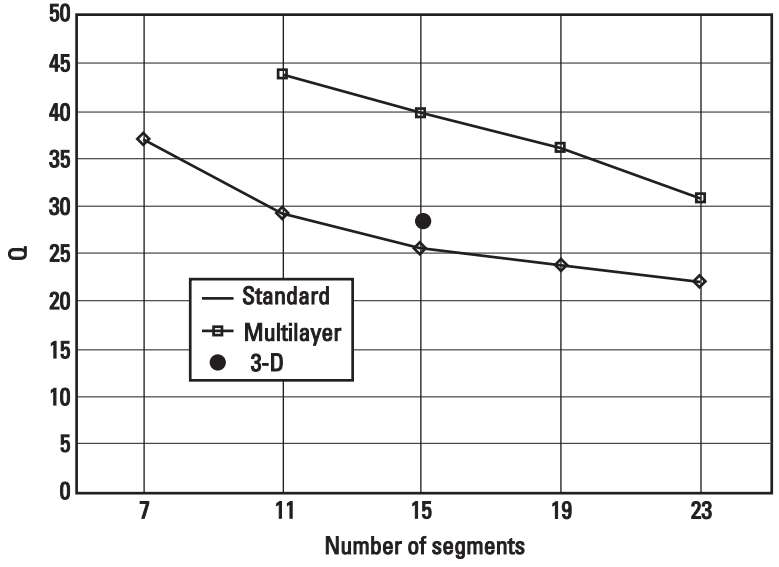


Figure 3.46 Variations of measured Q versus number of segments for standard, multilayer, and 3-D inductors.

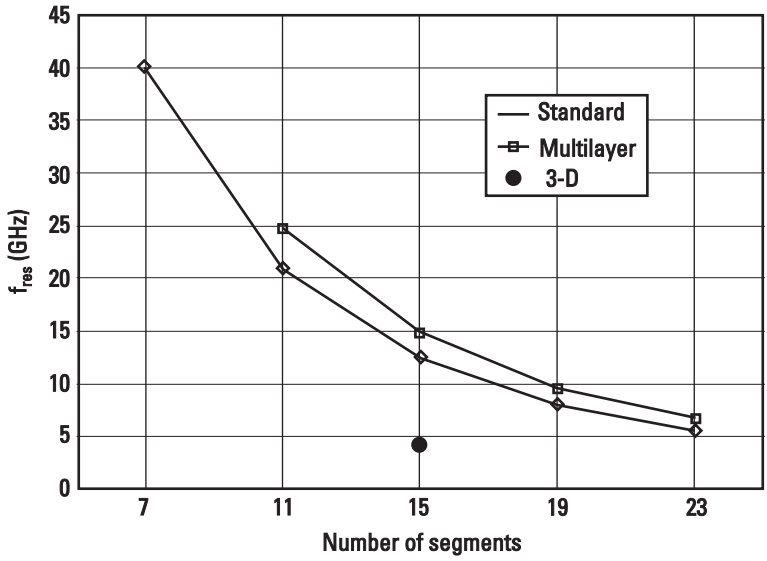


Figure 3.47 Variations of measured self-resonance frequency versus number of segments for standard, multilayer, and 3-D inductors.

Table 3.16
Comparison of Several 6.7-nH Inductors for Best Figure of Merit

Parameter	Standard Inductor	Multilayer Inductor	3-D Inductor	Units
f_{res}	5.0	6.4	4.43	GHz
Q	22.0	33.0	28.5	
Area	0.193	0.193	0.084	mm^2
FMI	5.7	10.9	15.03	10^2 GHz/mm^2

(2–3 mil) GaAs substrates, which help in the reliability of GaAs power ICs without increasing attenuation loss in the circuits.

Two- and three-level stacked square spiral inductors on GaAs substrate with different numbers of turns were EM simulated. Figure 3.48 shows the layout of a two-level inductor, and Figure 3.49 compares inductance and SRF versus inductor area for one-level, two-level, and three-level inductors. In all the three types, the inside hollow dimension is 50 μm, and line width and spacing are 8 μm. The GaAs substrate used was 75 μm thick.

For multilayer inductors, the inductance and f_{res} can be expressed in terms of area and number of turns. For example, for the inductor shown in Figure

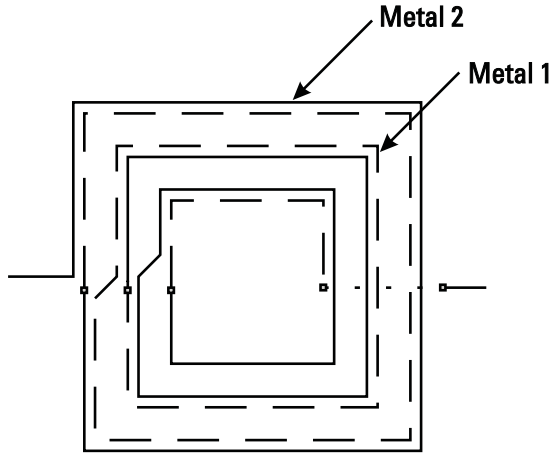


Figure 3.48 Physical layout of a two-level inductor using two metal layers.

3.48, the total inductance for single (L_1), two (L_2), and three layers (L_3) can be approximated as follows:

$$L_1 = 30An^{0.69} \tag{3.22a}$$

$$L_2 = 3.4L_1 \tag{3.22b}$$

$$L_3 = \left(2 + \frac{1.35}{n^2}\right) L_2 \tag{3.22c}$$

where A is the area of the inductor in square millimeters, and n is the number of turns. These empirical equations are derived from EM data taken on several sets of inductor structures tested on 75-μm-thick GaAs substrate with dimensions of $D_i = 50$ μm, $W = 8$ μm, and $S = 8$ μm. The thickness of inductors was assumed to be 4.5 μm. The resonance frequency is given by

$$f_{\text{res}} = \frac{26}{\sqrt{L_i}} \tag{3.23}$$

where $i = 1$, 2, and 3, and f_{res} and L_i are expressed in gigahertz and nanohenries, respectively.

3.2.6 High Current Handling Capability Inductors

Inductors fabricated using two levels of plating can be designed for much higher current capacity than is possible if one wiring layer must be thin, as is the case

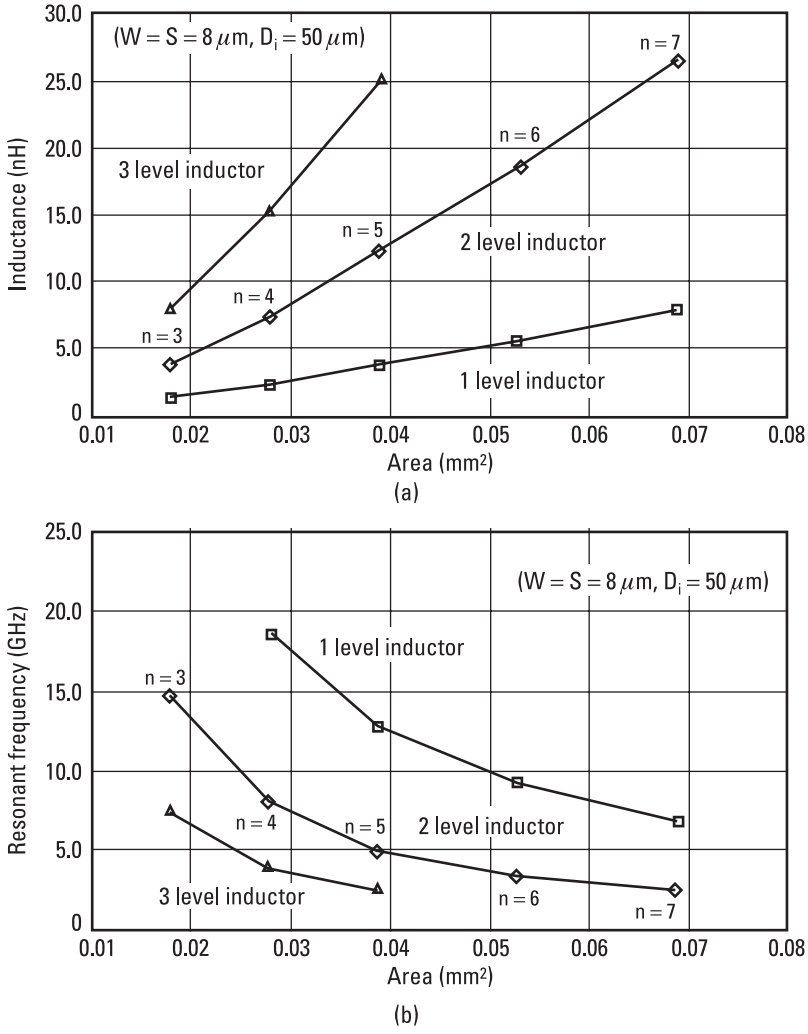


Figure 3.49 (a) Inductance and (b) SRF versus number of turns.

when only one layer of plating is available. Along with increased current capability, the Q-factor is enhanced due to lower resistance. The current-handling capability of a conductor is limited by the onset of electromigration. The conductor thickness and line width determine the current-carrying capacity of the inductor. A safe value of maximum current density for gold conductors on a flat surface is 3×10^5 A/cm^2 [80]. For example, for a 4.5-μm-thick conductor, the calculated maximum current-handling capability per unit width is 13.5 mA per micron so a 20-μm-wide line can handle up to 270 mA of current.

High current handling capability inductors were fabricated by using the multilayer process featuring two levels of global 4.5-μm plated gold metallization. Polyimide is used as an interlevel dielectric for the interconnect metal and a glassivation or buffer layer for mechanical protection of the finished circuitry. The thickness of the interlevel layers 1, 2, and buffer layer polyimide are 3, 7, and 7 μm, respectively. The thickness of the plated gold metallizations 1 and 2 are both about 4.5 μm. Thicker (9-μm) metallization 2 is also available for the MMIC process. The separation between the two plated metallizations is about 7 μm and they are connected by vias through the 7-μm-thick polyimide. Test data reported in Tables 3.14 and 3.15 were for high-current inductors and can handle current values of 0.27 and 0.54A, respectively. For Table 3.15, the metal 2 thickness is 9 μm and the width of metal 1 is twice the inductor's line width.

3.3 Printed Circuit Board Inductors

Printed circuit board (PCB) spiral inductors, used for biasing and matching active devices, have been designed and characterized on multilayer PCBs [85–87]. Figure 3.50(a) shows a cross-sectional view of a multiturn inductor embedded in a 1-mm-thick, copper-clad (9-μm) FR-4 substrate. The spacing between the conductors is 2 mil. Input and output connections to the inductor were made using via through holes in 25-μm-thick polyimide. The effects of inductor area and number of turns on its inductance, Q-factor, and resonant frequency were studied [85]. Figure 3.50(b) shows the variations of inductance, maximum quality factor, and the resonance frequency versus number of turns for various inductor area values. The summary of results is similar to that of monolithic inductors on GaAs. The maximum Q-factor decreases with increasing number of turns due to increased parasitic capacitance and eddy current resistance. Here also the inductance increases approximately as n^2 and the self-resonance frequency decreases because of increased parasitic capacitance.

As discussed in previous sections, several techniques including variable line width, thick conductors, thicker substrates, and multilayer dielectric configurations can be used to improve the Q-factor of inductors. The Q-factor can also be enhanced by replacing the ground plane with a two-dimensional periodic structure as shown in Figure 3.51. In this case, the ground plane consists of a thin, two-sided PCB having identical rectangular rings on both sides, with their centers connected using via through holes. Such a periodic structure lowers the eddy current resistance and reduces the parasitic shunt capacitance value. For a 1.5-turn inductor (1.5×1.5 mm) on Rogers 4003 ($\epsilon_r = 3.8$), the inductance and Q-values were improved by more than 30% [86].

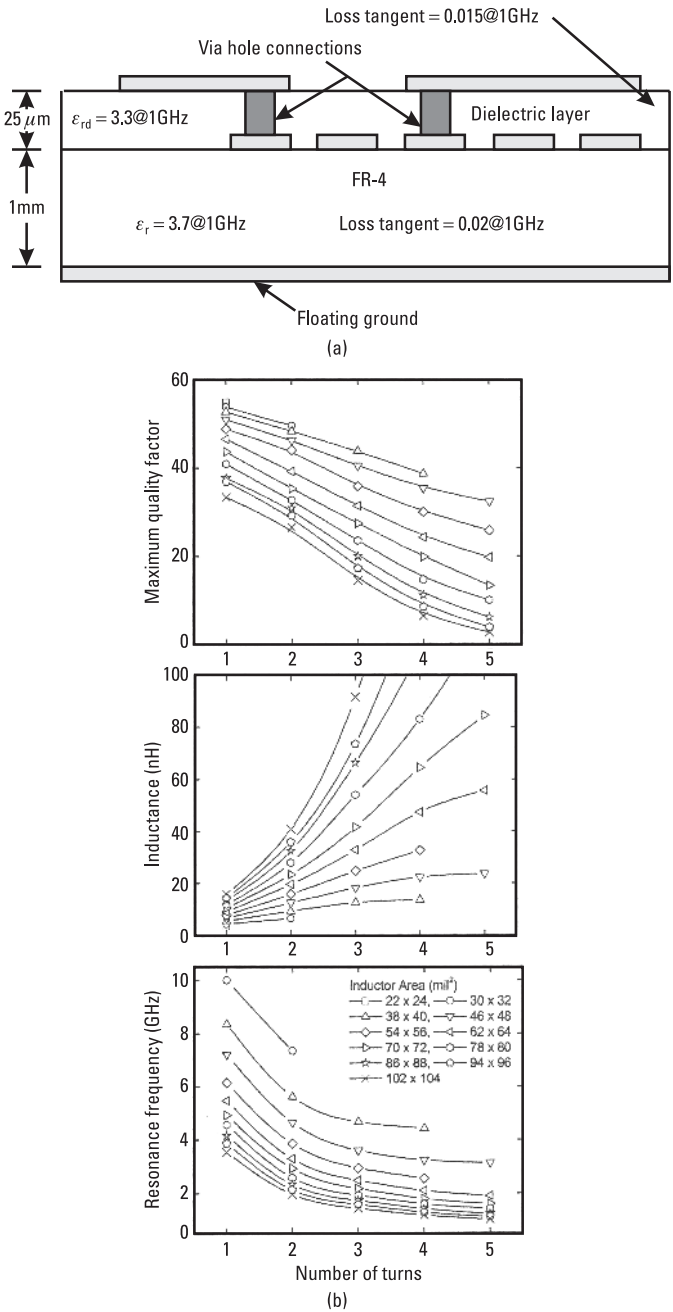


Figure 3.50 (a) Cross-sectional view of the PCB inductor; and (b) variations of inductance, self-resonance frequency, and maximum Q as a function of number of turns for various inductor areas. The separation between the turns was 2 mil. (*From:* [85]. © 2002 IEEE. Reprinted with permission.)

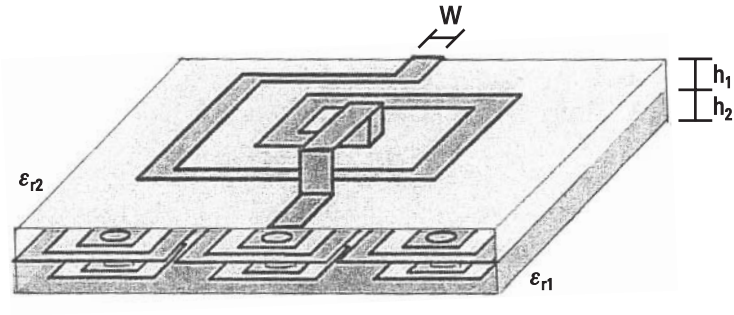


Figure 3.51 Two-dimensional periodic structure enhanced *Q*-inductor. (*From:* [86]. © 2002 IEEE. Reprinted with permission.)

The design of meander line inductors on PCBs has been described [87]. Meander line inductors have lower inductance per unit area than coil inductors; however, they do not require a multilevel process and thus have lower manufacturing cost. Figure 3.52(a) shows a one-turn meander line inductor, and its simplified lumped-element EC model is shown in Figure 3.52(b), where the R_c term is a result of dielectric loss. Closed-form expressions for EC parameters have been reported [87] and validated using experimental data for several different inductors. Table 3.17 provides dimensions and electrical data for a variety of such inductors. The electrical data are based on measured performance.

The Q-factor and f_{res} were calculated using the following relations [87]:

$$Q = \frac{R_c\,\omega(L - \omega^2 L^2 C - R_l^2\,C)}{R_l^2 + R_c R_l + \omega^2 L^2} \tag{3.24}$$

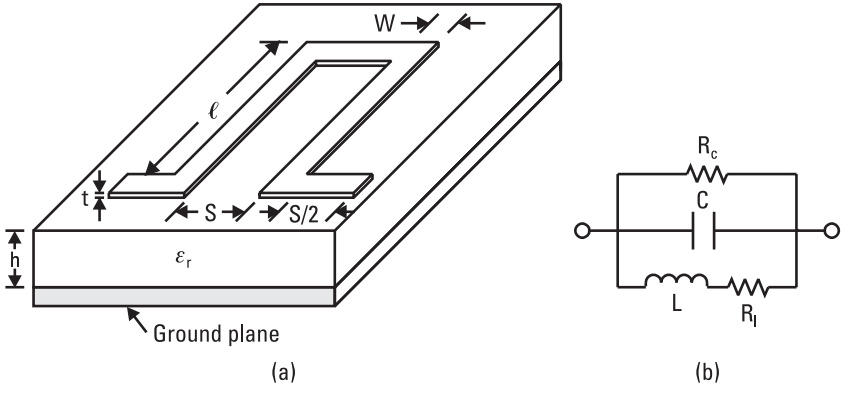


Figure 3.52 (a) Configuration of a one-turn meander line inductor. (b) LE model.

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{LC}} \tag{3.25}$$

3.4 Hybrid Integrated Circuit Inductors

The evaluation of lumped inductors using MIC technology for microwave applications began in the mid-1960s. The growth of inductors took off after the development of MIC techniques for printing high-resolution patterns on alumina substrates [88, 89]. In this section, inductors fabricated using hybrid integrated circuit technologies such as thin film, thick film, and LTCC are described.

3.4.1 Thin-Film Inductors

High-quality inductors developed using multilayer thin-film glass technology have been described [90]. The inductor pattern was made up of 3-μm-thick copper printed on a 5-μm-thick BCB ($\epsilon_{rd} = 2.7$) layer backed by 700-μm-thick low-loss borosilicate glass substrate ($\epsilon_r = 6.2$). The coils were designed in a coplanar configuration as shown in Figure 3.53 and have an inner diameter of 200 μm. The spacing between the inductor conductor and the coplanar ground plane was 200 μm. The connection between the center of the coil and the output was made using a second layer of copper printed on the second 5-μm-thick BCB layer on top of the inductor pattern.

Several inductors having different line widths and numbers of turns were characterized. Table 3.18 lists physical dimensions for nine inductors. Measured inductance and Q-factor values versus frequency, for these inductors, are plotted in Figure 3.54. Typical measured L, $Q_{\max}$, and f_{res} values for a 3.5-turn inductor (d in Table 3.18) are about 6.2 nH, 48.5, and 7.9 GHz, respectively.

The Q of thin-film inductors was enhanced by using suspended inductors with large air core area over the glass substrate. The inductors were fabricated by employing a multilayer thin-film process and surface-micromachining techniques. The rectangular spiral inductor pattern consisting of 9-μm-thick copper was suspended with the help of polyimide posts, and the center of the inductor was connected to the output using TiCu film on the glass substrate through a plated via hole. Figure 3.55 shows the rectangular spiral inductor, and measured electrical data for three different inductors are summarized in Table 3.19. The electrical data in this table represent state-of-the-art performance for printed inductors with reduced substrate loss and parasitic capacitance.

Table 3.17
Summary of Meander Line Inductor Dimensions and Electrical Parameters*

Number	Turns	*l* (mm)	*W* (mm)	*S* (mm)	*L* (nH)	*C* (pF)	R_l (Ω)	R_c (Ω)	*Q* (470 MHz)	f_{res} (GHz)
1	2	10	0.4	0.4	19	0.4	0.3	2,098	29	1.79
2	4	10	0.4	0.4	34	1.0	0.8	5,312	26	0.87
3	2	10	0.6	0.4	16	0.6	0.2	1,688	28	1.64
4	4	10	0.6	0.4	28	1.2	0.5	4,823	31	0.87
5	2	10	0.8	0.4	14	0.7	0.2	1,653	31	1.62
6	4	10	0.8	0.4	25	1.4	0.4	4,129	29	0.84
7	2	10	1.0	0.4	14	0.7	0.1	1,579	31	1.61
8	4	10	1.0	0.4	23	1.7	0.3	3,181	26	0.81
9	2	10	2.0	0.4	10	1.2	0.1	1,163	30	1.44
10	4	10	2.0	0.4	19	2.9	0.3	2,891	21	0.68
11	2	10	0.4	0.6	17	0.6	0.2	1,142	19	1.57
12	4	10	0.4	0.6	31	1.2	0.9	6,976	29	0.81
13	1	8	0.7	0.8	10	0.9	0.1	3,252	70	1.72
14	2	8	0.7	0.8	17	1.2	0.2	4,106	50	1.11
15	4	8	0.7	0.8	27	2.0	0.2	3,886	22	0.68
16	5	8	0.7	0.8	33	2.6	0.2	4,005	10	0.54

Table 3.17 *(continued)*
Summary of Meander Line Inductor Dimensions and Electrical Parameters*

Number	Turns	l (mm)	W (mm)	S (mm)	L (nH)	C (pF)	R_l (Ω)	R_c (Ω)	Q (470 MHz)	f_{res} (GHz)
17	6	8	0.7	0.8	36	3.2	0.3	3,576	0	0.47
18	1	8	0.9	0.8	9	1.0	0.1	2,917	78	1.65
19	2	8	0.9	0.8	15	1.4	0.1	3,374	52	1.08
20	4	8	0.9	0.8	25	2.2	0.2	4,146	25	0.67
21	5	8	0.9	0.8	28	2.7	0.2	4,016	14	0.57
22	6	8	0.9	0.8	32	3.4	0.2	3,955	2	0.48
23	2	10	0.4	0.8	20	0.7	0.2	1,537	21	1.34
24	4	10	0.4	0.8	34	1.4	0.8	5,455	23	0.74
25	2	4	1.0	1.0	8	0.9	0.1	951	33	1.84
26	2	6	1.0	1.0	12	1.1	0.1	1,479	32	1.37
27	2	8	1.0	1.0	13	1.3	0.1	1,840	34	1.20
28	4	10	0.4	1.0	39	1.4	1.0	7,254	21	0.68
29	2	10	1.0	1.0	17	1.5	0.2	4,004	45	0.99
30	2	15	1.0	1.0	24	2.1	0.3	4,446	29	0.72
31	2	20	1.0	1.0	27	2.7	0.3	4,427	16	0.58
32	4	10	0.4	2.0	46	1.9	1.0	8,280	10	0.53

*For PCBs, $\epsilon_r = 4.6$, $h = 1.5$ mm, and $t = 0.035$ mm

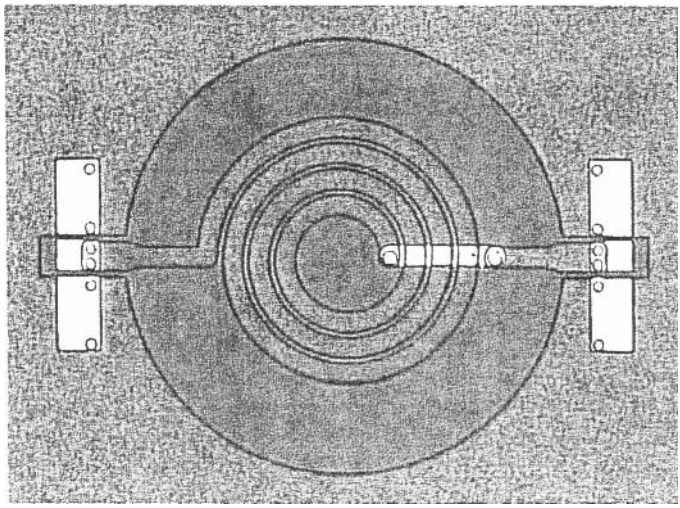


Figure 3.53 Top view of a 3.5-turn inductor with ground-signal ground RF probe pads. (*From:* [87]. © 2001 IEEE. Reprinted with permission.)

Table 3.18
Dimensions for Spiral Inductors with Different Conductor Widths and Number of Turns*

Spiral Label	a	b	c	d	e	f	g	h	i
Conductor width (μm)	30	50	100	30	50	100	30	50	100
Number of turns	1.5	1.5	1.5	3.5	3.5	3.5	5.5	5.5	5.5
Total outer diameter (μm)	380	460	660	580	740	1,140	780	1,020	1,620

*Conductor spacing is 20 μm, the inner diameter is 100 μm, and spacing to the coplanar ground plane is 200 μm.

3.4.2 Thick-Film Inductors

The design and test data for several rectangular and circular spiral inductors printed using a thick-film process on alumina substrate have been reported [91]. At RF and lower microwave frequencies, the thick-film process is a viable technology to develop low-cost MCMs. The inductors were designed using simple equations [92] on a 25-mil-thick alumina substrate (ϵ_r = 9.6). The inductance and Q-values were obtained by connecting a known capacitor across the inductor and measuring the one-port reflection coefficient as described in Section 2.4.5. The inside port of the inductor was grounded through a 12-mil-

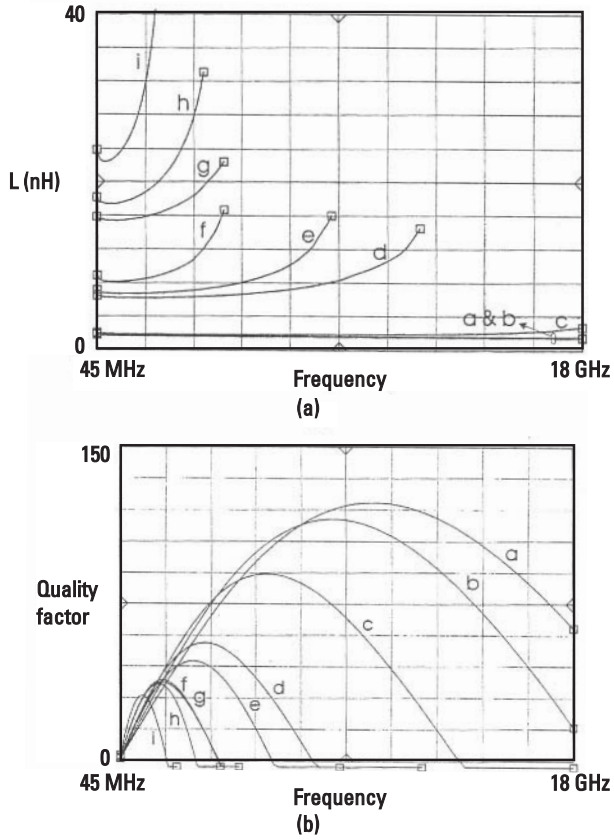


Figure 3.54 (a) Measured inductance and (b) Q versus frequency for several inductors listed in Table 3.18. (*From:* [90]. © 2001 IEEE. Reprinted with permission.)

diameter via hole and the output port was connected to a 25-mil RF pad. A shunt capacitor mounted on a grounded pad was connected to the RF pad through a 15-mil-long, 1-mil-thick gold wire to resonate out the inductor. One-port S-parameters were measured using RF probes by placing the center conductor of the probe on the inductor's RF pad and its ground connection on the capacitor ground pad as shown in Figure 3.56. Measuring the first parallel resonant frequency and 3-dB bandwidth, the inductance and Q-value were obtained as discussed in Section 2.3.5. Here two different capacitor values were used, 3.6 and 4.7 pF. Table 3.20 summarizes the measured data for three inductors having 2, 3, and 4 turns. Because the Q-values of the discrete capacitors were much greater than the printed inductor's Q, the effect of the capacitor Q was neglected. The self-resonant frequencies of the inductors are also several times greater than the capacitor tuned resonance frequencies.

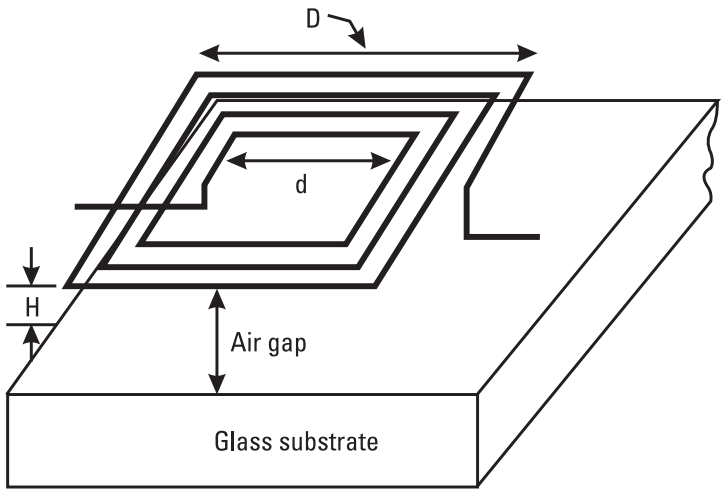


Figure 3.55 Configuration of a suspended rectangular spiral inductor having large air core area.

Table 3.19
Measured Data Summary for Three Suspended Inductors, with $t = 9$ μm and $H = 60$ μm

Line Width (μm)	Spacing (μm)	Inner Diameter d (μm)	Outer Diameter D (μm)	Number of Turns	L (nH)	Q_{max}	f_{res} (GHz)
40	40	800	1,280	3.5	27.3	50	2.85
40	40	500	1,300	5.5	37.8	44	2.40
40	50	500	1,030	3.5	16.5	46	4.20

3.4.3 LTCC Inductors

LTCC technology [93–97] offers great potential to realize compact, high-performance inductors. Multilevel thick plating enables the design of different inductor topologies including multilayer standard and offset 3-D, helical, solenoid, and meander line inductors. In standard, solenoid, and meander line inductors, the inductance is increased by increasing the number of turns laterally, resulting in increased area, series resistance, and parasitic capacitances. In contrast, in 3-D and helical inductors, the inductance is increased by increasing the number of inductor layers and keeping a larger separation between the layers, resulting in smaller area for given inductance value, lower series resistance due to reduced eddy current resistance, and lower parasitic capacitances. Thus, 3-D and helical inductors in LTCC technology have higher Q- and SRF values as compared

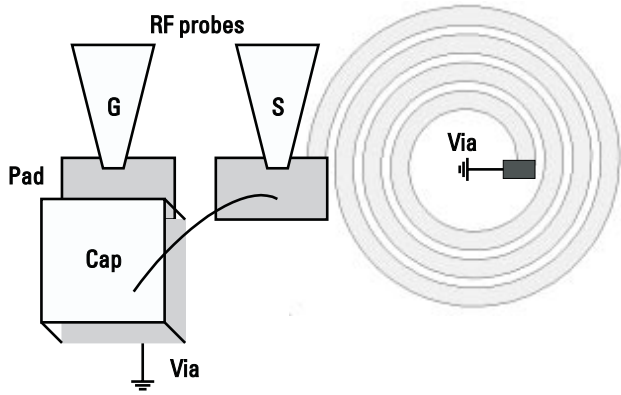


Figure 3.56 Capacitor tuned inductor.

Table 3.20
Measured Inductance and *Q*-Factor of Thick-Film Inductors on a 25-Mil-Thick Alumina Substrate, with Line Width and Spacing = 6 Mil

Number of Turns	*L* (nH)	*Q*
2	9.7	32.7
3	13.0	30.6
4	34.0	10.6

to 2-D standard inductors. Figure 3.57 shows conventional 2-D, 3-D, and helical inductor configurations.

3.5 Ferromagnetic Inductors

Thin-film ferromagnetic materials have been applied to integrated inductors to enhance their inductance and *Q*-values [98, 99] by increasing the magnetic flux associated with the coil. One ferromagnetic film material used is CoNbZr, which has a relative permeability of about 500 to 1,000 and a thickness of about 0.1 μm. The film is deposited using a RF sputtering technique. Test results report improved inductance and *Q*-values by about 10% to 20% at 2 GHz, probably due to the thin layer of CoNbZr.

Ferromagnetic inductors can be realized either by sandwiching the inductor coil between magnetic materials or by placing a magnetic material over the coil as shown in Figure 3.58. The sandwich-type configuration is preferred due to

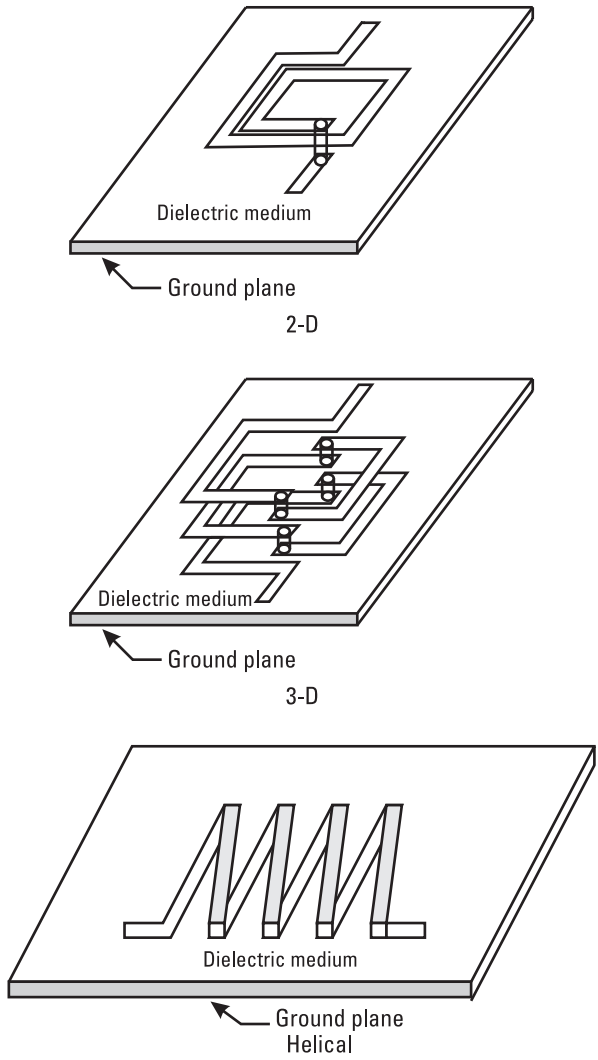


Figure 3.57 Various LTCC inductor configurations: 2-D standard, 3-D, and helical.

its larger increased magnetic flux in the coil. The frequency of operation of such inductors can be extended by cutting slits in the magnetic materials. Thicker ferromagnetic films will also give rise to higher inductance values.

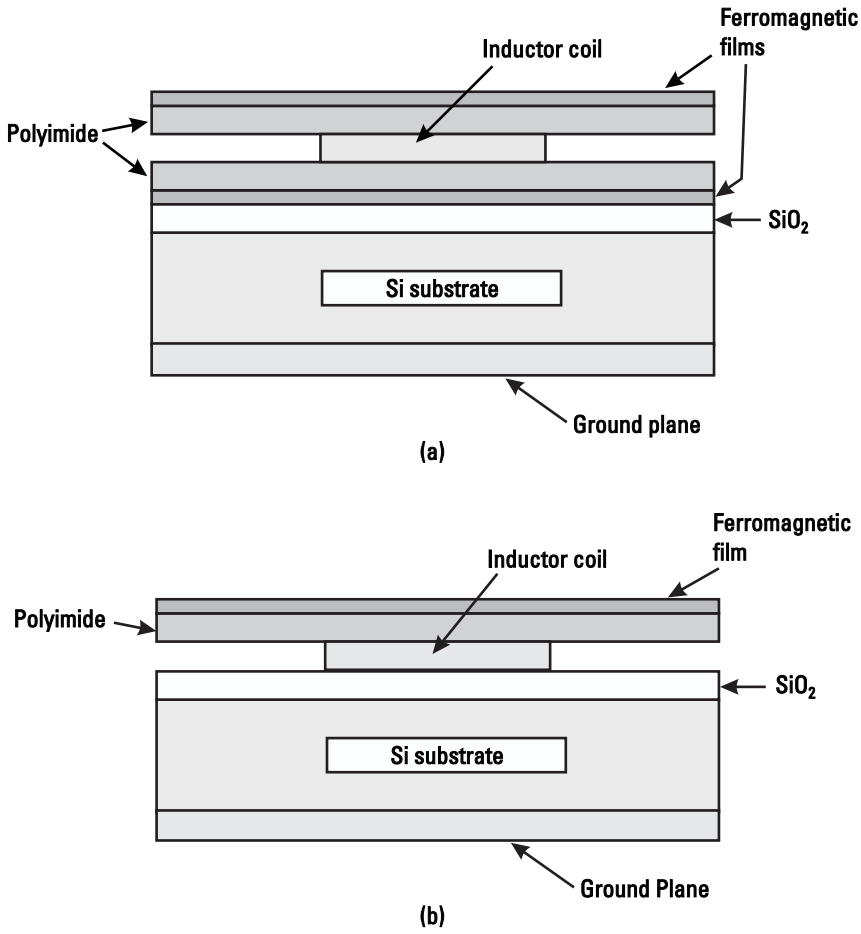


Figure 3.58 Cross-sectional view of ferromagnetic integrated inductors: (a) sandwich type and (b) on-top type.

References

[1] Neguyen, N. M., and R. G. Meyer, "Si IC-Compatible Inductors and IC Passive Filters," *IEEE J. Solid-State Circuits,* Vol. 25, August 1990, pp. 1028–1031.

[2] Chang, J. Y.-C., A. A. Abidi, and M. Gaitan, "Large Suspended Inductors on Silicon and Their Use in a 2-μm CMOS RF Amplifier," *IEEE Electron. Device Lett.,* Vol. 14, May 1993, pp. 246–248.

[3] Reyes, A. C., et al., "Coplanar Waveguides and Microwave Inductors on Silicon Substrates," *IEEE Trans. Microwave Theory Tech.,* Vol. 43, September 1995, pp. 2016–2022.

[4] Chi, C.-Y., and G. M. Rebeiz, "Planar Microwave and Millimeter-Wave Lumped Elements and Coupled-Line Filters Using Micro-Machining Techniques," *IEEE Trans. Microwave Theory Tech.,* Vol. 43, April 1995, pp. 730–738.

[5] Ashby, K. B., et al., "High Q Inductors for Wireless Applications in a Complementary Silicon Bipolar Process," *IEEE J. Solid-State Circuits,* Vol. 31, January 1996, pp. 4–9.

[6] Burghartz, J. N., M. Soyuer, and K. A. Jenkins, "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology," *IEEE Trans. Microwave Theory Tech.,* Vol. 44, January 1996, pp. 100–104.

[7] Zu, L., et al., "High *Q*-Factor Inductors Integrated on MCM Si Substrates," *IEEE Trans. Components, Packaging, and Manufacturing Tech.—Part B,* Vol. 19, August 1996, pp. 635–642.

[8] Burghartz, J. N., K. A. Jenkins, and M. Soyuer, "Multilevel-Spiral Inductors Using VLSI Interconnect Technology," *IEEE Electron. Device Lett.,* Vol. 17, September 1996, pp. 428–430.

[9] Johnson, R. A., et al., "Comparison of Microwave Inductors Fabricated on Silicon-on Sapphire and Bulk Silicon," *IEEE Microwave Guided Wave Lett.,* Vol. 6, September 1996, pp. 323–325.

[10] Park, M., et al., "High Q CMOS-Compatible Microwave Inductors Using Double-Metal Interconnection Silicon Technology," *IEEE Microwave Guided Wave Lett.,* Vol. 7, February 1997, pp. 45–47.

[11] Long, J. R., and M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's," *IEEE J. Solid-State Circuits,* Vol. 32, March 1997, pp. 357–369.

[12] Craninckx, J., and M. S. J. Steyaert, "A 1.8 GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE J. Solid-State Circuits,* Vol. 32, May 1997, pp. 736–744.

[13] Park, M., et al., "Optimization of High *Q*-CMOS-Compatible Microwave Inductors Using Silicon CMOS Technology," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1997, pp. 129–132.

[14] Zhao, J., et al., "S Parameter-Based Experimental Modeling of High Q MCM Inductor with Exponential Gradient Learning Algorithm," *IEEE Trans. Components, Packaging, and Manufacturing Tech.—Part B,* Vol. 20, August 1997, pp. 202–210.

[15] Nam, C., and Y.-S. Kwon, "High-Performance Planar, Inductor on Thick Oxidized Porous Silicon (OPS) Substrate," *IEEE Microwave Guided Wave Lett.,* Vol. 7, August 1997, pp. 236–238.

[16] Groves, R., D. L. Harame, and D. Jadus, "Temperature Dependence of Q and Inductance in Spiral Inductors Fabricated in a Silicon-Germanium/Bi CMOS Technology," *IEEE J. Solid-State Circuits,* Vol. 32, September 1997, pp. 1455–1459.

[17] Burghartz, J. N., et al., "Integrated RF Components in a SiGe Bipolar Technology," *IEEE J. Solid-State Circuits,* Vol. 32, September 1997, pp. 1440–1445.

[18] Burghartz, J. N., et al., "Spiral Inductor and Transmission Lines in Silicon Technology Using Copper-Damascene Interconnects and Low-Loss Substrates," *IEEE Trans. Microwave Theory Tech.,* Vol. 45, October 1997, pp. 1961–1968.

[19] Yie, C. P., and S. S. Wang, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE J. Solid-State Circuits,* Vol. 33, May 1998, pp. 743–752.

[20] Kim, J. S., et al., "F-Inductor and BC-MOS Technology for Monolithic Silicon RFIC's," *IEEE Radio Frequency Integrated Circuits Symp. Dig.,* 1998, pp. 165–168.

[21] Lopez-Villegas, J. M., et al., "Improvement of the Quality Factor of RF Integrated Inductors by Layout Optimization," *IEEE RFIC Symp. Dig.,* 1998, pp. 169–172.

[22] Danesh, M. et al., "A Q-Factor Enhancement Technique for MMIC Inductors," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1998, pp. 183–186.

[23] Okabe, H., et al., "Characterization of a Planar Spiral Inductor on a Composite-Resin Low-Impedance Substrate and Its Application to Microwave Circuits," *IEEE Trans. Components, Packaging, and Manufacturing Tech.—Part B,* Vol. 21, August 1998, pp. 269–272.

[24] Mernyei, F., et al., "Reducing the Substrate Losses of RF Integrated Inductors," *IEEE Microwave Guided Wave Lett.,* Vol. 8, September 1998, pp. 300–301.

[25] Xie, Y.-H., et al., "An Approach for Fabricating High-Performance Inductors on Low-Resistivity Substrates," *IEEE J. Solid-State Circuits,* Vol. 33, September 1998, pp. 1433–1438.

[26] Niknejad, A. M., and R. G. Meyer, "Analysis, Design and Optimization of Spiral Inductors and Transformers for Si RF ICs," *IEEE J. Solid-State Circuits,* Vol. 33, October 1998, pp. 1470–1481.

[27] Burghartz, J. N., "Spiral Inductors on Silicon-Status and Trends," *Int. J. RF Microwave Computer-Aided Engineering,* Vol. 8, November 1998, pp. 422–432.

[28] Burghartz, J. N., et al., "RF Circuit Design Aspect of Spiral Inductors on Si," *IEEE J. Solid-State Circuits,* Vol. 33, December 1998, pp. 2028–2034.

[29] Kuhn, W. B., and N. K. Yanduru, "Spiral Inductor Substrate Loss Modeling in Silicon RFICs," *Microwave J.,* Vol. 42, March 1999, pp. 66–81.

[30] Park, J. Y., and M. G. Allen, "Packaging-Compatible High Q Microinductors and Microfilters for Wireless Applications," *IEEE Trans. Advanced Packaging,* Vol. 22, May 1999, pp. 207–213.

[31] Lutz, R. D., et al., "Modeling and Analysis of Multilevel Spiral Inductors for RFICs," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1999, pp. 43–46.

[32] Kamogawa, K., et al., "A Novel High-Q-Inductor Based on Si 3D MMIC Technology and its Application," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1999, pp. 489–492.

[33] Sun, Y., et al., "Micromachined RF Passive Components and Their Applications in MMICs," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 9, July 1999, pp. 310–325.

[34] Arcioni, P., et al., "Modeling of Metal and Substrate Losses in CMOS and BiCMOS Inductors for RFICs," *Microwave J.,* Vol. 42, August 1999, pp. 62–74.

[35] Rautio, J. C., "Free EM Software Analyzes Spiral Inductor on Silicon," *Microwaves & RF,* Vol. 38, September 1999, pp. 165–172.

[36] Mohan, S. S., et al., "Simple Accurate Expressions for Planar Spiral Inductances," *IEEE J. Solid-State Circuits,* Vol. 34, October 1999, pp. 1419–1424.

[37] Park, M., et al., "Frequency-Dependent Series Resistance of Monolithic Spiral Inductors," *IEEE Microwave Guided Wave Lett.,* Vol. 9, December 1999, pp. 514–516.

[38] Lopez-Villegas, J. M., et al., "Improvement of the Quality Factor of RF Integrated Inductors by Layout Optimization," *IEEE Trans. Microwave Theory Tech.,* Vol. 48, January 2000, pp. 76–83.

[39] Ribas, R. P., et al., "Micromachined Microwave Planar Spiral Inductors and Transformers," *IEEE Trans. Microwave Theory Tech.,* Vol. 48, August 2000, pp. 1326–1335.

[40] Kuhn, W. B., and N. M. Ibrahim, "Analysis of Current Crowding Effects in Multiturn Spiral Inductors," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, January 2001, pp. 31–38.

[41] Niknezad, A. M., and R. G. Meyer, "Analysis of Eddy-Current Losses Over Conductive Substrates with Applications to Monolithic Inductors and Transformers," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, January 2001, pp. 166–176.

[42] Zolfaghari, A., A. Chan, and B. Razavi, "Stacked Inductors and Transformers in CMOS Technology," *IEEE J. Solid-State Circuits,* Vol. 36, April 2001, pp. 620–628.

[43] Chen, Y. E., et al., "A 2.4 GHz Integrated CMOS Power Amplifier with Micromachined Inductors," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2001, pp. 523–526.

[44] Chen, Y. E., et al., "Q-Enhancement of Spiral Inductor with N+-Diffusion Patterned Ground Shield," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2001, pp. 1289–1292.

[45] Aguilera, J., et al., "A Guide for On-Chip Inductor Design in a Conventional CMOS Process for RF Applications," *Applied Microwaves & Wireless,* Vol. 13, October 2001, pp. 56–65.

[46] Sieiro, J., et al., "A Physical Frequency-Dependent Compact Model for RF Integrated Inductors," *IEEE Trans. Microwave Theory Tech.,* Vol. 50, January 2002, pp. 384–392.

[47] Yim, S. M., T. Chen, and K. K. O, "The Effects of a Ground Shield on the Characteristics and Performance of Spiral Inductors," *IEEE J. Solid-State Circuits,* Vol. 37, February 2002, pp. 237–244.

[48] Tang, C. C., C. H. Wu, and S. I. Liu, "Miniature 3-D Inductors in Standard CMOS Process," *IEEE J. Solid-State Circuits,* Vol. 37, April 2002, pp. 471–480.

[49] Adan, A. O., et al., "Electromagnetic Coupling Effects in RFCMOS Circuits," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 39–42.

[50] Kamgaing, T., et al., "Modeling of Frequency Dependent Losses in Two-Port and Three-Port Inductors on Silicon," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 153–156.

[51] Chao, C., et al., "Characterization and Modeling of On-Chip Inductor Substrate Coupling Effect," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 157–160.

[52] Dubuc, D., et al., "High Quality Factor and High Self-Resonant Frequency Monolithic Inductor for Millimeter-Wave Si-Based ICs," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 193–196.

[53] Kuhn, W. B., et al., "Spiral Inductor Performance in Deep-Submicron Bulk-CMOS with Copper Interconnects," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 301–304.

[54] Huo, X., K. J. Chen, and P. C. H. Chan, "High-Q-Copper Inductors on Standard Silicon Substrate with a Low-k BCB Dielectric Layer," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 513–516.

[55] Chang, J. H., et al., "Effects of Dummy Patterns and Substrate on Spiral Inductors for Sub-Micron RFICs," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 529–532.

[56] Feng, H., et al., "Super Compact RFIC Inductors in 0.18 μm CMOS with Copper Interconnects," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 553–556.

[57] Bunch, R. L., D. I. Sanderson, and S. Raman, "Quality Factor and Inductance in Differential IC Implementations," *IEEE Microwave Magazine,* Vol. 3, June 2002, pp. 82–92.

[58] Lin, Y. S., and H. M. Hsu, "Study of Spiral Inductors Using Cu/Low-k Interconnect for High Performance Radio-Frequency Integrated Circuit (RF-IC) Applications," *Microwave Optical Tech. Lett.,* Vol. 34, July 2002, pp. 43–48.

[59] Yaojiang, Z., et al., "An Accurate Lumped Model for Micromachined Microwave Planar Spiral Inductors," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 13, 2003.

[60] Burghartz, J. N., and B. Rejaei, "On the Design of RF Spiral Inductors on Silicon," *IEEE Trans. Electron Devices,* 2003, in press.

[61] Sun, Y., et al., "Suspended Membrane Inductors and Capacitors for Application in Silicon MMICs," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.,* 1996, pp. 99–102.

[62] Jiang, H., et al., "On-Chip Spiral Inductors Suspended Over Deep Copper-Lined Cavities," *IEEE Trans. Microwave Theory Tech.,* Vol. 48, December 2000, pp. 2415–2423.

[63] Lakdawala, H., et al., "Micromachined High-Q-Inductors in a 0.18-μm Copper Interconnect Low-K Dielectric CMOS Process," *IEEE J. Solid-State Circuits,* Vol. 37, March 2002, pp. 394–403.

[64] Camp, Jr., W. O., S. Tiwari, and D. Parson, "2-6 GHz Monolithic Microwave Amplifier," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1983, pp. 46–49.

[65] Cahana, D., "A New Transmission Line Approach for Designing Spiral Microstrip Inductors for Microwave Integrated Circuits," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1983, pp. 245–247.

[66] Wolff, I., and G. Kibuuka, "Computer Models for MMIC Capacitors and Inductors," *14th European Microwave Conference Proc.,* 1984, pp. 853–858.

[67] Shepherd, P. R., "Analysis of Square-Spiral Inductors for Use in MMICs," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-34, April 1986, pp. 467–472.

[68] Krafcsik, D. M., and D. E. Dawson, "A Closed-Form Expression for Representing the Distributed Nature of the Spiral Inductor," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1986, pp. 87–92.

[69] Pettenpaul, E., et al., "CAD Models of Lumped Elements on GaAs up to 18 GHz," *IEEE Trans. Microwave Theory Tech.,* Vol. 36, February 1988, pp. 294–304.

[70] Geen, M. W., et al., "Miniature Mutilayer Spiral Inductors for GaAs MMICs," *IEEE GaAs IC Symp. Dig.,* 1989, pp. 303–306.

[71] Shih, Y. C., C. K. Pao, and T. Itoh, "A Broadband Parameter Extraction Technique for the Equivalent Circuit of Planar Inductors," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1992, pp. 1345–1348.

[72] Schmuckle, F. J., "The Method of Lines for the Analysis of Rectangular Spiral Inductors," *IEEE Trans. Microwave Theory Tech.,* Vol. 41, June/July 1993, pp. 1183–1186.

[73] Sadhir, V. K., I. J. Bahl, and D. A. Willems, "CAD Compatible Accurate Models of Microwave Passive Lumped Elements for MMIC Applications," *Int. J. Microwave and Millimeter-Wave Computer-Aided Engineering,* Vol. 4, April 1994, pp. 148–162.

[74] Engels, M., and R.H. Jansen, "Modeling and Design of Novel Passive MMIC Components with Three and More Conductor Levels," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1994, pp. 1293–1296.

[75] Fisher, D., and I. Bahl, *Gallium Arsenide IC Applications Handbook,* Boston: Academic Press, 1995.

[76] Chaki, S., et al., "Experimental Study of Spiral Inductors," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1995, pp. 753–756.

[77] Paek, S. W., and K. S. Seo, "Air-Gap Stacked Spiral Inductor," *IEEE Microwave and Guided Wave Lett.,* Vol. 7, October 1997, pp. 329–331.

[78] Chuang, J., et al., "Low Loss Air-Gap Spiral Inductors for MMICs Using Glass Microbump Bonding Technique," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1998, pp. 131–134.

[79] Bahl, I. J., "Improved Quality Factor Spiral Inductors on GaAs Substrates," *IEEE Microwave and Guided Wave Lett.,* Vol. 9, October 1999, pp. 398–400.

[80] Bahl, I. J., "High Current Capacity Multilayer Inductors for RF and Microwave Circuits," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 10, March 2000, pp. 139–146.

[81] Bahl, I. J., "High Performance Inductors," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, April 2001, pp. 654–664.

[82] Piernas, B., et al., "High *Q*-Factor Three-Dimensional Inductors," *IEEE Trans. Microwave Theory Tech.,* Vol. 50, August 2002, pp. 1942–1949.

[83] Bahl, I. J., et al., "Low Loss Multilayer Microstrip Line for Monolithic Microwave Integrated Circuits Applications," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 8, November 1998, pp. 441–454.

[84] Bahl, I. J., "High-Q-and Low-Loss Matching Network Elements for RF and Microwave Circuits," *IEEE Microwave Magazine,* Vol. 1, September 2000, pp. 64–73.

[85] Lee, S. H., et al., "High Performance Spiral Inductors Embedded on Organic Substrates for SOP Applications," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 2229–2232.

[86] Wu, H., and C. Tzuang, "PBG-Enhanced Inductor," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 1087–1090.

[87] Acuna, J. E., J. L. Rodriguez, and F. Obelleiro, "Design of Meander Line Inductors on Printed Circuit Boards," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 11, July 2001, pp. 219–230.

[88] Daly, D. A., "Lumped Elements in Microwave Integrated Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-15, December 1967, pp. 713–721.

[89] Caulton, M., et al., "Status of Lumped Elements in Microwave Integrated Circuits—Present and Future," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-19, July 1971, pp. 588–599.

[90] Pieters, P., et al., "Accurate Modeling of High-Q-Spiral Inductors in Thin-Film Multilayer Technology for Wireless Telecommunication Applications," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, April 2001, pp. 589–599.

[91] Park, J. Y., and M. G. Allen, " Packaging-Compatible High *Q*-Microinductors and Microfilters for Wireless Applications," *IEEE Trans. Advanced Packaging,* Vol. 22, May 1999, pp. 207–213.

[92] Dayal, H., and Q. Le, "Printed Inductors on Alumina Substrates," *IEEE Microwave Magazine,* Vol. 2, June 2001, pp. 78–86.

[93] Sutono, A., et al., "Development of Three Dimensional Ceramic-Based MCM Inductors for Hybrid RF/Microwave Applications," *IEEE RF Integrated Circuit Symp. Dig.,* 1999, pp. 175–178.

[94] Sutono, A., et al., "RF/Microwave Characterization of Multilayer Ceramic-Based MCM Technology," *IEEE Trans. Advanced Packaging,* Vol. 22, August 1999, pp. 326–336.

[95] Lahti, M., V. Lantto, and S. Leppavuori, "Planar Inductors on an LTCC Substrate Realized by the Gravure-Offset-Printing Technique," *IEEE Trans. Components Packaging Tech.,* Vol. 23, December 2000, pp. 606–615.

[96] Sutono, A., et al., "High *Q*-LTCC-Based Passive Library for Wireless System-on-Package (SOP) Module Development," *IEEE Trans. Microwave Theory Tech.,* October 2001, pp. 1715–1724.

[97] Lim, K., et al., "RF-System-On-Package (SOP) for Wireless Communications," *IEEE Microwave Magazine,* Vol. 3, March 2002, pp. 88–99.

[98] Yamaguchi, M., M. Baba, and K. Arai, "Sandwich-Type Ferromagnetic RF Integrated Inductor," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, December 2001, pp. 2331–2335.

[99] Yamaguchi, M., T. Kuribara, and K. Arai, "Two-Port Type Ferromagnetic RF Integrated Inductor," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2002, pp. 197–200.

4

Wire Inductors

Wire-wound inductors have traditionally been used in biasing chokes and lumped-element filters at radio frequencies, whereas bond wire inductance is an integral part of matching networks and component interconnection at microwave frequencies [1–10]. This chapter provides design information and covers practical aspects of these inductors.

4.1 Wire-Wound Inductors

Wire-wound inductors can be realized in several forms of coil including rectangular, circular, solenoid, and toroid. The inductance of a coil can be increased by wrapping it around a magnetic material core such as a ferrite rod. Figure 4.1 shows various types of wire-wound inductors currently used in RF and microwave circuits. The basic theory of such inductors is described next.

4.1.1 Analytical Expressions

In this section we describe analytical expressions used for the design of several types of wire-wound inductors.

4.1.1.1 Circular Coil

The inductance of a single-turn coil shown in Figure 4.2(a) is given by [7]

$$L = \mu(2r - a)\left[\left(1 - \frac{k^2}{2}\right)K(k) - E(k)\right] \tag{4.1}$$

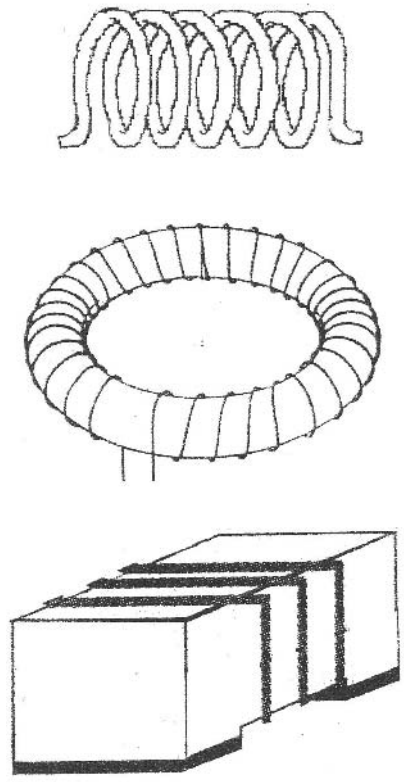


Figure 4.1 Wire-wound inductor configurations.

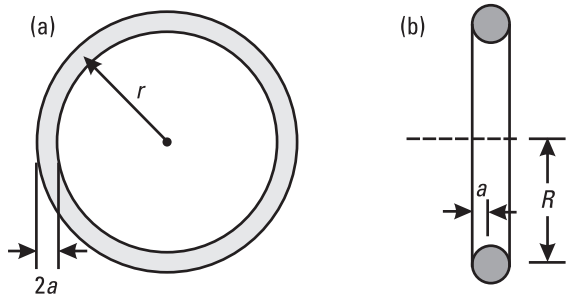


Figure 4.2 (a) Single turn circular and (b) multiturn coil having large radius-to-length ratio.

$$k^2 = \frac{4r(r-a)}{(2r-a)^2} \tag{4.2}$$

where r is the mean radius of the coil and $2a$ is the diameter of the wire, μ is the permeability of the medium, and $E(k)$ and $K(k)$ are complete elliptic integrals of the first and second kinds, respectively and are given by

$$E(k) = \int_0^{\pi/2} \sqrt{1 - k^2 \sin^2 \phi}\, d\phi \tag{4.3a}$$

$$K(k) = \int_0^{\pi/2} \frac{d\phi}{\sqrt{1 - k^2 \sin^2 \phi}} \tag{4.3b}$$

When $r >> a$, $k \cong 1$ and the expressions for $K(k)$, $E(k)$, and L become

$$K(k) \cong \ln\left(\frac{4}{\sqrt{1-k^2}}\right) \tag{4.4a}$$

$$E(k) \cong 1 \tag{4.4b}$$

$$L \cong r\mu\left[\ln\left(\frac{8r}{a}\right) - 2\right] \qquad H \tag{4.5}$$

Next let us consider a circular coil of closely wound n turns, with cross-sectional radius a and mean loop radius R as shown in Figure 4.2(b). An approximate expression for this case is obtained by multiplying (4.5) by a factor of n^2 and replacing r with R, that is,

$$L = n^2 R\mu\left[\ln\left(\frac{8R}{a}\right) - 2\right] \qquad H \tag{4.6}$$

Here the n^2 factor occurs due to n times current and n integrations to calculate the voltage induced about the coil. When the medium is air, $\mu = \mu_0 = 4\pi \times 10^{-9}$ H/cm, and

$$L = 4\pi n^2 R\left[\ln\left(\frac{8R}{a}\right) - 2\right] \qquad \text{(nH)} \tag{4.7}$$

where a and R are in centimeters.

4.1.1.2 Solenoid Coil

Consider a solenoid coil as shown in Figure 4.3 having number of turns n, mean radius of R, and length ℓ. As a first-order approximation we may consider ℓ much larger than the radius R and uniform field inside the coil. In this case the flux density can be written

$$B_z = \mu H_z = \frac{\mu nI}{\ell} \tag{4.8}$$

The total flux linkages for n turns is given by

$$\begin{aligned} \phi &= n \times \text{cross-section area} \times \text{flux density} \\ &= n\pi R^2 \, \mu n \, (I/\ell) \end{aligned} \tag{4.9}$$

The inductance of the solenoid becomes

$$L = \frac{\phi}{I} = \mu\pi R^2 n^2/\ell \tag{4.10}$$

or

$$L = 4\mu_r(\pi Rn)^2/\ell \qquad \text{(nH)}$$

where dimensions are in centimeters and μ_r is the relative permeability of the solenoid coil. For coils with the length comparable to the radius, several

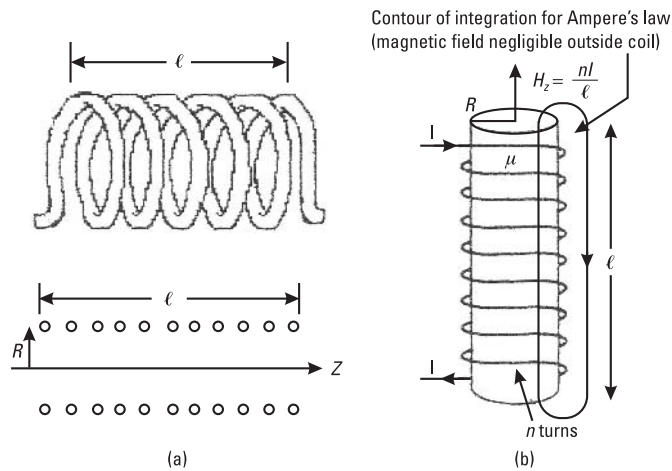


Figure 4.3 Solenoid coil configurations: (a) air core and (b) ferrite core.

semiempirical expressions are available. For $\ell > 0.8R$, an approximate expression, commonly used is

$$L = \frac{4\mu_r(\pi Rn)^2}{\ell + 0.9R} \qquad \text{(nH)} \tag{4.11}$$

More accurate expressions for an air core material are given in the literature [8, 10] and reproduced here. For $2R \leq \ell$ (long coil):

$$L = \frac{\mu_0 n^2 \pi R^2}{\ell}\left[f_1\left(\frac{4R^2}{\ell^2}\right) - \frac{8R}{3\pi\ell}\right] \tag{4.12a}$$

and for $2R > \ell$ (short coil):

$$L = \mu_0 n^2 R\left\{\left[\ln\left(\frac{8R}{\ell}\right) - 0.5\right] f_1\left(\frac{\ell^2}{4R^2}\right) + f_2\left(\frac{\ell^2}{4R^2}\right)\right\} \tag{4.12b}$$

where for $0 \leq x \leq 1.0$

$$f_1(x) = \frac{1.0 + 0.383901x + 0.017108x^2}{1.0 + 0.258952x} \tag{4.13a}$$

$$f_2(x) = 0.093842x + 0.002029x^2 - 0.000801x^3 \tag{4.13b}$$

4.1.1.3 Rectangular Solenoid Coil

Ceramic wire-wound inductors as shown in Figure 4.4 are used at high RF frequencies. These ceramic blocks are of rectangular shape and have connection

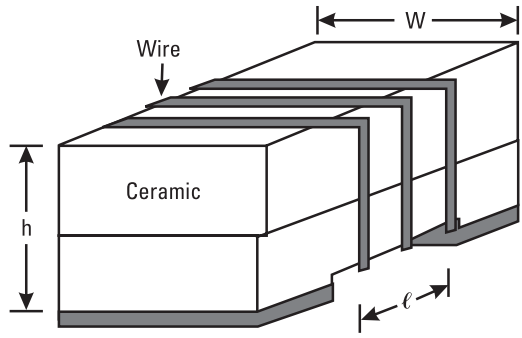


Figure 4.4 Ceramic block wire-wound inductor configuration.

pads. The inductance of these coils can be approximately calculated using (4.11) or (4.12), when

$$R = \frac{W + h + a}{\pi} \tag{4.14}$$

where W and h are the width and height of the ceramic block, respectively, and a is the radius of the wire.

As shown in (4.11) as a first-order approximation (W, $h >> a$), the inductance of a solenoid does not depend on the diameter of the wire used. Thus, the selection of wire diameter is dictated by the size of the coil, the highest frequency of operation, and the current-handling capability. For matching networks and passive components, the smallest size inductors with the highest possible SRF and Q-values are used.

4.1.1.4 Toroid Coil

If a coil is wound on a donut-shaped or toroidal core, shown in Figure 4.5(a), the approximate inductance is given as

$$L = \mu_o \mu_r \pi a^2 n^2 / \ell \tag{4.15}$$

where $\ell = 2\pi R$. Here a is the radius of the circular cross-section toroid, R is the radius of the toroid core, and $R >> a$. When R and a are comparable, an approximate expression for inductance is given by [8] as

$$L = 12.57 n^2 \left(R - \sqrt{R^2 - a^2}\right) \qquad \text{(nH)} \tag{4.16}$$

where R and a are in centimeters.

An approximate expression for the rectangular cross-section toroid, shown in Figure 4.5(b), can be derived as follows [6]. The magnetic field due to the net current flowing through the core is given by

$$H_\phi = \frac{nI}{2\pi} \qquad R_1 < r < R_2 \tag{4.17}$$

The flux through any single loop is

$$\phi = \mu_o \mu_r D \int_{R_1}^{R_2} H_\phi \, dr = \frac{\mu_o \mu_r D n I}{2\pi} \ln\left(\frac{R_2}{R_1}\right) \tag{4.18}$$

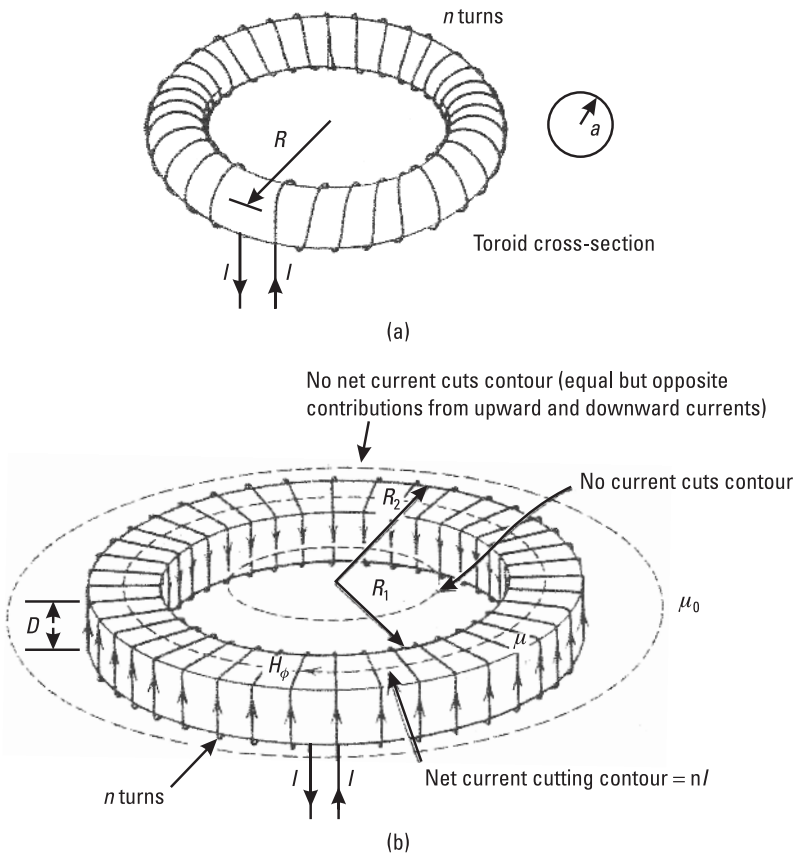


Figure 4.5 Toroid core inductors: (a) circular radius and (b) rectangular radius.

where D is the height of the core and R_1 and R_2 are the inner and outer radii of the core. The inductance due to n turns is given by

$$L = \frac{n\phi}{I} = 2\mu_r D n^2 \ln\left(\frac{R_2}{R_1}\right) \qquad \text{(nH)} \tag{4.19}$$

where D, R_1, and R_2 are in centimeters.

When the coil is tightly wound so that there is no gap between the enameled wire turns, it provides the maximum inductance and the minimum resonant frequency. Its inductance decreases as the coil is stretched along its axis. In this case, the interwinding capacitance decreases and increases the resonant frequency. The inductance of the coil can also be decreased or increased by inserting, respectively, a conductive (copper) or a magnetic (ferrite) material

rod inside the core of the winding. Thus, coil stretching or rod insertion in the core allows the inductance of the coil to vary making it a tunable component.

4.1.2 Compact High-Frequency Inductors

Chip inductors are widely used in RF circuits to realize passive components and matching networks and as RF chokes for bringing the bias to solid-state devices. Requirements for applications in passive and matching circuits are a high Q, high SRF, and low parasitic capacitance, whereas RF chokes need higher current-handling capability and lower dc resistance values. Also, low-cost RF front-ends need low profiles or compact size and inexpensive components. These inductors are commonly realized by winding an insulating wire around a ceramic block. Both regular Al_2O_3 ceramic and high-permeability ferrite materials are used.

Miniature chip coil inductors having inductance values from 1 to 4,700 nH with SRF ranging from 90 MHz to 6 GHz are commercially available [2]. The Q-values at 250 MHz for 3.6- and 39-nH inductors are 22 and 40, respectively. Table 4.1 provides the summary of ceramic wire-wound RF inductor parameters. In the table L Freq, Q Freq, and SRF Min represent the measurement frequency of inductance, the measurement frequency of Q-factor, and the minimum value of self-resonant frequency, respectively.

4.1.2.1 High-SRF Inductors

Chip inductors with high SRF are required for applications such as matching networks and passive components. Chip inductors with inductance values

Table 4.1
Summary of Ceramic Wire-Wound RF Inductor Parameters

L (nH)	*L* Freq (MHz)	*Q* Min	*Q* Freq (MHz)	SRF Min (MHz)	dc Resistance (Ohm)	Current Rating dc Max (mA)
1.0	250	16	250	6,000	0.045	1,360
2.2	250	19	250	6,000	0.070	960
3.9	250	22	250	5,900	0.080	1,000
6.8	250	27	250	5,700	0.110	1,000
12.0	250	35	250	4,000	0.130	986
22.0	250	55	500	2,600	0.220	758
39.0	250	60	500	2,000	0.290	660
100.0	150	65	500	1,200	0.460	524
470.0	25	45	100	450	1.19	449
1,000.0	25	35	50	290	1.75	370
4,700.0	7.9	20	25	90	4.90	221

up to 15 nH and a SRF greater than 4 GHz are commercially available. The L · SRF product for smaller value inductors is as large as 24 nH-GHz, whereas for large value inductors (<100 nH) this product is as large as 120 nH-GHz. For example, a 100-nH inductor's SRF is about 1.2 GHz.

4.1.2.2 High-*Q* Inductors

High-*Q* chip inductors are required for low-loss matching network, filter, and resonator applications. For chip inductors, a maximum *Q*-value of 100 can be obtained. Figure 4.6 shows the variation of *Q* for several inductor values.

4.1.2.3 High Current Capability Inductors

Bias chokes used in power amplifiers require high current capabilities. The current rating given in Table 4.1 for high inductance values ($L \cong 40$ nH, adequate at 1-GHz applications) is about 660 mA. However, other chip inductors with a current rating of 1.3A are also available [1].

The material properties of gold, aluminum, and copper wires are compared in Table 4.2. Because copper has a higher melting temperature, lower resistivity value, and the best thermal conductivity, the material is exclusively used for low-loss and high current carrying capacity wires. Table 4.3 lists copper wire parameters for various AWG gauge values.

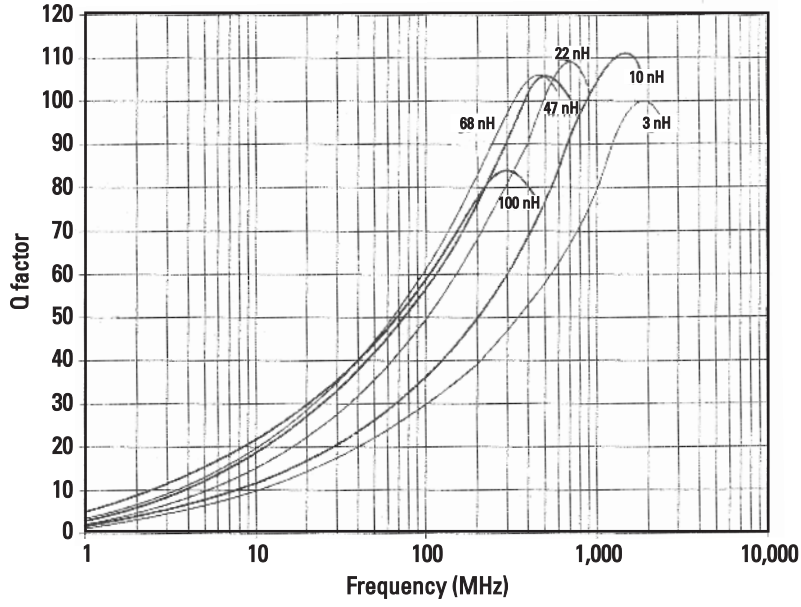


Figure 4.6 Typical variation of *Q* as a function of frequency for several chip inductors [1].

Table 4.2
Material Properties of Wires

Material Property	Units	Gold	Aluminum	Copper
Melting temperature, T_m	°C	1063	660	1093
Heat of fusion	W-s/g	64	400	202
Thermal conductivity, k	W/m-°C	297	240	393
Density	G/cm^3	19.3	2.7	8.96
Specific heat	W-s/g-°C	0.31	0.886	0.92
Electrical resistivity	Ω.cm	2.4×10^{-6}	2.6×10^{-6}	1.7×10^{-6}
Thermal expansion coefficient	ppm/°C	14.2	23	17

Table 4.3
Copper Wire Parameters at 20°C

AWG Gauge	Bare Diameter (mm, mil)	Enamel Coated Diameter (mm, mil)	Resistance (Ω/m)	Maximum Current (A)
32	0.203, 8.0	0.224, 8.8	0.5385	0.53
30	0.254, 10.0	0.274, 10.8	0.3385	0.86
28	0.320, 12.6	0.343, 13.5	0.2129	1.40
26	0.404, 15.9	0.429, 16.9	0.1339	2.20
24	0.511, 20.1	0.541, 21.3	0.0878	3.50
22	0.643, 25.3	0.676, 26.6	0.0610	7.0
20	0.813, 32.0	0.848, 33.4	0.0343	11.0
18	1.024, 40.3	1.062, 41.8	0.0220	16.0
16	1.290, 50.8	1.331, 52.4	0.0152	22.0
14	1.628, 64.1	1.674, 65.9	0.0086	32.0
12	2.052, 80.8	2.101, 82.7	0.0055	41.0
10	2.588, 101.9	2.639, 103.9	0.0035	55.0

The current-handling values given in Table 4.3 are for straight wires in air. The current handling capacity of inductors depends on several factors including the type of winding (tight or loose), the number of turns, and the core material used. Closely spaced windings tend to modify the current distribution in the wire cross section, making it more uneven and thus reducing the current handling ability.

4.2 Bond Wire Inductor

Most RF and microwave circuits and subsystems use bond wires to interconnect components such as lumped elements, planar transmission lines, solid-state

devices, and ICs. These bond wires have 0.5- to 1.0-mil diameters and their lengths are electrically short compared to the operating wavelength. Bond wires are accurately characterized using simple formulas in terms of their inductances and series resistances. As a first-order approximation, the parasitic capacitance associated with bond wires can be neglected.

Commonly used bond wires are made of gold and aluminum. Table 4.2 compares the important properties of these two materials with copper used for wire-wound inductors.

4.2.1 Single and Multiple Wires

In hybrid MICs, bond wire connections are used to connect active and passive circuit components, and in MMICs bond wire connections are used to connect the MMIC chip to other circuitry. The free-space inductance L (in nanohenries) of a wire of diameter d and length ℓ (in microns) is given by [11–13]

$$L = 2 \times 10^{-4}\ell \left[\ln\left\{ \frac{2\ell}{d} + \sqrt{1 + \left(\frac{2\ell}{d}\right)^2} \right\} + \frac{d}{2\ell} - \sqrt{1 + \left(\frac{d}{2\ell}\right)^2} + C \right] \tag{4.20}$$

where the frequency-dependent correction factor C is a function of bond wire diameter and its material's skin depth δ expressed as

$$C = 0.25 \tanh(4\delta/d) \tag{4.21a}$$

$$\delta = \frac{1}{\sqrt{\pi\sigma f \mu_0}} \tag{4.21b}$$

where σ is the conductivity of the wire material. For gold wires, $\delta = 2.486 f^{-0.5}$, where frequency f is expressed in gigahertz. When δ/d is small, $C = \delta/d$. When $\ell >> d$, (4.20) reduces to

$$L = 2 \times 10^{-4}\ell \left(\ln\frac{4\ell}{d} + 0.5\frac{d}{\ell} - 1 + C \right) \tag{4.22}$$

The wire resistance R (in ohms) is given by

$$R = \frac{R_s \ell}{\pi d} \tag{4.23a}$$

where R_s is the sheet resistance in ohms per square. Taking into account the effect of skin depth, (4.23a) can be written

$$R = \frac{4\ell}{\pi\sigma d^2}\left[0.25\frac{d}{\delta} + 0.2654\right] \tag{4.23b}$$

4.2.1.1 Ground Plane Effect

The effect of the ground plane on the inductance value of a wire has also been considered [11, 14]. If the wire is at a distance h above the ground plane [Figure 4.7(a)], it sees its image at $2h$ from it. The wire and its image result in a mutual inductance L_{mg}. Because the image wire carries a current opposite to the current flow in the bond wire, the effective inductance of the bond wire becomes

$$L_e = L - L_{mg} \tag{4.24a}$$

where

$$L_{mg} = 2\times 10^{-4}\ell\left[\ln\left\{\frac{\ell}{2h} + \sqrt{1+\left(\frac{\ell}{2h}\right)^2}\right\} + \sqrt{1+\left(\frac{\ell}{2h}\right)^2} + \frac{2h}{\ell} - \sqrt{1+\left(\frac{2h}{\ell}\right)^2} + C\right] \tag{4.24b}$$

From (4.20) and (4.24)

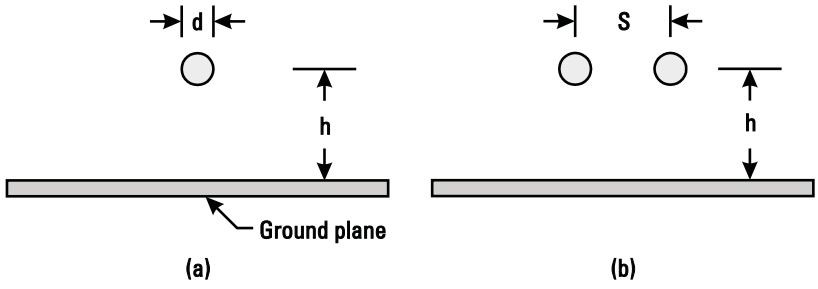


Figure 4.7 Wires above a ground plane: (a) single and (b) twin.

$$L_e = 2 \times 10^{-4} \ell \left[\ln \frac{4h}{d} + \ln \left(\frac{l + \sqrt{l^2 + d^2/4}}{l + \sqrt{l^2 + 4h^2}} \right) + \sqrt{1 + \frac{4h^2}{l^2}} - \sqrt{1 + \frac{d^2}{4l^2}} - 2\frac{h}{l} + \frac{d}{2l} \right] \tag{4.25}$$

Here L_e is in nanohenries, and ℓ, h, and d are in microns.

4.2.1.2 Multiple Wires

In many applications, multiple wires are required to carry higher currents, to reduce wire inductance, or improve wire reliability. For example, in the case of two wires placed parallel to each other at a distance S between their centers [Figure 4.7(b)], above the ground plane, the total inductance of the pair becomes

$$L_{ep} = (L_e + L_m)/2 \tag{4.26}$$

Here both wires carry current in the same direction; therefore, the mutual inductances L_m and self-inductances are in parallel, and for each wire the self-inductances and mutual inductances add up. In this case, L_m is given by

$$L_m = 2 \times 10^{-4} \ell \left[\ln \left\{ \frac{\ell}{S} + \sqrt{1 + \left(\frac{\ell}{S}\right)^2} \right\} + \sqrt{1 + \left(\frac{\ell}{S}\right)^2} - \sqrt{1 + \left(\frac{S}{\ell}\right)^2} + \frac{S}{\ell} \right] \tag{4.27}$$

Equations (4.24b) and (4.27) are identical under $2h = S$ and $C = 0$. The same procedure can be carried out to calculate the mutual inductance for multiple wires.

Table 4.4 lists inductances for 1-mil-diameter gold wires [15–17]. So far we have treated uniformly placed horizontal wires above the ground plane. However, in practice, the wires are curved, nonhorizontal, and are not parallel to each other. In such situations, an average value of S and h can be used. Also wire/wires have shunt capacitance that can also be calculated [18].

The inductance of a bond wire connection is generally reduced by connecting multiple wires in parallel. However, as shown in Table 4.4, the inductance of multiple wires in parallel depends on the separation between them. For a very large distance between two wires, the net inductance of two wires is half that of a single wire. When the distance between two wires is four to six times the diameter of the wires, the net inductance is only $1/\sqrt{2}$ times of a single wire, and for n wires it is approximately $1/\sqrt{n}$ times of a single wire.

Table 4.4
Wire Inductance of 1-Mil-Diameter Gold Wires

Length (mil)	Number of Wires	Loop Height (mil)	Spacing Between Wires (mil)	Inductance Value (nH)	Method
19	1	7	—	0.28	EM simulated [15]
34	1	—	—	0.49	Calculated [16]
45	1	—	—	0.67	Calculated [16]
34	2	—	2	0.39	Calculated [16]
34	2	—	6	0.31	Calculated [16]
34	2	—	15	0.27	Calculated [16]
45	2	—	2	0.54	Calculated [16]
45	2	—	6	0.44	Calculated [16]
45	2	—	15	0.37	Calculated [16]
45	3	—	2	0.46	Calculated [16]
45	3	—	6	0.34	Calculated [16]
45	3	—	15	0.26	Calculated [16]
57	2	20	—	0.93	Measured [17]
57	3	20	—	0.73	Measured [17]
57	9	20	—	0.43	Measured [17]
57	13	20	—	0.38	Measured [17]
93	2	20	—	1.22	Measured [17]
93	8	20	—	0.60	Measured [17]
93	12	20	—	0.40	Measured [17]
93	14	20	—	0.42	Measured [17]

4.2.2 Wire Near a Corner

The inductance and capacitance per unit length of a wire near a corner of package or shield, as shown in Figure 4.8, is given by

$$L = 0.0333Z_0 \qquad \text{(nH/cm)} \tag{4.28a}$$

and

$$C = 33.33Z_0 \qquad \text{(pF/cm)} \tag{4.28b}$$

where Z_0 is the characteristic impedance of the wire, and an expression for Z_0 (having an accuracy of about 1%) is given by Wheeler [19] as follows:

$$Z_0 = 30 \ln\left\{\left(\frac{D}{d}\right)^2 + \sqrt{\left[\left(\frac{D}{d}\right)^2 - 1\right]^2 + \left(\frac{D}{d}\right)^2 - 1}\right\} \quad (\Omega) \tag{4.29}$$

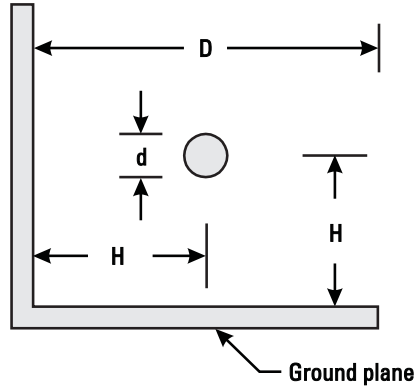


Figure 4.8 Wire near a corner of a shield.

where d is the diameter of the wire and $D = 2H$, where H is the distance from the center of the wire to the shield plane.

4.2.3 Wire on a Substrate Backed by a Ground Plane

In many practical cases, the bond wire might be placed on a PCB or alumina substrate or GaAs chip. In this case (Figure 4.9), the inductance and capacitance per unit length of a wire can again be obtained by using (4.28), where

$$Z_0 = \frac{60}{\sqrt{\epsilon_{re}}} \cosh^{-1}\left(\frac{2h}{d}\right) = \frac{60}{\sqrt{\epsilon_{re}}} \ln\left\{\left(1 + \frac{2h}{d}\right) + 2\sqrt{\frac{h}{d}\left(1 + \frac{h}{d}\right)}\right\} \tag{4.30}$$

When wire diameter $d << h$,

$$Z_0 = \frac{60}{\sqrt{\epsilon_{re}}} \ln\left[\frac{4h}{d}\right] \tag{4.31}$$

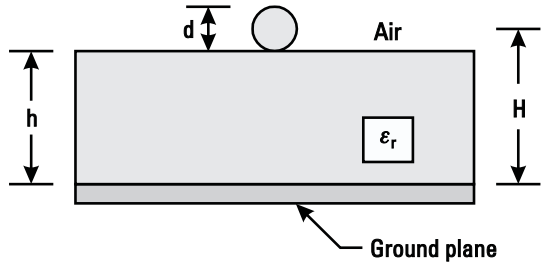


Figure 4.9 Wire on a dielectric substrate backed by a ground plane.

and as a first-order approximation

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} \tag{4.32}$$

Accurate expressions for L and C are also given in [20] and are reproduced here:

$$L = 2\sqrt{Q(Q+S)} \qquad \text{(nH/cm)} \tag{4.33a}$$

$$C = 0.556\left[\ln\left\{1 + \frac{1}{2x}\left(1 + \sqrt{1+4x}\right)\right\} + \sum_{n=0}^{\infty}(-P)^{n+1}\ln\left\{\frac{(n+2+x)}{(n+x)}\right\}\right]^{-1} \quad \text{(pF/cm)} \tag{4.33b}$$

where

$$Q = \ln\left[1 + \frac{1}{2x}\left(1 + \sqrt{1+4x}\right)\right] \tag{4.34a}$$

$$x = d/4h \tag{4.34b}$$

$$S = \sum_{n=0}^{\infty}(-P)^{+1}\ln\left(1 + \frac{2}{n+x}\right) \tag{4.34c}$$

$$P = \frac{\epsilon_r - 1}{\epsilon_r + 1} \tag{4.34d}$$

Figure 4.10 shows the variation of Z_0 as a function of h/H for various substrates. These data can also be used to calculate wire inductance (nH/cm) and capacitance (pF/cm) by using the following relations:

$$L = 0.0333\sqrt{\epsilon_{re}}\,Z_0 \tag{4.35a}$$

$$C = 33.33\sqrt{\epsilon_{re}}/Z_0 \tag{4.35b}$$

where

$$\sqrt{\epsilon_{re}} = \frac{Z_0\ (\epsilon_r = 1)}{Z_0(\epsilon_r)} \tag{4.36}$$

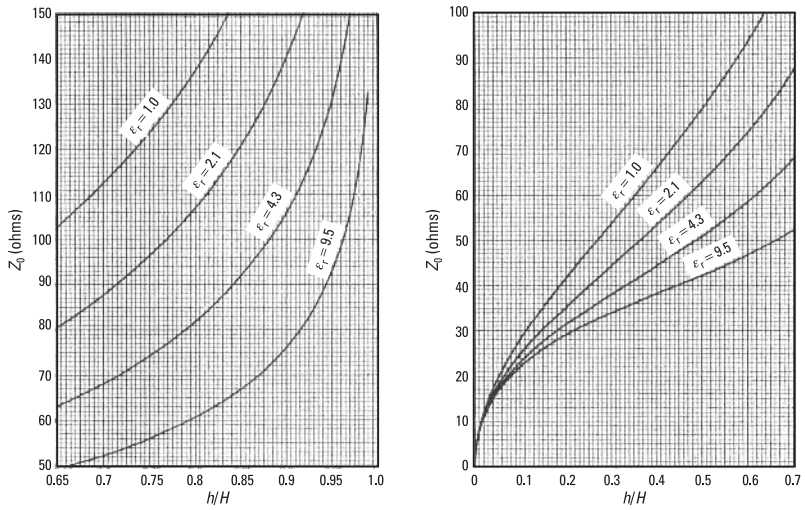


Figure 4.10 Characteristic impedance of a round wire microstrip as a function of its position.

4.2.4 Wire Above a Substrate Backed by a Ground Plane

The wire above a grounded substrate occurs frequently in microwave integrated circuits. Figure 4.11 shows this configuration and (4.35) can be used to calculate the values of L and C. Here Z_0 and ϵ_{re} are given as follows [18]:

$$Z_0 = \frac{60}{\sqrt{\epsilon_{re}}} \cosh^{-1}\left(\frac{1-u^2}{2R} + \frac{R}{2}\right) \tag{4.37}$$

where

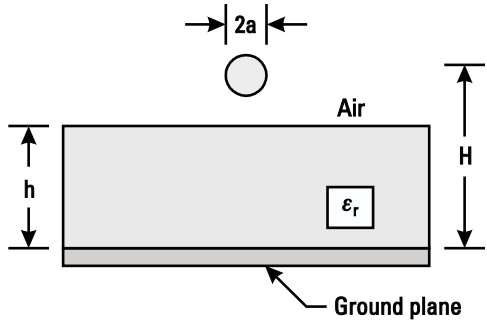


Figure 4.11 Wire above a dielectric substrate backed by a ground plane.

$$R = \frac{2}{(4H/a - a/H)} \tag{4.38a}$$

$$u = \frac{1}{(2H/a)^2 - 1} \tag{4.38b}$$

$$\epsilon_{re} = \frac{\ln\left(\dfrac{2H}{a}\right)}{\ln\left[\dfrac{2(H-h)}{a} + \dfrac{2h}{a\epsilon_r}\right]} \tag{4.38c}$$

4.2.5 Curved Wire Connecting Substrates

Many times a wire connecting two substrates or components is not straight. Expressions for L and C for a bond wire arc (Figure 4.12) are given by Mondal [21] as follows:

$$L = 10 \int_0^{d/2} \ln\left[p(x)\right]\, dx \qquad \text{(nH)} \tag{4.39}$$

where d, h, and a are all in inches, a is the radius of wire, and

$$p(x) = \frac{2}{a}\left[\sqrt{\left(\frac{d \operatorname{cosec} \beta}{2}\right)^2 - x^2} + \left(h - \frac{d}{2}\cot \beta\right)\right] \tag{4.40}$$

The capacitance is calculated from

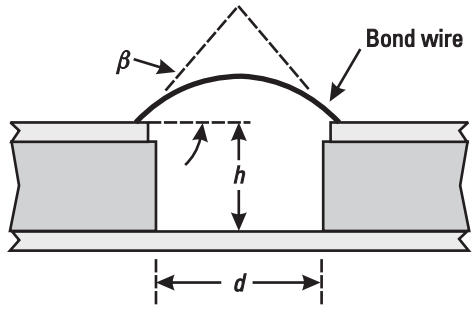


Figure 4.12 Configuration of a bond wire connecting two microstrip substrates.

$$C = \frac{1.4337}{\ln [p(x)]} \qquad \text{(pF/in)} \tag{4.41}$$

4.2.6 Twisted Wire

Twisted-wire transmission lines are used in transformers, couplers, and power dividers. The inductance of each wire for a twisted-wire pair shown in Figure 4.13 and the interwire capacitance are given next:

$$L = \frac{\mu_0}{\pi}\left[\sqrt{1 + (\pi TS)^2}\,\cosh^{-1}\left(\frac{S}{d}\right) + \frac{(\pi TS)^2}{4}\right] \qquad \text{(H/m)} \tag{4.42a}$$

$$C = \int_0^{\pi} \frac{\epsilon_0 \epsilon_r d[1 + (\pi TS)^2]^{1/2}}{\epsilon_r S\theta \tan\left(\dfrac{\theta}{2}\right) + 2t}\, d\theta \qquad \text{(F/m)} \tag{4.42b}$$

where d is the diameter of the bare wire, S is the separation between the wire centers, t is the thickness, ϵ_r is the relative permittivity of the insulation, and T is the number of twists per unit length.

4.2.7 Maximum Current Handling of Wires

When a large current is passed through a wire, there is a maximum current value that the wire can withstand due to its finite resistance. At this maximum value, known as the *fusing current,* the wire will melt or burn out due to metallurgical fatigue. The factors affecting the fusing mechanism in a wire are its melting point, resistivity, thermal conductivity, and temperature coefficient of resistance. The fusing current is given by

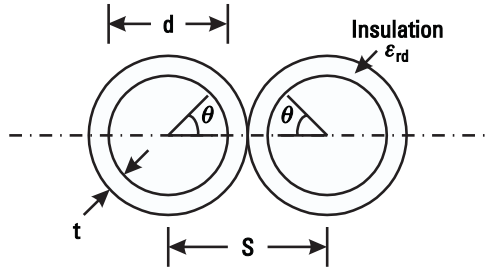


Figure 4.13 Cross-sectional view of a twisted-wire pair.

$$I_f = Kd^{1.5} \tag{4.43}$$

where K depends on the wire material and the surrounding environment and d is the diameter of the wire. Thicker wires have larger current-carrying capability than thinner wires. When the wire diameter d is expressed in millimeters, the K values for gold, copper, and aluminum wires are 183, 80, and 59.2, respectively. For 1-mil-diameter wires, I_f values for gold, copper, and aluminum wires are 0.74A, 0.32A, and 0.24A, respectively. A safer maximum value for the current in wires used in assemblies is about half of the fusing current value. For example, to apply 1A current one requires three 1-mil-diameter wires of gold. When a wire is placed on a thermally conductive material such as Si or GaAs, its fusing current value is higher than the value given above. Longer wires will take a longer time to fuse than shorter wires because of larger area for heat conduction.

4.3 Wire Models

Coils and bond wires can also be accurately characterized by numerical methods or by using measurement techniques as discussed in Chapter 2. Both methods provide the desired accuracy including all parasitic effects.

4.3.1 Numerical Methods for Bond Wires

Several numerical methods, including the method of moments [16] and finite-difference time-domain technique [22, 23], have been used to accurately model bond wires. These simulations also include the curvature of wire, substrate height, spacing between substrates, the effect of ground plane, and frequency of operation. Figure 4.14 shows the variation of inductance [16] as a function of frequency for various bond wire heights above a GaAs substrate. The height H varied from 70 to 210 μm and the corresponding total wire length varied from 480 to 720 μm. The steep change in inductance value occurs at frequencies near SRF.

4.3.2 Measurement-Based Model for Air Core Inductors

Air core inductors have low series resistance and high Q, and their accurate characterization is difficult when using S-parameters in a 50-Ω system. An indirect method as described in earlier was used to characterize several high-Q air core inductors [24]. To accurately measure the low values of *effective series resistance* (ESR), the indirect method using the TRL de-embedding technique in a 3Ω system was employed. The inductance L, ESR, and Q were measured

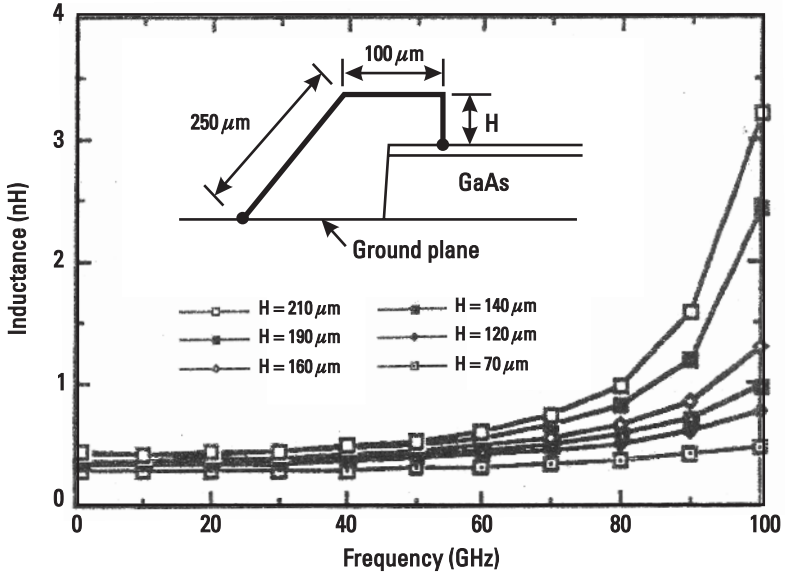


Figure 4.14 Bond wire inductance versus frequency for various wire heights. Gold wire diameter is 25 μm.

by measuring the series LC resonance using a known value of capacitor C, which was much higher than the parasitic capacitance of the inductor.

The copper wire wound air core and chip capacitor were mounted on a copper-clad Arlon substrate with $\epsilon_r = 10.2$, $h = 0.635$ mm, $t = 0.043$ mm, and $\tan \delta = 0.001$. The TRL standards were also printed on the same board. The equivalent circuit representation of the LC resonator is shown in Figure 4.15, where the chip capacitor and ground via models are de-embedded separately.

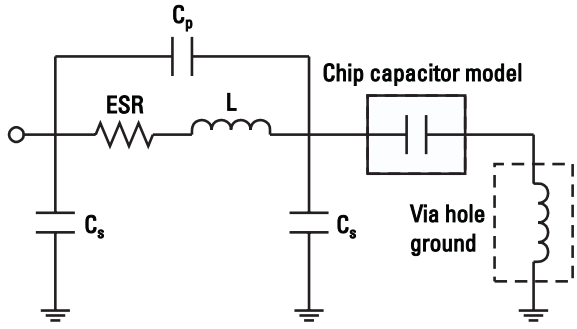


Figure 4.15 EC model representation of an air core inductor and its LC resonator circuit.

The chip capacitor values were selected to keep the resonant frequency close to approximately 800 MHz.

Table 4.5 gives the inductor parameters and measured inductance, ESR, resonant frequency, and Q-values. The resonant frequency f_0 is lower than the SRF f_{res} of the coil. The relationships between various parameters are given below:

$$Q = \frac{\omega_0 L}{R} \tag{4.44}$$

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}} \tag{4.45}$$

$$\text{ESR} = a + b\sqrt{f} \tag{4.46}$$

where C is the de-embedded capacitance value of the chip capacitor, f is the operating frequency in gigahertz, and R = ESR at $f = f_0$.

4.3.3 Measurement-Based Model for Bond Wires

When a wire bond inductor is modeled from the measured S-parameter data, it might result in a lower value than the actual value if one is not careful. This can be explained by using Figure 4.16. A simple model of a short wire bond is shown in Figure 4.16(a). The series inductance can be split into two parts as shown in Figure 4.16(b). A part of the series inductance L_2 with shunt capacitance C_s is equivalent to a 50-Ω line, that is,

$$Z_0 = \sqrt{L_2 / C_s} = 50\Omega \tag{4.47}$$

This is shown in Figure 4.16(c). Thus, during de-embedding, a part of the inductance is absorbed in the de-embedding impedance, which lowers the series inductance value. To obtain an accurate model, one must carefully compare both the magnitude and phase of the modeled response with the measured S-parameter data. Also by measuring the SRF, one can de-embed the shunt capacitance C_s. The SRF is given by

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{LC_s}} \tag{4.48}$$

For example, two 30-mil-long wires have $L \cong 0.4$ nH, $C_s = 0.06$ pF, and SRF = 32.49 GHz.

Table 4.5
Parameters of Several Air Coil Inductors and Their Measured Performance

Inductor Number	Wire Diameter (mm)	Total Wire Length (mm)	Number of Turns	Inductance (nH)	*a*	*b*	ESR (Ω)	Resonant Frequency f_0 (MHz)	*Q*
1	0.643	14.6	3	4.22	0.0008	0.1423	0.123	735	158
2	0.643	15.8	3	5.34	0.0008	0.1526	0.138	808	196
3	0.511	16.9	3	6.75	0.0014	0.2433	0.226	852	160
4	0.643	27.4	4	13.9	0.0015	0.3493	0.302	740	214
5	0.320	21.0	5	16.28	0.0045	0.5190	0.462	777	172
6	0.643	36.3	6	19.97	0.0019	0.5265	0.444	705	199
7	0.320	26.7	7	23.75	0.0057	0.7471	0.633	705	166

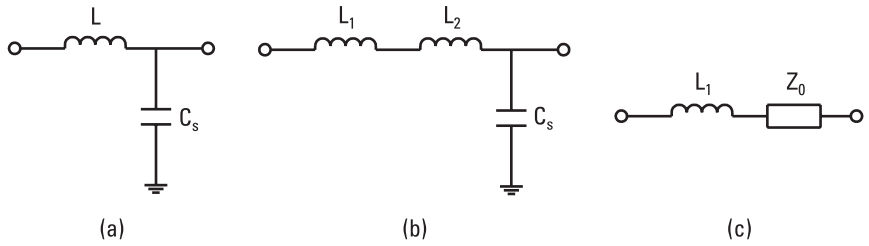


Figure 4.16 (a–c) Simplified bond wire models.

4.4 Magnetic Materials

The inductance of a coil or a transformer can be increased by replacing the air core with a high permeability (μ) magnetic material core. In this case, the magnetic flux density is proportional to the relative permeability value. The materials exhibiting high relative permeability values are known as *ferrimagnetic,* and *ferrite* is a generic term for such materials. Ferrite materials are extensively used in isolators, circulators, limiters, YIG tuned oscillators, switches, phase shifters, and so on. Most of these components are commercially available at frequencies up to 140 GHz.

Ferrites have specific resistivities larger than about 10^6 Ω-cm and are available with a dielectric constant of 10 or more. Relative permeabilities of several thousands are common. The basic chemical composition of ferrites is MFe_2O_4, where M is a divalent metallic ion such as manganese (Mn), nickel (Ni), zinc (Zn), iron (Fe), or a mixture of these. Ferrite materials are classified as ceramics because they are made by ceramic technology [25–27]. Powders of appropriate oxides are mixed and formed into required shapes (cylinders, slab, toroid, or binocular core) by die pressing or extruding. Different combinations of oxides can be selected to meet a wide range of electrical requirements. The composition is then fired at temperatures of 1,100°C to 1,200°C.

The ferrites used for RF inductor and transformer cores use MnZn and NiZn as divalent metal ion. Many grades of such ceramics are commercially available and their basic properties are listed in Table 4.6. The ferrite parameters are a strong function of frequency and temperature. The relative permeability decreases and the loss factor increases with frequency. The relative permeability increases with temperature and suddenly drops to 1 at the Curie temperature. The density of ferrite materials is about 5 g/cm^3 and thermal conductivity is in the range of 0.06 to 0.1 W/(cm-°C).

Table 4.6
Parameters of Ferrite Materials

Parameter	NiZn Ferrite	MnZn Ferrite
Relative permeability (μ_r)	20–850	800–10,000
Temperature coefficient of μ_r (percent/°C)	0.05–0.15	0.1–1.2
Dielectric constant	10–30	10–105
Relative loss factor (tan δ/μ_r) $\times 10^6$	30–400	5–35
Resistivity (Ω-cm)	10^5–10^9	50–1500
Curie temperature (°C)	130–150	120–200

References

[1] Inductor Product Catalog, Cary, IL: Coilcraft.

[2] Inductor Product Catalog, Gowanda, NY: Gowanda Electronics.

[3] *RF Transformer Designers' Guide,* Mini-Circuits, Brooklyn, NY.

[4] Medhurst, R. G., "HF Resistance and Self-Capacitance of Single-Layer Solenoids," *Wireless Engineer,* February 1947, pp. 35–43, and March 1947, pp. 80–92.

[5] Grover, F. W., *Inductance Calculations,* Princeton, NJ: Van Nostrand, 1946; reprinted by Dover Publications, New York, 1962.

[6] Zahn, M., *Electromagnetic Field Theory,* New York: John Wiley, 1979.

[7] Ramo, S., J. R. Whinnery, and T. Van Duzer, *Fields and Waves in Communication Electronics,* 2nd ed., New York: John Wiley, 1984.

[8] Richard, L., "A Handbook Formula for the Inductance of a Single-Layer Circular Coil," *Proc. IEEE,* Vol. 73, September 1985, pp. 1428–1429.

[9] Abrie, P. D., *Design of RF and Microwave Amplifiers and Oscillators,* Norwood, MA: Artech House, 1999, Chap. 7.

[10] Wadell, B. C., *Transmission Line Design Handbook,* Norwood, MA: Artech House, 1991, Chap. 6.

[11] Gupta, K. C., R. Garg, and R. Chadha, *Computer-Aided Design of Microwave Circuits,* Dedham, MA: Artech House, 1981.

[12] Wheeler, H. A., "Simple Inductance Formulas for Radio Coils," *Proc. IRE,* Vol. 16, October 1928, pp. 1398–1400.

[13] March, S. L., "Simple Equations Characterize Bond Wires," *Microwaves & RF,* Vol. 30, November 1991, pp. 105–110.

[14] Terman, F. E., *Radio Engineer Handbook,* New York: McGraw-Hill, 1943, p. 51.

[15] Lee, H.-Y., "Wide-Band Characterization of a Typical Bonding Wire for Microwave and Millimeter-Wave Integrated Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. 43, January 1995, pp. 63–68.

[16] Patterson, H., "Analysis of Ground Wire Arrays for RFICs," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1997, pp. 765–768.

[17] Liang, T., et al., "Equivalent-Circuit Modeling and Verification of Metal-Ceramic Packages for RF and Microwave Power Transistors," *IEEE Trans. Microwave Theory Tech.,* Vol. 47, June 1999, pp. 709–713.

[18] Caverly, R. H., "Characteristic Impedance of Integrated Circuit Bond Wire," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-34, September 1986, pp. 982–984.

[19] Wheeler, H. A., "Transmission-Line Properties of a Round Wire in a Polygon Shield," *IEEE Trans. Microwave Theory and Techniques,* Vol. MTT-27, August 1979, pp. 717–721.

[20] Gunston, M. A. R., *Microwave Transmission-Line Impedance Data,* New York: Van Nostrand Reinhold, 1971.

[21] Mondal, J. P., "Octagonal Spiral Inductor Measurement and Modelling for MMIC Applications," *Int. J. Electronics,* Vol. 68, 1990, pp. 113–125.

[22] Alimenti, F., et al., "Modeling and Characterization of the Bonding-Wire Interconnection," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, January 2001, pp. 142–149.

[23] Schuster, C., G. Leonhardt, and W. Fichtner, "Electromagnetic Simulation of Bonding Wires and Comparison with Wide Band Measurements," *IEEE Trans. Advanced Packaging,* Vol. 23, February 2000, pp. 69–79.

[24] Gross, S., and T. Weller, "Determining the RF Resistance and Q-Factor of Air-Core Inductors," *Microwave Optical Tech. Lett.,* Vol. 29, April 2001, pp. 89–93.

[25] Chang, K., (Ed.), *Handbook of Microwave and Optical Components,* Vol. 2, New York: John Wiley, 1989, Chap. 5.

[26] MacDonald, M., "Design Broadband Passive Components with Ferrites," *Microwaves and RF,* Vol. 32, October 1993, pp. 81–132.

[27] Sevick, J., *Transmission Line Transformers,* Atlanta, GA: Noble Publishing, 1996.

5

Capacitors

5.1 Introduction

When a voltage is applied across the two plates of a capacitor, the amount of energy stored depends on the work done in charging the capacitor. *Capacitance* is defined as the capacity to store energy in an electric field between two electrodes or efficiency of the structure in storing a charge when voltage difference exists between the plates. Its value depends on the area of the electrodes, separation between the electrodes, and the dielectric material between them. Dielectrics with high values of permittivity and higher breakdown voltage are the most desirable. The capacitor structure might have two or more conductors. The capacitance, C, in farads, of a capacitor structure consisting of two conductors is expressed as:

$$C = \frac{Q}{V} \tag{5.1}$$

where Q is the total charge in coulombs on each electrode or conductor and V is the voltage between the two conductors in volts. At the positive polarity the charge is positive, whereas at the negative polarity it is negative. Field lines start from the positive plate and terminate at negative plate.

The basic structure of a capacitor as shown in Figure 5.1 consists of two parallel plates also called electrodes, each of area A and separated by an insulator or dielectric material of thickness d and permittivity $\epsilon_0 \epsilon_{rd}$, where ϵ_0 and ϵ_{rd} are free-space permittivity and relative dielectric constant, respectively [1–8]. Gauss's law gives the total charge on each plate:

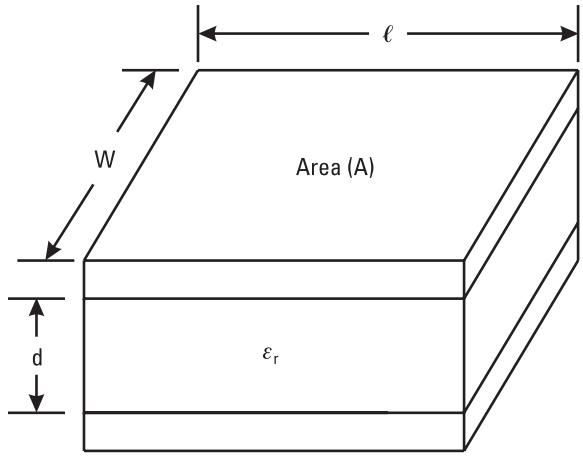


Figure 5.1 Basic parallel plate capacitor configuration.

$$Q = \oint_s \epsilon_0 \epsilon_r E_x \cdot ds = \epsilon_0 \epsilon_r E_x A \tag{5.2}$$

where E_x (V/d) is the electric field produced by the applied voltage V. From (5.1) and (5.2),

$$C = \epsilon_0 \epsilon_r \frac{A}{d} = \epsilon_0 \epsilon_r \frac{W \times \ell}{d} \tag{5.3}$$

where W and ℓ are the width and length of one of the plates. Equation (5.3) does not include the effect of fringing field. Equation (5.3) can be expressed in commonly used units as follows:

$$C = 0.2249 \epsilon_r \frac{W \times \ell}{d} \qquad \text{(pF), } W, \ell, \text{ and } d \text{ in inches} \tag{5.4a}$$

$$C = 8.85 \times 10^{-3} \epsilon_r \frac{W \times \ell}{d} \qquad \text{(pF), } W, \ell, \text{ and } d \text{ in millimeters} \tag{5.4b}$$

$$C = 8.85 \times 10^{-6} \epsilon_r \frac{W \times \ell}{d} \qquad \text{(pF), } W, \ell, \text{ and } d \text{ in microns} \tag{5.4c}$$

A unit of capacitance is the farad (F) and depending on its value it can be expressed in microfarads (μF or 10^{-6}F), nanofarads (nF or 10^{-9}F), picofarads

(pF or 10^{-12} F), or sometimes in very small values, femtofarads (fF or 10^{-15} F). Generally, low-frequency bypass capacitor values are expressed in microfarads and nanofarads, RF and microwave bypass and tuning capacitors are expressed in picofarads, and parasitic or fringing capacitance is written in femtofarads.

Almost every chip capacitor has a rectangular area. Other shapes such as octagonal and circular are also used in MMICs, as discussed in the next chapter. Rounded corner capacitors have higher yields in terms of electrostatic discharge failure. Table 5.1 lists plate areas of several possible geometries for the parallel-plate monolithic capacitors.

5.2 Capacitor Parameters

Selection of a particular capacitor depends on the application at hand. When selecting a capacitor, one should consider several of its parameters including capacitance value, tolerances, thermal stability or temperature coefficient, the quality factor Q, equivalent series resistance, series resonant frequency, parallel resonant frequency, dissipation factor, voltage rating, current rating, insulation resistance, time constant, physical requirements, and cost. These are briefly discussed in this section.

5.2.1 Capacitor Value

Chip or discrete capacitors are available [9–11] in a large range of capacitance values. A typical range for RF and microwave applications is from 0.1 pF to 1 μF. In monolithic circuits their range is from 0.05 to 100 pF.

Table 5.1
Surface Area of Various Geometries

Geometry	Dimensions				Area
	Width	Length	Side	Radius	A
Square	W	W			$W \times W$
Rectangle	W	ℓ			$W \times \ell$
Circle				r	πr^2
Regular polygon			a		$1/4\ na^2 \cot(180°/n)$, where n is the number of sides
Parallelogram	W	ℓ			$W \times \ell \sin\theta$, where θ is the angle between sides W and ℓ
Triangle			a, b		$1/2\ a \times b \sin\theta$, where θ is the angle between sides a and b

5.2.2 Effective Capacitance

For chip capacitors, the nominal capacitance value is measured at 1 MHz and in typical RF applications the operating frequency is much higher. Because the capacitor has an associated parasitic series inductance as shown in Figure 5.2(a), the impedance of the capacitance (neglecting series resistance) can be written

$$Z_c = j\left[\omega L_s - \frac{1}{\omega C}\right] = -\frac{j}{\omega C}[1 - \omega^2 L_s C] \tag{5.5}$$

or

$$Z_c = -\frac{j}{\omega C_e} \tag{5.6a}$$

where

$$C_e = C[1 - \omega^2 L_s C]^{-1} = C[1 - (\omega/\omega_s)^2]^{-1} \tag{5.6b}$$

Here ω_s is the series resonant frequency $\left(= 1/\sqrt{L_s C}\right)$, which is discussed in Section 5.2.7. The equivalent capacitance C_e is known as the *effective capacitance* and below the resonance frequency, its value is generally greater than the nominal specified value.

5.2.3 Tolerances

Chip capacitors are available with tolerances of ±5%, ±10%, and ±20%. For matching and other circuits, one needs tight tolerance capacitors, whereas for bypass or dc block applications, ±20% tolerance is generally acceptable. Typical tolerances in monolithic capacitors are better than ±10%.

5.2.4 Temperature Coefficient

The rate of change of capacitance value with temperature is known as its *temperature coefficient* (TC) and is expressed in parts per million per degree

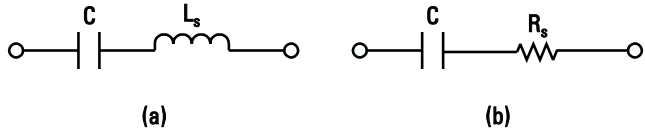


Figure 5.2 (a, b) Series representations of a capacitor.

Celsius (ppm/°C). A smaller value of TC is desirable in most applications, where circuit stability with temperature is of prime importance. The TC value may be negative or positive. Sometimes, by selecting the right TC value, the circuit's temperature dependence might be minimized. Small-value capacitors have a TC value of less than ±50 ppm/°C. The TC value for monolithic capacitors using silicon nitride is about +30 ppm/°C.

5.2.5 Quality Factor

Quality factor is an important FOM for capacitors and measures the capacitor's capability to store energy. When a capacitor is represented by a series combination of capacitance C and resistance R_s as shown in Figure 5.2(b), the quality factor, Q is defined by the following relation:

$$Q = \frac{1}{\omega C R_s} = \frac{1}{2\pi f C R_s} \tag{5.7}$$

where $\omega = 2\pi f$, and f is the operating frequency. For discrete capacitors, the value of Q is typically measured at low frequencies. Figure 5.3(a) shows typical measured Q values of ATC series 180, case R chip capacitors. For a 22-pF capacitor, the Q is greater than 100 at 1 GHz.

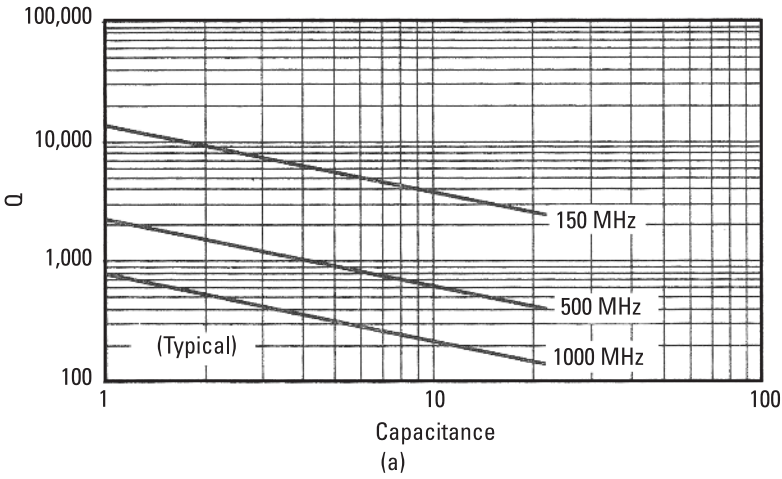
5.2.6 Equivalent Series Resistance

All capacitors exhibit parasitic inductance due to their finite size and series resistance due to contact and electrode resistance. This series resistance is commonly known as ESR, and is an important parameter in circuit design using capacitors. Chip capacitors with extra-low ESR values are also available. Figure 5.3(b) shows typical measured ESR values for ATC series 180, case R chip capacitors. For a 22-pF capacitor, the ESR value is about 0.05 ohm at 1 GHz.

5.2.7 Series and Parallel Resonances

Unlike inductors, from the equivalent circuit shown in Figure 5.4, we see that capacitors have both series and parallel resonance frequencies where the series and first parallel resonance frequencies are dominant. Below the series resonance frequency, the capacitor works as a capacitor as designed. However, above the resonance frequency, the capacitor's total reactance is inductive and it becomes again capacitive after the first parallel resonance frequency.

A lumped-element equivalent circuit of a capacitor is shown in Figure 5.4, where L_s is the electrode inductance and C_p is the parasitic parallel capacitance. The impedance of the capacitance between the two electrodes can be written



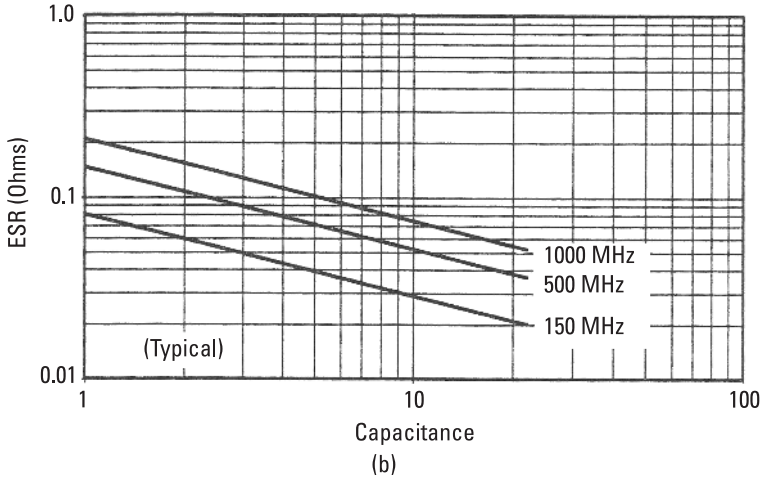


Figure 5.3 Typical performance of ATC chip capacitors: (a) *Q* versus capacitance and (b) ESR versus capacitance.

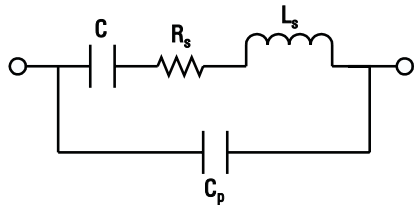


Figure 5.4 Equivalent circuit of a parallel plate capacitor.

$$Z_c = \frac{1}{j\omega C_p + \left(R_s + j\omega L_s + \dfrac{1}{j\omega C}\right)^{-1}} \tag{5.8}$$

Thus, the value of Z_c is infinite (because of C and C_p) at dc and decreases with frequency. Finally it becomes zero at infinite frequency (because of inductance L_s). However, as shown in Figure 5.5, the behavior of Z_c is nonideal. Figure 5.5 also shows variations of an ideal inductor L, for an ideal capacitor C, and for a parasitic capacitor C_p. When $C >> C_p$, at frequency ω_s, the reactances of series elements C and L_s become equal, that is, $\omega_s L_s = \dfrac{1}{\omega_s C}$, resulting in total reactance equal to zero. The frequency ω_s at which this happens is called the *series resonant frequency* (SRF), and the capacitor's impedance is equal to resistor R_s. Thus, at SRF, a capacitor mounted in a series configuration is represented by a small resistor and its insertion loss is low. As the frequency increases, the reactance of the capacitance becomes very small and the reactances of the parallel elements L_s and C_p become equal, that is, $\omega_p L_s = \dfrac{1}{\omega_p C_p}$. The frequency ω_p at which this occurs is known as the *parallel resonant frequency* (PRF), and the capacitor becomes a very large resistor whose value is given by

$$R_p = \frac{1}{R_s(\omega_p C_p)^2} \tag{5.9}$$

Thus, at PRF, R_p is infinite when $R_s = 0$.

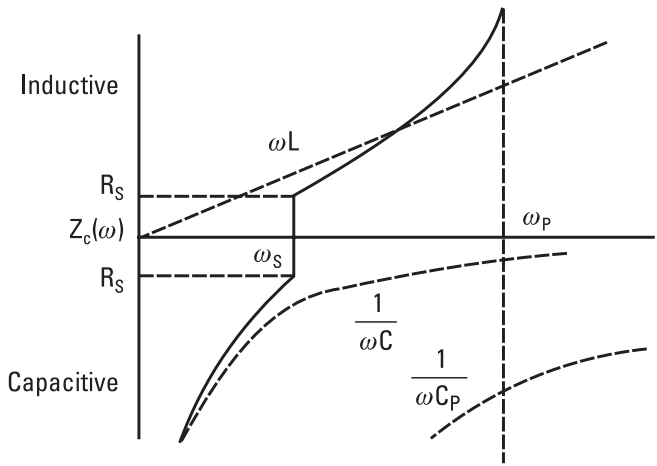


Figure 5.5 Variation of input impedance of ideal series inductor, series capacitor and parallel capacitor, and parallel plate capacitor.

5.2.8 Dissipation Factor or Loss Tangent

The *dissipation factor* (DF) of a capacitor is defined as a ratio of the capacitor's series resistance to its capacitive reactance, that is,

$$\text{DF} = \omega C R_s = \frac{1}{Q} = \tan \delta \tag{5.10}$$

where Q was defined earlier in (5.7). The dissipation factor tells us the approximate percentage of power lost in the capacitor and converted into heat. For example, DF = tan $\delta = 0.01$ means that the capacitor will absorb 1% of total power. To dissipate negligible power, one needs a capacitor with very high Q on the order of 1,000 to 10,000.

5.2.9 Time Constant

In a circuit when an ideal capacitor C is connected in series with a resistor R, and a dc voltage is applied, it takes a finite time τ to charge the capacitor to the applied voltage. This is known as the *time constant* and is given by

$$\tau = RC \tag{5.11}$$

where τ, R, and C are expressed in seconds, ohms, and farads, respectively.

5.2.10 Rated Voltage

The maximum voltage that can be applied between the capacitor terminals safely without affecting its reliability or destroying it, is known as the *rated voltage* or *working voltage*. The value of the rated voltage for chip capacitors is between 50 and 500V, whereas for monolithic capacitors, it is less than 100V. A typical value for Si_3N_4 capacitors is about 50V.

5.2.11 Rated Current

The maximum current allowed to pass through a capacitor without destroying or overheating it is known as the *rated current* or *maximum current rating*. The rated current is either limited due to the breakdown voltage of the capacitor or power dissipated. In the former case, it depends on the frequency of operation and the capacitance value, whereas in the latter case, it depends on the ESR value.

5.3 Chip Capacitor Types

Chip capacitors are of the parallel plate type and are an integral part of RF and microwave ICs. Their sizes are generally much smaller than the operating wavelength. They are made by sandwiching high-dielectric-constant materials between parallel plate conductors. Dielectric materials used are of ceramic or porcelain or similar type material. Generally, they do not have leads. These capacitors can be connected using surface mounting techniques or soldered or they are epoxied and connected with gold wires or ribbons. The dielectric in a capacitor can be of the single layer type as shown in Figure 5.1 or of the multilayer dielectric type as shown in Figure 5.6.

5.3.1 Multilayer Dielectric Capacitor

If a capacitor is made using different dielectric layers (Figure 5.6) with dielectric constant values of $\epsilon_{r1}, \epsilon_{r2}, \ldots \epsilon_{rn}$ and thickness $d_1, d_2, \ldots d_n$, the equivalent dielectric constant, ϵ_{req}, is given by

$$\epsilon_{\text{req}} = \left[\sum_{m=1}^{n} \frac{d_m}{d_T \epsilon_{rm}} \right] \tag{5.12}$$

where d_m is the thickness and ϵ_{rm} is the dielectric constant of the mth layer, and d_T is the total thickness, that is,

$$d_T = d_1 + d_2 + \ldots + d_n \tag{5.13}$$

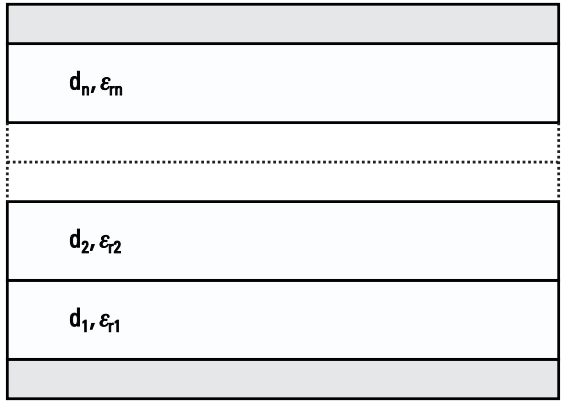


Figure 5.6 Multilayer dielectric parallel plate capacitor configuration.

For example: for two layers

$$\epsilon_{\text{req}} = \left[\frac{1}{(d_1 + d_2)}\left(\frac{d_1}{\epsilon_{r1}} + \frac{d_2}{\epsilon_{r2}}\right)\right]^{-1} = \frac{(d_1 + d_2)\,\epsilon_{r1}\,\epsilon_{r2}}{d_1\,\epsilon_{r2} + d_2\,\epsilon_{r1}} \tag{5.14}$$

and the capacitance C is expressed as:

$$C = 8.854 \times 10^{-6}\epsilon_{\text{req}}\frac{A}{d} \qquad \text{(pF)}$$

where A and d are in square microns and microns, respectively.

5.3.2 Multiplate Capacitor

The capacitance of a multiplate commonly known as a *multilayer capacitor* having n plates as shown in Figure 5.7 can be calculated using the following relation:

$$C = 8.854 \times 10^{-6}\frac{\epsilon_r A(n-1)}{d} \qquad \text{(pF)} \tag{5.15}$$

where area A is in square microns and d is in microns. In this relation it is assumed that the overlap area A and separation between plates are constant for all plates. Because there are 2.54×10^4 μm in an inch,

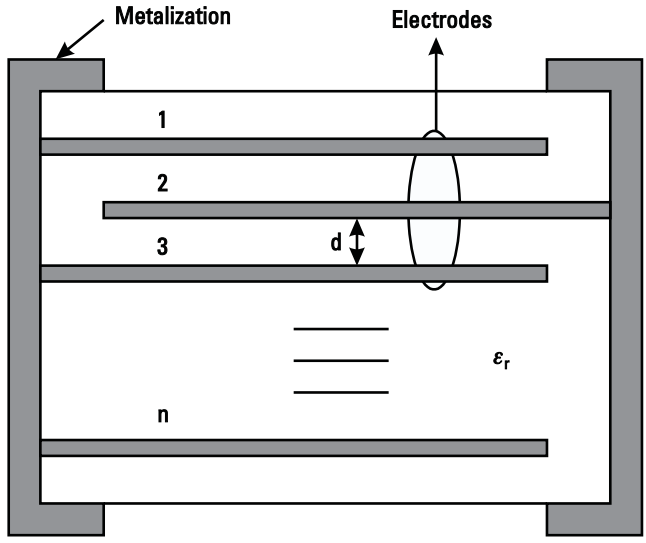


Figure 5.7 Multiplate capacitor configuration.

$$C = 0.2249 \frac{\epsilon_r A(n-1)}{d} \qquad \text{(pF)} \tag{5.16}$$

where units of A and d are in inches.

The characterization of *multilayer capacitors* (MLCs) has been described in the literature [12–20]. This includes accurate analytical models, series, parallel, and higher order resonances, field distributions, and power ratings. It is not within the scope of this book to go into such detail, and readers are referred to the above-mentioned references.

5.4 Discrete Parallel Plate Capacitor Analysis

Because chip capacitors in RF and microwave circuits are connected in various configurations and because mechanical orientation influences the parasitic parameters, their approximate analyses are discussed next.

5.4.1 Vertically Mounted Series Capacitor

A parallel plate capacitor is used commonly as a dc block in MICs, where the microstrip line has a gap and the capacitor is mounted as shown in Figure 5.8(a). In this case the capacitor can be treated as an open-ended stub connected in series between two microstrip lines. The equivalent circuit for this configuration can be represented as shown in Figure 5.8(b). Ignoring the open-end effects, the input impedance of the capacitor is given by

$$Z_{\text{in}} = Z_{0c} / \tanh(\gamma \ell) = Z_{oc} \frac{1 + j \tanh(\alpha \ell) \cdot \tan(\beta \ell)}{\tanh(\alpha \ell) + j \tan(\beta \ell)} \tag{5.17}$$

where Z_{0c} is the characteristic impedance of the capacitor considered as a transmission line in vertical direction, ℓ is the length of the capacitor, and $\gamma = \alpha + j\beta$ is the propagation constant of the capacitor line.

For capacitor dimensions much smaller than the operating wavelength, the single-layer capacitor's characteristic impedance is given by

$$Z_{0c} = \frac{120\pi}{\sqrt{\epsilon_{rd}}\, W/d} \qquad \text{for } W/d,\ \epsilon_r >> 10 \tag{5.18a}$$

or

$$Z_{0c} = \frac{120\pi}{\sqrt{\epsilon_{rd}}} \left[W/d + 0.443 + \frac{\epsilon_{rd} + 1}{2\pi\epsilon_{rd}} \ln \frac{\pi e(W/d + 0.94)}{2} \right]^{-1} \tag{5.18b}$$

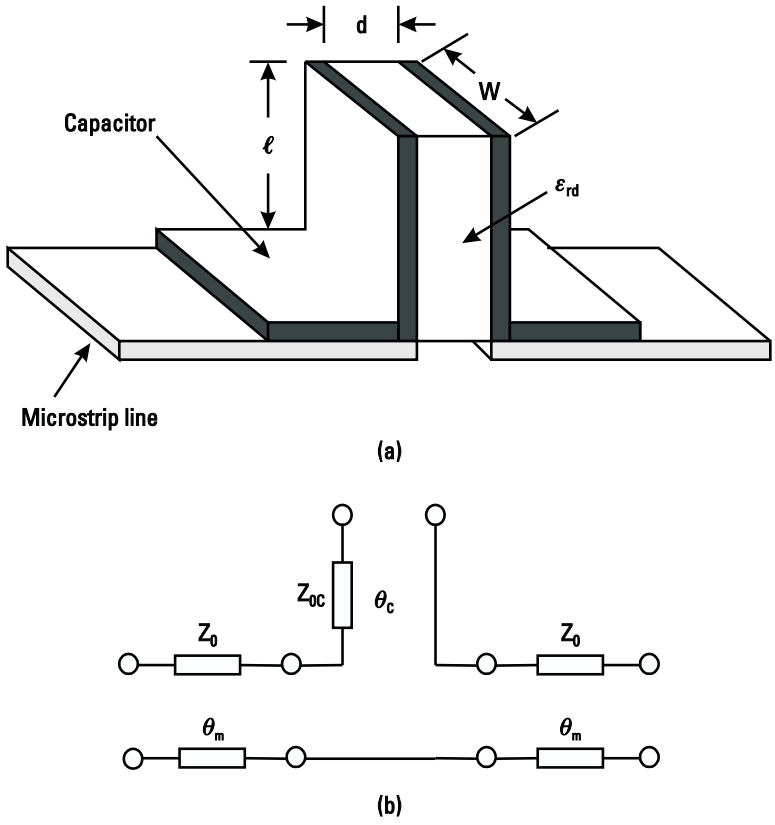


Figure 5.8 Vertical-parallel plate chip capacitor: (a) microstrip mounting and (b) EC model.

where ϵ_{rd}, W, and d are the capacitor's dielectric constant, width and thickness, respectively (Figure 5.8). More accurate Z_{0c} will be the average of the above two equations and $\beta = \dfrac{2\pi\sqrt{\epsilon_{rd}}}{\lambda_0}$.

Using ABCD matrix, the insertion loss (in decibels) of the capacitor can be calculated using the transmission coefficient given by

$$IL = -20 \log T = -20 \log \left| \frac{2}{A + B/Z_0 + CZ_0 + D} \right| \tag{5.19}$$

where Z_0 is the characteristic impedance of the microstrip as well as the source and load impedance.

For series impedance Z_{in}, $A = 1$, $B = Z_{\text{in}}$, $C = 0$, $D = 1$, and

$$IL = 20 \log \left| 1 + 0.5 Z_{\text{in}}/Z_0 \right| \tag{5.20}$$

When a capacitor has a series resonance, $\beta\ell = (2n - 1)\,\pi/2$ ($n = 1, 2, \ldots$), or $\ell = (2n - 1)\,\lambda/4$ and from (5.17) and (5.20),

$$IL = 20 \log [1 + 0.5 Z_{0c} \tanh (\alpha\ell)/Z_0] \tag{5.21}$$

For $Z_{0c} = 20\Omega$, $Z_0 = 50\Omega$, and $\alpha\ell = 0.1$,

$$IL = 20 \log [1 + 0.5 \times 20 \times 0.0997/50] \text{ dB} = 0.17 \text{ dB}$$

In the case of parallel resonance, $\beta\ell = 2n\pi/2$ ($n = 1, 2, \ldots$) or $\ell = n\lambda/2$ and from (5.17) and (5.20)

$$IL = 20 \log [1 + 0.5 Z_{0c} /\{Z_0 \tanh (\alpha\ell)\}] = 9.56 \text{ dB} \tag{5.22}$$

Thus, for a high-Q capacitor ($\alpha\ell << 1$) the insertion loss in the series resonance is much less than the insertion loss in the parallel resonance case. This is also verified by measurements as shown in Figure 5.9. For the configuration in Figure 5.8, when the capacitor is "ideal" the insertion loss is zero for the series resonance and infinite for the shunt resonance.

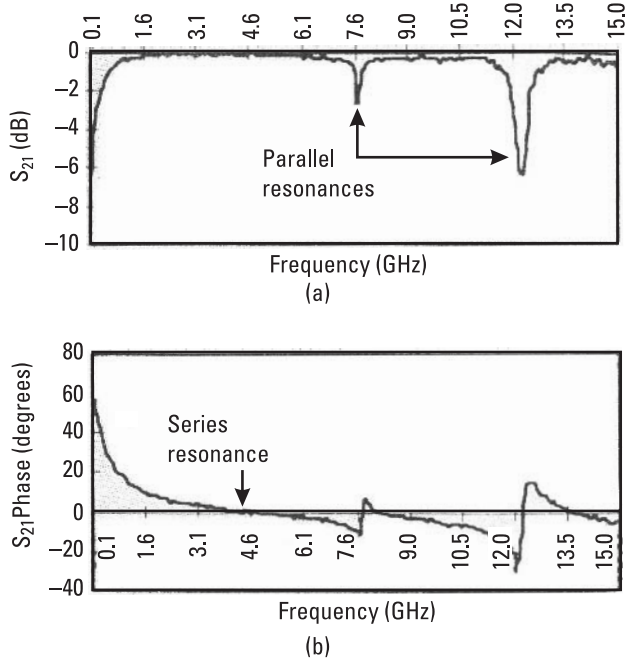


Figure 5.9 Measured transmission response of a microstrip-mounted series chip capacitor: (a) magnitude and (b) phase.

5.4.2 Flat-Mounted Series Capacitor

Another series connection is shown in Figure 5.10(a) and for a lossless case its equivalent circuit is shown in Figure 5.10(b), where Y_c is the capacitor's admittance given by

$$Y_c = jY_{0c}\frac{2\sin(\beta\ell)}{1+\cos(\beta\ell)} = j2Y_{0c}\tan(\beta\ell/2) \tag{5.23a}$$

$$\cong jY_{0c}\beta\ell \tag{5.23b}$$

where Y_{0c} is the characteristic admittance of the capacitor considered as a transmission line along the length ℓ, and L_w, L_c, and L_m are the bond wire, capacitor, and microstrip line inductance, respectively. Approximate expressions for L_c and L_m are given next:

$$L_c = [Z_{0c}\sqrt{\epsilon_{rd}}/c]\,\ell \tag{5.24a}$$

$$L_m = [Z_0\sqrt{\epsilon_{re}}/c]\,\ell \tag{5.24b}$$

where Z_{0c} and Z_0 are the characteristic impedances of the capacitor and microstrip line, respectively. In this case series resonance occurs when $\beta\ell = \pi$ and parallel resonance takes place when $\beta\ell = 2\pi$. In an actual circuit, the series

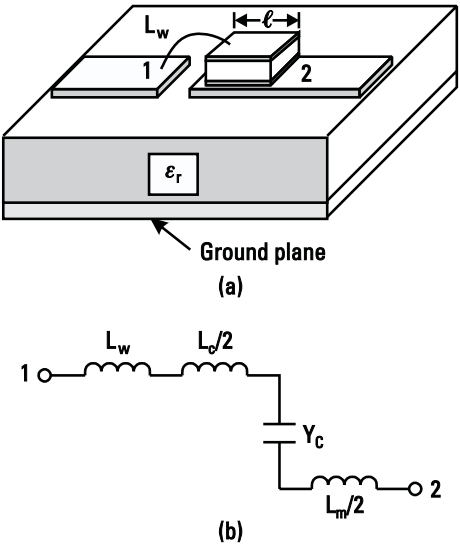


Figure 5.10 Horizontal-parallel plate chip capacitor: (a) microstrip mounting and (b) EC model.

resonance will occur sooner due to series inductors L_w and L_c and the parallel resonance is not significantly influenced by the series inductors [6].

5.4.3 Flat-Mounted Shunt Capacitor

Let us consider a bypass capacitor connected at the end of a microstrip line, where the top plate is wire bonded to a microstrip and the bottom plate is soldered or silver epoxied on a ground plane. Figure 5.11 shows this configuration as well as its distributed EC model. Here L_w and C_o represent the wire bond inductance and open-end fringing capacitance of the capacitor. The input admittance Y_{inc} of the shunt capacitor is given by

$$Y_{\text{inc}} = Z_{0c}\frac{j\omega C_o + Z_{0c}\tanh(\gamma\ell)}{Z_{0c} + j\omega C_o \tanh(\gamma\ell)} \tag{5.25}$$

In this case the input impedance of the wire-bonded capacitor becomes

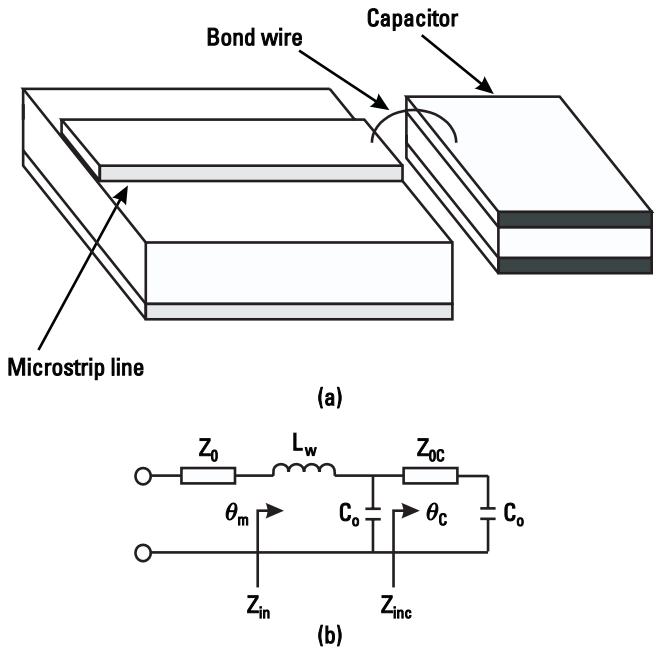


Figure 5.11 Grounded-parallel plate chip capacitor: (a) microstrip connection and (b) EC model.

$$Z_{\text{in}} = j\omega L_w + \frac{1}{j\omega C_o + Y_{\text{inc}}} \tag{5.26}$$

where Z_{0c} and γ are defined in the previous section.

5.4.4 Measurement-Based Model

Accurate models of chip capacitors can be developed by making *S*-parameter measurements in a series mounting configuration as shown in Figure 5.12(a). The devices are mounted across 50-Ω microstrip lines on a high-purity alumina substrate as the *S*-parameter measurements are made in a 50-Ω system. The thickness of the alumina substrate is usually 15 mil, whereas 25 mil can be used below C-band and 10 mil is recommended above X-band. The device's *S*-parameter data are de-embedded using TRL standards on the alumina substrate. At RF frequencies below 2 GHz, FR-4 PCBs are also used. A simplified equivalent circuit is shown in Figure 5.12(b).

The *S*-matrix of Figure 5.12(b) is given by

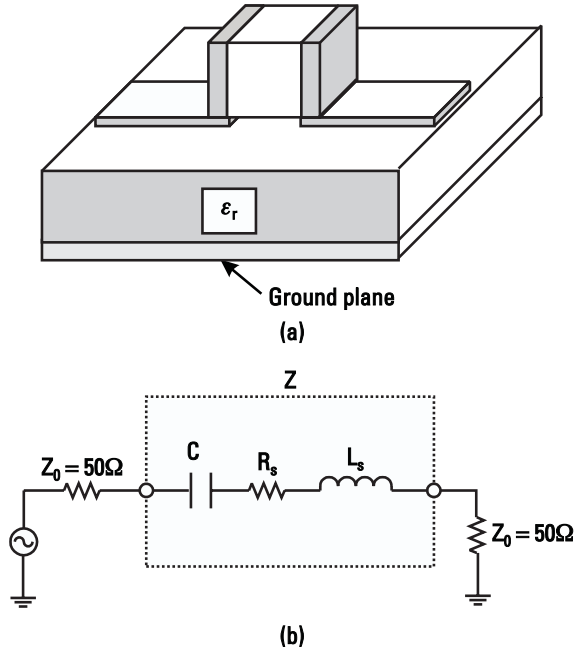


Figure 5.12 (a) Series mounting of a chip capacitor in microstrip environment and (b) EC representation.

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{Z + 2Z_0} \begin{bmatrix} Z & 2Z_0 \\ 2Z_0 & Z_0 \end{bmatrix} \tag{5.27a}$$

Here,

$$S_{11} = \frac{Z}{Z + 2Z_0} \tag{5.27b}$$

$$S_{21} = \frac{2Z_0}{Z + 2Z_0} \tag{5.27c}$$

If S_{21r} and S_{21i} are the real and imaginary parts of S_{21}, then

$$\frac{R_s + j\omega L_s - \dfrac{j}{\omega C} + 2Z_0}{2Z_0} = \frac{S_{21r} - jS_{21i}}{S_{21r}^2 + S_{21i}^2} \tag{5.28}$$

Equating real and imaginary parts,

$$R_s = 2Z_0 \left[\frac{S_{21r}}{S_{21r}^2 + S_{21i}^2} - 1 \right] \tag{5.29a}$$

$$\frac{1}{\omega C} - \omega L_s = \frac{2Z_0 S_{21i}}{S_{21r}^2 + S_{21i}^2} \tag{5.29b}$$

At series resonance ω_s, the angle of $S_{21} = 0$ and

$$L_s = \frac{1}{C\omega_s^2} \tag{5.30}$$

and (5.29b) becomes

$$C = \left[1 - \frac{\omega^2}{\omega_s^2} \right] \frac{S_{21r}^2 + S_{21i}^2}{2\omega Z_0 S_{21i}} \tag{5.31}$$

Thus, the capacitor EC model parameters are determined from (5.29), (5.30), and (5.31) or extracted by computer optimization. The simplified model is valid when capacitor dimensions are much smaller than the wavelength and does not predict the parallel and higher order series and parallel resonances.

An EC model for a capacitor that predicts higher order resonances is shown in Figure 5.13 [18], where C_s and C_g represent the interaction between the capacitor bond pads and substrate mounting. Additional RLC elements such as L_1, L_2, C_1, C_2, R_1, and R_2 are added to predict higher order resonances. The 0805 style capacitor has a footprint of 2.0×1.25 mm^2, and results in a C_g value of 0.154 pF when mounted on 31-mil-thick FR-4 substrate [18]. The model parameter values can be determined either from analytical expressions given in [18] or extracted by computer optimization. EC model parameters for 15- and 22-pF 0805 style ceramic multilayer capacitors are given in Table 5.2 [18]. The expression for L_s is given by

$$L_s = [a + bf\,]\,K_g \tag{5.32}$$

where

$$K_g = K_{ga} - K_{gb} \ln\left(\frac{W_{\text{cap}}}{h}\right) \tag{5.33}$$

Here f is the operating frequency in gigahertz, W_{cap} is the width of the capacitor, and h is the thickness of the substrate on which the capacitor is mounted. The values of R_s are same as ESR at 1 GHz. As a first-order approximation, the values of K_{ga}, K_{gb}, and b for the 15-pF capacitor are assumed to be the same as those for a 22-pF capacitor.

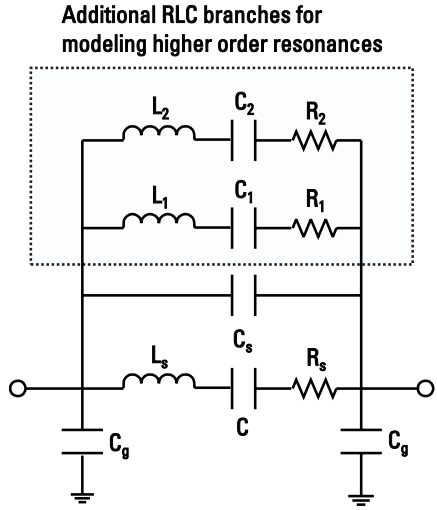


Figure 5.13 Substrate-dependent EC model of ceramic multilayer chip capacitor.

Table 5.2
EC Model Parameters for 15- and 22-pF 0805 Style Ceramic Multilayer Capacitors Extracted by Computer Optimization

Parameter	15-pF	22-pF
K_{ga}	0.654	0.654
K_{gb}	0.283	0.283
a (nH)	1.53	1.49
b (nH/GHz)	–0.016	–0.016
C (pF)	15	22
R_s (Ω)	0.11	0.11
C_s (pF)	0.016	0.016
C_g (pF)	0.154	0.154
C_1 (pF)	0.019	0.029
L_1 (nH)	71.995	74.764
R_1 (Ω)	38.458	38.426
C_2 (pF)	0.0258	0.050
L_2 (nH)	22.070	15.945
R_2 (Ω)	22.091	14.481

5.5 Voltage and Current Ratings

For high-voltage, high-power applications, circuit designers must have maximum voltage, current, and power handling ratings for the components they intend to use in their circuit designs. For chip capacitors such ratings depend on the materials used in the fabrication, capacitance value, and the area.

5.5.1 Maximum Voltage Rating

For chip capacitors, the maximum voltage rating depends on the breakdown voltage (V_B) between the plates. For porcelain capacitors the dielectric field strength is greater than 1,000 V/mil of dielectric thickness, whereas high-K materials such as barium titanate ($BaTiO_3$) have a much lower dielectric field strength value. Typical values of V_B for porcelain capacitors are 200V to 500V. Many times, the surface breakdown due to sharp edges, contamination, and surrounding humidity conditions sets the working voltage ratings rather than internal breakdown voltage between plates. Surface breakdown occurs outside of the device package and is also known as the *flashover voltage.*

5.5.2 Maximum RF Current Rating

If V_B is the capacitor's breakdown voltage and V_a is the dc applied voltage, the maximum (rms) current I_{mv} allowed to pass through a capacitor C is given by

$$I_{mv} = \frac{1}{\sqrt{2}}(V_B - V_a)\,\omega C \tag{5.34}$$

Thus, for given values of V_B, V_a, and C, the maximum current is proportional to the operating frequency. For example, for $V_B = 200$V, $V_a = 10$V, and $C = 5$ pF, the values of I_{mv} are 4.22 and 21.1A at 1 GHz and 5 GHz, respectively.

5.5.3 Maximum Power Dissipation

At higher frequencies and larger values of capacitance, the maximum value of current in a capacitor is limited by the maximum allowed power dissipation, due to the finite value of ESR. If P_{dis} is the maximum allowed power dissipation, the maximum current I_{mp} is given by

$$I_{mp} = \sqrt{\frac{P_{\text{dis}}}{\text{ESR}}} \tag{5.35}$$

where P_{dis} is calculated based on the thermal resistance and the maximum allowed temperature rise of the capacitor.

Calculation of the thermal resistance of single-layer and multilayer chip capacitors is complex and an approximate analysis is described here [9]. In this analysis, the heat removed from the capacitor is considered to be only by conduction. The thermal conductivity of electrodes and dielectric layers is considered constant up to 125°C, the maximum operating temperature of the capacitor. The heat sinking has been assumed in the direction of current flow. Because some heat removal will occur as a result of convection and radiation, as well as through vertical paths, the values for thermal resistance calculated next are relatively conservative providing extra margins in the current ratings.

The thermal resistance of the chip capacitors is calculated by considering Figure 5.14, where A is the terminal cross-section area (in centimeters) normal to heat flow and ℓ is the separation (in centimeters) between two terminals at temperature T_1 and T_2. If P_{dis} is the power dissipated (in watts), R_{TH} is the thermal resistance (°C/W) of the capacitor and K is the thermal conductivity (W/cm-°C) of the medium between terminals 1 and 2. The temperature difference between terminals 1 and 2 is given by

$$\Delta T = T_2 - T_1 = P_{\text{dis}} R_{\text{TH}} \tag{5.36a}$$

where

$$R_{\text{TH}} = \frac{\ell}{KA} \tag{5.36b}$$

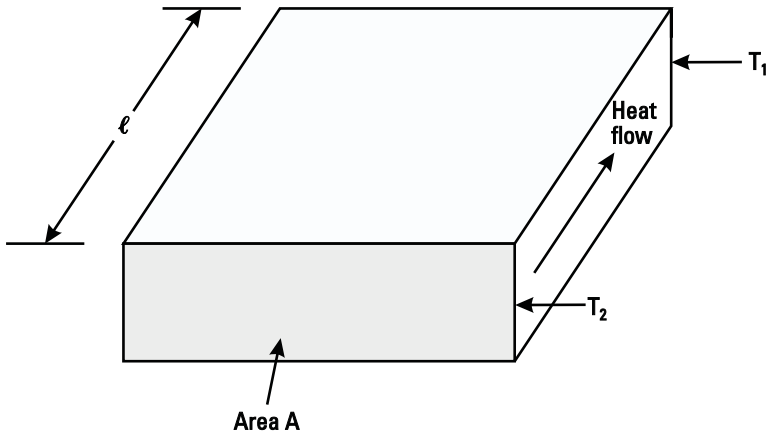


Figure 5.14 Heat flow diagram representation of a chip capacitor.

The thermal resistance of a multilayer capacitor is determined by considering the structure as shown in Figure 5.15. In this configuration, first the total power dissipated due to electrode and dielectric losses in a vertical column of length d_x at a position of x from terminal 1, is calculated, then thermal resistances $R_{\mathrm{TH1}x}$ and $R_{\mathrm{TH2}x}$ are calculated. Equations (5.36a) and (5.36b) then become

$$\Delta T_x = P_{\mathrm{dis}x} \frac{R_{\mathrm{TH1}x} R_{\mathrm{TH2}x}}{R_{\mathrm{TH1}x} + R_{\mathrm{TH2}x}} \tag{5.37}$$

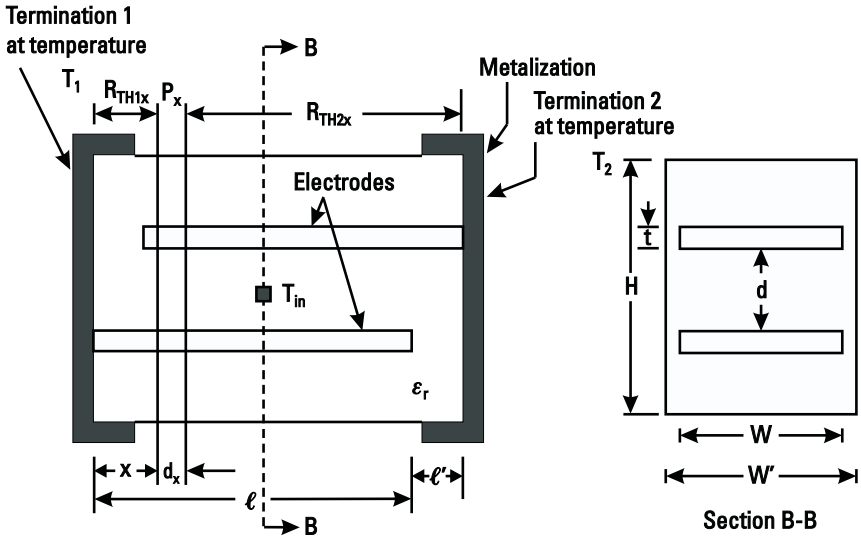


Figure 5.15 Cross-sectional views of a chip capacitor for thermal resistance calculations.

$$R_{\mathrm{TH}1x} = \frac{x}{KA} \tag{5.38a}$$

$$R_{\mathrm{TH}2x} = \frac{\ell + \ell' - x}{KA} \tag{5.38b}$$

where

$$P_{\mathrm{dis}x} = i^2 R_x d_x + i^2 (\tan\ \delta\omega\Delta C)^{-1} \tag{5.38c}$$

Here, i is the total current at plane x, R_x is the total resistance per unit length of electrodes, and ΔC is the capacitance of length d_x. The thermal equivalent circuit of Figure 5.15 is shown in Figure 5.16, where heat generation is in the middle and several thermal resistances are defined as:

$R_{\mathrm{TH}d}$ = thermal resistance of dielectric for the heat flow over length $(\ell + \ell')/2$;

$R_{\mathrm{TH}m}$ = thermal resistance of parallel combination of all electrodes for the heat flow over length $(\ell - \ell')/2$;

$R_{\mathrm{TH}ms}$ = thermal resistance of parallel combination of all short electrodes for the heat flow over length $(\ell + \ell')/2$;

$R_{\mathrm{TH}dl}$ = thermal resistance of parallel combination of dielectric from the ends of electrodes to the opposite terminal of the capacitor for the heat flow over length ℓ'.

The expressions for various thermal resistances are given next:

$$R_{\mathrm{TH}d} = \frac{0.5(\ell + \ell')}{K_d A_d} \tag{5.39a}$$

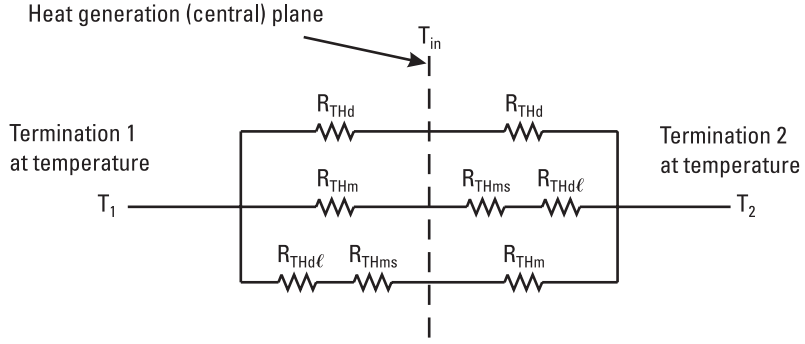


Figure 5.16 Schematic for a thermal resistance calculation for metal and dielectric layer.

$$R_{\mathrm{TH}m} = \frac{0.5(\ell + \ell')}{K_m\left(\frac{NA_m}{2}\right)} \tag{5.39b}$$

$$R_{\mathrm{TH}ms} = \frac{0.5(\ell - \ell')}{K_m\left(\frac{NA_m}{2}\right)} \tag{5.39c}$$

$$R_{\mathrm{TH}dl} = \frac{\ell}{K_d\left(\frac{NA_m}{2}\right)} \tag{5.39d}$$

where N is the number of electrodes, the cross-sectional area of one electrode is $A_m = Wt$ and of N electrodes is NWt, and the cross-sectional area of the dielectric is $A_d = W'H - NWt$. Here t, W, W', d, and H are electrode thickness, electrode width, total capacitor width, separation between electrodes, and capacitor height, respectively. The subscripts d and m designate dielectric and metal, respectively. Assuming a symmetrical configuration, the thermal resistance of the capacitor [for the heat generated at $x = (\ell + \ell')/2$] can be written as

$$R_{\mathrm{TH}C} = \frac{0.5}{\frac{1}{R_{\mathrm{TH}d}} + \frac{1}{R_{\mathrm{TH}m}} + \frac{1}{R_{\mathrm{TH}ms} + R_{\mathrm{TH}dl}}} \tag{5.40}$$

Table 5.3 provides chip capacitor dimensions, number of electrodes, thermal conductivity and thermal resistance values, and maximum power dissipation for several ATC capacitors. For high-power applications, 100B series capacitors can handle approximately twice as much power as 100A series.

5.6 Capacitor Electrical Representation

5.6.1 Series and Shunt Connections

When n capacitors (having capacitance values $C_1, C_2, \ldots, C_n$) are connected in series, the total capacitance C_T is given by

$$C_T = \frac{1}{1/C_1 + 1/C_2 + \ldots + 1/C_n} \tag{5.41}$$

Table 5.3
Thermal Resistance Calculations for Electrodes, Dielectric Layers, and Chip Capacitors [9]*

Electrodes					
Cap value (pF)**	1	100	1	100	1,000
N = number of electrodes	2	28	2	18	62
ℓ (cm)	0.1	0.1	0.22	0.22	0.22
ℓ' (cm)	0.04	0.04	0.06	0.06	0.06
A_m (cm^2)	0.00006	0.00006	0.000141	0.000141	0.000141
NA_m (cm^2)	0.00012	0.00168	0.000282	0.002538	0.00874
K_m (W/cm-°C)	0.6991	0.6991	0.6991	0.6991	0.6991
R_{THm} (°C/W)	1,670	120	1,420	158	46
R_{THms} (°C/W)	715	51	812	90	26
Dielectric					
$\ell + \ell'$ (cm)	0.14	0.14	0.28	0.28	0.28
A_{cap} (cm^2)	0.02	0.02	0.07	0.07	0.07
A_d	0.01988	0.0183	0.06972	0.06746	0.06126
K_d (W/cm-°C)	0.1256	0.1256	0.1256	0.1256	0.1256
R_{THd} (°C/W)	28	30	16	16.5	18
R_{THdl} (°C/W)	5310	380	3390	376	109
Capacitor					
R_{THC} (°C/W)	13.7	11.4	7.9	7.2	5.9
Maximum power dissipation (W)	7.3	8.8	12.7	13.9	16.9

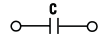
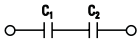
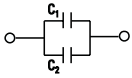
*For maximum power dissipation calculations, internal and heat sink temperatures are 125°C and 25°C, respectively.
**The first two capacitors are from the 100A series and last three are from the 100B series in the ATC catalog.

and its value is always less than the value of the smallest capacitor. To increase the capacitance value, the capacitors are connected in parallel. In this case the total capacitance becomes

$$C_T = C_1 + C_2 + \ldots + C_n \tag{5.42}$$

where C_T is larger than the largest value of the capacitor. Impedance, admittance and transmission phase angle formulas for various combinations of capacitors are given in Table 5.4.

Table 5.4
Impedance, Admittance, and Transmission Phase Angle Representations of Capacitors, with $R = 0$

Capacitor Configuration	Impedance $Z = R + jX$	Admittance $Y = 1/Z$	Phase Angle $\phi = \tan^{-1}(X/R)$
	$-j/\omega C$	$j\omega C$	$-\pi/2$
	$-(j/\omega)(1/C_1 + 1/C_2)$	$j\omega C_1 C_2/(C_1 + C_2)$	$-\pi/2$
	$-j/\omega(C_1 + C_2)$	$j\omega(C_1 + C_2)$	$-\pi/2$

When a voltage is applied across a group of capacitors in parallel, each capacitor is at the same voltage. However, when a voltage V is applied across a combination of capacitors connected in series, the voltage V_i across C_i capacitor is given by

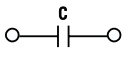
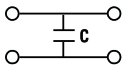
$$V_i = V\frac{C_i}{C_T} \tag{5.43}$$

5.6.2 Network Representations

At RF and the lower end of the microwave frequency band, the capacitor can be represented by its capacitance value C. If Z_0 is the characteristic impedance of the lines across which the capacitor is connected, the *ABCD*-, *S*-parameter-, *Y*-, and *Z*-matrices for a capacitor C connected in series and shunt configurations are given in Table 5.5, where ω is the operating radial frequency. As discussed in Section 5.6, when resistance and parasitic inductance are included in the capacitor model, results in Table 5.5 may be used by replacing $j\omega C$ with Y_c or $1/Z_c$, where Y_c and Z_c are the admittance and impedance of the capacitor, respectively.

The discussion on capacitors is continued in Chapters 6 and 7, where monolithic and interdigital capacitors are treated in detail, respectively.

Table 5.5
ABCD-, *S*-, *Y*-, and *Z*-Matrices for Ideal Lumped Capacitors

	***ABCD* Matrix**	***S*-Parameter Matrix**	***Y*-Matrix**	***Z*-Matrix**
	$\begin{bmatrix} 1 & \frac{-j}{\omega C} \\ 0 & 1 \end{bmatrix}$	$\frac{1}{\frac{-j}{\omega C} + 2Z_0} \begin{bmatrix} \frac{-j}{\omega C} & 2Z_0 \\ 2Z_0 & \frac{-j}{\omega C} \end{bmatrix}$	$\begin{bmatrix} j\omega C & -j\omega C \\ -j\omega C & j\omega C \end{bmatrix}$	
	$\begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix}$	$\frac{1}{Z_0 - \frac{j2}{\omega C}} \begin{bmatrix} -Z_0 & \frac{-j2}{\omega C} \\ \frac{-j}{\omega C} & -Z_0 \end{bmatrix}$		$\begin{bmatrix} \frac{-j}{\omega C} & \frac{-j}{\omega C} \\ \frac{-j}{\omega C} & \frac{-j}{\omega C} \end{bmatrix}$

References

[1] Ballou, G., *Capacitors and Inductors in Electrical Engineering Handbook,* R. C. Dorf, (Ed.), Boca Raton, FL: CRC Press, 1997.

[2] Walker, C. S., *Capacitance, Inductance and Crosstalk Analysis,* Norwood, MA: Artech House, 1990.

[3] Durney, C. H., and C. C. Johnson, *Introduction to Modern Electronic Genetics,* New York: McGraw-Hill, 1969.

[4] Zahn, M., *Electromagnetic Field Theory,* New York: John Wiley, 1979.

[5] Ramo, S., J. R. Whinnery, and T. Van Duzer, *Fields and Waves in Communication Electronics,* 2nd ed., New York: John Wiley, 1984.

[6] Abrie, P. D., *Design of RF and Microwave Amplifiers and Oscillators,* Norwood, MA: Artech House, 1999, Chap. 7.

[7] Weber, R. J., *Introduction to Microwave Circuits,* New York: IEEE Press, 2001.

[8] Weber, R. J., *Introduction to Microwave Circuits,* New York: IEEE Press, 2001.

[9] American Technical Ceramics, Huntington Station, NY.

[10] Dielectric Lab, New York.

[11] AVX Corporation, Myrtle Beach, SC.

[12] Ingalls, M., and G. Kent, "Monolithic Capacitors as Transmission Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-35, November 1987, pp. 964–970.

[13] de Vreede, L. C. N., et al., "A High Frequency Model Based on the Physical Structure of the Ceramic Multilayer Capacitor," *IEEE Trans Microwave Theory Tech.,* Vol. 40, July 1992, pp. 1584–1587.

[14] Sakabe, Y., et al., "High Frequency Measurement of Multilayer Ceramic Capacitors," *IEEE Trans. Components, Packaging Manufacturing Tech.—Part B,* Vol. 19, February 1996, pp. 7–12.

[15] Murphy, A. T., and F. J. Young, "High Frequency Performance of Multilayer Capacitors," *IEEE Trans. Microwave Theory Tech.,* Vol. 43, September 1995, pp. 2007–2015.

[16] Goetz, M. P., "Time and Frequency Domain Analysis of Integral Decoupling Capacitors," *IEEE Trans. Components, Packaging Manufacturing Tech.—Part B,* Vol. 19, August 1996, pp. 518–522.

[17] Fiore, R., "RF Ceramic Chip Capacitors in High RF Power Applications," *Microwave J.,* Vol. 43, April 2000, pp. 96–109.

[18] Lakshminarayanan, B., H. C. Gordon, and T. M. Weller, "A Substrate-Dependent CAD Model for Ceramic Multilayer Capacitors," *IEEE Trans. Microwave Theory Tech.,* Vol. 48, October 2000, pp. 1687–1693.

[19] Semouchkina, E., et al., "Numerical Modeling and Experimental Investigation of Resonance Properties of Microwave Capacitors," *Microwave Optical Tech. Lett.,* Vol. 29, April 2001, pp. 54–60.

[20] Fiore, R., "Capacitors in Broadband Applications," *Applied Microwave and Wireless,* May 2001, pp. 40–54.

6

Monolithic Capacitors

Monolithic or integrated capacitors (Figure 6.1) are classified into three categories: microstrip, interdigital, and *metal–insulator–metal* (MIM). A small length of an open-circuited microstrip section can be used as a lumped capacitor with a low capacitance value per unit area due to thick substrates. The interdigital geometry has applications where one needs moderate capacitance values. Both microstrip and interdigital configurations are fabricated using conventional MIC techniques. MIM capacitors are fabricated using a multilevel process and provide the largest capacitance value per unit area because of a very thin dielectric layer sandwiched between two electrodes. Microstrip capacitors are discussed briefly below. The interdigital capacitors are the topic of the next chapter and MIM capacitors are treated in this chapter.

All metals printed on a GaAs substrate will establish a shunt capacitance to the back side ground plane, C, given by

$$C = C_p + C_e \tag{6.1}$$

where C_p is the parallel plate capacitance and C_e is the capacitance due to edge effects. The parallel plate capacitance to the backside metal may be expressed as

$$\begin{aligned} C_p &= A\ 152 \times 10^{-8}\ \text{pF}/\mu\text{m}^2 \quad (75\text{-}\mu\text{m substrate}) \\ &= A\ 91 \times 10^{-8}\ \text{pF}/\mu\text{m}^2 \quad (125\text{-}\mu\text{m substrate}) \end{aligned} \tag{6.2}$$

where A is the top plate area in square microns. As an approximation, C_e can be taken as [1]

$$C_e = P\,3.5 \times 10^{-5}\ \text{pF}/\mu\text{m} \quad (75\text{-}\mu\text{m substrate}) \qquad (6.3)$$
$$= P\,5 \times 10^{-5}\ \text{pF}/\mu\text{m} \quad (125\text{-}\mu\text{m substrate})$$

where P is the perimeter of the capacitor in microns.

An accurate printed capacitor model must treat the capacitor as a microstrip section with appropriate end discontinuities as discussed in Chapter 14.

Monolithic MIM capacitors are integrated components of any MMIC process. Generally, larger value capacitors are used for RF bypassing, dc blocking, and reactive termination applications, whereas smaller value capacitors find usage as tuning components in matching networks. They are also used to realize compact filters, dividers/combiners, couplers, baluns, and transformers.

MIM capacitors are constructed using a thin layer of a low-loss dielectric between two metals. The bottom plate of the capacitor uses first metal, a thin unplated metal, and typically the dielectric material is silicon nitride (Si_3N_4) for ICs on GaAs and SiO_2 for ICs on Si. The top plate uses a thick plated conductor to reduce the loss in the capacitor. The bottom plate and the top plate have typical sheet resistances of 0.06 and 0.007 Ω/square, respectively, and a typical dielectric thickness is 0.2 μm. The dielectric constant of silicon nitride is about 6.8, which yields a capacitance of about 300 pF/mm^2. The top plate is generally connected to other circuitry by using an airbridge or dielectric crossover, which provides higher breakdown voltages. Typical process variations for microstrip and MIM capacitors are compared in Table 6.1.

Normally MIM capacitors have two plates, however, three plates and two-layer dielectric capacitors have also been developed.

6.1 MIM Capacitor Models

Several models for MIM capacitors on GaAs substrate have been described in the literature [2–5]. These include both EC and distributed models, which are discussed next.

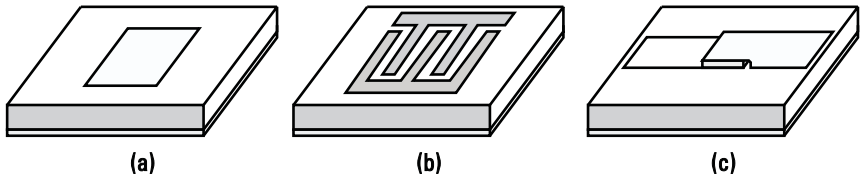


Figure 6.1 Monolithic capacitor configurations: (a) microstrip, (b) interdigital, and (c) MIM.

Table 6.1
Capacitance Variations of Microstrip and MIM Capacitors on GaAs Substrate

Capacitor	Range	Design Uncertainty	Process Variation
Microstrip (shunt only)	0.0–0.1 pF	±2%	±2%
MIM	1.0–30.0 pF	±5%	±10%
MIM	0.1–1.0 pF	±5%	±20%
MIM	0.05–0.1 pF	±5%	±30%

6.1.1 Simple Lumped Equivalent Circuit

When the largest dimension of the MMIC capacitor is less than $\lambda/10$, in the dielectric film at the operating frequency, the capacitor can be represented by an equivalent circuit, as shown in Figure 6.2, where B and T depict the bottom and top plate, respectively. The model parameter values can be calculated from the following relations:

$$C = \epsilon_0 \epsilon_{rd} \frac{W\ell}{d} = \frac{\epsilon_{rd}\, 10^{-15}}{36\pi} \frac{W\ell}{d} \text{ (F)} \tag{6.4a}$$

$$R = \frac{2}{3} \frac{R_s}{W} \ell \tag{6.4b}$$

$$G = \omega C \tan \delta = \frac{1}{18} \epsilon_{rd} f \frac{W\ell}{d} \times 10^{-6} \tan \delta \text{ (mho)} \tag{6.4c}$$

where ϵ_{rd} and tan δ are the dielectric constant and loss tangent of the dielectric film, respectively; R_s is the surface resistance of the bottom plate expressed in ohms per square; and W, ℓ, and d are in microns, and f is in gigahertz. The value of L can be obtained from (2.13a) in Chapter 2.

The conductor (Q_c) and dielectric (Q_d) quality factors can be expressed as

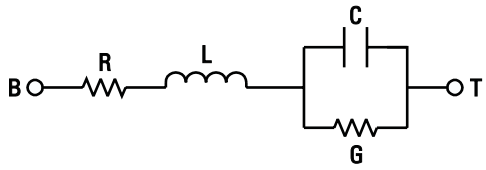


Figure 6.2 EC model of a MIM capacitor.

$$Q_c = \frac{1}{\omega RC} = \frac{3W}{2\pi f 2R_s \ell C} = \frac{27 \times 10^6 d}{f R_s \ell^2 \epsilon_r} \tag{6.5a}$$

$$Q_d = \frac{1}{\tan \delta} \tag{6.5b}$$

where f is in gigahertz and $\ell$and d are in microns.

The total quality factor Q_T is given by

$$Q_T = \left[\frac{1}{Q_c} + \frac{1}{Q_d}\right]^{-1} \tag{6.6}$$

Figure 6.3 shows another simple lumped EC. Model parameter values for MIM capacitors on a 125-μm-thick GaAs substrate are given in Table 6.2. The model parameters were extracted from measured S-parameter data as discussed in Chapter 2. Empirically fit closed-form values for such capacitors were obtained as follows:

$$L \text{ (nH)} = 0.02249 \times \log(10 \times C) + 0.01 \tag{6.7a}$$

$$C_1 \text{ (pF)} = 0.029286 \times C + 0.007 \tag{6.7b}$$

$$C_2 \text{ (pF)} = 0.00136 \times C + 0.004 \tag{6.7c}$$

where C is capacitor value in picofarads, the substrate thickness is 125 μm, capacitor range is 1 to 30 pF, and the frequency range is dc to 19 GHz.

6.1.2 Coupled Microstrip-Based Distributed Model

Mondal [2] described a distributed lumped-element MIM capacitor model based on coupled microstrip lines. The model parameter values can be either extracted

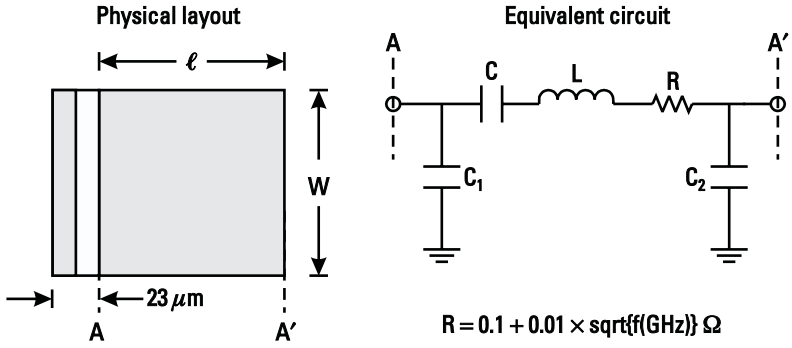


Figure 6.3 MIM capacitor and its EC model.

Table 6.2
Typical Model Parameter Values for MIM Capacitors

C (pF)*	$W = \ell$ (μm)	L (nH)	C_1 (pF)	C_2 (pF)	Q** at 10 GHz
1.0	58	0.0325	0.001	0.0054	120.0
2.0	82	0.0393	0.0129	0.0067	60.0
5.0	130	0.0482	0.0219	0.0108	24.0
10.0	182	0.055	0.0363	0.0176	12.0
15.0	223	0.0589	0.0509	0.0244	8.0
20.0	258	0.0618	0.0656	0.0312	5.0

*Based on 300 pF/mm^2 MIM capacitance.
**$Q = 1/\omega CR$.

from the measured two-port S-parameter data or approximately calculated as discussed later.

The cross-sectional view and the distributed model based on coupled transmission lines of a MIM capacitor are shown in Figure 6.4. The model parameters are defined as follows:

L_{11} = inductance/unit length of the top plate;

L_{22} = inductance/unit length of the bottom plate;

L_{12} = mutual inductance between the plates/unit length of the capacitor;

R_1 = loss resistance/unit length of the top plate;

R_2 = loss resistance/unit length of the bottom plate;

G = loss conductance of the dielectric/unit length of the capacitor;

C_{12} = capacitance/unit length of the capacitor;

C_{10} = capacitance with respect to ground/unit length of the top plate;

C_{20} = capacitance with respect to the ground/unit length of the bottom plate.

C_{10} and C_{20} are due to substrate effects. The voltage and current equations, relating the model parameters, based on coupled-mode transmission lines can be written as follows:

$$-\begin{bmatrix} \dfrac{\partial v_1}{\partial x} \\ \dfrac{\partial v_2}{\partial x} \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_{11} & j\omega L_{12} \\ j\omega L_{12} & R_2 + j\omega L_{12} \end{bmatrix} \begin{bmatrix} i_1 \\ -i_2 \end{bmatrix} \tag{6.8}$$

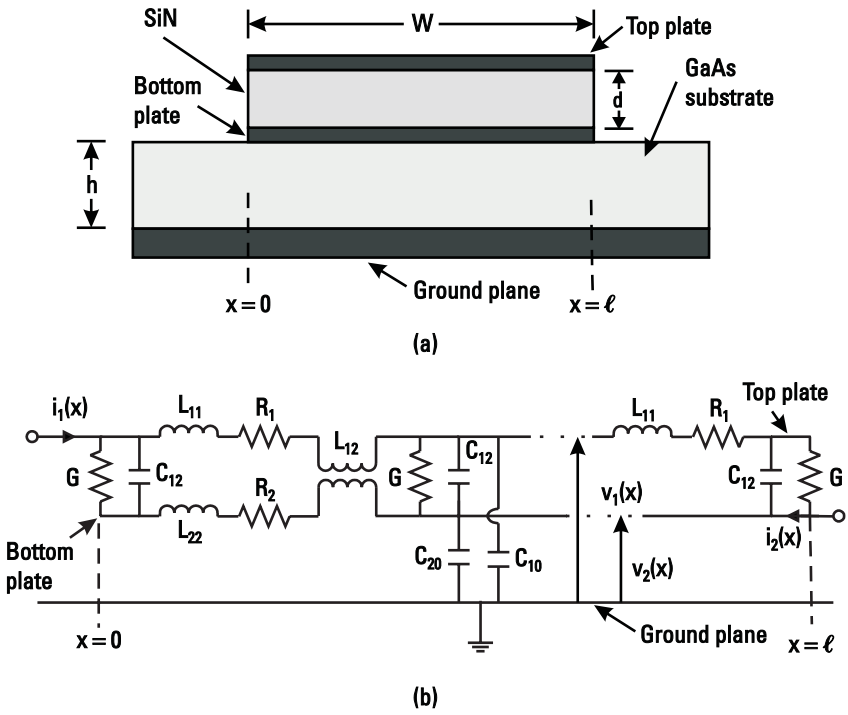


Figure 6.4 MIM capacitor: (a) cross-sectional view and (b) distributed model.

$$-\begin{bmatrix} \dfrac{\partial i_1}{\partial x} \\ \dfrac{-\partial i_2}{\partial x} \end{bmatrix} = \begin{bmatrix} G + j\omega(C_{10} + C_{12}) & -(G + j\omega C_{12}) \\ -(G + j\omega C_{12}) & G + j\omega(C_{20} + C_{12}) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{6.9}$$

where ω is the operating angular frequency. Equations (6.8) and (6.9) are solved for the Z-matrix [6] by applying the boundary conditions $i_1(x = \ell)$ and $i_2(x = 0) = 0$, and the values of the LE parameters are obtained by comparing the measured two-port S-parameters for the capacitor and converting it into the Z-matrix.

The LE parameter values can also be calculated by using analytical equations as described here:

$$C_{12} = \epsilon_0 \epsilon_{rd} W/d \tag{6.10}$$

or $C_{12} = W \times$ capacitance per unit area and

$$C_{20} = C_p + (C_2 - C_p) \cdot \frac{\epsilon_{re}}{\epsilon_r} \tag{6.11}$$

$$C_{10} = C_T - C_{20} \tag{6.12}$$

where

$$C_T = \left(\frac{Z_{0m} c}{\sqrt{\epsilon_{re}}} \right)^{-1} \tag{6.13}$$

$$C_p = \epsilon_0 \epsilon_r \frac{W}{h} \tag{6.14}$$

$$C_2 = \frac{1}{2} \cdot \left(\frac{Z_{os} c}{\sqrt{\epsilon_r}} \right)^{-1} \tag{6.15}$$

and c is the velocity of light, Z_{om} and ϵ_{re} are the characteristic impedance and effective dielectric constant of the microstrip (Figure 6.5) of capacitor width and GaAs as the substrate, respectively, and Z_{os} is the characteristic impedance of the stripline of width W. Terms ϵ_r and ϵ_{rd} are the dielectric constants for the substrate and capacitor film, respectively. The various inductance values are calculated using the following relations:

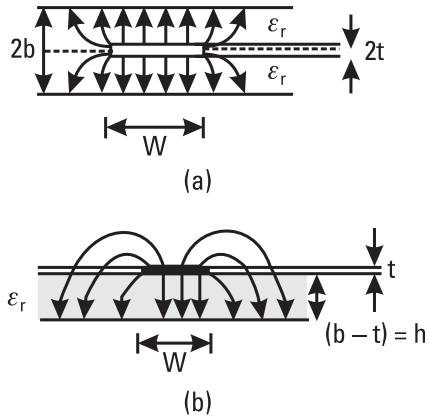


Figure 6.5 (a) Stripline used for calculating C_2 capacitance and (b) microstrip used for calculating C_T capacitance.

$$[L] = \frac{1}{c^2}\begin{bmatrix} C_{10} + C_{12} & -C_{12} \\ -C_{12} & C_{20} + C_{12} \end{bmatrix}^{-1}_{\text{air}} \tag{6.16}$$

where

$$[L] = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \tag{6.17}$$

and the element where C_{10}, C_{12}, and C_{20} are with $\epsilon_r = 1$.

Table 6.3 shows model values that were obtained by fitting two-port S-parameter data on a 4-mil-thick GaAs substrate. The number of elements required to model a MIM capacitor are prohibitively large and have limited usage in circuit simulation.

6.1.3 Single Microstrip-Based Distributed Model

Sadhir and Bahl [4] reported a simple and generalized distributed model for the MIM capacitors, based on microstrip line theory. The model element values have been related to the substrate thickness, thereby ensuring the capability of the model to accommodate different substrate thicknesses and also not be limited in terms of physical dimensions of the capacitor as long as width or length is less than half a wavelength. The model values have been validated by comparing the measured two-port S-parameter data obtained for several capacitors ranging from 0.5 to 30 pF on the 125-μm-thick substrate using TRL calibration techniques.

Table 6.3
Model Parameter Values for a 101-μm Dimension Capacitor on 4-Mil-Thick GaAs Substrate

Elements	Units	Calculated	Optimized
C_{10}	pF/m	40	22
C_{20}	pF/m	200	300
C_{12}	pF/m	44,692	33,000*
L_{11}	nH/m	4,222	400
L_{22}	nH/m	421.6	340
L_{12}	nH/m	421	360

*Fabricated dielectric film was found to be 0.17 μm thick instead of nominal 0.14 μm.

In the distributed EC (Figure 6.6), the bottom plate is considered to be a microstrip transmission line of the same width (W) and length (ℓ) as are the dimensions of a capacitor. The shunt conductance G is the dielectric film loss of the capacitor. The series resistance R_o represents the conductor loss in the metallization of the bottom plate whose thickness is much less than the skin depth. C_1 is the modified fringing capacitance associated with the top plate, which can be calculated from the fringing capacitance [7, 8] using the following relation:

$$C_f = C_T - C_p \tag{6.18}$$

where the total capacitance C_T and the parallel plate capacitance C_p are obtained using (6.13) and (6.14). All of these capacitances are expressed per unit length. In the case of the MIM capacitor, the bottom plate acts as a "sink" for some of the field lines from the top plate. The fringing capacitance is optimized so that the model best fits the measured data. The optimized fringing capacitance value is related to the theoretical value by the following relation:

$$C_1 = C_f \ell / 3 \tag{6.19}$$

which can be simplified as

$$C_1 \text{ (pF)} = 1.11 \times 10^{-3} \left(\sqrt{\epsilon_{re}}/Z_{om} - 0.034W/h\right)\ell \tag{6.20}$$

where ℓ is the length of the capacitor in microns.

Figures 6.7 and 6.8 show an excellent correlation between the modeled values and the measured data for S_{21} and S_{11} for 2- and 10-pF capacitors. Figure 6.9 illustrates the variation of Q-factor for various capacitors as a function of frequency. As expected, higher capacitor values indicate lower Q at a given frequency. Figure 6.10 shows the series SRF of various capacitors. Table 6.4 summarizes the model parameters of several MIM capacitors.

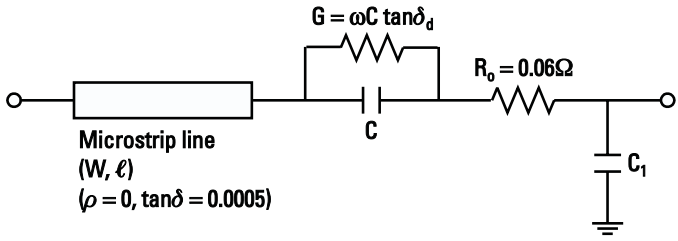


Figure 6.6 Microstrip distributed EC model of MIM capacitor.

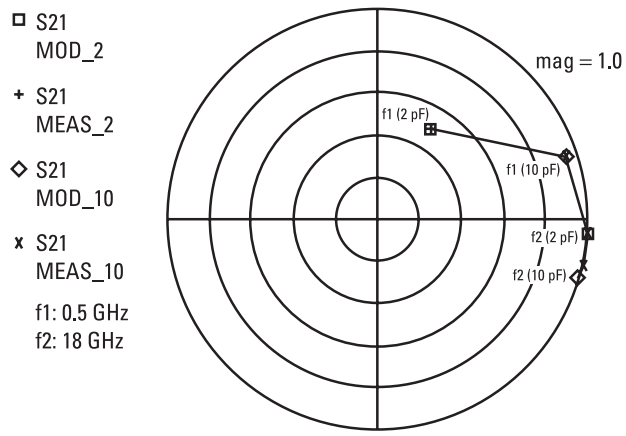


Figure 6.7 Modeled and measured S_{21} for 2- and 10-pF MIM capacitors on 125-μm-thick GaAs substrate.

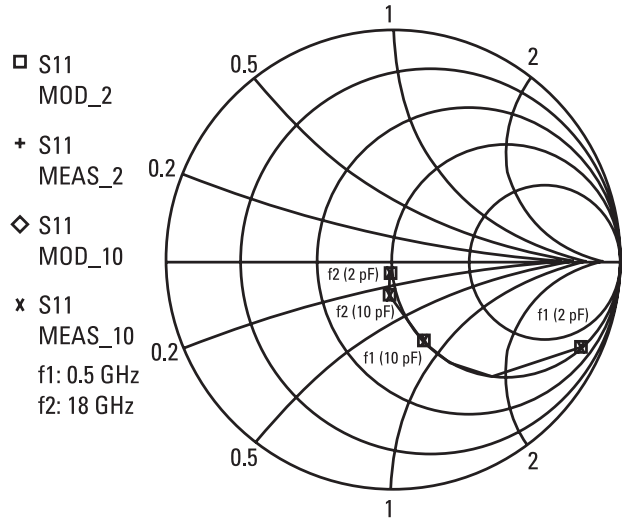


Figure 6.8 Modeled and measured S_{11} for 2- and 10-pF MIM capacitors on 125-μm-thick GaAs substrate.

When the MIM capacitor value is small, on the order of, say, 0.2 pF, the measured value of capacitance is always larger than the design value based on capacitance per unit area. This is due to the fact that the dielectric thickness along the periphery is thinner than at other places and this effect is more pronounced for smaller capacitor areas. Based on measured data an empirical

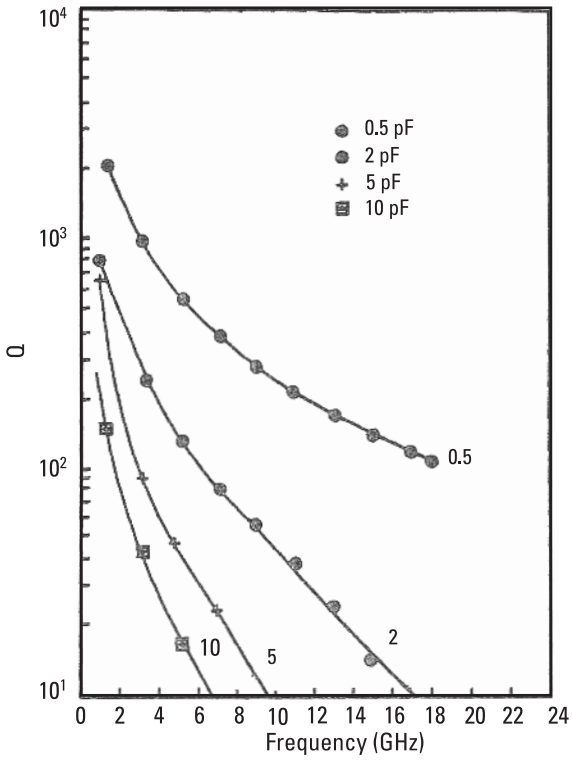


Figure 6.9 Q-factor versus frequency for various MIM capacitors on 125-μm-thick GaAs substrate.

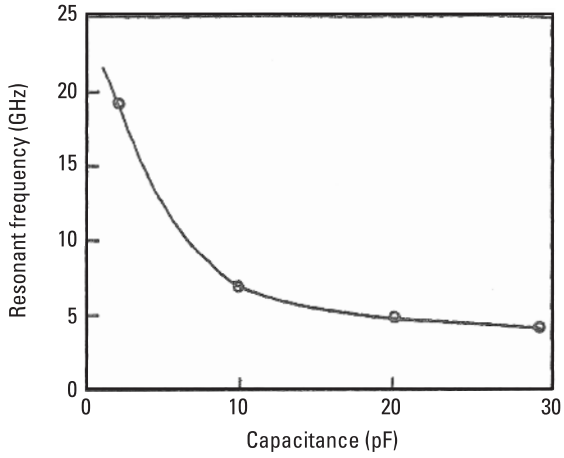


Figure 6.10 Series SRF of various MIM capacitors on 125-μm-thick GaAs substrate.

Table 6.4
Distributed Model Values of the MIM Capacitors

C (pF)	W (μm)	ℓ (μm)	ϵ_{re}	Z_{om}	C_1 (pF) (for h = 125 μm)
0.5	42	42	7.68	67.05	0.0014
2.0	82	82	8.08	52.3	0.0029
5.0	130	130	8.44	42.08	0.0049
10.0	182	182	8.75	35.51	0.0068
15.0	223	223	8.95	31.68	0.0084
20.0	258	258	9.13	28.63	0.0101

relation was derived that relates the designed capacitor value C to the measured value C_m by the following equation:

$$C_m = C(1 + 0.012/C) \tag{6.21}$$

where units are in picofarads.

6.1.4 EC Model for MIM Capacitor on Si

An EC model for MIM capacitors on Si using CMOS technology has been described by Xiong and Fusco [9]. The capacitor configuration and its EC model are shown in Figure 6.11. The parallel plate capacitance C is calculated by using (6.4a) and the expressions for other parameters describing the parasitic effects are given below.

$$r(\Omega) = \frac{2}{3}\frac{\rho l}{W}\left(\frac{1}{\delta_1\left(1 - e^{-t_1/\delta}\right)} + \frac{1}{\delta_2\left(1 - e^{-t_2/\delta}\right)}\right) \tag{6.22a}$$

$$\delta_1 = \begin{cases} t_1, & \delta > t_1 \\ \delta, & t_1 > \delta \end{cases} \tag{6.22b}$$

$$\delta_2 = \begin{cases} t_2, & \delta > t_2 \\ \delta, & t_2 > \delta \end{cases} \tag{6.22c}$$

$$\delta = \sqrt{\frac{2\rho}{2 \times 10^{-4}\pi^2 f}} \tag{6.22d}$$

$$L_1 = \frac{2}{3}(L_1 + L_2) \tag{6.22e}$$

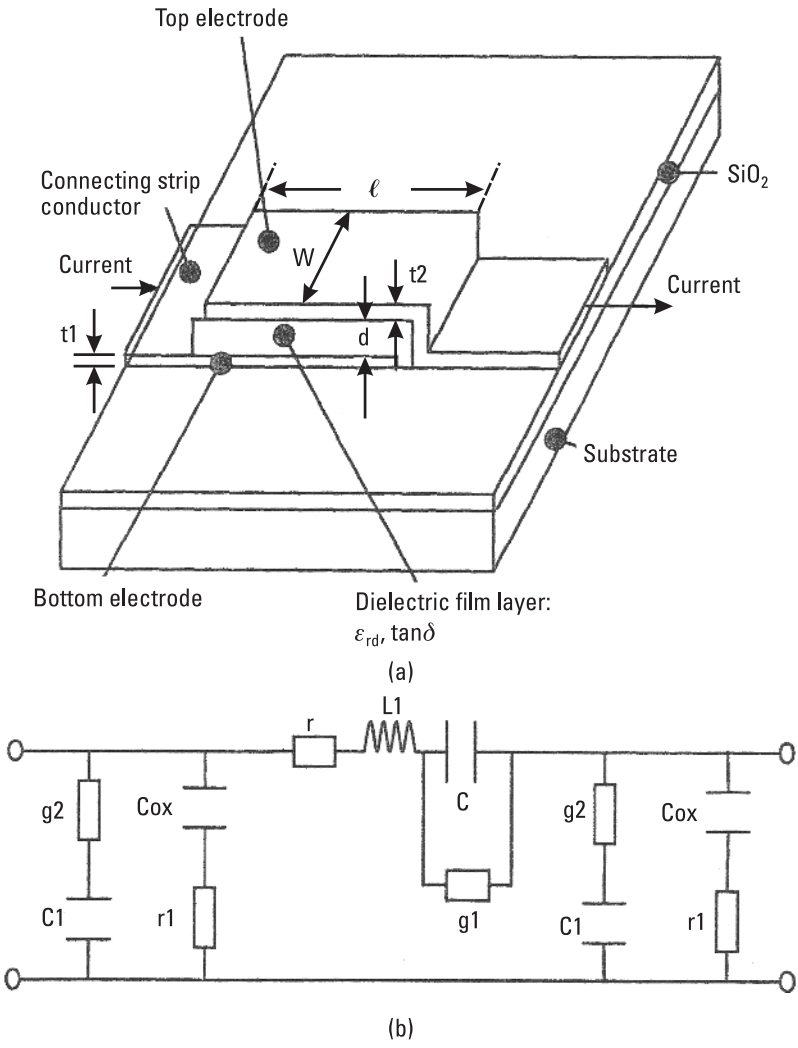


Figure 6.11 (a) MIM capacitor structure on Si substrate and (b) EC model. (*From:* [9]. © 2002 John Wiley. Reprinted with permission.)

$$L_1 = 2 \times 10^{-4} l \left(\ln \frac{2l}{W + t_1} + 0.5 + \frac{W + t_1}{3l} \right) \tag{6.22f}$$

$$L_2 = 2 \times 10^{-4} l \left(\ln \frac{2l}{W + t_2} + 0.5 + \frac{W + t_2}{3l} \right) \tag{6.22g}$$

$$g1 = \frac{1}{\omega C \tan \delta} \tag{6.22h}$$

$$C_{ox} = 0.5 \times 10^3 Wl\epsilon_{rox}/(36 \times 3.14159 d_{ox}) \tag{6.22i}$$

$$g2 = \frac{1}{\omega C_{ox} \tan \delta_{ox}} \tag{6.22j}$$

$$C1 = \frac{1}{2} \cdot l \cdot W \cdot \epsilon_r / h \tag{6.22k}$$

$$r1 = \frac{2}{l \cdot W \cdot G_{sub}} \tag{6.22l}$$

where W, l, t_1, t_2, h, and d_{ox} are in microns, capacitance is in picofarads, and inductance is in nanohenries. The substrate conductance per unit area is G_{sub}.

6.1.5 EM Simulations

6.1.5.1 One-Port MIM Capacitor Connection

When a MIM bypass capacitor is grounded through a via hole, the feed line or stub may be connected to the capacitor at various locations as shown in Figure 6.12. The Si_3N_4 capacitor value in this figure is approximately 10 pF and feed line width is 20 μm. Configurations (a) and (b) are approximately similar in electrical behavior, whereas in configurations (c) and (d) the capacitors are electrically shorter, that is, the parasitic effect is lower. Table 6.5 gives the phase angle of S_{11} EM simulated [10] at reference plane A. The GaAs substrate thickness is 75 μm. In configurations (c) and (d), the 10-pF capacitor's effective physical length is calculated to be 38% and 72% shorter, respectively, with respect to configuration (a). As a first-order approximation, the decrease in capacitor's length is independent of substrate thickness and capacitance value.

6.1.5.2 Two-Port MIM Capacitor Connection

Usually in monolithic ICs, the two port connections to MIM capacitor electrodes as shown in Figure 6.13(a) are on the opposite sides and have a colinear nature. The models described in the previous sections are valid for this assumption. Occasionally, due to electrical and physical requirements, the two port connections made as shown in Figure 6.13(b) are not colinear. In this case, as a first-order approximation, models based on a colinear assumption may be used for most applications. However, when one of the connecting ports moves perpendicular to the other one, as shown in Figure 6.13(c, d), the parasitic portion of the capacitor model is modified and its effect on the circuit performance becomes noticeable at higher frequencies. The effect is more pronounced when the two ports come closer to each other. Figure 6.14 shows the variation

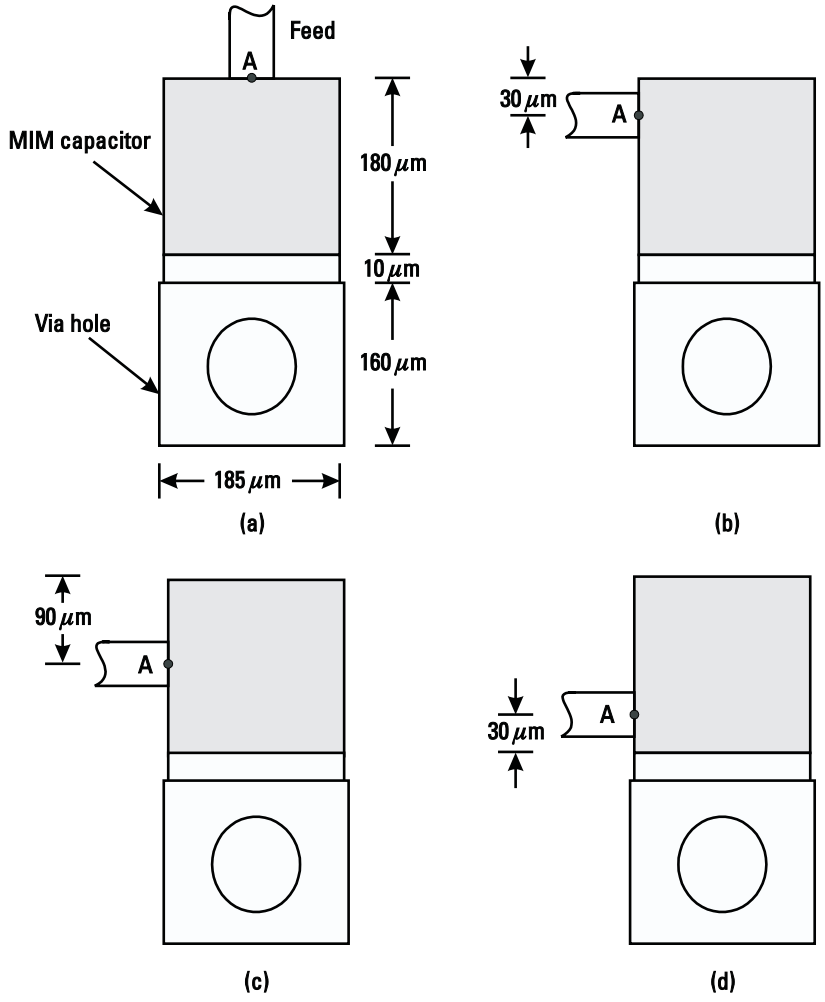


Figure 6.12 One-port connections of MIM capacitors: (a) in-line and (b–d) side-fed.

of S_{11} magnitude and S_{21} phase as a function of frequency for the four different 5-pF capacitor configurations shown in Figure 6.13. As ports 1 and 2 come closer, as expected, the electrical length becomes shorter and its effect on S_{11} magnitude is also more pronounced. The feed line width used in this case is 20 μm.

6.1.5.3 Three-Port MIM Capacitor Connection

When a capacitor is connected using three ports, the situation becomes more complex and the parasitic portion of the model is modified including three-port discontinuity effects, depending on the connecting lines. Figure 6.15 shows

Table 6.5
EM Simulated Phase Angle of S_{11} for Various Feed Configurations Connected to a 10-pF MIM Capacitor, with GaAs Substrate Thickness of 75 μm

Frequency (GHz)	Feed Configuration a	b	c	d
2	–168.8	–163.5	–162.7	–162.1
4	–174.8	–174.9	–173.8	–172.8
6	180.0	179.9	–178.5	–177.1
8	176.4	176.4	178.4	–179.7
10	173.3	173.4	175.9	178.2
12	170.6	170.7	173.8	176.5
14	168.1	168.1	171.7	175.0
16	165.6	165.7	169.8	173.5
18	163.2	163.3	167.9	172.2
20	160.8	160.9	166.1	170.8

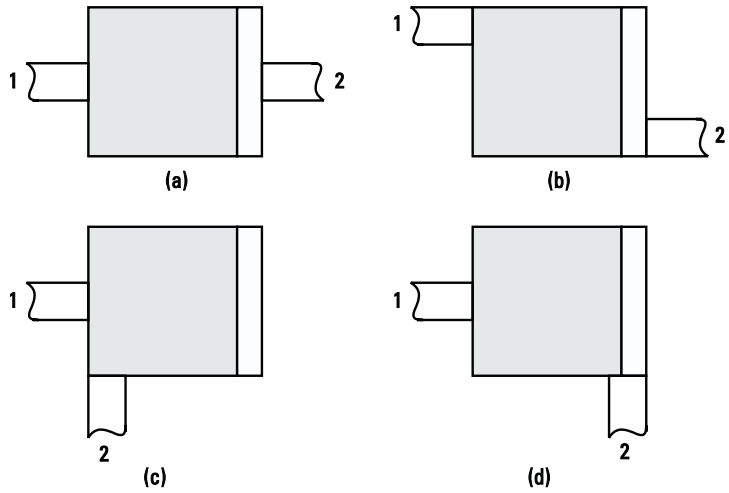


Figure 6.13 Two-port connections of MIM capacitors: (a) colinear, (b) offset linear, and (c, d) orthogonally fed.

four different configurations and their simulated phase for S_{21} and S_{31} is shown in Figure 6.16. Note that the phase of S_{31} is a strong function of the locations of ports 1 and 2.

6.2 High-Density Capacitors

RF and microwave circuits require high-value bypass capacitors to provide a very low impedance for RF signals and to suppress low-frequency instabilities

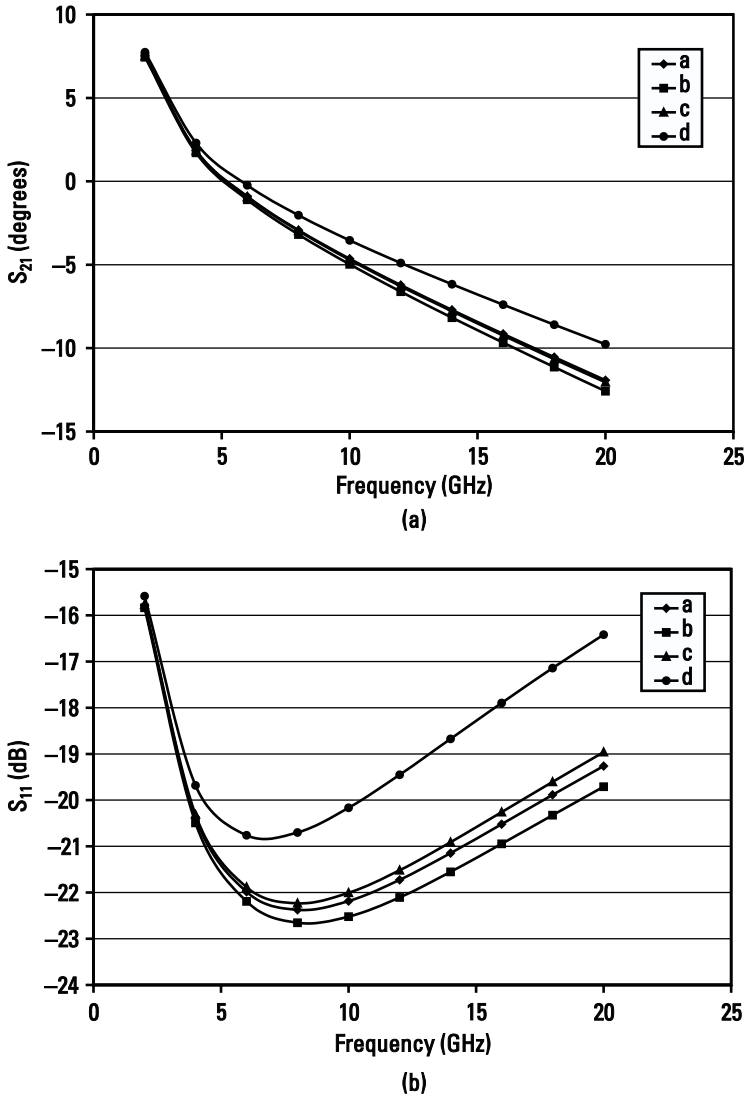


Figure 6.14 (a) Angle of S_{21} versus frequency for four 2-port connections and (b) magnitude of S_{11} versus frequency.

due to feedback or bias oscillations. On MMICs, it is not possible to utilize such capacitors because they occupy a large area due to the low value of dielectric constant of the commonly used silicon nitride (Si_3N_4) material. Such circuits are connected with external capacitors on a carrier or in a package, resulting in a higher parts count and an increase in the package size and assembly costs. To overcome these drawbacks and minimize the wire bond effects at higher

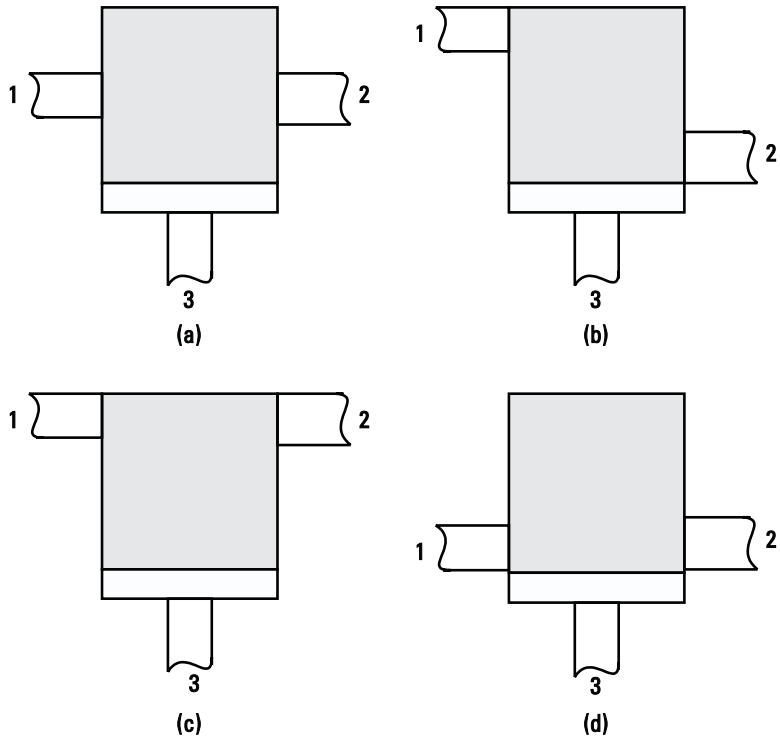


Figure 6.15 (a–d) Three-port connections of MIM capacitors.

frequencies, MIM capacitors fabricated with very high dielectric materials are required. This section deals with such materials as well as with other techniques used to increase many-fold the capacitance per unit area.

6.2.1 Multilayer Capacitors

A MIM capacitor's density can be increased by using a multiplate structure as discussed in the previous chapter. However, this configuration is not readily available in the monolithic form because the multilevel metal layers in the complex IC process are not available. A two-layer capacitor using *metal–insulator–metal–insulator–metal* (MIMIM) in the 0.18-μm Cu/SiO_2 interconnect CMOS IC technology has been developed [11]. Figure 6.17(a) shows the cross-sectional view of a MIMIM capacitor having length ℓ and width W. The capacitor dielectric film was 0.07-μm-thick Si_3N_4. The capacitance densities are 850 and 1,700 pF/mm^2 for MIM and MIMIM capacitors, respectively. Figure 6.17(b) shows a simplified EC model used for these capacitors on a Si substrate. Measured breakdown voltage values for MIM and MIMIM capacitors

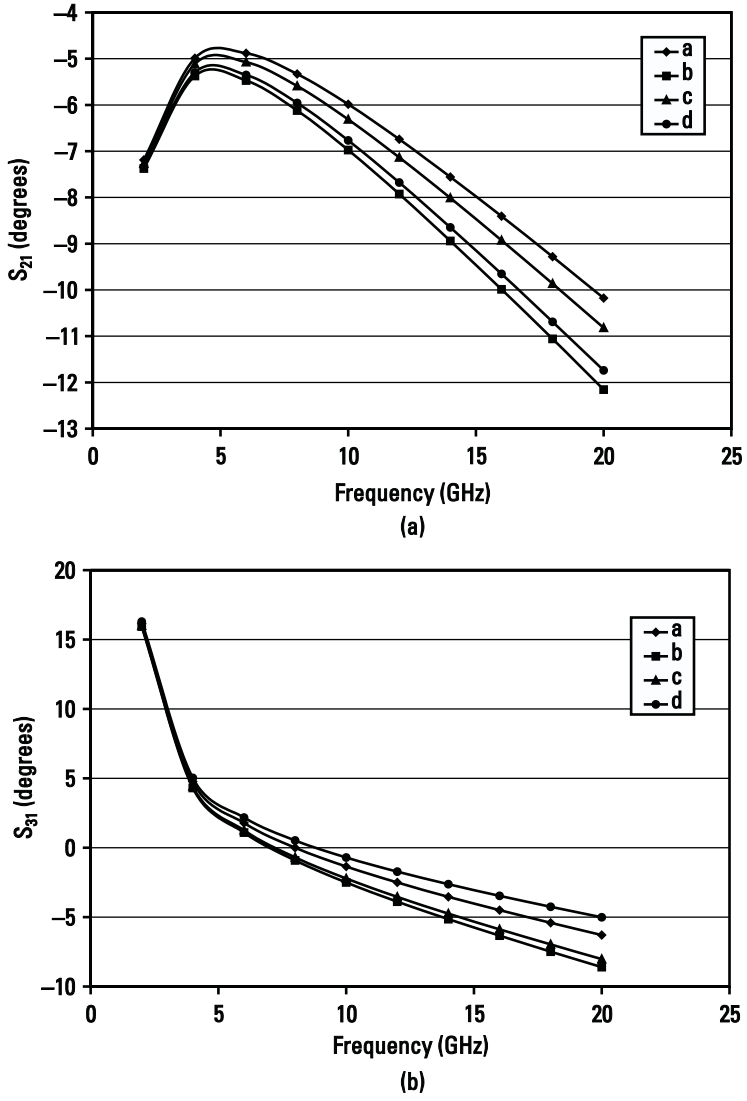


Figure 6.16 (a) Angle of S_{21} versus frequency for four 3-port connections and (b) angle of S_{31} versus frequency.

were almost the same and the values were greater than 40V for 10^4-μm^2 capacitor area and about 30V for a 10^5-μm^2 capacitor area. Table 6.6 compares EC model parameters for MIM and MIMIM capacitors with $W = 50$ μm and $\ell = 25$ μm. Figure 6.18 compares the series inductance of these capacitors when the capacitors aspect ratio $\ell / W = 0.5$. In this configuration the series inductance is lower because of the wider and shorter conductor used compared

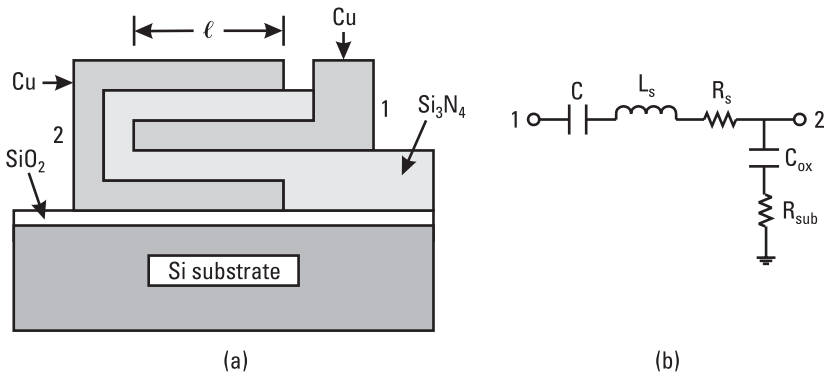


Figure 6.17 (a) Cross-sectional view of a MIMIM capacitor on Si substrate and (b) EC model for MIM and MIMIM capacitors.

Table 6.6
EC Model Parameters for MIM and MIMIC Capacitors with $25 \times 50\ \mu m^2$ Size on Si Substrate

	C (pF)	L_s (nH)	R_s (Ω)	C_{ox} (fF)	R_{sub} (kΩ)
MIM	1.02	0.128	0.61	7.01	4.50
MIMIM	1.91	0.124	0.36	8.49	4.03

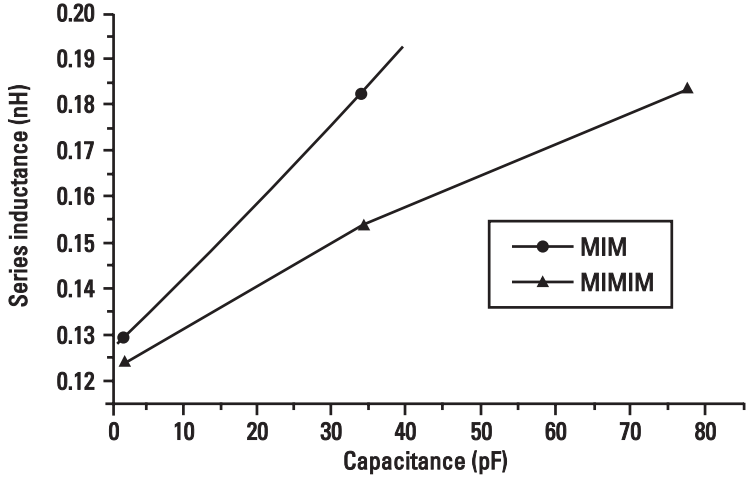


Figure 6.18 Series inductance versus capacitance value for MIM and MIMIM capacitors having $\ell/W = 0.5$.

to the conventional square geometry that gives rise to a higher resonant frequency. Figure 6.19 shows a MIM capacitor using four layers of metals in CMOS process.

6.2.2 Ultra-Thin-Film Capacitors

In general, MMIC capacitors use a 0.15- to 0.3-μm-thick layer of Si_3N_4, which gives a capacitance density of 400 to 200 pF/mm^2 and breakdown voltage in the range of 50 to 100V. The capacitance per unit area can be increased by either using ultra-thin films or employing high dielectric constant materials. Lee et al. [12] have reported increasing the capacitance density by using thinner layers of Si_3N_4. They obtained high-quality Si_3N_4 layers using a remote PECVD technique and achieved 0.02- to 0.1-μm-thick layers with dielectric breakdown voltage on the order of 3.5×10^2 V/μm. Since in several wireless applications, operating voltages are on the order of 3 to 4V, using 0.06-μm-thick Si_3N_4 is a viable approach to achieve a capacitance density of about 1,200 pF/mm^2. For such films, the achievable breakdown voltage is about 20V. Figure 6.20 shows the variation of capacitance density as a function of dielectric thickness. The capacitance density increases from 725 to about 3,000 pF/mm^2 by reducing the Si_3N_4 thickness from 0.1 to 0.02 μm, which corresponds to an increase of capacitance by a factor of 4.14 when the dielectric thickness is reduced by a factor of 5.

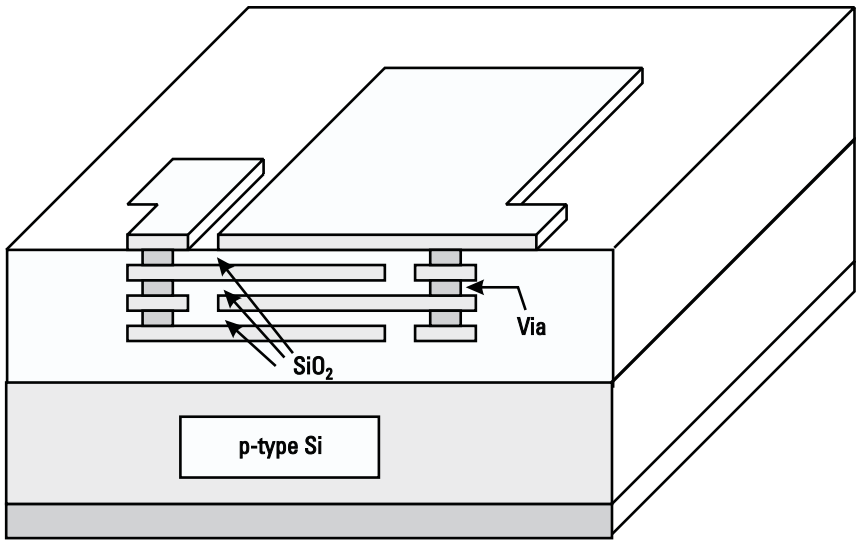


Figure 6.19 MIM capacitor using four layers of metal in CMOS technology.

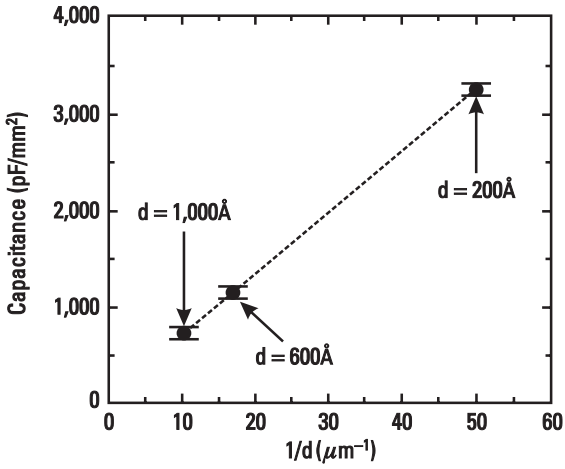


Figure 6.20 Capacitance density versus 1/dielectric thickness. (*From:* [12]. © 1999 IEEE. Reprinted with permission.)

6.2.3 High-K Capacitors

A higher value of capacitance per unit area can also be obtained by using a higher dielectric constant material, such as tantalum oxide (Ta_2O_5) [13–16]. Such capacitors can be realized either using anodized Ta anodes to make Ta_2O_5 thin film or using reactively sputtered Ta_2O_5 film. Anodized Ta_2O_5 capacitors have lower operating frequency and capacitance density than the sputtered Ta_2O_5 capacitors. Sputtered Ta_2O_5 capacitors with dielectric film thicknesses of 0.175 μm and capacitance values of 1,430 pF/mm^2 have been reported [13]. Measured insertion loss for a 29-pF capacitor was about 0.1 dB up to 9 GHz.

For MMICs, Ta_2O_5 is one of the most suitable materials because of its high dielectric constant ($\epsilon_{rd} \cong 25$) value. High quality and high-K thin films were developed by mixing very high-K titanium oxide (TiO_y) into tantalum oxide (TaO_x). A low-temperature deposition process using reactive pulsed dc magnetron sputtering was used to develop high-K composite and multilayered TaO_x-TiO_y materials for high-density capacitors [15]. Both materials have a dielectric constant value 70% to 100% greater than that of tantalum oxide. The multilayered structure consists of several alternating layers of the two dielectrics, with the thickness ratio and the total thickness of each pair being approximately 0.008 μm. In the composite material the percentage content of TiO_y is about 22%. Table 6.7 summarizes capacitor parameters for several high-K films.

6.2.4 Fractal Capacitors

Samavati et al. [17] demonstrated that the parallel plate capacitance density can be increased by using cross-connected fractal metal geometries, which use both

Table 6.7
MIM Capacitors Parameters for Several High-K Materials

Film Type	ϵ_{rd}	Thickness (μm)	Capacitance Density (nF/cm^2)	Leakage Current Density (μA/cm^2) at 0.5 MV/cm	Dielectric Strength (MV/cm)
TaO_x	22	0.2	97.3	0.005	5
TiO_x	67	0.2	296.2	10	0.9
TaO_x-TiO_y	38	0.2	168.0	1.2	2.3
TaO_x-TiO_y multilayered	44	0.2	194.5	0.034	2.3

parallel plate capacitance and lateral fringing field capacitance, similar to the interdigital structures discussed in the next chapter. Figure 6.21(a) shows a commonly used parallel plate capacitor and Figure 6.21(b) shows the top and bottom plates broken into cross-connected sections. When the lateral gap

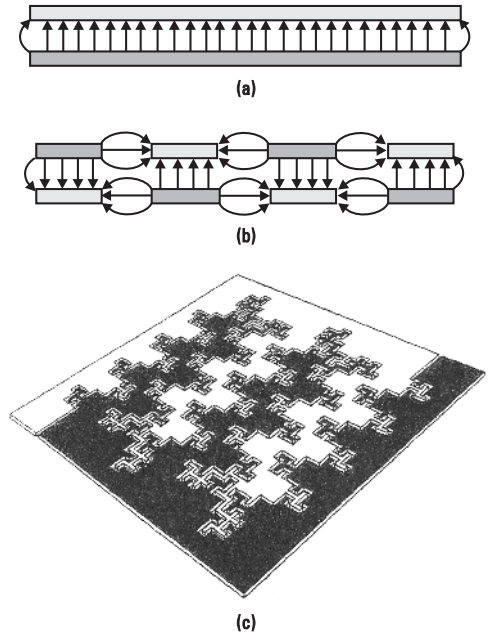


Figure 6.21 Field configurations in (a) a parallel plate capacitor and (b) cross-connected metal layers, and (c) a three-dimensional representation of a fractal capacitor. (*From:* [17]. © 1998 IEEE. Reprinted with permission.)

between the plates is very small, structure (b) results in higher capacitance due to both the vertical electric flux and lateral electric flux lines. If a parallel plate area is divided onto large fractals each having much larger perimeters than its equivalent square or rectangle geometries, the lateral fringing field capacitance can be increased significantly, resulting in a very large total capacitance. This can be achieved with the help of CAD tools. A simple example is an interdigital parallel plate capacitor. A major difference between the interdigital parallel plate and fractal capacitors is that the latter structure is of a random nature and supports random flow of current. Due to random flow of current in the fractal capacitors they have much lower series inductance as compared to interdigital capacitors. Figure 6.21(c) shows a three-dimensional representation of a fractal capacitor using a single metal layer. Samavati et al. [17] have demonstrated about 23 times the parallel capacitance of a fractal capacitor using 0.6-μm spacing between the cross-connected fractal geometries. Thus, fractal capacitors add one more degree of freedom to the design of parallel plate capacitors. This approach can also be used in multilevel geometries [18].

6.2.5 Ferroelectric Capacitors

High-value capacitors have also been realized using ferroelectric materials [19–23] with high dielectric constant values. The commonly used ferroelectric materials at RF and microwave frequencies are barium strontium titanate $Ba_{0.5}Sr_{0.5}TiO_3$ (BSTO) and strontium titanate $SrTiO_3$ (STO). Although, BSTO and STO materials do not contain iron, they are called ferroelectric because their permittivity is a function of the dc electric field, analogous to a ferromagnetic material's permeability dependency on the applied magnetic field. The dielectric constant value of a bulk BSTO ceramic material is about 1,000 and their maximum value occurs when no dc bias is applied. The dielectric constant value can be lowered by decreasing the barium content and increasing the oxide constant. In such materials, the dielectric constant value also depends on the operating temperature. Table 6.8 shows typical dielectric constant values for two compositions of BSTO materials at room temperature.

The temperature dependence of ϵ_{rd} and tan δ for single-crystal $SrTiO_3$ ferroelectric material has been reported by Krupka et al. [24] and is summarized in Table 6.9. Because these values are taken from graphs they are approximate. The expansion coefficient of the $SrTiO_3$ material is about 10 ppm/°C.

In thin-film technology, BSTO films are pulsed laser ablated on a magnesium oxide (MgO) substrate ($\epsilon_r \cong 9.7$). A general chemical formula for BSTO is $Ba_x Sr_{1-x} TiO_3$, where the Curie temperature is adjusted for a specific operating temperature by adjusting the value of x. Around the Curie temperature, the value of ϵ_{rd} is constant over a narrow temperature range. The value of x is about 0.5 to 0.6 for a Curie temperature of 25°C.

Table 6.8
Dielectric Constant and Loss Tangent of BSTO Materials at Room Temperature

	Material			
	$Ba_{0.5}Sr_{0.5}TiO_3$		$Ba_{0.2}Sr_{0.8}TiO_3$	
Frequency (GHz)	**Dielectric Constant**	**Loss Tangent**	**Dielectric Constant**	**Loss Tangent**
12.4	1,288	0.115	356	0.014
13.0	1,345	0.099	351	0.030
14.0	1,266	0.062	335	0.025
15.0	1,222	0.082	335	0.021
16.0	1,333	0.082	336	0.012
17.0	1,306	0.057	349	0.008
18.0	1,229	0.044	358	0.014

Table 6.9
Dielectric Constant and Loss Tangent of Single-Crystal $SrTiO_3$ Material at Various Temperatures

Temperature (°C)	ϵ_{rd}	$\tan \delta \times 10^{-4}$
−50	438	4.1
−25	380	4.5
0	350	4.8
+25	320	5.2

In BSTO or simply BST capacitors, dielectric thin films are also formed using a sol-gel technique [21]. The bottom plate electrode is of Ti/Pt while the top plate metal is Pt. The thickness and dielectric constant of the BST film are 0.25 μm and 300, respectively. The frequency dependence of a 100-pF BST capacitor is shown in Figure 6.22(a), whereas Figure 6.22(b) shows the temperature dependence of the capacitor. The frequency roll-off point is about 2 GHz, and the temperature coefficient is about 500 ppm/°C.

Data for the sputtered $SrTiO_3$ thin-film capacitors were also reported [20]. The dielectric constant value was about 100 and the dielectric film thickness was about 0.3 μm. The measured breakdown voltage was about 30V. Figure 6.23 shows the measured capacitance and insertion loss for various capacitor area values as a function of frequency. The measured insertion loss for 10-pF or higher values at 2 GHz was less than 0.05 dB.

Another $SrTiO_3$ film capacitor with a dielectric constant of 180 and having a frequency of operation up to 20 GHz was reported by Nishimura et al. [22].

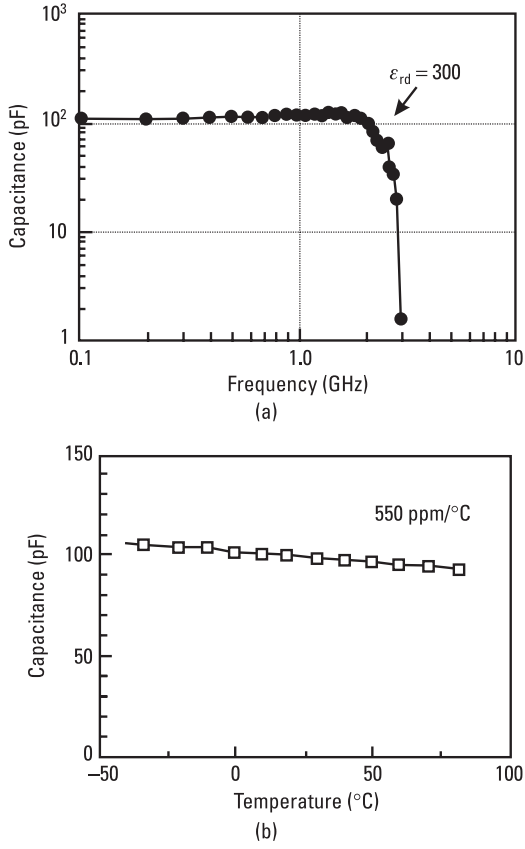


Figure 6.22 BST capacitor: (a) capacitance versus frequency and (b) capacitance versus temperature. (*From:* [21]. © 1995 IEEE. Reprinted with permission.)

Figure 6.24 shows the I-V characteristics for a capacitor having $50 \times 50\ \mu m^2$ area. The breakdown voltage defined by 10 mA/cm^2 leakage current was more than 50V for a 0.2-μm-thick $SrTiO_3$ film. The calculated capacitance value is almost 8,000 pF/mm^2. We use a parallel plate capacitance that is given by capacitance/mm^2 = $8.854 \times 10^{-3}\ \epsilon_{rd}/d$ pF/mm^2, where area and d are in square millimeters and millimeters, respectively, and the area reduction for various dielectric constant value is given in Table 6.10.

6.3 Capacitor Shapes

Among various possible MIM capacitor shapes, rectangular, circular, and octagonal geometries are used, but the rectangular geometry is the most popular. These are briefly discussed next.

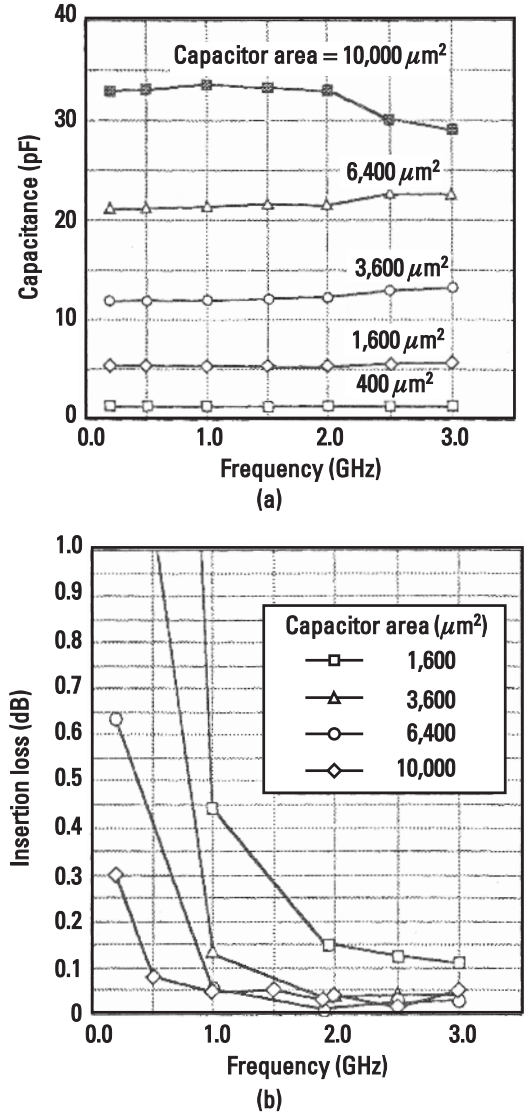


Figure 6.23 $SrTiO_3$ MIM capacitor: (a) capacitance versus frequency and (b) insertion loss versus frequency for several capacitor areas. (*From:* [20]. © 1993 IEEE. Reprinted with permission.)

6.3.1 Rectangular Capacitors

The rectangular shape is the most popular because its layout is easy to draw, area calculations are simple, and connections are straightforward. One of the major problems with this geometry is the higher ESD failure due to sharp

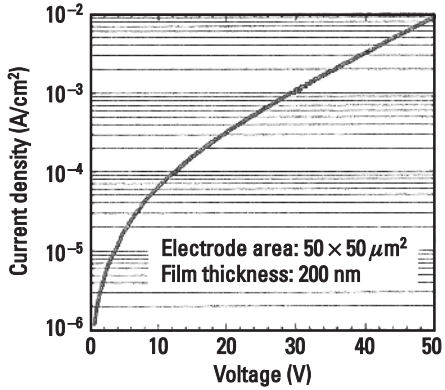


Figure 6.24 I-V data for STO capacitor having dielectric film thickness of 0.2 μm. (*From:* [22]. © 1997 IEEE. Reprinted with permission.)

Table 6.10
Area Reduction for MIM Capacitors for STO Dielectric Materials

ϵ_{rd}	d (mm) $\times 10^{-3}$	Capacitance/mm^2	Area for 100 pF (mm^2)	Area Reduction Factor
6.77	0.20	300	0.3333	1
108	0.30	3,200	0.0313	10.7
300	0.25	10,625	0.0094	37.5

corners. Noncolinear connections have higher discontinuity reactances at higher microwave frequencies, as discussed in Section 6.1.5.

6.3.2 Circular Capacitors

Circular capacitors are seldom used due to the higher complexity of their layout and their connections to other circuitry, especially wide lines. Because such configurations do not have sharp corners, ESD failures are lower compared to other geometries.

6.3.3 Octagonal Capacitors

When MIM capacitors are used in MMICs, generally two or more connections are made between the capacitors and other circuitry. Flexibility and compactness of the circuit layout mandate these connections to be made anywhere along the periphery of the capacitors. In such situations, any connection made off the straight path (noncolinear) at defined ports or connections made at right

angles add extra reactances due to discontinuities in the current path in the circuit, which in turn degrade the MMIC performance. An octagonal MIM capacitor (Figure 6.25) structure for MMIC applications has the flexibility of multiport connections with minimum added discontinuity reactances [25], and also has much lower ESD failure due to tapered corners.

Advantages of this structure as compared to rectangular or square capacitors are as follows:

1. Chamfered corners reduce step discontinuity reactance between the feed line and the capacitor, which improves frequency performance of the MMICs.
2. Reduced bend discontinuity reactance for noncolinear feed points also improves frequency performance of the MMICs.
3. Provides more than four ports (eight total) for interconnections. When ICs require more than four ports for matching networks, it provides an ideal situation with reduced discontinuity reactances.

This structure in general has better performance at millimeter-wave frequencies compared to conventional rectangular-shaped capacitors. We simulated and tested several capacitor structures as shown in Figure 6.26 using 125-μm-thick GaAs substrate. The TRL calibration technique was used to accurately de-embed the components performance by measuring the S-parameters. Figure 6.27 compares the simulated reflection coefficients (S_{11} or return loss in decibels) for the square-sided and octagonal-sided capacitors in straight and bend feed configurations. The results were obtained using a very accurate electromagnetic simulator. Lower values of S_{11} for similar feed illustrate the improvement in the performance. Similar performance trends are shown in Figure 6.27 for the measured data.

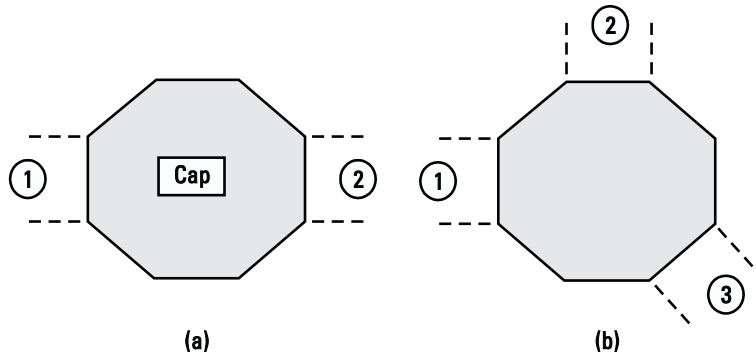


Figure 6.25 (a, b) Octagonal MIM capacitor showing flexibility in multiport connections.

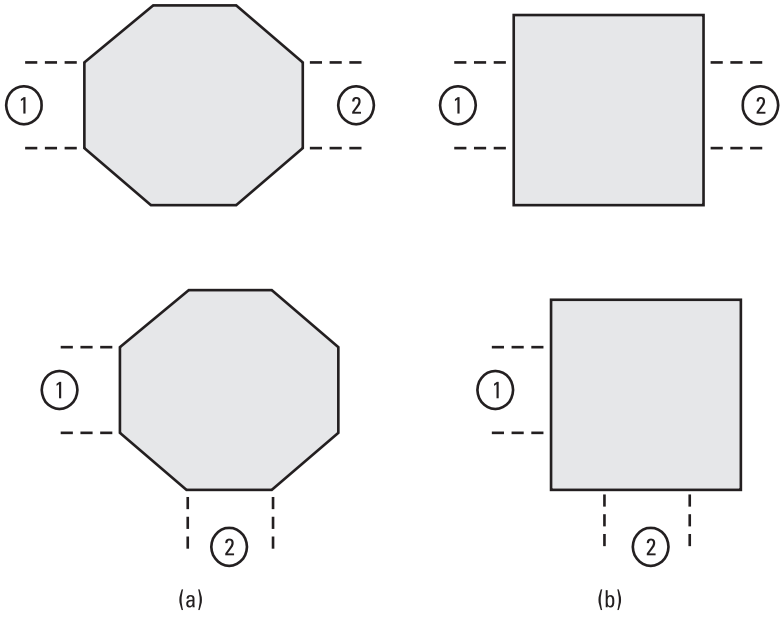


Figure 6.26 (a) Octagonal-sided MIM capacitor with two feed configurations—colinear and perpendicular, and (b) square-sided MIM capacitor with two feed configurations–colinear and perpendicular.

6.4 Design Considerations

In this section we describe several techniques to enhance the quality factor of capacitors, tunability of capacitors, and power-handling capability of capacitors.

6.4.1 *Q*-Enhancement Techniques

Several techniques to improve the *Q*-factor of MIM capacitors have been used, including thicker and high conductivity metal 1, increasing the aspect ratio (width is greater than length), and micromachining. These are briefly discussed in the following sections.

6.4.1.1 Thicker and High Conductivity Metal 1

In MIM capacitors, the bottom metal known as metal 1 is thin, and in Si technologies, it has low conductivity. The quality factor of MIM capacitors can be enhanced by using thicker and higher conductivity metal 1, as discussed in Chapter 3 (Section 3.2).

6.4.1.2 Aspect Ratio

The resistance of the bottom plate (metal 1) can be reduced by increasing the thickness and reducing the aspect ratio of the conductor and by using a higher

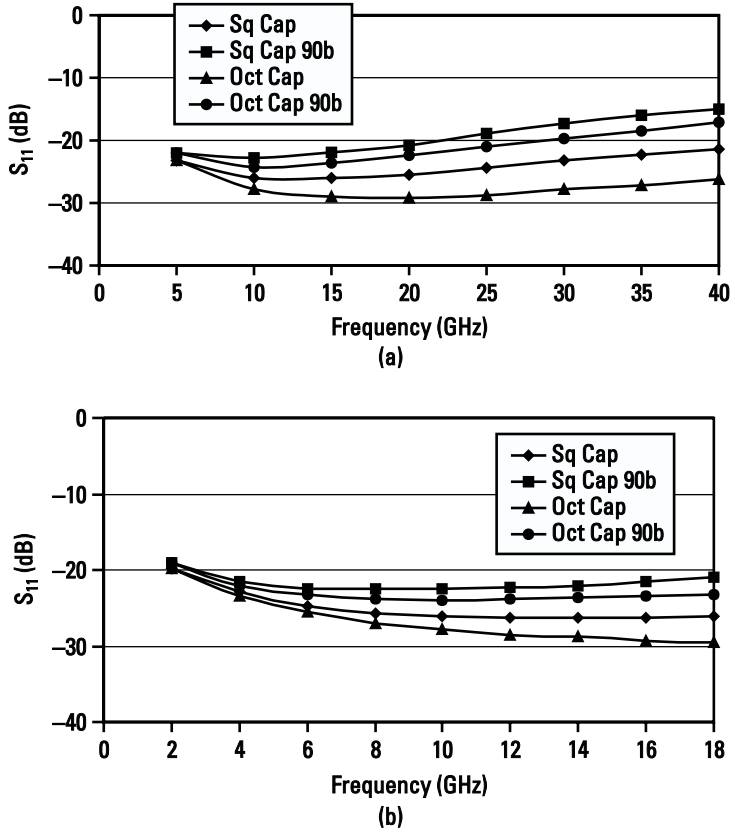


Figure 6.27 Simulated and measured S_{11} of square and octagonal capacitors having collinear and perpendicular feed: (a) simulated and (b) measured.

conductivity material. For standard fabrication processes, a conductor's thickness and conductivity cannot be changed; however, the capacitor's aspect ratio is at the designer's disposal. For example, for a given capacitance value, $W = 2l$, Figure 6.28 lowers the dc resistance by a factor of 2, compared to the conventional square geometry, and also reduces the parasitic inductance and increases the series resonance frequency. The aspect ratio (l/W) of a capacitor can be decreased up to a point so that transverse effects (discontinuity and resonance) are negligible. Figure 6.28 shows the calculated value of Q for a 5-pF capacitor having three different aspect ratios.

6.4.1.3 Micromachined MIM Capacitors on Si

The Q of MIM capacitors on Si substrate is drastically improved using micromachining techniques [26–28], in which the parasitic substrate loss is reduced by removing Si below the bottom plate of a capacitor. A photograph of a MIM

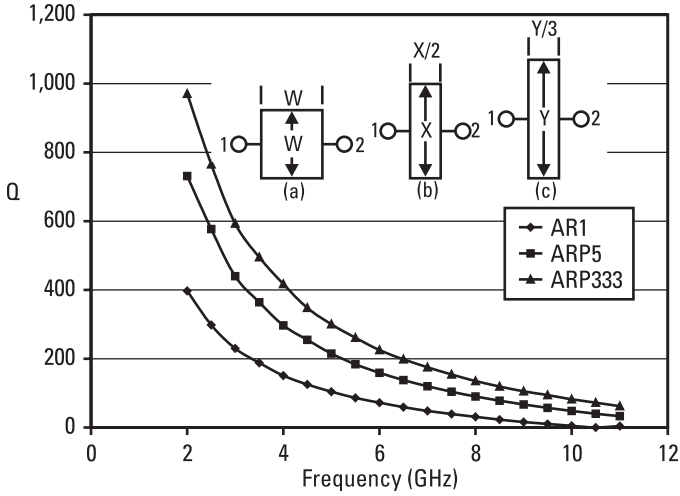
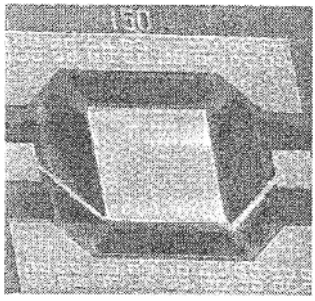
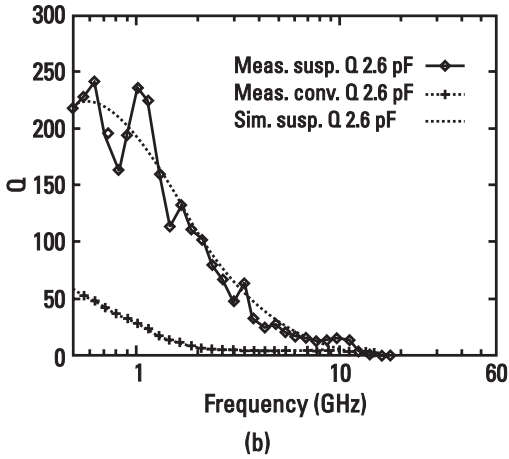


Figure 6.28 Q-factor of a MIM capacitor for three aspect ratios: 1, 0.5, and 0.333.

capacitor on a suspended membrane is shown in Figure 6.29(a). The capacitors were realized by sandwiching Al_2O_3 (ϵ_{rd} = 9.9) between a 1.4-μm-thick metal 2 and 0.6-μm-thick metal 1. The p-type Si substrate has a resistivity value of 3.5 Ω-cm and the etch depth is about 100 μm. Measured and simulated Q-factor values for 2.6-pF capacitors fabricated directly on Si and on suspended SiN membrane are compared in Figure 6.29(b). The measured Q-value of a



(a)



(b)

Figure 6.29 (a) Photograph of a suspended MIM capacitor fabricated using Si technology and (b) comparison of measured and simulated Q-values of conventional and suspended MIM capacitors. (*From:* [27]. © 1996 IEEE. Reprinted with permission.)

suspended capacitor was greater than 100 at 2 GHz compared to less than 10 for the capacitor directly on Si substrate. The measured series resonance frequency was 15.9 GHz.

6.4.2 Tunable Capacitor

The voltage dependence of the dielectric constant of ferroelectric materials allows one to make variable voltage capacitors. Compared to varactor diodes, they have low voltage tunability, no junction noise, high speed, low cost, and are easily integrated with MMICs. Such components have applications in tunable filters, phase shifters, VCOs, and so on. The major disadvantage of such components lies in the fact that their operation is nonlinear and the capacitance tunability decreases with increasing signal power level [29].

Parallel plate capacitors were fabricated on Si substrates using 0.05-μm-thick $Ba_{0.7}Sr_{0.3}TiO_3$. The ferreolectric layer was grown using a *metalorganic chemical vapor deposition* (MOCVD) technique. The measured value of capacitance for a 50- × 50-μm^2 capacitor was 65 pF at 0V dc bias. The variation of ϵ_{rd} versus dc bias using this capacitor is shown in Figure 6.30. The relative permittivity value was found to be constant over 45 to 500 MHz. The loss tangent value at 500 MHz was about 0.009 and the breakdown voltage was about 8V.

6.4.3 Maximum Power Handling

The power handling of MIM capacitors can be treated similar to that for chip capacitors as discussed in the previous chapter.

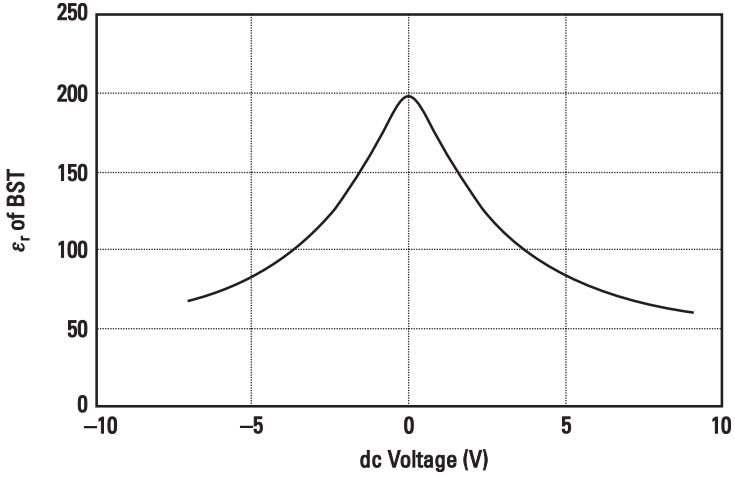


Figure 6.30 Variation of ϵ_r versus dc bias of a BST material. (*From:* [29]. © 2002 IEEE. Reprinted with permission.)

6.4.3.1 Maximum RF Current Rating

The maximum RF current limits due to breakdown voltage and power dissipation in a MIM capacitor are given by (5.34) and (5.35) in Chapter 5. If the breakdown voltage is much larger than the dc applied voltage, (5.34) becomes

$$I_{mv} = \frac{V_B \omega C}{\sqrt{2}} \tag{6.23}$$

Thus, the maximum current is proportional to V_B, operating frequency, and capacitance C. For a capacitor operating at 2 GHz, and with a breakdown voltage of 50V,

$$I_{mv} = 0.444C \tag{6.24}$$

where I_{mv} is in amperes and C is in picofarads. For ferroelectric and high-density capacitors, when the breakdown voltage is low, the current rating of MIM capacitors can be increased by connecting more capacitors in series. For example, when two capacitors of double capacitance value are used in series as shown in Figure 6.31, the current rating is increased by more than four times. Here for RF design, $C_1 = 2C$ and the breakdown voltage across a series combination of two capacitors is doubled. Equation (6.24) then becomes

$$I_{mv} = 1.776C \tag{6.25}$$

6.4.3.2 Maximum RF Voltage Rating

The maximum RF voltage rating of a capacitor can be calculated by referring to Figure 6.32. If V_a is the dc applied voltage and P_o is the output power across the load, the maximum voltage (rms) across C is given by

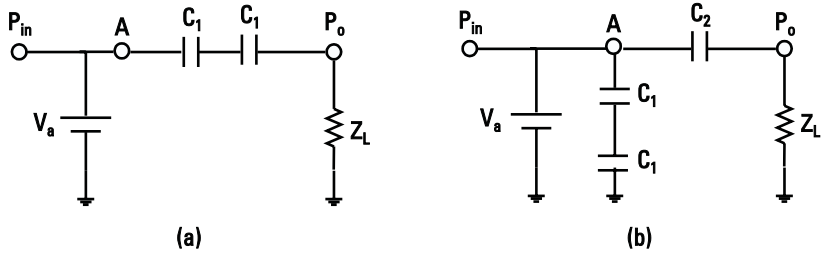


Figure 6.31 Series connections of MIM capacitors to improve current ratings: (a) two-series capacitors in series configuration and (b) two-series capacitors in shunt configuration.

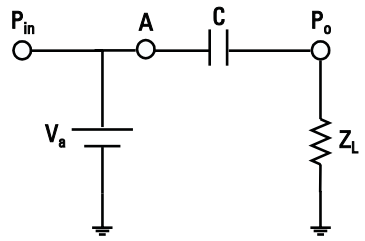


Figure 6.32 Series configuration of a dc block MIM capacitor at the output of an amplifier.

$$V_{mc} = V_a + \sqrt{P_o R_L} \tag{6.26}$$

which should be less than V_B. If $V_{mc} > V_B$, the maximum working voltage of the capacitor can be increased by connecting more capacitors in series as shown in Figure 6.31(a). Equation (6.26) does not include any voltage standing wave effects as discussed in Chapter 14.

6.4.3.3 Maximum Power Dissipation

The maximum current rating of a capacitor is also determined from the maximum allowed power dissipation to maintain the capacitor's temperature below the rated value, for example, 150°C for a monolithic MIM capacitor on GaAs substrate. If P_{diss} is the maximum allowed power dissipation, the maximum current is given by

$$I_{mp} = \sqrt{\frac{P_{\text{diss}}}{\text{ESR}}} \tag{6.27}$$

where ESR is the effective series resistance of the capacitor. The maximum allowed power dissipation is calculated in the following.

The calculation of thermal resistance for a MIM capacitor is based on vertical heat flow as shown in Figure 6.33. Consider the RF power to be dissipated in both top and bottom conductors having the surface resistance of R_{ST} and R_{SB}. Assuming the MIM capacitor as a square structure and ignoring dielectric losses, the temperature rise is given by

$$\Delta T = P_{DCT} R_{\text{THC}} + (P_{DCT} + P_{DCB}) R_{\text{THG}} \tag{6.28}$$

where P_{DCT} and P_{DCB} are the power dissipated in the top and bottom plates and R_{THC} and R_{THG} are the thermal resistances of the capacitor and GaAs substrate. Assuming a 45° heat spreading rule for the bottom conductor only and a capacitor dielectric of Si_3N_4 of thickness d,

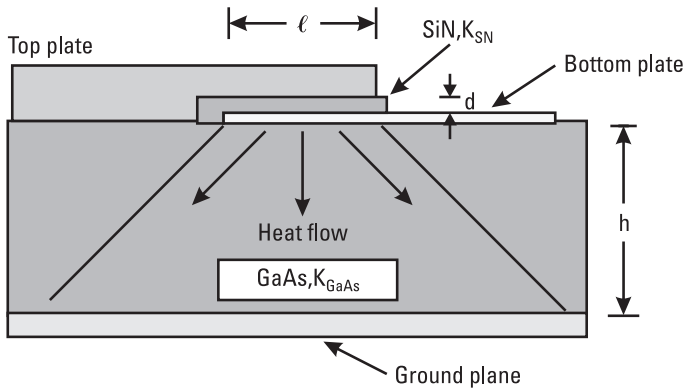


Figure 6.33 Heat flow schematic of a MIM capacitor.

$$\Delta T = I^2 \left[R_{ST} \frac{d}{K_{\text{SN}} \ell W} + (R_{ST} + R_{SB}) \frac{h}{K_{\text{GaAs}} \ell (W + 2h)} \right] \quad (6.29)$$

where K_{SN} and K_{GaAs} are the thermal conductivities of the Si_3N_4 and GaAs, respectively. Table 6.11 lists the maximum power dissipation and I_{mp} for various capacitor values. The parameters used in the calculations are as follows:

$$\ell = W = 0.5774 \times 10^{-2} \sqrt{C} \text{ cm}$$

$$d = 0.2\ \mu\text{m},\ h = 75\ \mu\text{m}$$

$$K_{SN} = 0.1 \text{ W/cm} \cdot {}^\circ\text{C and } K_{\text{GaAs}} = 0.294 \text{ W/cm} \cdot {}^\circ\text{C at } 150^\circ\text{C}$$

Table 6.11
Calculated Maximum Power Dissipation and I_{mp} for MIM Capacitors on 75-μm-Thick GaAs Substrate

C (pF)	P_{diss} (max) (W)	I_{mp} (A)
0.5	0.27	1.44
1.0	0.44	1.84
2.0	0.71	2.34
5.0	1.43	3.32
10.0	2.50	4.38
20.0	4.48	5.87
50.0	10.07	8.80

$$T_m = 150°C,\ T_a = 25°C,\ \Delta T = 125°C$$

$$R_{ST} = 0.007\Omega,\ R_{SB} = 0.07\Omega$$

and

$$\text{ESR} = 0.13\Omega$$

References

[1] Gupta, K. C., et al., *Microstrip Lines and Slotlines,* 2nd ed., Norwood, MA: Artech House, 1996, Chap. 3.

[2] Mondal, J. P., "An Experimental Verification of a Simple Distributed Model of MIM Capacitors for MMIC Applications," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-35, April 1987, pp. 403–407.

[3] Pettenpaul, E., et al., "CAD Models of Lumped Elements on GaAs Up to 18 GHz," *IEEE Trans. Microwave Theory Tech.,* Vol. 36, February 1988, pp. 294–304.

[4] Sadhir, V. K., and I. J. Bahl, "An Accurate Distributed Model for MIM Capacitors," *Microwave Optical Tech. Lett.,* Vol. 4, May 1991, pp. 219–222.

[5] Sadhir, V. K., I. J. Bahl, and D. A. Willems, "CAD Compatible Accurate Models of Microwave Passive Lumped Elements for MMIC Applications," *Int. J. Microwave and Millimeter-Wave Computer-Aided Engineering,* Vol. 4, April 1994, pp. 148–162.

[6] Tripathi, V. K., "Asymmetric Coupled Transmission Lines in an Inhomogeneous Medium," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-23, September 1975, pp. 734–739.

[7] Garg, R., and I. J. Bahl, "Characteristics of Coupled Microstrip Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-27, July 1979, pp. 700–705.

[8] Gupta, K. C., et al., *Microstrip Lines and Slotlines,* 2nd ed., Norwood, MA: Artech House, 1996, pp. 491–495.

[9] Xiong, X. Z., and V. F. Fusco, "A Comparison Study of EM and Physical Equivalent Circuit Modeling for MIM CMOS Capacitors," *Microwave Optical Tech. Lett.,* Vol. 34, August 2002, pp. 177–181.

[10] EM Sonnet Software, Liverpool, NY.

[11] Zhen, C., et al., "A Study of MIMIM On-Chip Capacitor Using Cu/SiO_2 Interconnect Technology," *IEEE Microwave Wireless Components Lett.,* Vol. 12, July 2002, pp. 246–248.

[12] Lee, J. H., et al., "DC and RF Characteristics of Advanced MIM Capacitors for MMICs Using Ultra-Thin Remote—PECVD Si_3N_4, Dielectric Layers," *IEEE Microwave and Guided Wave Lett.,* Vol. 9, September 1999, pp. 345–347.

[13] Chu, A., et al., "A Two-Stage Monolithic IF Amplifier Utilizing a Ta_2O_5 Capacitor," *IEEE Trans. Microwave Theory Tech.,* Vol. 31, January 1983, pp. 21–25.

[14] Kambe, R., et al., "MCM Substrate with High Capacitance," *IEEE Trans. Components, Packaging and Manufacturing Tech.—Part B,* Vol. 18, February 1995, pp. 23–27.

[15] Nielsen, M. C., et al., "Composite and Multilayered TaO_x-TiO_y High Dielectric Constant Thin Films," *IEEE Trans. Components, Packaging, Manufacturing Tech.—Part B,* Vol. 21, August 1998, pp. 274–280.

[16] Kim, J. Y., et al., "High Frequency Response of Amorphous Tantalum Oxide Thin Films," *IEEE Trans. Components Packaging Tech.,* Vol. 24, September 2001, pp. 526–533.

[17] Samavati, H., et al., "Fractal Capacitors," *IEEE J. Solid-State Circuits,* Vol. 33, December 1998, pp. 2034–2041.

[18] Aparicio, R., and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors," *IEEE J. Solid-State Circuits,* Vol. 37, March 2002, pp. 384–393.

[19] Varadan, V. K., et al., "Ceramic Phase Shifters for Electronically Steerable Antenna Systems," *Microwave J.,* Vol. 35, January 1992, pp. 116–127.

[20] Nishitsuji, M., et al., "Advanced GaAs–MMIC Process Technology Using High-Dielectric Constant Thin Film Capacitors by Low-Temperature RF Sputtering Method," *IEEE GaAs IC Symp. Dig.,* 1993, pp. 329–332.

[21] Koizumi, H., et al., "A GaAs MMIC Chip-Set for Mobile Communications Using On-Chip Ferroelectric Capacitors," *IEEE J. Solid-State Circuits,* Vol. 31, June 1995, pp. 835–840.

[22] Nishimura, T. B., et al., "Single 2.2V Operation MMIC Power Amplifier Utilizing $SrTiO_3$ Capacitors for 2.4 GHz Wireless Communication Systems," *IEEE Radio Engineering Integrated Circuits Symp. Dig.,* 1997, pp. 37–40.

[23] Patel, D. P., J. M. Pond, and J. B. L. Rao, "Microwave Ferroelectric Devices," *Wiley Encyclopedia of Electrical and Electronic Engineering,* Vol. 13, New York: John Wiley, 1999.

[24] Krupka, J., et al., "Dielectric Properties of Single Crystals of Al_2O_3, $LaAlO_3$, $NdGaO_3$, $SrTiO_3$, and MgO at Cryogenic Temperatures," *IEEE Trans. Microwave Theory Tech.,* Vol. 42, October 1994, pp. 1886–1889.

[25] Bahl, I. J., "Multiple Port Thin Film Capacitor," U.S. Patent 5,338,950, August 16, 1994.

[26] Chi, C.-Y., and G. M. Rebeiz, "Planar Microwave and Millimeter-Wave Lumped Elements and Coupled-Line Filters Using Micro-Machining Techniques," *IEEE Trans. Microwave Theory Tech.,* Vol. 43, April 1995, pp. 730–738.

[27] Sun, Y., et al., "Suspended Membrane Inductors and Capacitors for Application in Silicon MMICs," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.,* 1996, pp. 99–102.

[28] Sun, Y., et al., "Micromachined RF Passive Components and Their Applications in MMICs," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 9, July 1999, pp. 310–325.

[29] Tombak, A., et al., "Tunable Barium Strontium Titanate Thin Film Capacitors for RF and Microwave Applications," *IEEE Microwave Wireless Components Lett.,* Vol. 12, January 2002, pp. 3–5.

7

Interdigital Capacitors

In addition to overlay-type capacitors as describes in Chapters 5 and 6, interdigital or interdigitated capacitors can be used as lumped circuit elements in microwave circuits, especially at higher microwave frequencies. The quality factor for such a capacitor is higher than that for overlay capacitors and they are much larger in size. The maximum capacitance per inch area of interdigital capacitors is less than 1% of that of the overlay type and therefore is not available in chip form.

The interdigital capacitor is a multifinger periodic structure as shown in Figure 7.1. Interdigital capacitors use the capacitance that occurs across a narrow gap between thin-film conductors. These gaps are essentially very long and folded to use a small amount of area. As illustrated in Figure 7.1, the gap meanders back and forth in a rectangular area forming two sets of fingers that are interdigital. By using a long gap in a small area, compact single-layer small-value capacitors can be realized. Typically, values range from 0.05 to about 0.5 pF. The capacitance can be increased by increasing the number of fingers, or by using a thin layer of high dielectric constant material such as a ferroelectric between the conductors and the substrate, or by using an overlay high-K dielectric layer, which also acts as a protective shield.

One of the important design considerations is to keep the size of the capacitor very small relative to a wavelength so that it can be treated as a lumped element. A larger total width-to-length ratio results in the desired higher shunt capacitance and lower series inductance. This type of capacitor can be fabricated by the hybrid technology used in the fabrication of conventional IC or MMIC technology and does not require any additional processing steps. This chapter describes the design and modeling of interdigital capacitors.

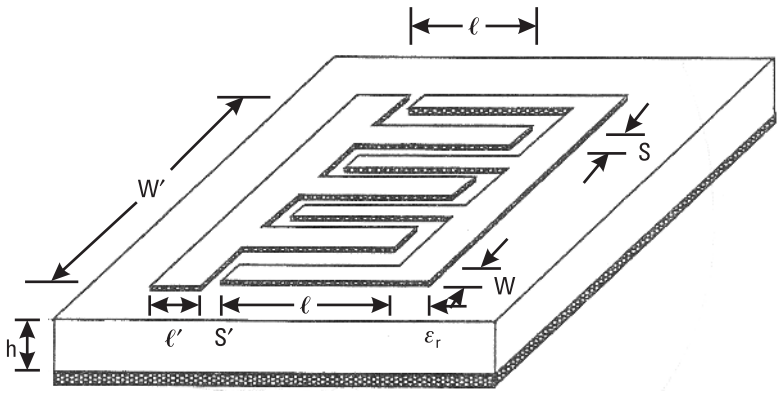


Figure 7.1 An interdigital capacitor configuration.

7.1 Interdigital Capacitor Models

Several methods have been used to characterize interdigital capacitors, including approximate analysis, *J*-inverter network equivalent representation, full-wave methods, and measurement-based models. These techniques are discussed next.

7.1.1 Approximate Analysis

Analysis and characterization of interdigital capacitors have been reported in the literature [1–8]. Data from earlier analyses [1–3], when compared with measured results, showed that these analyses were inadequate to describe capacitors accurately. The analyses were based on lossless microstrip coupled lines [1] and lossy coupled microstrip lines [2]. A more accurate characterization of these capacitors can be performed if the capacitor geometry is divided into basic microstrip sections such as the single microstrip line, coupled microstrip lines, open-end discontinuity, unsymmetrical gap, 90° bend, and T-junction discontinuities [5] as shown in Figure 7.2. This model provides better accuracy than the previously reported analyses. However, this method still provides an approximate solution, due to several assumptions in the grouping of subsections and does not include interaction effects between the basic microstrip sections described above. Figure 7.3 shows a simple EC model used to describe the characteristics of the interdigital capacitors shown in Figure 7.1. An approximate expression for the interdigital capacitance is given by [1]

$$C = \frac{\epsilon_r + 1}{W'} \ell \left[(N - 3) A_1 + A_2 \right] \tag{7.1}$$

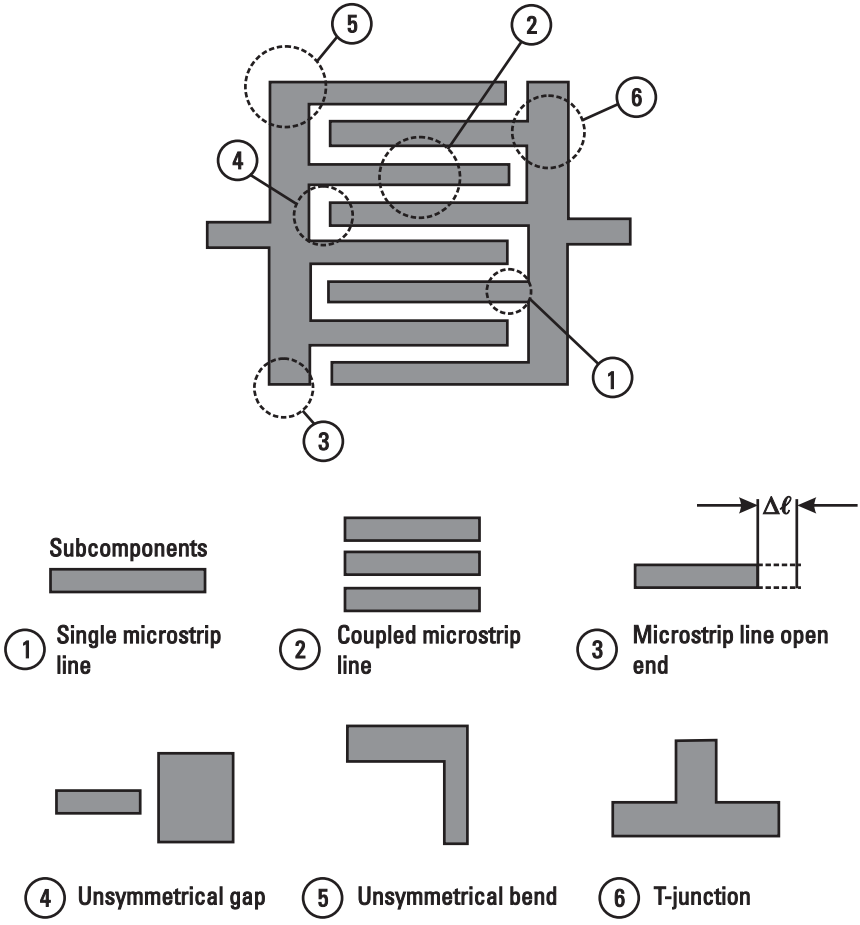


Figure 7.2 The interdigitated capacitor and its subcomponents.

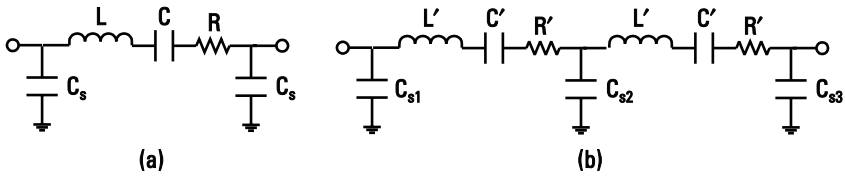


Figure 7.3 Lumped-element EC models of the interdigital capacitor: (a) low frequency and (b) high frequency.

where C is the capacitance per unit length along W', A_1 (the interior) and A_2 (the two exterior) are the capacitances per unit length of the fingers, N is the number of fingers, and the dimensions W' and ℓ are shown in Figure 7.1 and expressed in microns. For infinite substrate thickness (or no ground plane), $A_1 = 4.409 \times 10^{-6}$ pF/μm and $A_2 = 9.92 \times 10^{-6}$ pF/μm. The total capacitance of an interdigital structure of length ℓ is expressed as

$$C = (\epsilon_r + 1)\,\ell\,[(N-3)A_1 + A_2] \quad \text{(pF)} \tag{7.2}$$

For a finite substrate, the effect of h must be included in A_1 and A_2. In the final design, usually $S = W$ and $\ell \leq \lambda/4$. Approximate expressions for A_1 and A_2 are obtained by curve fitting the data given in [1]. These expressions are as follows:

$$A_1 = 4.409 \tanh\left[0.55\left(\frac{h}{W}\right)^{0.45}\right] \times 10^{-6} \quad (\text{pF}/\mu\text{m}) \tag{7.3a}$$

$$A_2 = 9.92 \tanh\left[0.52\left(\frac{h}{W}\right)^{0.5}\right] \times 10^{-6} \quad (\text{pF}/\mu\text{m}) \tag{7.3b}$$

The series resistance of the interdigital capacitor is given by

$$R = \frac{4}{3}\frac{\ell}{WN}R_s \tag{7.4}$$

where R_s is the sheet resistivity in ohms per square of the conductors used in the capacitors.

The effect of metal thickness t plays a secondary role in the calculation of capacitance. The Q of this capacitor is given by

$$Q_c = \frac{1}{\omega CR} = \frac{3WN}{\omega C4\ell R_s} \tag{7.5}$$

The capacitance C_s and inductance L are approximately calculated on the basis that for $S/h \ll 1$, magnetic field lines do not loop around each finger but around the cross section of the interdigital width W' (Figure 7.1). Under this assumption L and C_s are calculated from microstrip transmission-line theory using ℓ as the length of the structure. Here C_s is half of the microstrip total shunt capacitance. Expressions for these quantities are given next:

$$L = \frac{Z_0\sqrt{\epsilon_{re}}}{c}\ell \tag{7.6a}$$

$$C_s = \frac{1}{2}\frac{\sqrt{\epsilon_{re}}}{Z_0 c}\ell \tag{7.6b}$$

where Z_0 and ϵ_{re} are calculated using W' and h microstrip parameters and $c = 3 \times 10^{10}$ cm/s is the velocity of light in free space.

A general expression for the total series capacitance of an interdigital capacitor can also be written as [6]

$$C = 2\epsilon_0 \epsilon_{re}\frac{K(k)}{K'(k)}(N-1)\ell \quad \text{(F)} \tag{7.7a}$$

$$= \frac{10^{-11}}{18\pi}\epsilon_{re}\frac{K(k)}{K'(k)}(N-1)\ell \times 10^{-4} \quad \text{(F)}$$

or

$$C = \frac{\epsilon_{re}10^{-3}}{18\pi}\frac{K(k)}{K'(k)}(N-1)\ell \quad \text{(pF)} \tag{7.7b}$$

where ℓ is in microns, N is the number of fingers, and ϵ_{re} is the effective dielectric constant of the microstrip line of width W. The ratio of complete elliptic integral of first kind $K(k)$ and its complement $K'(k)$ is given by

$$\frac{K(k)}{K'(k)} = \begin{cases} \dfrac{1}{\pi}\ln\left\{2\dfrac{1+\sqrt{k}}{1-\sqrt{k}}\right\} & \text{for } 0.707 \le k \le 1 \quad (7.8a) \\ \dfrac{\pi}{\ln\left[2\dfrac{1+\sqrt{k'}}{1-\sqrt{k'}}\right]} & \text{for } 0 \le k \le 0.707 \quad (7.8b) \end{cases}$$

and

$$k = \tan^2\left(\frac{a\pi}{4b}\right), \quad a = W/2, \quad \text{and} \quad b = (W+S)/2, \quad \text{and} \quad k' = \sqrt{1-k^2} \tag{7.9}$$

Design curves for interdigital capacitors are given in Figure 7.4 [9, 10]. The following example illustrates how to determine an interdigital capacitor's EC model (Figure 7.3) parameters.

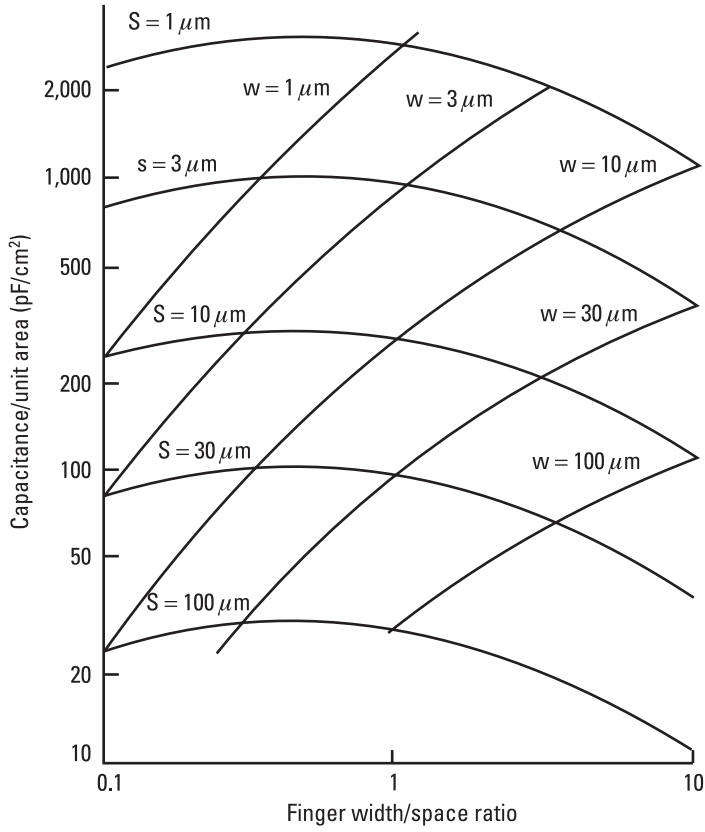


Figure 7.4 Design curves of interdigital capacitors on GaAs substrate.

Example

Design a 0.5-pF interdigital capacitor on 125-μm-thick GaAs substrate (ϵ_r = 12.9) using 5-μm-thick gold conductors having $W = S = 10$ μm. Also determine its series resonance frequency and Q_c at 10 GHz.

From Figure 7.4, the capacitance/area $\cong$ 300 pF/cm^2. Therefore, area $A = 0.5/300$ cm^2 = 0.1667 mm^2. Let us select the total width of the interdigital structure $\cong$ 300 μm, which is given as $W' = (W + S)N - S \cong 300$ μm. This gives the number of fingers N = 16, and final W' = 310 μm. Area $A = \ell \times W'$ gives ℓ = 538 μm. From Table 14.6 (Chapter 14), the values of L and C_s are given as L = 0.140 nH and C_s = 0.107 pF. From (7.4),

$$R = 1.333\,\frac{538 \times 0.0049}{10 \times 16} = 0.022\Omega$$

The series resonance frequency, f_{res}, is given by

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{6.2832\sqrt{0.14 \times 0.5 \times 10^{-21}}} = 19.02 \text{ GHz}$$

From (7.5),

$$Q_c = \frac{1}{6.2832 \times 10 \times 10^9 \times 0.5 \times 10^{-12} \times 0.022} = 1446.9$$

The preceding calculations do not include the effect of skin depth, dielectric loss, and radiation loss at the open ends of microstrip fingers.

7.1.2 *J*-Inverter Network Equivalent Representation

An interdigital capacitor like that shown in Figure 7.5(a) can be modeled using a π-network as shown in Figure 7.5(b). The reactances X_1 and X_2 represent the discontinuity effects between the feed lines and the capacitors, and the B's are the susceptance parameters for the admittance matrix. R_1 and R_2 are the reference planes. Here the structure is assumed lossless. The equivalent J-inverter network is shown in Figure 7.5(c), where ϕ_1 and ϕ_2 denote the equivalent line lengths and J is the inverter susceptance, and they are related to the admittance matrix parameters by the following relations [11]:

$$\frac{J}{\sqrt{Y_1 Y_2}} = \frac{\sin(-\phi_1/2) + \overline{B}_{11}\cos(-\phi_1/2)}{\overline{B}_{12}\sin(-\phi_2/2)} \tag{7.10}$$

$$\phi_1 = M_1\pi + \tan^{-1}\left\{\frac{2\left(\overline{B}_{11} + \overline{B}_{22}|\overline{B}|\right)}{1 + \overline{B}_{22}^2 - \overline{B}_{11}^2 - |\overline{B}^2|}\right\} \tag{7.11a}$$

$$\phi_2 = M_2\pi + \tan^{-1}\left\{\frac{2\left(\overline{B}_{22} + \overline{B}_{11}|\overline{B}|\right)}{1 + \overline{B}_{11}^2 - \overline{B}_{22}^2 - |\overline{B}|^2}\right\} \tag{7.11b}$$

where $\overline{B}_{11} = B_{11}/Y_1$, $\overline{B}_{22} = B_{22}/Y_2$, $\overline{B}_{12} = B_{12}/\sqrt{Y_1 Y_2}$, and $|\overline{B}|^2 = \overline{B}_{11}\overline{B}_{22} - \overline{B}_{12}^2$. M_1 and M_2 are the positive integer numbers. Y_1 and Y_2 are the characteristic admittances of two feed lines in the interdigital capacitor structure.

Several different structures were analyzed and their simulated data were reported by Zhu and Wu [11]. Figure 7.6 shows the inverter susceptance value and the equivalent electrical line lengths for several finger (N) values as a function of frequency. The substrate used is 1.27-mm-thick alumina, $\epsilon_r = 10.2$.

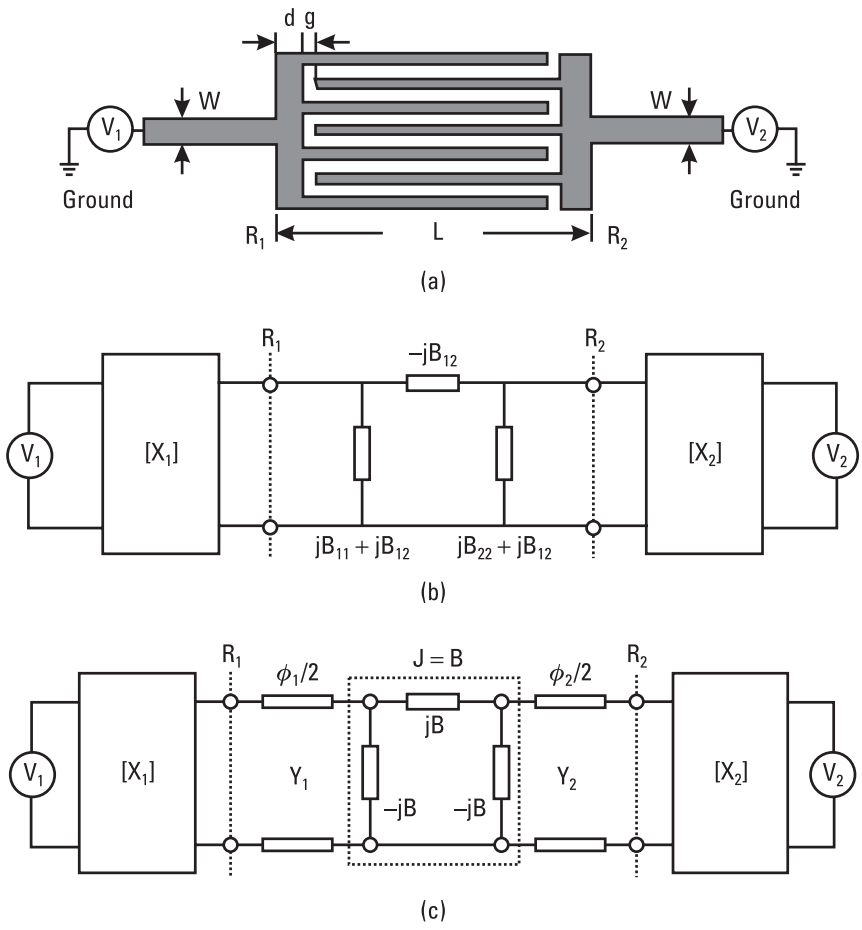


Figure 7.5 (a) Interdigital capacitor configuration for a network representation and (b) susceptance equivalent network representation and (c) *J*-inverter network equivalent representation. (*From:* [11]. © 2002 IEEE. Reprinted with permission.)

The electrical length increases monotonically and the susceptance parameter shows nonlinear behavior due to invalid lumped-element assumption, that is, $L/\lambda << 0.05$. The above-described model has applications in the design of end-coupled microstrip resonator filters and lumped-element filters using classical filter theory.

7.1.3 Full-Wave Analysis

Quasistatic and full-wave numerical methods have been extensively employed to analyze transmission lines and their discontinuities. The numerical data

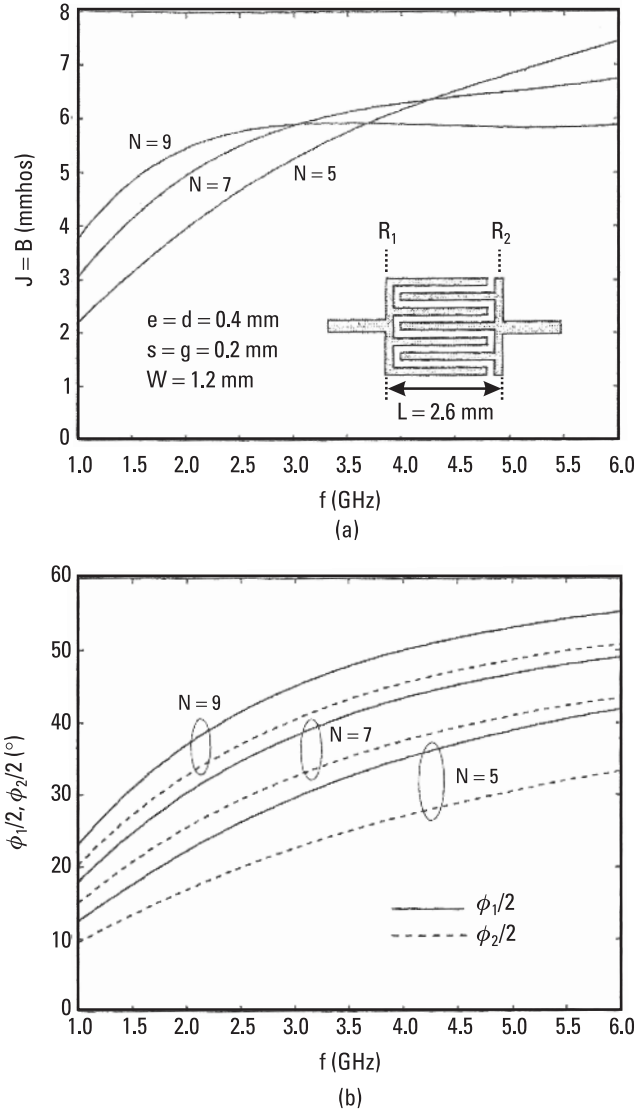


Figure 7.6 Frequency variation of (a) J-inverter susceptance j and (b) equivalent electrical line lengths ϕ_1 and ϕ_2 for various values of N. (*From:* [11]. © 2002 IEEE. Reprinted with permission.)

obtained from these methods have been used to develop analytical and empirical design equations along with EC models to describe the electrical performance of planar transmission lines and their discontinuities, including microstrip coplanar waveguide and slot lines. These equations and EC models have been exclusively

used in commercial microwave CAD tools. The EM simulators [12–17] as discussed in Section 2.4.4 play an important role in the simulation of single-layer elements such as transmission lines, patches, and their discontinuities; multilayer components, namely, inductors, capacitors, packages, and so on; and mutual coupling between various circuit elements. An accurate evaluation of the effects of radiation surface waves and interaction between components on the performance of densely packed MMICs can only be calculated using EM simulators.

Table 7.1 lists the physical parameters of a typical interdigital capacitor (Figure 7.1) analyzed using EM simulators, and Figures 7.7 and 7.8 compare the simulated performances [18–21].

7.1.4 Measurement-Based Model

Interdigital capacitor EC models have been developed using measured S-parameters for the structures. Although this approach gives quick and accurate results, it is limited to just the components measured. Table 7.2 summarizes the physical dimensions and the EC model parameters of several interdigital capacitors. Figure 7.9 compares commercial Agilent Eesof's Touchstone Library model, EC model, and measured S-parameter data. Figure 7.9(a) shows excellent correlation between both models and the measured data at low frequencies for S_{11}. However, at frequencies above 6 GHz, the commercial model departs dramatically from the measured data. Figure 7.9(b) also illustrates the same phenomena on a polar plot by comparing S_{21} of the two different models with the measured data.

Table 7.1
Parameters for the Interdigital Structures

Substrate height, $h = 100\ \mu$m
Substrate dielectric constant, $\epsilon_r = 12.9$
Conductor thickness, $t = 0.8\ \mu$m
Conductor's bulk conductivity, $\sigma = 4.9 \times 10^7$ S/m
Substrate loss tangent, tan $\delta = 0.0005$
$W = 40\ \mu$m
$S = 20\ \mu$m
$\ell = 440\ \mu$m
$W' = 520\ \mu$m
$S' = 40\ \mu$m
$\ell' = 60\ \mu$m
Number of fingers = 9
Enclosure: No

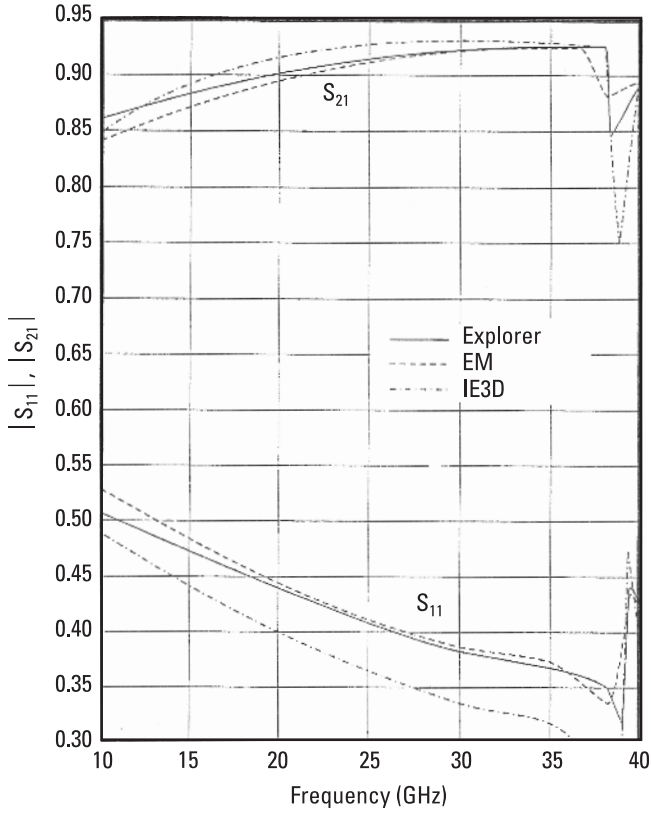


Figure 7.7 Interdigitated capacitor's $|S_{11}|$ and $|S_{21}|$ responses.

7.2 Design Considerations

In this section we discuss several design considerations such as compact size, high-voltage operation, multilayer structure, and voltage tunable capacitor.

7.2.1 Compact Size

The capacitor size can be reduced by reducing the dimensions of the structure or by using a high dielectric constant value substrate. The achievable Q-value and fabrication photoetching limit on the minimum line width and separation dictate the size of the capacitor. For ceramic and GaAs substrates, these limits are about 12 and 6 μm, respectively. It is well known that the wavelength of a signal is inversely proportional to the square root of the dielectric constant of the medium in which the signal propagates. Hence, increasing the dielectric constant of the medium a hundred-fold will reduce the component dimensions

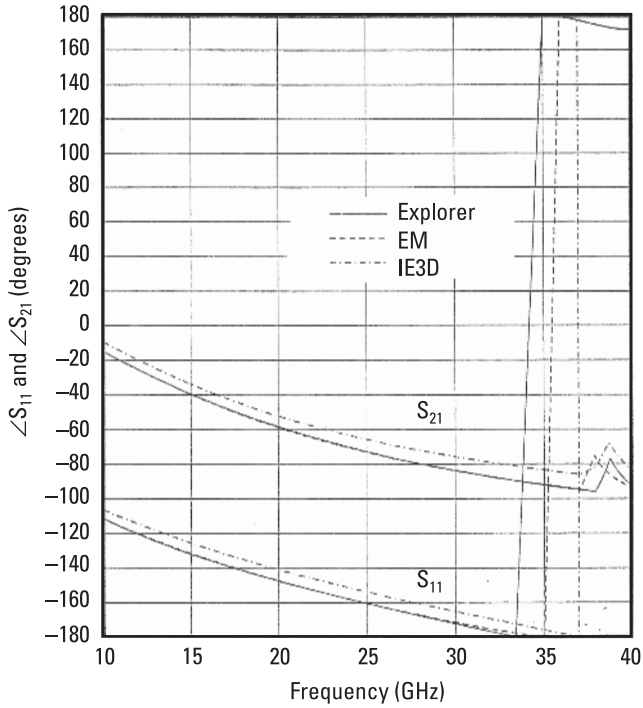


Figure 7.8 Interdigitated capacitor's $\angle S_{11}$ and $\angle S_{21}$ responses.

Table 7.2
Physical Dimensions and Equivalent Model Values for Interdigital Capacitors

Physical Dimensions	**INDIG80**	**INDIG180**	**INDIG300**	**INDIG400**	**UNITS**
Finger length, ℓ	80	180	300	400	μm
Finger width, W	12	12	12	12	μm
Finger spacing, side, S	8	8	8	8	μm
Finger spacing, end, S'	12	12	12	12	μm
Finger thickness, t	5	5	5	5	μm
Number of fingers, N	20	20	20	20	μm
Substrate thickness, h	125	125	125	125	μm
Capacitance, C	0.126	0.252	0.405	0.527	pF
Inductance, L	0.001	0.025	0.064	0.101	nH
Resistance, R_{dc}	1.89	0.850	0.500	0.441	Ω
Shunt capacitance, C_s	0.028	0.052	0.080	0.104	pF

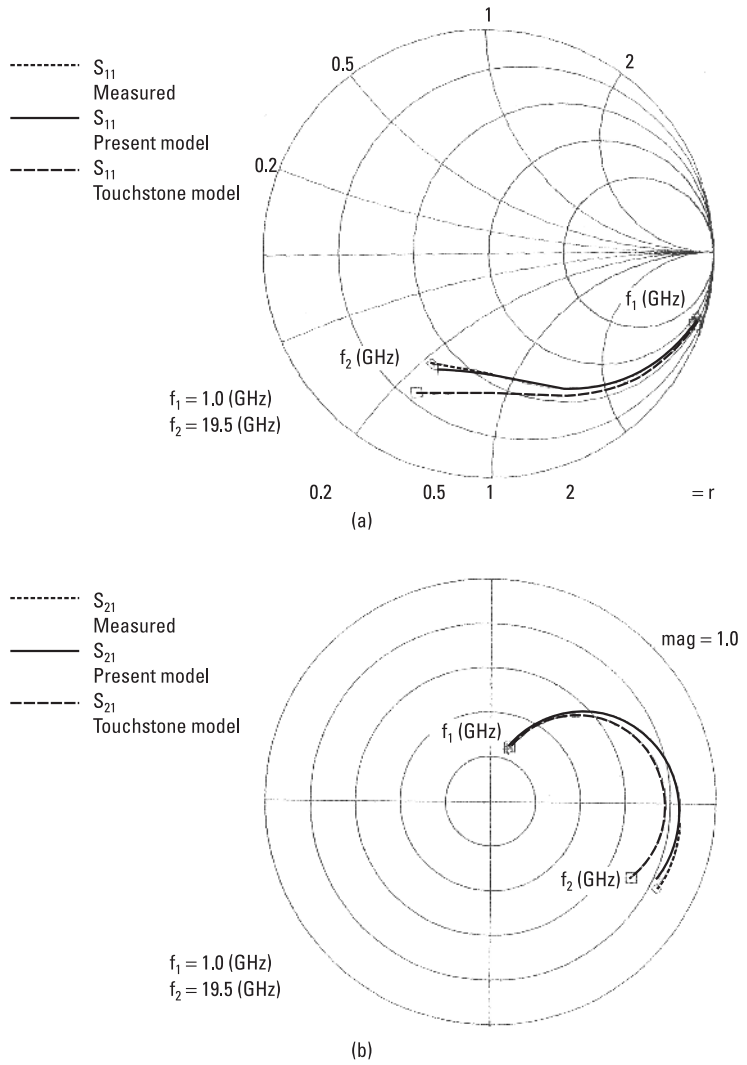


Figure 7.9 The measured performance of an interdigital capacitor compared with the present model and Touchstone model: (a) reflection coefficient and (b) transmission coefficient.

by a factor of 10. This simple concept is being exploited extensively as distributed circuit technology is being adopted at RF and lower microwave frequencies.

7.2.2 Multilayer Capacitor

Gevorgian et al. [22] have reported closed-form expressions for interdigital capacitors, on two- and three-layered substrates, using conformal mapping

technique. Figure 7.10 shows the interdigital capacitor configuration, and the total capacitance is given by

$$C = C_3 + C_n + C_{\text{end}} \tag{7.12}$$

where C_3, C_n, and C_{end} represent the three-finger capacitance, capacitance of the periodical $(n - 3)$ structure, and a correction term for the fringing fields of the ends of the strips, respectively. Closed-form expressions for these capacitance components are given next.

C_3 capacitance:

$$C_3 = 4\epsilon_0 \epsilon_{e3} \frac{K(k'_{03})}{K(k_{03})} \ell \tag{7.13}$$

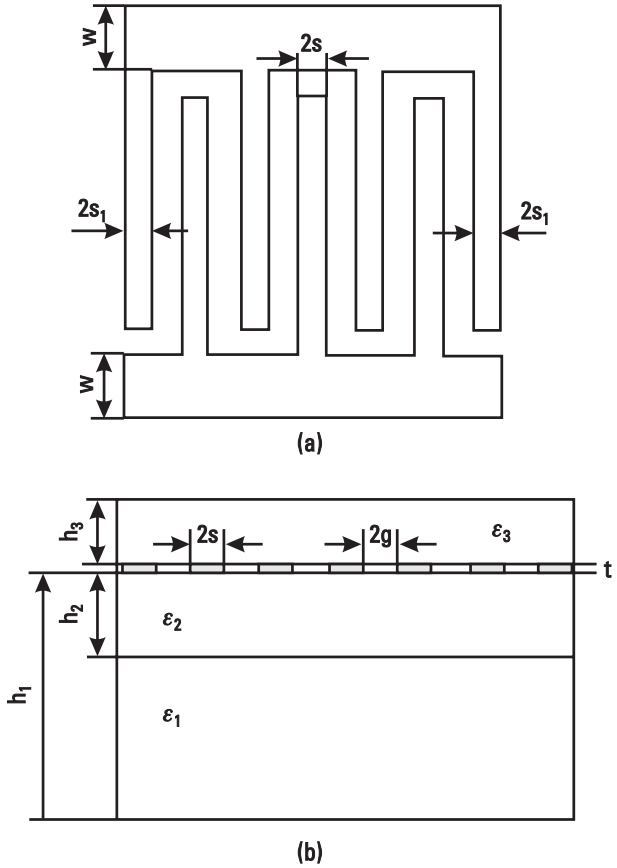


Figure 7.10 (a) Physical layouts and (b) cross-sectional view of the interdigital capacitor. (*From:* [22]. © 1996 IEEE. Reprinted with permission.)

where ℓ is the length of strip fingers and

$$\epsilon_{e3} = 1 + q_{13}\frac{\epsilon_1 - 1}{2} + q_{23}\frac{\epsilon_2 - \epsilon_1}{2} + q_{33}\frac{\epsilon_3 - 1}{2} \tag{7.14a}$$

$$q_{i3} = \frac{K(k_{i3})}{K(k'_{i3})}\frac{K(k'_{03})}{K(k_{03})}, \quad \text{for } i = 1, 2, 3 \tag{7.14b}$$

$$k_{03} = \frac{S}{S + 2g}\sqrt{\frac{1 - \left(\dfrac{(S + 2g)}{(S + 2S_1 + 2g)}\right)^2}{1 - \left(\dfrac{S}{(S + 2S_1 + 2g)}\right)^2}} \tag{7.14c}$$

$$k_{i3} = \frac{\sinh\left(\dfrac{\pi S}{2h_i}\right)}{\sinh\left(\dfrac{\pi(S + 2g)}{2h_i}\right)} \cdot \sqrt{\frac{1 - \sinh^2\left[\dfrac{\pi(S + 2g)}{2h_i}\right] \Big/ \sinh^2\left[\dfrac{\pi(S + 2S_1 + 2g)}{2h_i}\right]}{1 - \sinh^2\left[\dfrac{\pi S}{2h_i}\right] \Big/ \sinh^2\left[\dfrac{\pi(S + 2S_1 + 2g)}{2h_i}\right]}} \tag{7.14d}$$

and $k'_{i3} = \sqrt{1 - k_{i3}^2}$, $i = 1, 2, 3$. In the preceding formulas, $S_1 = S$ should be used where the widths of the external and middle fingers are the same.

C_n capacitance:

$$C_n = (n - 3)\,\epsilon_0\,\epsilon_{en}\frac{K(k_0)}{K(k'_0)}\ell \tag{7.15}$$

where

$$\epsilon_{en} = 1 + q_{1n}\frac{\epsilon_1 - 1}{2} + q_{2n}\frac{\epsilon_2 - \epsilon_1}{2} + q_{3n}\frac{\epsilon_3 - 1}{2} \tag{7.16a}$$

$$q_{in} = \frac{K(k_{in})}{K(k'_{in})}\frac{K(k'_0)}{K(k_0)}, \quad \text{for } i = 1, 2, 3 \tag{7.16b}$$

$$k_{in} = \frac{\sinh\left(\frac{\pi S}{2h_i}\right)}{\sinh\left(\frac{\pi(S+g)}{2h_i}\right)} \cdot \sqrt{\frac{\cosh^2\left(\frac{\pi(S+g)}{2h_i}\right) + \sinh^2\left(\frac{\pi(S+g)}{2h_i}\right)}{\cosh^2\left(\frac{\pi S}{2h_i}\right) + \sinh^2\left(\frac{\pi(S+g)}{2h_i}\right)}} \tag{7.16c}$$

C_{end} *capacitance:*

$$C_{\text{end}} = 4ns(2+\pi)\,\epsilon_0\,\epsilon_{e\text{end}}\,\frac{K(k_{0\text{end}})}{K(k'_{0\text{end}})} \tag{7.17}$$

where

$$\epsilon_{e\text{end}} = 1 + q_{1\text{end}}\,\frac{\epsilon_1 - 1}{2} + q_{2\text{end}}\,\frac{\epsilon_2 - \epsilon_1}{2} + q_{3\text{end}}\,\frac{\epsilon_3 - 1}{2} \tag{7.18a}$$

$$k_{0\text{end}} = \frac{x}{x + 2g_{\text{end}}}\sqrt{\frac{1 - \left(\frac{(x + 2g_{\text{end}})}{(x + w + 2g_{\text{end}})}\right)^2}{1 - \left(\frac{x}{(x + w + 2g_{\text{end}})}\right)^2}} \tag{7.18b}$$

where $x \cong 0.5S$. The effect of strip thickness t can be accounted for when the inductor and the gap are replaced by $2S = 2S' + \Delta t$ and $2g = 2g' - \Delta t$, where

$$\Delta t = \frac{t}{\pi}\left[1 + \ln\frac{8\pi S'}{t}\right]$$

and $2S'$ and $2g'$ are the physical width of the strip and the gap between them.

7.2.3 *Q*-Enhancement Techniques

The Q-factor of interdigital capacitors can be enhanced by using high-conductivity conductors and low-loss tangent dielectric substrate materials. Other Q-enhancement techniques include suspended substrate, multilayer structure, and micromachining. These are briefly discussed in the following subsections.

7.2.3.1 Suspended Substrate

The suspended-substrate technique provides a lower loss than the conventional microstrip structure. Figure 7.11(a) shows a suspended-substrate interdigital

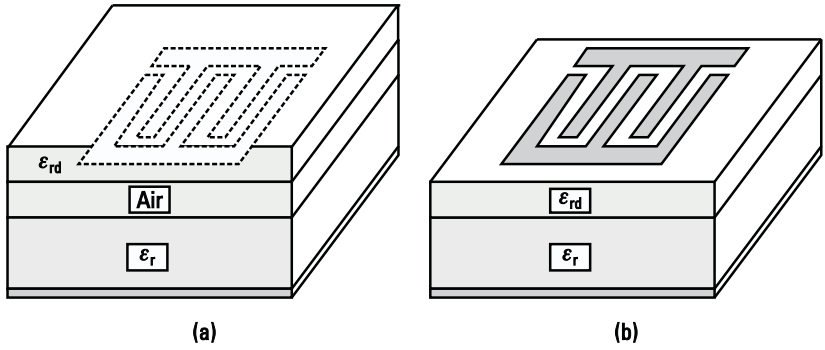


Figure 7.11 (a) Suspended-substrate interdigital capacitor and (b) multilayer interdigital capacitor.

capacitor. By selecting the proper substrate thickness and air spacing between the substrate and ground plane, one can reduce the capacitor loss by a factor of 25% to 50%. The EM simulated performance of a suspended-substrate interdigital capacitor is compared with that for a conventional interdigital capacitor in Table 7.3. The capacitor dimensions are $W = 20\ \mu$m, $S = S' = 10\ \mu$m, $\ell' = 20\ \mu$m, $\ell = 600\ \mu$m, $h = 100\ \mu$m, and $N = 9$. The conductors are 4-μm-thick gold.

7.2.3.2 Multilayer Microstrip

The Q-factor of an interdigital capacitor can also be enhanced by using a modified microstrip structure, as shown in Figure 7.11(b). This structure is compatible with the standard MMIC fabrication process. The strip conductor is fabricated on a thin polyimide dielectric layer, which is placed on top of a GaAs substrate. This allows more of the electric flux lines in the air and resembles a suspended-substrate microstrip line, which has much lower dissipation loss than a conventional microstrip. Another way to think of this is that, instead of inserting 50 to 75 μm of additional GaAs beneath the line, we have inserted a thinner layer of polyimide (a material with lower permittivity) in order to reduce the dissipation loss. This fabrication technique has also been used to improve the performance of single-layer and multilayer inductors as discussed in Chapter 3. The performance of a multilayer interdigital capacitor is compared with that of conventional and suspended-substrate interdigital capacitors in Table 7.3. Here the dielectric under the conductors is 10-μm polyimide ($\epsilon_r = 3.2$), but the other parameters are the same. In this example, both of these techniques reduce the interdigital series capacitance by a factor of 3.2.

7.2.3.3 Micromachined Technique

The Q of interdigital capacitors on Si substrate is drastically improved by using the micromachining technique [23] as discussed in Section 3.1.5, in which the

Table 7.3
High-Frequency EC Model Parameters of Standard, Suspended-Substrate and Multilayer Interdigital Capacitors, with GaAs Substrate Thickness of 100 μm

Capacitor Configuration	L' (nH)	C' (pF)	R_{dc}	R_{ac}	R_d	C_{S1} (pF)	C_{S2} (pF)	C_{S3} (pF)	Q at 10 GHz	f_{res} (GHz)
Standard	0.100	0.695	0.011	0.0085	0.0010	0.068	0.188	0.025	398	19.11
Suspended substrate	0.106	0.220	0.011	0.0095	0.0011	0.029	0.093	0.002	1,735	33.00
Multilayer	0.110	0.225	0.011	0.0095	0.0015	0.045	0.156	0.004	1,533	30.6

Note: The EC model used is shown in Figure 7.3(b) and $R' = R/2$, where R is given by (3.14).

parasitic substrate loss is reduced by removing Si below the interdigital structure. This approach reduces the parasitic capacitance by a factor of ϵ_r and results in better millimeter-wave circuits. However, micromachining techniques also reduce the interdigital series capacitance approximately by a factor of $(1 + \epsilon_r)/2$.

7.2.4 Voltage Tunable Capacitor

The voltage tunability of interdigital capacitors is achieved by using ferroelectric materials such as barium strontium titanate or strontium titanate. The properties of ferroelectric materials were discussed in Section 6.2.5. A voltage tunable structure could be realized either using bulk material or by employing thin films as shown in Figure 7.12. The latter configuration is compatible with MIC technology and can be realized using widely used thin-film deposition techniques. In the thin-film case, the voltage required to change the material dielectric constant values is lower than that used for the bulk material configuration. The dielectric strength for such materials is in the range of a few volts per micron, which means that the films must be more than 10 μm thick to operate such structures at 5V to 10V, before breakdown occurs. Relatively higher losses and a lower breakdown voltage limit the power levels of such structures. Such capacitors can be designed using the analysis discussed in the previous section.

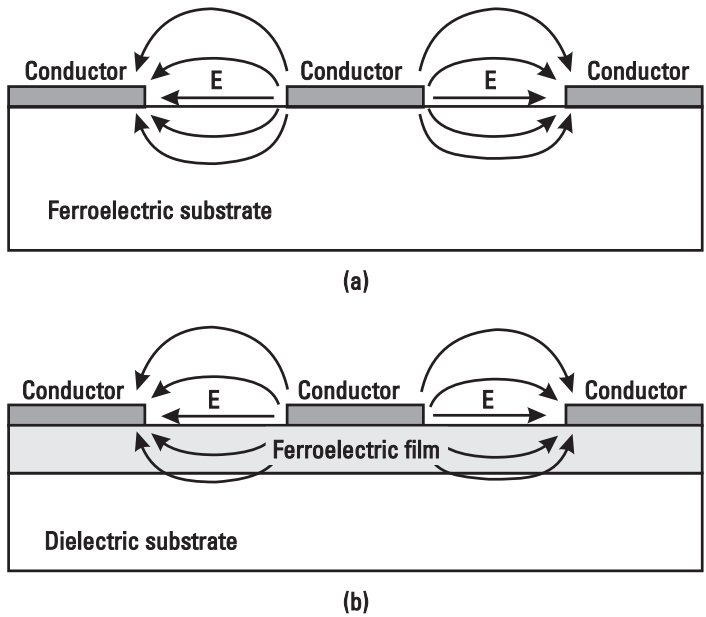


Figure 7.12 Field configurations between interdigital fingers: (a) bulk ferroelectric substrate and (b) thin-film ferroelectric on a dielectric substrate.

Measured capacitance versus bias voltage and Q-factor versus operating frequency of an interdigital capacitor on a thin ferroelectric covered substrate [Figure 7.12(b)] are shown in Figure 7.13 [24]. The ferroelectric thin film of $Sr_{0.5}Ba_{0.5}TiO_3$ was deposited on an MgO substrate. The interdigital structure has 12 fingers, line width $W \cong 20\ \mu$m, gap between fingers $S \cong 6\ \mu$m, and

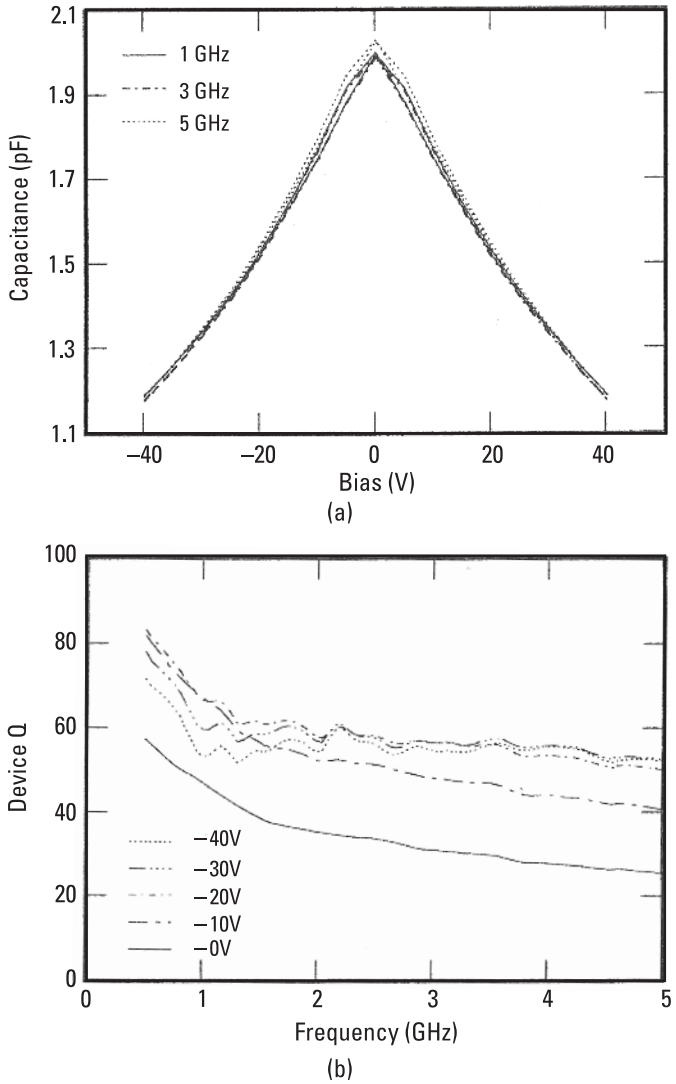


Figure 7.13 (a) Capacitance versus bias voltage at 1, 3, and 5 GHz, and (b) Q-factor versus frequency at various bias voltages of a $Sr_{0.5}Ba_{0.5}TiO_3$ thin-film interdigital capacitor on an MgO substrate. (*From:* [24]. © 1999 John Wiley. Reprinted with permission.)

finger length $\ell \cong 150$ μm. At 5 GHz, the capacitance value varied by 40% and the Q-value by 100% when the structure was biased from 0 to 40V.

7.2.5 High-Voltage Operation

Conventional interdigitally coupled line structures are capable of handling voltages of less than 200V, depending on the fabrication tolerances and humidity [25]. To increase the protection against voltage breakdown across the gap, an overlay of silicon rubber as shown in Figure 7.14 has been used. Because dielectric loading modifies the electrical characteristics of the coupled line, accurate design or simulation methods such as EM simulators are required to determine the new parameters. A dc block fabricated on RT/duroid substrate with spacing $S = 50$ μm and width $W = 60$ μm achieved a breakdown voltage of more than 4.5 kV. Breakdown generally occurs at one of the open ends of the coupled lines [25].

7.3 Interdigital Structure as a Photodetector

An interdigital structure (Figure 7.1) on a semi-insulating GaAs substrate can be realized as a photodetector. When a dc voltage that is much higher than the threshold for electron velocity saturation is applied across the electrodes of an interdigital structure, the incident photon energy is absorbed by the GaAs

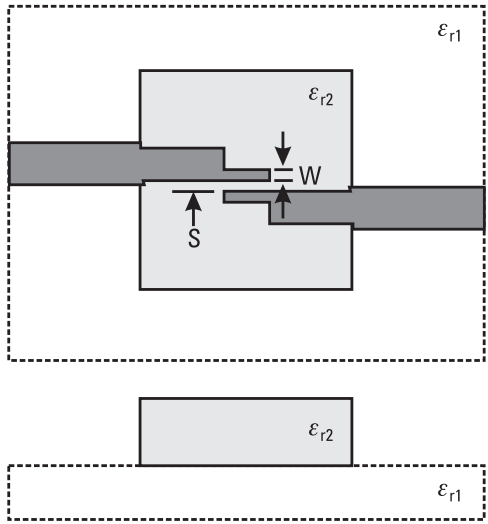


Figure 7.14 Top and side views of high-voltage dc block showing high-voltage insulator dielectric.

material, producing electron-hole pairs [26]. These charge carriers induce electric current between the electrodes, giving rise to the photodetection effect. In such structures, the semiconductor is usually undoped, the photon energy is larger than the bandgap of the semiconductor, and the dark current is lower than in photoconductive detectors. In an interdigital structure, each TiAu electrode makes a Schottky diode, resulting in a back-to-back diode configuration. When a voltage is applied across the electrodes, one diode is forward biased and the other is reverse biased, giving rise to reduced dark current.

A typical interdigital photodetector consists of multilayer GaAs layers as shown in Figure 7.15(a). The multilayer structure comprises a 0.1-μm-thick *intermediate growth temperature* (IGT) GaAs layer grown at 350°C on a 0.4-μm-thick GaAs buffer layer placed on a semi-insulating GaAs substrate. Both layers are of undoped GaAs type. The fingers have line width $W = 4\ \mu$m, line spacing $S = 5\ \mu$m, and an active area of $300 \times 300\ \mu\text{m}^2$.

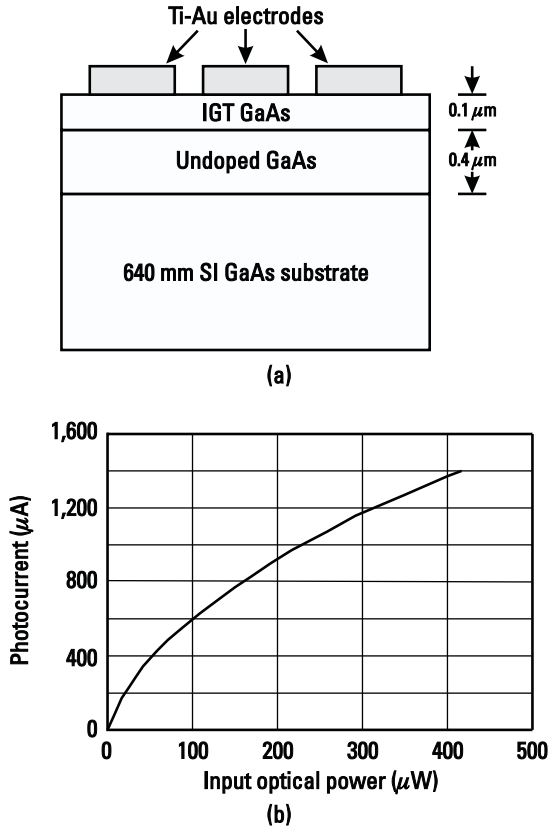


Figure 7.15 (a) Cross-sectional view of an interdigital photodetector and (b) measured photocurrent versus input optical power.

The structure was tested using 0.85-μm wavelength optical power. The devices were biased at 10V. Figure 7.15(b) shows the measured photocurrent response as a function of optical power. This device can also be used as an electron detector [26].

References

[1] Alley, G. D., "Interdigital Capacitors and Their Application in Lumped Element Microwave Integrated Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-18, December 1970, pp. 1028–1033.

[2] Hobdell, J. L., "Optimization of Interdigital Capacitors," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-27, September 1979, pp. 788–791.

[3] Esfandiari, R., D. W. Maki, and M. Sircusa, "Design of Interdigitated Capacitors and Their Application to GaAs Filters," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-31, January 1983, pp. 57–64.

[4] Joshi, J. S., J. R. Cockril, and J. A. Turner, "Monolithic Microwave Gallium Arsenide FET Oscillators," *IEEE Trans. Electron Devices,* Vol. ED-28, February 1981, pp. 158–162.

[5] Pettenpaul, E., et al., "CAD Models of Lumped Elements on GaAs Up to 18 GHz," *IEEE Trans. Microwave Theory Tech.,* Vol. 36, February 1998, pp. 294–304.

[6] Bahl, I. J., and P. Bhartia, *Microwave Solid State Circuit Design,* New York: John Wiley, 1988, Chap. 2.

[7] Sadhir, V., I. Bahl, and D. Willems, "CAD Compatible Accurate Models for Microwave Passive Lumped Elements for MMIC Applications," *Int. J. Microwave and Millimeter Wave Computer Aided Engineering,* Vol. 4, April 1994, pp. 148–162.

[8] Gupta, K. C., et al., *Microstrip Lines and Slotlines,* 2nd ed., Norwood, MA: Artech House, 1996, Chap. 8.

[9] Wilson, K., "Other Circuit Elements for MMICs," *GEC J. Research* (Special Issue on Monolithic Microwave Integrated Circuits), Vol. 4, 1986, 126–133.

[10] Ladbrooke, P. H., *MMIC Design GaAs FETs and HEMTs,* Norwood, MA: Artech House, 1989.

[11] Zhu, L., and K. Wu, "Accurate Circuit Model of Interdigital Capacitor and its Application to Design of New Quasi-Lumped Miniaturized Filters With Suppression of Harmonic Resonance," *IEEE Trans. Microwave Theory Tech.,* Vol. 48, March 2000, pp. 347–356; also see correction in *Trans. MTT,* Vol. 50, October 2002, p. 2412.

[12] Sonnet Software, Liverpool, NY: EM.

[13] Maxwell SV, Pittsburgh: Ansoft.

[14] High Frequency Structure Simulator, Santa Rosa, CA: Agilent.

[15] LINMIC + Analysis Program, Ratingen, Germany: Jansen Microwave.

[16] MSC/EMAS, Milwaukee, WI: MacNeal Schwendler.

[17] IE3D, San Francisco: Zeland Software.

[18] Kattapelli, K., J. Burke, and A. Hill, "Simulation Column," *Int. J. Microwave and Millimeter Wave Computer-Aided Engineering,* Vol. 3, January 1993, pp. 77–79.

[19] Rautio, J., "Simulation Column," *Int. J. Microwave and Millimeter Wave Computer-Aided Engineering,* Vol. 3, January 1993, pp. 80–81.

[20] Zhang, J. X., "Simulation Column," *Int. J. Microwave and Millimeter Wave Computer-Aided Engineering,* Vol. 3, July 1993, pp. 299–300.

[21] Mongia, R., I. Bahl, and P. Bhartia, *RF and Microwave Coupled-Line Circuits,* Norwood, MA: Artech House, 1999.

[22] Gevorgian, S. S., et al., "CAD Models for Multi-Layered Substrate Interdigital Capacitors," *IEEE Trans. Microwave Theory Tech.,* Vol. 44, June 1996, pp. 162–164.

[23] Chi, C.-Y., and G. M. Rebeiz, "Planar Microwave and Millimeter-Wave Lumped Elements and Coupled-Line Filters Using Micro-Machining Techniques," *IEEE Trans. Microwave Theory Tech.,* Vol. 43, April 1995, pp. 730–738.

[24] Patel, D. P., J. M. Pond, and J. B. L. Rao, "Microwave Ferroelectric Devices," *Wiley Encyclopedia of Electrical and Electronics,* Vol. 13, New York: John Wiley, 1999, pp. 109–118.

[25] Koscica, T. E., "Microstrip Quarter-Wave High Voltage DC Block," *IEEE Trans. Microwave Theory Tech.,* Vol. 41, January 1993, pp. 162–164.

[26] Yost, T. A., A. Madjar, and P. R. Herczfeld, "Frequency Response Mechanisms for the GaAs MSM Photodetector and Electron Detector," *IEEE Trans. Microwave Theory Tech.,* Vol. 49, October 2001, pp. 1900–1907.

8

Resistors

8.1 Introduction

Lumped-element resistors [1–13] are used in RF, microwave, and millimeter-wave ICs. The applications include terminations, isolation resistors, feedback networks, lossy impedance matching, voltage dividers, biasing elements, attenuators, gain equalizing elements, and as stabilizing or damping resistors that prevent parasitic oscillations. The design of these resistors requires a knowledge of (1) sheet resistance, (2) thermal resistance, (3) current-handling capacity, (4) nominal tolerances, and (5) temperature coefficient of the film. These resistors can be realized either by depositing thin films of lossy material on a dielectric base using thin-film, thick-film, or monolithic technologies or by employing semiconductor films on a semi-insulating substrate between two electrodes. Nichrome and tantalum nitride are the most popular and useful film materials for thin-film resistors (thickness: 0.05–0.2 μm).

The resistance R value of a planar resistor, as shown in Figure 8.1, depends on the material properties and its dimensions, and is given by

$$R = \rho\frac{\ell}{A} = \rho\frac{\ell}{Wt} = \frac{\ell}{\sigma Wt} \tag{8.1}$$

where ρ is the bulk resistivity of the material expressed in Ω-m, σ is the bulk conductivity expressed in S/m, ℓ is the length of the resistor along the direction of current flow (Figure 8.1), W is the width, t is the thickness, A is the cross-sectional area, and dimensions are in meters. The resistance can also be calculated from the sheet resistance R_s (ohms/square) of the resistive film (for given thickness t) using the following relation:

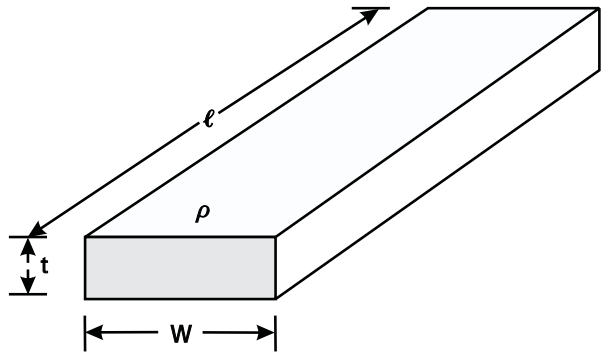


Figure 8.1 Geometry of a planar resistor.

$$R = R_s \frac{\ell}{W}, \quad \text{where } R_s = \rho/t = \frac{1}{\sigma t} \tag{8.2}$$

For given material R_s, the resistance can easily be calculated from the number of squares of width in total length. For example, a line of width 50 μm that is 1,000 μm long has 2.5 times less resistance than a line of width 20 μm that is also 1,000 μm long. Thus the key in increasing the resistance is to keep the number of metallization squares as large as possible in a given length. Figure 8.2 shows six squares between terminals 1 and 2 and if the R_s value is 10 Ω/square, the total resistance is 60Ω.

When a voltage is applied across a resistor (Figure 8.3), the current flowing through it depends on the resistance or conductance (reciprocal of resistance) value, or when a current flows through the resistor, the voltage developed across its terminals again depends on its resistance value.

The ratio of voltage and current is equal to the resistance R, also known as Ohm's law:

$$R = \frac{V}{I}\ \Omega \tag{8.3}$$

where voltage V and current I are expressed in volts and amperes, respectively.

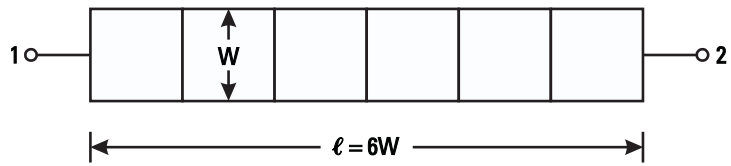


Figure 8.2 Resistance calculation representation of a resistor from sheet resistance.

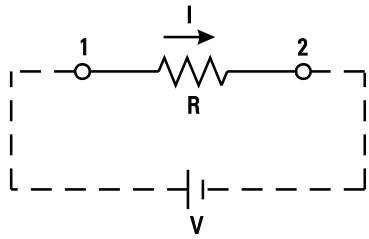


Figure 8.3 Electrical representation of a resistor.

The power dissipated, P_{dc}, in the resistor due to the applied voltage is given by

$$P_{dc} = V \cdot I = \frac{V^2}{R} = I^2 R \tag{8.4}$$

where unit of P_{dc} is in watts. An ideal resistor, or a resistor with length very small compared to the operating wavelength, dissipates only electric energy and constitutes negligible electric and magnetic stored energies because of negligible associated parasitic capacitance and inductance, respectively.

Like low-frequency resistors, RF and microwave resistors must have the following properties:

- Sheet resistance in the range of 1 to 1,000 Ω/square;
- Low temperature coefficient of resistance;
- Good stability;
- Required power dissipation capability;
- Low parasitics.

Table 13.4 in Chapter 13 provides some of the resistive materials used in the fabrication of resistors. From those materials specified, nichrome and tantalum nitride are the most widely used. The exact properties of these materials vary with fabrication process and thickness.

8.2 Basic Definitions

In this section various terms used to specify a resistor are defined.

8.2.1 Power Rating

The *power rating* of a resistor is defined as the maximum power a resistor can withstand without affecting its base value and reliability. Power rating depends

on its area (larger area can sink more dissipated power) and ambient temperature. High-power rated resistors have large areas and appreciable parasitics, which can affect their RF performance at microwave frequencies.

8.2.2 Temperature Coefficient

The rate of change of resistor value with temperature is known as the *temperature coefficient of resistors* (TCR) or simply TC and is expressed in percent per degree Celsius or parts per million per degree Celsius (ppm/°C). When the resistance increases with increasing temperature, the TC value has a positive sign; if it decreases, the TC value has a negative sign. The resistor's temperature dependence is given by

$$R_{\mathrm{OT}} = R_{\mathrm{RT}} + TC(T_{\mathrm{OT}} - T_{\mathrm{RT}}) \tag{8.5}$$

where OT and RT denote the operating and room or ambient temperature, respectively. If a resistor has +TC value of 40 ppm/°C, the resistance value will increase with temperature by about 0.4% at 125°C; when the ambient temperature is 25°C, a 100-Ω resistor at room temperature will be about 100.4Ω at 125°C.

8.2.3 Resistor Tolerances

Variations in the specified resistor values in a batch or batch to batch are expressed in terms of *resistor tolerances.* In general, depending on the resistor manufacturing technology and the application, resistor tolerances in the range of ±1%, ±5%, ±10%, or ±20% can be achieved.

8.2.4 Maximum Working Voltage

The maximum voltage one can apply across a resistor without affecting its resistance value is termed the *maximum working voltage.* The maximum working voltage depends on the resistor material, allowed resistance deviations from a small voltage value, and physical configuration. The voltage coefficient of a resistor in percentage is expressed as

$$\text{Voltage coefficient} = \frac{R - R_m}{RV_m} 100 \tag{8.6}$$

where R and R_m are the resistance values at a very low voltage and the maximum allowed voltage V_m, respectively.

8.2.5 Maximum Frequency of Operation

A resistor value also depends on its *frequency of operation.* Planar resistors have associated parasitic reactances and their values increase with frequency, affecting the net resistance value. At a certain frequency, the capacitive and inductive reactances become equal and give rise to self-resonance. This will be discussed in detail in Section 8.3.

8.2.6 Stability

In most applications, the change of resistance value with time is not a desirable characteristic. The drift in resistance value over an extended time period is expressed in terms of *stability* of the resistor. Typically, thin-film resistors might change within ±0.2% during a 5-year period.

8.2.7 Noise

Every resistor has *Johnson noise* proportional to its resistance value due to unwanted random voltage fluctuations generated within the resistor. Depending on the resistor material and its fabrication, the resistors also have additional noise sources. For example, in a monolithic thin-film resistor on a GaAs semiconductor substrate, additional noise is a result of imperfect ohmic contact and the resistor film.

Johnson noise, also known as "white" or thermal noise, depends on the temperature and is independent of frequency of operation. The rms voltage v_n expressed in volts is given by

$$v_n = (4kRT\Delta f)^{1/2} \tag{8.7}$$

where k is the Boltzmann constant (1.38×10^{-23} J/K), R is the resistance in ohms, T is the operating temperature in kelvins, and Δf is the bandwidth in hertz over which the noise voltage is measured.

8.2.8 Maximum Current Rating

Each resistor has a specified *maximum current rating* above which the resistor might fail due to current density being higher than the allowed value.

8.3 Resistor Types

The manufacturing of LE resistors can be divided into three categories: chip, monolithic, and multichip module resistors. These are briefly discussed in this section.

8.3.1 Chip Resistors

Thin-film and thick-film hybrid technologies have been used to manufacture chip resistors for low-power and high-power applications. In thin-film hybrid technology, resistive thin films consisting of nichrome (NiCr) or tantalum nitride (TaN) are deposited on alumina for low-power applications and on beryllia or aluminum nitride for high-power applications.

Thick-film resistors are manufactured using various compositions of ruthenium dioxide (RuO_2) paste and a screen printing process. Sheet resistance values ranging from 1Ω to 10 kΩ per square are obtained by mixing RuO_2 with silver (Ag) and palladium (Pd) conducting particles for values less than 100 Ω/square, and by mixing RuO_2 with Ag lead ruthenate and bismuth ruthenate for values higher than 100 Ω/square. Commonly used base substrate materials are alumina, beryllia, and aluminum nitride. More detailed discussion of this subject is provided in Chapter 13.

8.3.2 MCM Resistors

MCM technologies include PCBs, cofired ceramic, and thin film on silicon. In PCB technology, the resistor material is deposited on a polyimide layer and covered with another polyimide film for encapsulation. The electrode connections through contact holes are made with copper using photolithography techniques. The resistive film materials used are NiCr, TaN, and CrSi. The other two MCM technologies use resistor fabrication as discussed for hybrid and monolithic technologies.

8.3.3 Monolithic Resistors

Resistors are an integral part of MICs and can be realized either by depositing thin films of lossy metal or by employing bulk semiconductor films on a semi-insulating substrate as shown in Figure 8.4.

Nichrome and tantalum nitride are the most popular and useful film materials for thin-film resistors (thickness: 0.05–0.2 μm). Resistors based on semiconductor (e.g., GaAs or Si) films can be fabricated by forming an isolated land of semiconductor conducting layer (thickness: 0.05–0.5 μm). Both types are fabricated by defining the desired pattern by photolithography. Factors such as resistance value, tolerance, reproducibility, and power handling are determined based on the resistor type. Table 8.1 summarizes typical parameters of monolithic resistors fabricated on GaAs substrate.

In monolithic resistors, the total resistance is the sum of resistive film and the resistance of the two ohmic contacts and is given as

$$R = R_s \frac{\ell}{W} + 2R_{sc} \frac{\ell_c}{W_c} \tag{8.8}$$

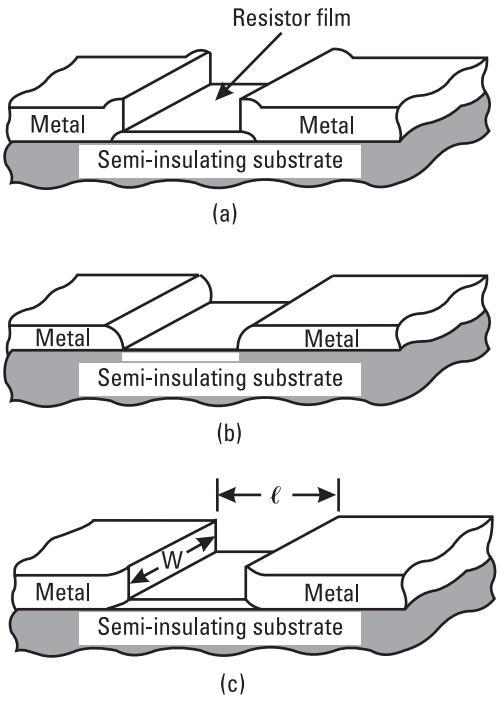


Figure 8.4 Planar resistors: (a) thin film, (b) mesa, and (c) implanted.

where R_{sc}, ℓ_c and W_c are the sheet resistance, length, and width of the ohmic contacts, respectively.

8.3.3.1 Thin-Film Resistors

Thin-film resistor materials are of metal types such as GeAu, Ta, Ti, Cr, and NiCr or of composite material type such as TiWN, TaN, and Ta_2N. Thin-film resistors are typically 0.1 to 0.4 μm thick and have limited current-carrying capability. The maximum current density allowed by electromigration requirements in thin films is about 3×10^5 A/cm^2. Therefore, the current density per unit width for such resistors is of the order of 0.3 to 1.2 mA/μm.

8.3.3.2 Bulk Semiconductor Resistors

Bulk semiconductor resistors form an integral part of MIC fabrication and no additional fabrication steps are required. The sheet resistance (R_s) value of such resistors depends on the doping of the material such as n^-, n, and n^+. For GaAs semiconductors, the typical value of R_s lies between 100 and 1,500 Ω/square, and is lowest for n^+ layers and highest for n^- layers. However, GaAs resistors have four potential problems: change in surface potential, low current

Table 8.1
Typical Room Temperature Parameters of Monolithic Resistors Fabricated on GaAs Substrate

Resistor Type	Material	Thickness (μm)	Sheet Resistance Value (ohm/square)	Nominal Tolerance (%)	TCR (ppm/°C)	Maximum Current (mA/μm)
Thin film	TiWN	0.18	10.8	±10	+100	1.0
Implanted	n^+ GaAs	0.2	140.0	±20	+2,000	0.6
Ohmic	Ni/Ge/Au	0.14	0.9	±30	+100	0.4
Metal 1	Ti/Pd/Au	0.60	0.05	±20	+100	1.0

saturation, Gunn domain formation, and large temperature coefficient. These are briefly discussed next.

Change in Surface Potential

The first potential problem is the change in surface potential under resistor areas over an extended period of time. Such drifts affect the sheet resistance of the resistor. A dielectric protection layer over such resistors minimizes this change.

Low Current Saturation

Bulk resistors have nonlinear behavior at high electric fields as a result of carrier velocity saturation. The electric field at which this phenomenon takes place is known as the *critical electric field* and its value for GaAs is 3.3 kV/cm. In practice, this can be avoided by designing resistor dimensions such that maximum field strength across the resistor's electrodes is less than about 2 kV/cm (0.2 V/μm). Assuming that 10V is a safe operating voltage, the minimum resistor's length required is 50 μm. If the sheet resistance of an n^+-type GaAs layer is 150 Ω/square, the widths required for 50-, 200-, and 500-Ω resistors calculated using $W = R_s \ell / R$ are 150, 37.5, and 15 μm, respectively.

Gunn Domains

Gunn domains are formed only above the critical field across the resistor electrodes. Because the operating electric field across the bulk resistors is much less than critical field, the occurrence of Gunn domains in such resistors is nonexistent.

Temperature Coefficient

The temperature coefficient of GaAs resistors is positive and large. The approximate value is about 300 ppm/°C and is about 10 times higher than the values for thin-film resistors. This results in appreciable increase in resistance value with temperature. In most MMIC applications, bulk resistors are used when their value is not critical to the circuit design; otherwise, one has to include temperature dependence in the design or some temperature compensation techniques must be utilized to offset the change in resistance with temperature.

Because bulk resistors or GaAs resistors are fabricated from single-crystal GaAs material, the electromigration phenomenon is not present, because this phenomenon deals with crystalline grain boundaries.

8.3.3.3 Parasitic Effects

A problem common to all planar resistors is the parasitic capacitance attributable to the underlying dielectric region and the distributed inductance, which makes such resistors exhibit a frequency dependence at high frequencies. If the substrate

has a ground plane, one can determine the frequency dependence by treating the resistor as a section of a very lossy microstrip line. Figure 8.5 shows how the VSWR increases dramatically at low values of R_{SH} because the length of the resistor becomes too large.

Also shown in Figure 8.5 is the thermal resistance. Clearly, a trade-off is necessary between VSWR and thermal resistance. The smaller the resistor size meeting the current-handling and thermal requirements the better the electrical performance due to lower parasitic effects.

8.3.3.4 Power Handling

The power-handling capacity of monolithic resistors is limited due to burnout of the thin film by overheating. The power-handling capacity of monolithic resistors can be determined in a way similar to that of microstrip lines (discussed in Chapter 14). In this case, the resistor strip is considered to be a lossy microstrip line. Because the loss in the resistor conductor is much higher than the dielectric loss, only conductor loss is considered in the calculation of power dissipated. The temperature difference ΔT (in degrees Celsius) between the resistor film and the back side of the substrate due to P_{dc} (in watts) power dissipated in the resistor is given by

$$\Delta T = P_{dc} R_{TH} = P_{dc} \frac{h}{KA} \tag{8.9}$$

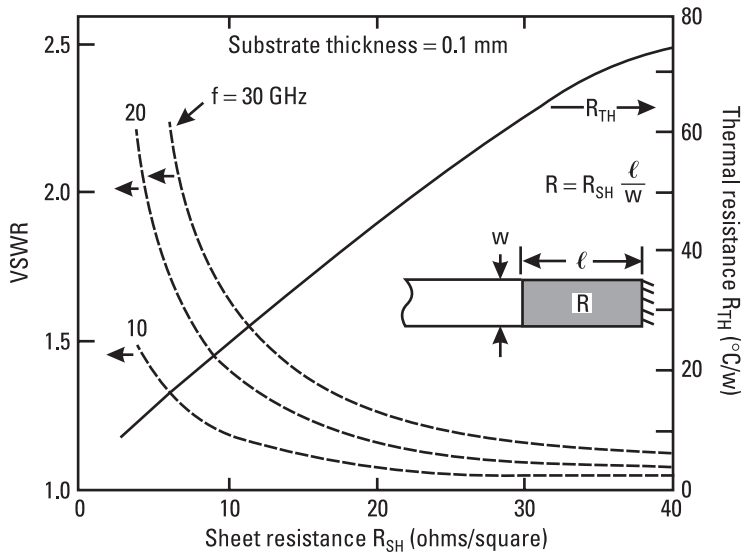


Figure 8.5 Thermal resistance and VSWR of a planar resistor as a function of sheet resistance and frequency.

where R_{TH} is the thermal resistance, A is the equivalent area of the resistor of length ℓ, h is the thickness, and K is the thermal conductivity of the substrate. Dimensions of h, A, and K are meters, square meters, and W/m-°C, respectively. The resistor area is given by

$$A = W_e(\ell + 2\ell') \tag{8.10}$$

where ℓ' is the length of the ohmic contact used to connect the resistor film to other circuitry and W_e is the effective width calculated from the parallel plate waveguide model. Approximately $W_e = W + 2h$. If R_s is the sheet resistance of the film, the total resistance R is given by

$$R = R_s \frac{\ell}{W} \tag{8.11}$$

From (8.10) and (8.11),

$$A = (W + 2h)\left(\frac{R}{R_s} W + 2\ell'\right) \tag{8.12}$$

From (8.9) and (8.12),

$$W^2 + pW - q = 0 \tag{8.13}$$

where

$$p = 2h + \frac{2\ell' R_s}{R} \tag{8.14a}$$

$$q = \frac{R_s h}{R}\left[\frac{P_{dc}}{K\Delta T} - 4\ell'\right] \tag{8.14b}$$

Equation (8.14b) is valid for positive values of q.

The solution of (8.13) for positive a value of W is

$$W = \frac{-p + \sqrt{p^2 + 4q}}{2} \tag{8.15}$$

Thus, the required resistor width for given power dissipation and resistance value can be calculated from (8.15). Consider an example of a 50-Ω resistor

to dissipate 1W with the top surface's maximum allowed operating temperature of 150°C. The baseplate temperature is 25°C. Other parameters are given here:

$h = 100\ \mu$m;
$\ell' = 20\ \mu$m;
$R_s = 10.8\ \Omega$/square;
$K = 0.294$ W/cm°C (GaAs at 150°C).

The calculated values of ΔT, p, and q are

$\Delta T = 125$°C;
$p = 208.64 \times 10^{-4}$ cm;
$q = 0.4150 \times 10^{-4}$ cm^2;
$W = 18.3\ \mu$m

Table 8.2 summarizes values of W for several power dissipation and resistor values.

The following design notes are applicable for monolithic resistors:

- Select resistor width to meet electromigration rules as provided by the manufacturer.
- Maximize resistor area for best power dissipation capability.
- Make the resistor width as close to the transmission line width as possible to minimize discontinuity effects. Discontinuity effects can usually be ignored if $1/3 < W_M/W_R < 3$, where W_M and W_R are the

Table 8.2
Calculated Required Minimum Width (in Microns) for Thin-Film Resistors on 100-μm-Thick GaAs Substrate for Several Dissipated Power Values, with $T_m = 150$°C and $T_a = 25$°C

Power Dissipated (W)	Resistor Value (Ω)		
	10	20	50
0.5	22.7	12.9	5.6
1.0	66.8	39.7	18.3
2.0	133.2	82.4	40.3
5.0	269.6	174.5	92.0
10.0	426.0	282.7	156.3
20.0	648.9	438.5	251.5

line widths of the microstrip and resistor. Resistors shorter than $\lambda/50$ can simply be treated as a lumped resistance in series with a microstrip line of equivalent line dimension.

8.4 High-Power Resistors

High-power chip resistors and terminations are required to absorb unwanted power in RF and microwave couplers/hybrids and in power dividers/combiners. Reliable design of such components requires substrate materials having the following electrical and mechanical characteristics:

- Low dielectric constant (ϵ_r);
- High thermal conductivity (K) at high operating temperatures;
- *Coefficient of thermal expansion* (CTE) close to that of resistive film and of copper used as a heat sink;
- Good insulator having high electrical resistivity;
- Good adhesion to resistive film and bonding contact metal;
- Good machinability for batch production;
- Low cost.

Table 8.3 lists several potential candidates for chip resistors, and beryllium oxide (BeO) has been widely used for such applications as a substrate of choice. However, BeO powder and dust require special handling because they are known to be hazardous materials. A comparable material to BeO is aluminum nitride

Table 8.3
Comparison of Dielectric Substrates for High-Power Chip Resistors

Property	Alumina	BN	BeO	AlN	SiC	Diamond
ϵ_r	9.9	4.2	6.7	8.5	45	5.7
K (W/m-°C)						
at 25°C	30	70	280	170	270	1,400
at 100°C	25	200	200	150	190	—
at 200°C	—	—	150	125	150	—
CTE (ppm/°C)	6.9	5.0	6.4	4.6	3.8	1.2
Shunt capacitance	Medium	Small	Small	Medium	Large	Small
Film adhesion	Excellent	Poor	Excellent	Good	Good	Poor
Machinability	Good	Good	Good	Good	Good	Poor
Cost	Low	Low	Medium	Medium	Medium	High

(AlN) and its usage is steadily increasing because of the international community concern regarding the hazards of BeO. Other possible replacement substrate materials are silicon carbide (SiC), boron nitride (BN), alumina (Al_2O_3), and diamond. As compared in Table 8.3, diamond has the highest thermal conductivity and is used where good heat sinks are required.

Both thin-film and thick-film technologies are being used to manufacture high-power chip resistors. Nichrome and tantalum nitride are commonly used resistor thin films; TaN is preferred to NiCr due to the presence of undesirable nickel in NiCr that is believed to introduce unwanted intermodulation products in multicarrier communication system application apparatus.

The power-handling capacity of a chip resistor is defined as the maximum allowed power dissipation that does not cause the film to burn out and is determined by the temperature rise of the resistor film. The parameters that play major roles in the calculation of maximum power handling are (1) total power dissipated in the resistor, (2) thermal conductivity of the substrate material, (3) surface area of the resistor film, (4) thickness of the substrate, (5) ambient temperature, that is, temperature of the medium surrounding the resistor or heat sink temperature, and (6) maximum allowed temperature of the resistor film.

If R_{th} is the thermal resistance of the substrate and T_m is the maximum operating temperature, the maximum allowed dissipated power in the resistor, P_{dc} (in watts) is given by

$$P_{\text{dc}} = \frac{T_m - T_a}{R_{\text{TH}}} \tag{8.16}$$

where T_a is the ambient temperature and R_{TH} is approximately calculated from

$$R_{\text{TH}} = \frac{d}{KA} = \frac{d}{KW\ell} \tag{8.17}$$

or

$$A = P_{\text{dc}}\, d/[K(T_m - T_a)] \tag{8.18}$$

Here dimensions d, W, and ℓ shown in Figure 8.6 are expressed in meters and the unit of K is W/m-°C.

The substrate thickness is selected based on mechanical strength, handling, parasitic capacitance, and cost. Maximum allowed film temperature is usually 150°C and the ambient temperature with chip resistors attached to heat sinks with additional cooling is about 25°C. Let us assume that the BeO substrate is 25 mil (0.635×10^{-3}m) thick and K at 150°C is about 175 W/m-°C. The

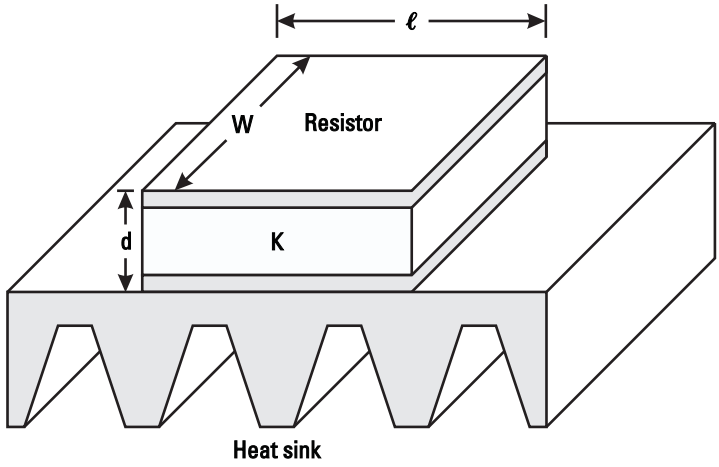


Figure 8.6 High-power chip resistor mounting on a heat sink.

calculated resistive film areas for 10, 20, 50, 100, and 200W power handling are summarized in Table 8.4. If the substrate selected is 50 mil thick, the resistor width and length for a square area given in Table 8.4 are $\sqrt{2}$ times more.

8.5 Resistor Models

The characterization of lumped-element resistors can be accomplished using various techniques including analytical, lumped-element EC, and distributed line approaches. Among these, EC and distributed approaches are commonly used and are briefly discussed in this section.

Table 8.4
Chip Resistor Film Dimensions for Various Power-Handling Levels Using 25-Mil BeO Substrate, with $T_m = 150°C$ and $T_a = 25°C$

Dissipated Power (W)	Area (m^2)	$W = \ell$ (mm)
10	0.29×10^{-6}	0.539
20	0.58×10^{-6}	0.762
50	1.45×10^{-6}	1.204
100	2.90×10^{-6}	1.703
200	5.80×10^{-6}	2.408

8.5.1 EC Model

A simple representation of a resistor and its two-port EC model are shown in Figure 8.7(a, b), respectively. Assuming that the resistor is divided into two symmetrical halves, the various elements are as follows: R is the total equivalent resistance, C_p is the capacitance across the resistor ports due to voltage difference, C_{s1}, C_{s2}, and L are the "pi" equivalent shunt capacitors and series inductance of each half of the resistor structure. The shunt capacitance C_{s1} and series inductance L also include the parasitics of any wire/ribbon bonds used. Because resistor (chip or monolithic) sizes used in RF and microwave frequencies are much smaller than the operating wavelength, using total resistance R in the center in the EC model is a valid first-order approximation. Because the voltage difference across a resistor is usually significant, the use of C_p in the EC model is generally required [13].

When a resistor is used as a one-port element in a shunt configuration (i.e., port 2 is grounded), its model is further simplified as shown in Figure 8.7(c). Here $C_t = C_p + C_{s1} + 2C_{s2}$ and $L_t = 2L$. In this case, the input admittance Y_{in} is written as

$$Y_{\text{in}} = G_{\text{in}} + jB_{\text{in}} = \frac{1}{R + j\omega L_t} + j\omega C_t \tag{8.19}$$

or

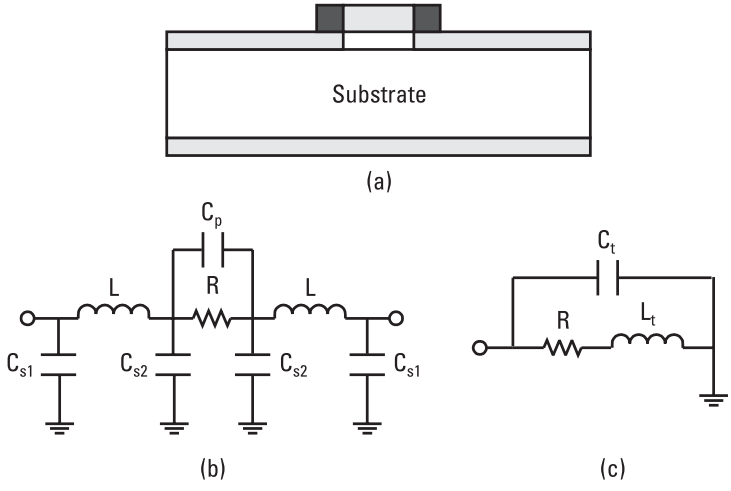


Figure 8.7 Thin-film resistor: (a) microstrip mounting, (b) two-port EC representation, and (c) simplified one-port EC representation.

$$G_{\text{in}} + jB_{\text{in}} = \frac{R}{R^2 + \omega^2 L_t^2} + j\omega \frac{C_t(R^2 + \omega^2 L_t^2) - L_t}{R^2 + \omega^2 L_t^2} \tag{8.20}$$

At resonance (i.e., $B_{\text{in}} = 0$), the input impedance is real and greater than R, given by

$$R_{\text{in}} = \frac{1}{G_{\text{in}}} = R + \frac{\omega^2 L_t^2}{R} \tag{8.21}$$

The resonant frequency ω_0 is given by

$$\omega_0 \frac{C_t(R^2 + \omega_0^2 L_t^2) - L_t}{R^2 + \omega_0^2 L_t^2} = 0$$

or

$$\omega_0 = \frac{1}{C_t L_t} - \frac{R^2}{L_t^2} \tag{8.22}$$

Below the resonance frequency, B_{in} is negative; that is, the resistor's parasitic reactance is of the inductive type, while above ω_0 it is of the capacitive type. Model parameters are extracted using dc resistance and S-parameter measurements as discussed in previous chapters.

8.5.2 Distributed Model

MMICs use both metal film resistors and active semiconductor layer (e.g., n^+ ion-implanted) resistors. Typical sheet resistance values of thin-film (TiWN) and n^+ resistors, being used at M/A-COM in Roanoke, Virginia, are approximately 10.8 and 150 Ω/square, respectively. Figure 8.8(a) shows the physical layout of a thin-film resistor. Models of thin-film resistors were developed using several resistor values from 25 to 200Ω. Figure 8.8(b) shows the microstrip transmission-line-based model of the thin-film resistor, which consists of several sections of an ideal resistor in series with a transmission-line section. The total sum of all transmission-line sections is equal to the length of the thin-film resistor. The model also includes the ohmic contact resistance of 0.3Ω and the ohmic line length of 17 μm. This model is valid for both resistor types (e.g., thin-film and active semiconductor layer).

The number of sections n required to accurately model a resistor is indicated by the ℓ/λ ratio where ℓ is the total length of the resistor and λ is the guide

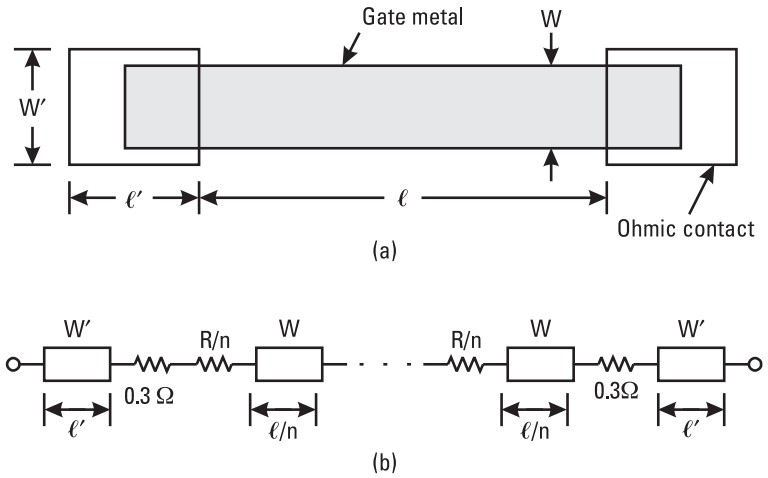


Figure 8.8 (a) Physical layout of a thin-film resistor. Each end of the resistor has an ohmic contact pad with the shaded section representing the resistor metal. (b) Distributed model of the thin-film resistor consists of *n* number of microstrip lines and resistors.

wavelength for the microstrip transmission line at the model's highest operating frequency. The ideal resistor has a value of $R' = R/n$ where R is the total dc resistance of the resistor. As a general rule of thumb, the number of sections n can be indicated by the following relation:

$$\text{for } \ell/\lambda \leq 0.02 \qquad n = 1$$
$$\text{for } \ell/\lambda \geq 0.02 \qquad n \geq (50\ell/\lambda)$$

Figure 8.9 shows excellent correlation between the measured and modeled performance of a 100Ω resistor. Similar agreement was achieved for other resistor values. Also, Figure 8.9 shows that the model found in the commercial CAD tool compares well to this model and the measured data. (Spikes in the measured transmission phase are caused by the sweeper shifting bands.)

8.5.3 Meander Line Resistor

Normally, small resistors are realized using straight sections of resistive materials. However, larger and compact resistors take the shape of a meander line as shown in Figure 8.10(a) in order to fit into a compact area. The resistance of the meander line of width W is given by

$$R = \frac{\rho}{Wt}[\ell + 4(0.44)\ell_c] \quad \Omega \tag{8.23}$$

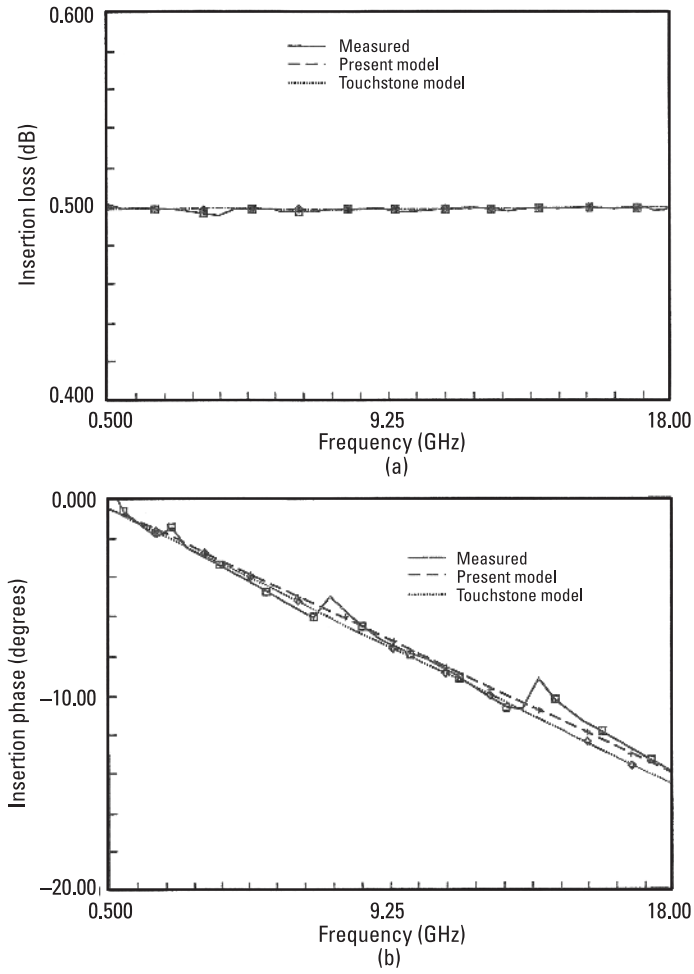


Figure 8.9 A comparison of the measured transmission coefficient of a 100-Ω resistor with the simulated data using the present model and the Touchstone model: (a) magnitude and (b) phase.

where $\ell = 2\ell_1 + 2\ell_2 + \ell_3$. The second term in the preceding equation corresponds to four corners with reduced resistance value. The resistance of the 90° angled corner is about half of an equivalent straight section. The uncertainty in the resistor value, where one needs better accuracy, can be minimized by using a modified meander line configuration shown in Figure 8.10(b). In this case, the resistor components have only straight sections.

Meander line resistors are accurately characterized by using the distributed approach, where resistor sections are treated as lossy transmission-line sections and the coupling between the sections is evaluated using parallel-coupled lines.

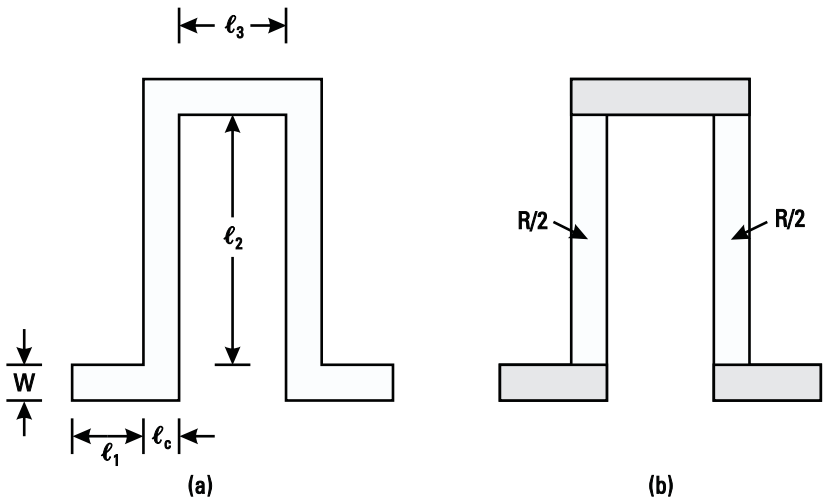


Figure 8.10 (a) Meander line resistor configuration and (b) accurate realization of a meander line resistor.

More accurate characterization of such resistors is performed by using EM field solvers.

8.6 Resistor Representations

8.6.1 Network Representations

At RF and the lower end of the microwave frequency spectrum, the resistor can be represented simply by its resistance value R. $ABCD$-, S-parameter, Y-, and Z-matrices for series and shunt resistors are given in Table 8.5 where Z_0 is the characteristic impedance of the lines across which the resistor is connected.

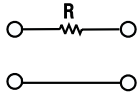
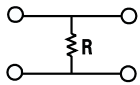
8.6.2 Electrical Representations

Resistors can be connected in various configurations: series, shunt, and series-shunt as shown in Figure 8.11. When n resistors ($R_1, R_2, \ldots, R_n$) are connected in series, the total resistance R_T is given by

$$R_T = R_1 + R_2 + \ldots + R_n \tag{8.24}$$

whereas for parallel connection

Table 8.5
ABCD-, S-, Y-, and *Z*-Matrices for Ideal Lumped Resistors

	***ABCD*-Matrix**	***S*-Parameter Matrix**	***Y*-Matrix**	***Z*-Matrix**
Series 	$\begin{bmatrix} 1 & R \\ 0 & 1 \end{bmatrix}$	$\frac{1}{R+2Z_0}\begin{bmatrix} R & 2Z_0 \\ 2Z_0 & R \end{bmatrix}$	$\begin{bmatrix} \frac{1}{R} & -\frac{1}{R} \\ -\frac{1}{R} & \frac{1}{R} \end{bmatrix}$	
Shunt 	$\begin{bmatrix} 1 & 0 \\ \frac{1}{R} & 1 \end{bmatrix}$	$\frac{1}{Z_0+2R}\begin{bmatrix} -Z_0 & 2R \\ 2R & -Z_0 \end{bmatrix}$		$\begin{bmatrix} R & R \\ R & R \end{bmatrix}$

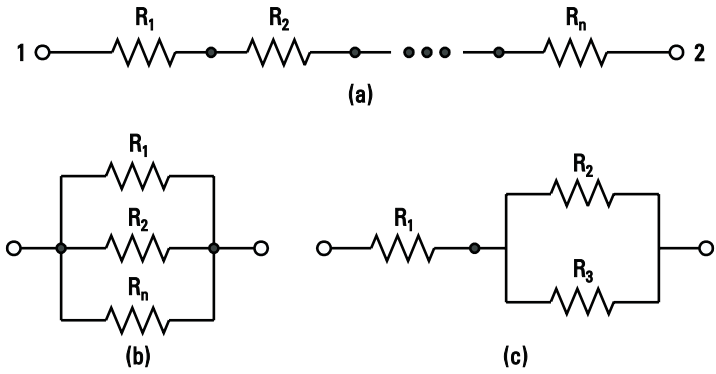


Figure 8.11 Resistor connections: (a) series, (b) shunt, and (c) series-shunt.

$$\frac{1}{R_T} = \sum_{i=1}^{n} \frac{1}{R_i}$$

or

$$R_T = \frac{1}{1/R_1 + 1/R_2 + \ldots + 1/R_n} \tag{8.25}$$

In the case of a series-shunt configuration as shown in Figure 8.11(c), the total resistance is given by

$$R_T = R_1 + \frac{R_2 R_3}{R_2 + R_3} \tag{8.26}$$

If a 25Ω resistor is connected in series with two 50Ω resistors connected in parallel, the total resistance is

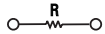
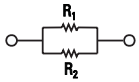
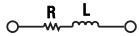
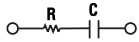
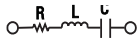
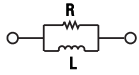
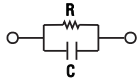
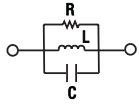
$$R_T = 25 + \frac{50 \times 50}{50 + 50} = 50\Omega \tag{8.27}$$

Table 8.6 provides impedance, admittance, and transmission phase angle representations of various combinations of R, C, and L.

8.7 Effective Conductivity

The calculation for resistance of thin films is based on the assumption that the thickness of the films is much larger than the mean free path of electrons in

Table 8.6
Impedance, Admittance, and Transmission Phase Angle Representations of Various Combinations of *R, C,* and *L*

Configuration	Impedance $Z = R + jX$	Admittance $Y = 1/Z$	Phase Angle $\phi = \tan^{-1}(X/R)$
	R	$1/R$	0
	$R_1 R_2/(R_1 + R_2)$	$(1/R_1 + 1/R_2)$	0
	$R + j\omega L$	$(R - j\omega L)/R^2 + \omega^2 L^2)$	$\tan^{-1}(\omega L/R)$
	$R - j/\omega C$	$(R + j/\omega C)/$ $(R^2 + 1/\omega^2 C^2)$	$-\tan^{-1}(1/\omega CR)$
	$R + j(\omega L - 1/\omega C)$	$\frac{R - j(\omega L - 1/\omega C)}{R^2 + (\omega L - 1/\omega C)^2}$	$\tan^{-1}[(\omega L - 1/\omega C)/R]$
	$\omega LR\left(\frac{\omega L + jR}{R^2 + \omega^2 L^2}\right)$	$1/R - j/\omega L$	$\tan^{-1}(R/\omega L)$
	$R(1 - j\omega CR)/$ $(1 + \omega^2 C^2 R^2)$	$1/R + j\omega C$	$-\tan^{-1}(\omega CR)$
	$\frac{1/R - j(\omega C - 1/\omega L)}{(1/R)^2 + (\omega C - 1/\omega L)^2}$	$\frac{1}{R} + j(\omega C - 1/\omega L)$	$\tan^{-1}[R(1/\omega L - \omega C)]$

the film metal. However, very thin films have decreased conductivity from the bulk value, due to the scattering of electrons from the film surface [14, 15]. Hansen and Pawlewicz [15] report a general formula for the effective conductivity σ_e in terms of the bulk conductivity σ, the film thickness t, and the electron mean free path p that is given as

$$\frac{\sigma_e}{\sigma} = 1 - \frac{3}{8x} + \frac{e^{-x}}{16x}(6 - 10x - x^2 + x^3) + \frac{x}{16}(12 - x^2)E_1(x) \tag{8.28}$$

where $x = t/p$ and $E_1(x)$ is the exponential integral [16]. Figure 8.12 provides a plot for σ_e/σ as a function of t/p.

Liao [14] gives an approximate formula for σ_e/σ as follows:

$$\frac{\sigma_e}{\sigma} = 0.75x\left[\ln\left(\frac{1}{x}\right) + 0.4228\right] \tag{8.29}$$

which is valid for $x \leq 0.2$.

Another approximate formula by curve fitting the data in Figure 8.12 is obtained and is given below:

$$\frac{\sigma_e}{\sigma} = \tanh\left(0.84\sqrt{x}\right) \tag{8.30}$$

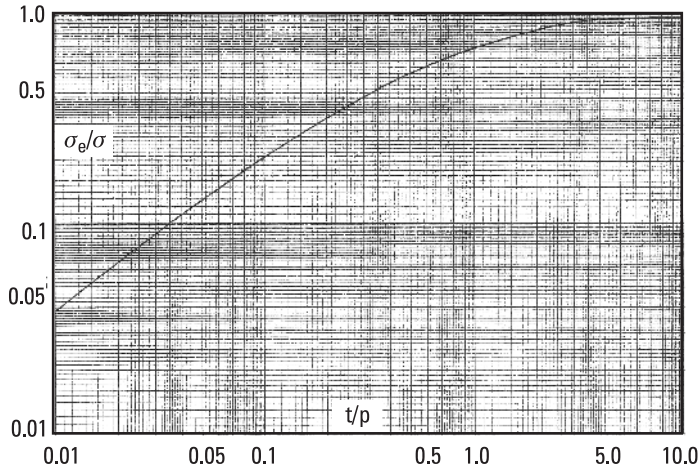


Figure 8.12 Effective conductivity as a function of thickness to electron mean free path ratio.

This equation is valid for $x \geq 0.5$. By comparing average data obtained using the above two expressions with data plotted in Figure 8.12, a reasonably good agreement was found over $0.2 < x < 0.5$. Table 8.7 provides the electron mean free path for several materials.

8.8 Thermistors

Thermistors are resistors having very large TC values usually with positive sign and their resistance value increases exponentially with increasing temperature. The resistance-temperature relationship for thermistors may be expressed as [11]

$$R(T) = A + Be^{CT} \tag{8.31}$$

where coefficients A, B, and C are determined by conducting measurements on the materials used. Thermistor materials commonly used are $BaTiO_3$, $SrTiO_3$, and $PbTiO_3$. Thermistors are commonly used in RF and microwave power meter sensors.

In summary, thin-film resistors as compared to bulk GaAs resistors have a much lower temperature dependence, are more linear, and exhibit less noise. However, in general, they need additional masks and processing steps. In M/A-COM's MSAG process, no additional masks are required because the titanium tungsten nitride (TiWN) used as a thin-film resistor material is also used as a Schottky gate metal for FET fabrication [17–19].

Table 8.7
Electron Mean Free Path, Bulk Conductivity, and Bulk Resistivity of Good Conductors

Material	Electron Mean Free Path p (Å)	$\sigma \times 10^7$ (S/m)	$\rho \times 10^{-8}$ (Ω-m)
Ag	570	6.17	1.62
Cu	420	5.80	1.724
Au	570	4.10	2.44

References

[1] Pucel, R. A., "Design Considerations for Monolithic Microwave Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-29, June 1981, pp. 513–534.

[2] Pengally, R. S., *Microwave Field-Effect Transistors-Theory, Design and Applications,* New York: John Wiley, 1982.

[3] Williams, R. E., *Gallium Arsenide Processing Techniques,* Dedham, MA: Artech House, 1984.

[4] Bahl, I. J., and P. Bhartia, *Microwave Solid State Circuit Design,* New York: John Wiley, 1988, Chap. 15.

[5] Ladbrooke, P. H., *MMIC Design: GaAs FETs and HEMTs,* Norwood, MA: Artech House, 1989.

[6] Goyal, R., (Ed.), *Monolithic Microwave Integrated Circuits: Technology and Design,* Norwood, MA: Artech House, 1989.

[7] Wadell, B. C., *Transmission Line Design Handbook,* Norwood, MA: Artech House, 1991, Chap. 8.

[8] Sadhir, V. K., I. J. Bahl, and D. A. Willems, "CAD Compatible Accurate Models of Microwave Passive Lumped Elements for MMIC Applications," *Int. J. Microwave and Millimeter-Wave Computer-Aided Engineering,* Vol.4, April 1994, pp. 148–162.

[9] Goyal, R., (Ed.), *High Frequency Analog Integrated Circuit Design,* New York: John Wiley, 1995.

[10] Gupta, K. C., et al., *Microstrip Lines and Slotlines,* 2nd ed., Norwood, MA: Artech House, 1996.

[11] Pecht, M., and P. Lall, "Resistors," *Electrical Engineering Handbook,* R. C. Dorf, (Ed.), Boca Raton, FL: CRC Press, 1997.

[12] Lenihan, T., et al., "Embedded Thin Film Resistors, Capacitors, and Inductors in Flexible Polyimide Films," *Int. J. Microcircuits Electronic Packaging,* Vol. 20, 1997, pp. 474–481.

[13] Weber, R. J., *Introduction to Microwave Circuits,* New York: IEEE Press, 2001.

[14] Liao, S. Y., *Microwave Devices and Circuits,* Upper Saddle River, NJ: Prentice Hall, 1980, Chap. 2.

[15] Hansen, R. C., and W. T. Pawlewicz, "Effective Conductivity and Microwave Reflectivity of Thin Metallic Films," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-30, November 1982, pp. 2064–2067.

[16] Abramowitz, M., and I. A. Stegun, (Eds.), *Handbook of Mathematical Functions with Formulas, Graphs, and Mathematical Tables,* Washington, D.C.: National Bureau of Standards, 1964.

[17] Bahl, I. J., et al., "Multifunction SAG Process for High-Yield, Low-Cost GaAs Microwave Integrated Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-38, September 1990, pp. 1175–1182.

[18] Fisher, D., and I. Bahl, *Gallium Arsenide IC Applications Handbook,* San Diego, CA: Academic Press, 1995.

[19] Bahl, I. J., "Monolithic Microwave Integrated Circuits," *Wiley Encyclopedia of Electrical and Electronics,* Vol. 13, New York: John Wiley, 1999, pp. 490–513.

9

Via Holes

In RF and microwave circuits, low-loss and low-inductance grounds are very important to achieve good gain, noise figure, insertion loss, VSWR, output power, *power-added efficiency* (PAE), and bandwidth performance. In MICs/MMICs, one needs the backside ground metallization to be connected with minimum possible inductance path to the top side of the substrate having RF ground pads. In MICs four basic techniques are used to achieve such ground connections. As shown in Figure 9.1, these are via hole, wire bonds, ribbon bonds, and wrap-around grounds. For RF applications of MMICs, via hole and wire bond techniques are commonly used, whereas the via hole is an integral part of monolithic microwave and millimeter-wave integrated circuits. A comparison of these ground connections is given in Table 9.1.

9.1 Types of Via Holes

There are two types of via holes (Figure 9.2): one used for interconnections of metal layers in a multilayer technology and the second type used for a backside via hole ground. These are briefly discussed next.

9.1.1 Via Hole Connection

In multilayer ceramics, via hole connections are an integral part of the process. The holes are punched in each green ceramic sheet and subsequently filled with a metal paste consisting of tungsten or molybdenum, which makes interconnections from layer to layer. Computer-controlled step and repeat equipment is

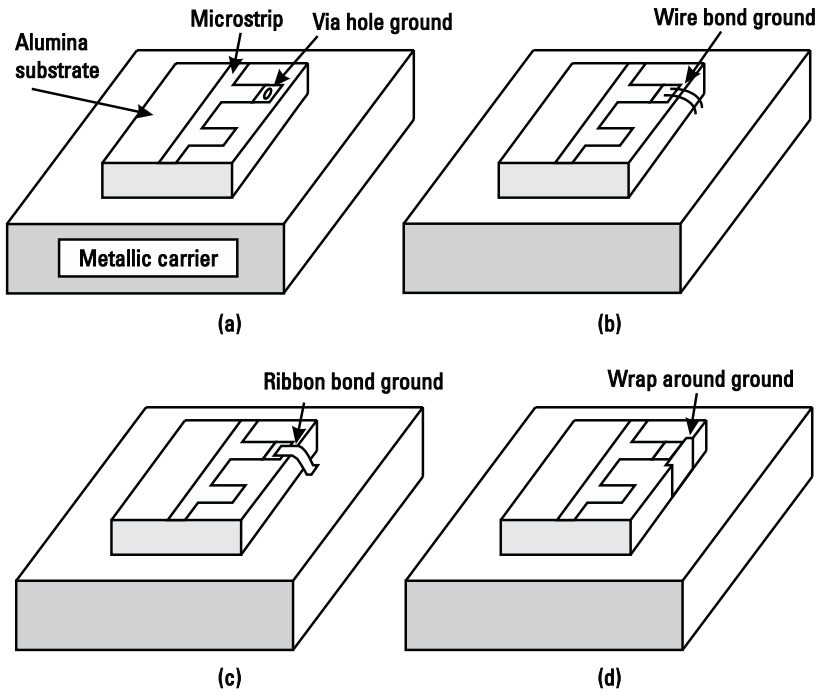


Figure 9.1 Various ground connection techniques in MICs: (a) via hole, (b) wire bond, (c) ribbon bond, and (d) wrap-around.

Table 9.1
Comparison of Various Ground Connections

Feature	Via Hole	Wire Bond	Ribbon Bond	Wrap-Around
Inductance value	Very low	Low	Very low	Very low
Layout flexibility	Excellent	Poor	Poor	Very poor
Realization in complex circuits	Easy	Difficult	Difficult	Very difficult
RF performance	Excellent	Good	Very good	Poor
Fabrication	Difficult	Easy	Easy	Very difficult
Throughput	Excellent	Good	Good	Poor
Cost	Moderate	Low	Low	High

used to punch holes with high precision. The minimum diameter used is about 6 mils.

In multilayer MMICs and digital ICs, the interconnection between different level metals is made by using via holes in the separating dielectric layer or

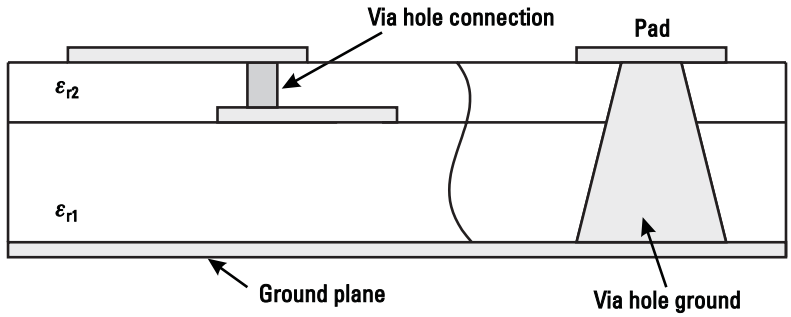


Figure 9.2 Via hole connection through dielectric and backside via hole ground.

layers, which are generally of 1- to 3-μm-thick polyimide. For a 3×3-μm contact via hole, the dc resistance is about 0.1Ω. They have minimum parasitics, are very reproducible, and are fabricated with almost 100% yield. Via hole connections are integral parts of transistors, inductors, transformers, and Lange couplers.

9.1.2 Via Hole Ground

A via hole ground is an opening in the dielectric substrate (e.g., GaAs, polyimide, or Al_2O_3) made either by dry or wet etching or punching techniques or by using laser drilling. In thin-film Al_2O_3 technology, laser drilling is exclusively used, whereas in LTCC multilayer ceramic technology, numeric precision-controlled punching is used. Via hole walls are then metallized to make a connection between the top and bottom sides.

In MMICs, the ground connection for active devices and passive components operating above L-band frequencies is traditionally achieved by backside via hole technology. They provide low-inductance grounding for transistors, diodes, capacitors, resistors, inductors, and transmission lines. They also provide great flexibility in the physical layout of the circuit. Otherwise, all of the circuit elements that need RF grounding have to be placed near the edge of the circuit or use open-circuited radial line stubs to realize effective RF grounds. The former approach adds uncertainty in the inductance value in addition to extra processing steps, whereas the latter approach requires more space and makes the circuit size larger. However, at millimeter-wave frequencies the latter technique is quite effective.

In MMICs, via holes are etched through the backside of the substrate. Via hole etching is usually performed by using dry etching employing reactive gases. This technique is also known as *plasma etching* and is a well-controlled process leading to vertical sidewalls and excellent yield. Via hole walls are then metallized using thick gold, which also completely fills the backside, making

good connections with the via pads located on the front side of the locations of via holes. Thus, gold-filled via holes make good low-resistance ($\leq 0.03\Omega$) and low-inductance (≤ 0.02 nH) connections between the front side pads and the backside wherever RF or dc grounding is desired.

Via holes require additional backside processing steps, including wafer thinning, via etching, and metallization, that increase fabrication time and wafer cost. Also backside processing lowers the yield because now one has to remount wafers with the front side, which has most of the circuitry, down. On the whole, via hole technology adds about 20% to 30% additional cost to wafers. Because most of the present wireless applications are below 3 GHz, where bond wire parasitic effects are not significant, almost all MIMC for such applications are produced without via hole technology, in order to compete with hybrid and printed circuit technologies. Salient features of via hole grounds can be summarized [1, 2] as follows:

1. *Low-inductance grounds:* Low-inductance grounds result in good RF ground returns, which are needed in FET power amplifier stages. An inductance in the source lead manifests itself as a resistive loss in the gate circuit and, hence, results in a reduction in power gain. At 20 GHz, an inductance of 50 pH reduces the gain of a 600-μm gate periphery FET by nearly 2 dB, whereas a 4-pH inductance degrades the gain by only 0.2 dB. Low-inductance grounds improve significantly the device performance at millimeter-wave frequencies. Via hole connections also provide good short circuits for microwave passive circuits.
2. *Excellent thermal paths:* Excellent thermal connections provide better heat-sinking paths for power transistors and also improve their reliability. The source contacts carry away some of the heat generated in FETs, which results in low-noise performance due to low thermal resistance. Thus via holes play an important role in low-noise and power devices.
3. *Compatible with MIC technology:* Although via holes require two more levels of processing steps, the processing is compatible with MIC technology. Other methods of grounding, namely, wrap-arounds, sheet grounding, transformers, and so on, consume a large portion of the available area, whereas via holes require minimal substrate area resulting in much better real estate utilization.

9.2 Via Hole Models

Several different techniques have been applied to develop via hole models. These include analytical methods [3], a quasistatic approach [4], full-wave analysis [5–15], time-domain measurements [16, 17], and *S*-parameter measurement-

based models [18]. Analytical models have limited accuracy; quasistatic models are valid for dimensions much smaller than the operating wavelengths; full-wave techniques provide accurate results but require long computational times; and measurement-based models are valid for only those geometries used in the characterization. These methods are briefly discussed in this section.

9.2.1 Analytical Expression

An analytical expression for the inductance, L_{via}, of a cylindrical via hole shown in Figure 9.3 was obtained by Goldfarb and Pucel [3] and is given below.

$$L_{\text{via}} = 0.2\left[h - \ln\left(\frac{h+\sqrt{r^2+h^2}}{r}\right) + \frac{3}{2}\left(r - \sqrt{r^2+h^2}\right)\right] \quad \text{(pH)} \qquad (9.1)$$

where r and h, the radius and height of the via hole, respectively, are expressed in microns.

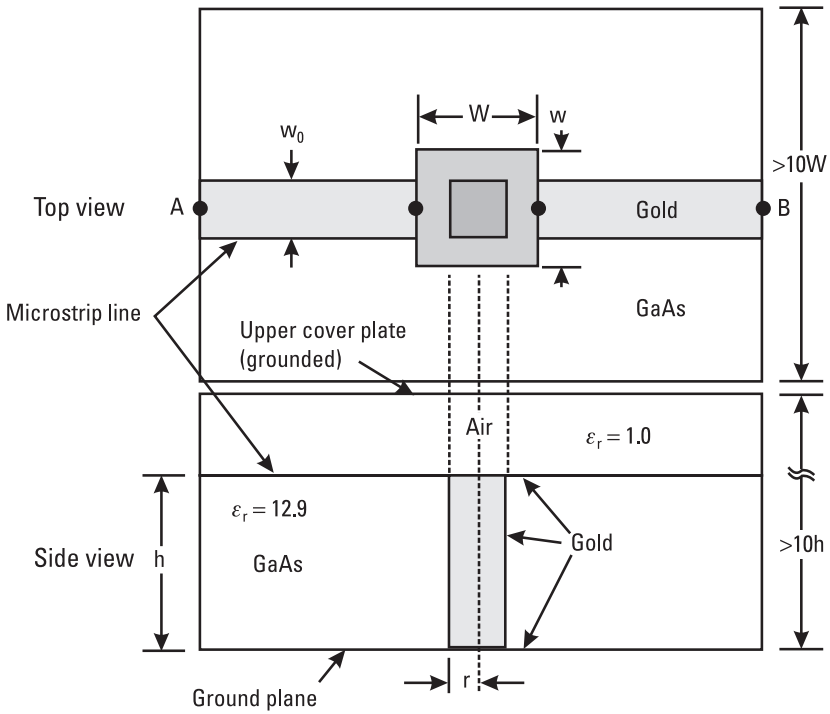


Figure 9.3 Top and side views of a cylindrical via in microstrip configuration. (*From:* [3]. © 1991 IEEE. Reprinted with permission.)

The preceding expression shows good agreement with the measured and EM simulated data. Figure 9.4 shows the variation of via inductance obtained using (9.1) and numerical simulation [5] versus d/h ($d = 2r$) ratio for several GaAs substrate heights. Numerical calculations and (9.1) do not include the effect of via hole pad.

The resistance of the via hole may be approximately calculated using the following expression:

$$R_{\text{via}} = R_{\text{dc}}\sqrt{1 + \frac{f}{f_\delta}} \tag{9.2a}$$

where

$$f_\delta = \frac{1}{\pi \mu_0 \sigma t^2} \tag{9.2b}$$

Here f is the operating frequency, μ_0 the free-space permeability, σ the conductivity of the metal, and t its thickness.

9.2.2 Quasistatic Method

Configuration of two semi-infinitely long wires connected by a via through a circular hole in a ground plane were analyzed using the method of moments by Wang et al [4]. The geometry studied is shown in Figure 9.5. The pi-equivalent circuit model consisting of two excess capacitances C_{e1} and C_{e2} and

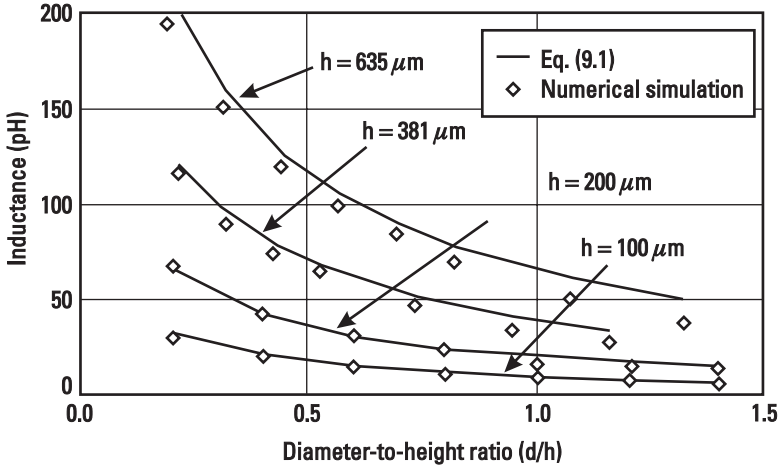


Figure 9.4 Variation of via hole inductance versus diameter-to-height ratio. (*From:* [3]. © 1991 IEEE. Reprinted with permission.)

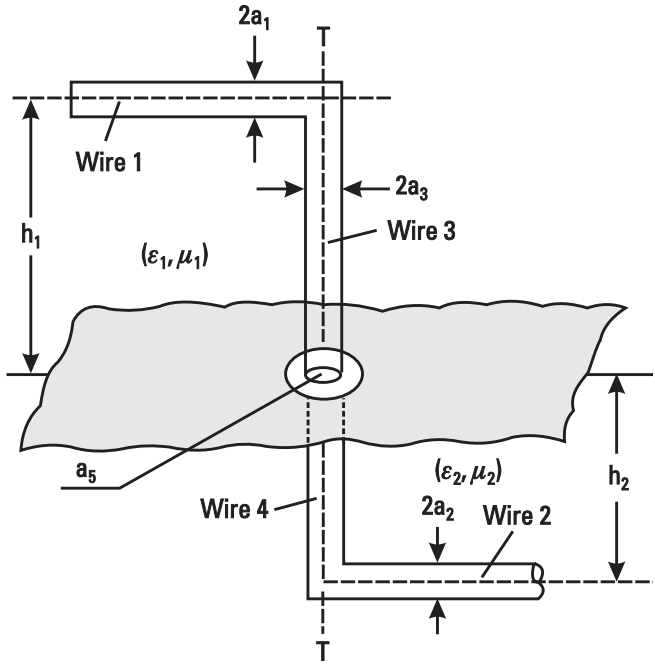


Figure 9.5 Microstrip via through a hole in a ground plane configuration. (*From:* [4]. © 1998 IEEE. Reprinted with permission.)

an excess inductance is shown in Figure 9.6. The via consists of wires 3 and 4 and TT is the plane of reference. The radii of four wire sections 1, 2, 3, and 4 are a_1, a_2, a_3, and a_4, and a_5 is the radius of the via hole. The media above and below the ground plane have permittivities and permeabilities as ϵ_1, μ_1 and ϵ_2, μ_2, respectively, and their heights, h_1 and h_2, are much longer than the wire radii. For nonmagnetic media, $\mu_1 = \mu_2 = \mu_0$. An expression for the excess inductance is given by

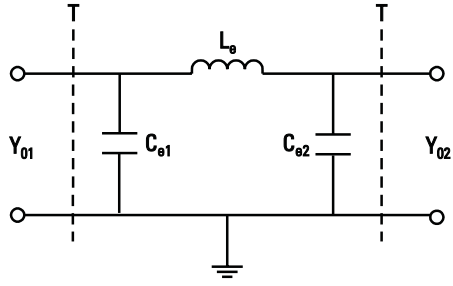


Figure 9.6 EC model for a via through a hole in a ground plane.

$$L_e = \frac{\mu_1}{2\pi} h_1 \ln\left(k_1 \frac{h_1}{a_3}\right) + \frac{\mu_2}{2\pi} h_2 \ln\left(k_2 \frac{h_2}{a_3}\right) \tag{9.3}$$

where k_1 and k_2 are constants and their approximate value is $k_1 = k_2 = 0.5413$. No simple expressions for the excess capacitances are available. Figure 9.7 shows the normalized C_{e1} capacitance as a function of normalized h_1. The curves are also applicable for C_{e2} by replacing subscript 1 by 2.

9.2.3 Parallel Plate Waveguide Model

Hoffman [19] described a via hole model located between the microstrip conductor and ground plane as shown in Figure 9.8 (inset) along with EC model. The model parameter values were obtained using the parallel plate waveguide model as discussed in Chapter 14. Figure 9.8 shows the variations of series inductance and shunt inductance values (normalized with respect to the substrate height) versus the diameter of the via hole (normalized with respect to the microstrip width). The values were calculated for $\epsilon_r = 9.8$ and $h/\lambda_0 = 0.001$. The normalized L_s/h and L_p/h values are functions of ϵ_r, d/W, and h/λ_0. However, it is suggested that the data in Figure 9.8 are still valid within reasonable accuracy over $2.3 \leq \epsilon_r \leq 20$ and $h/\lambda_0 \leq 0.02$. As shown in Figure 9.8, the series element L_s becomes smaller and shunt element L_p becomes larger with decreasing d/W and W/h values.

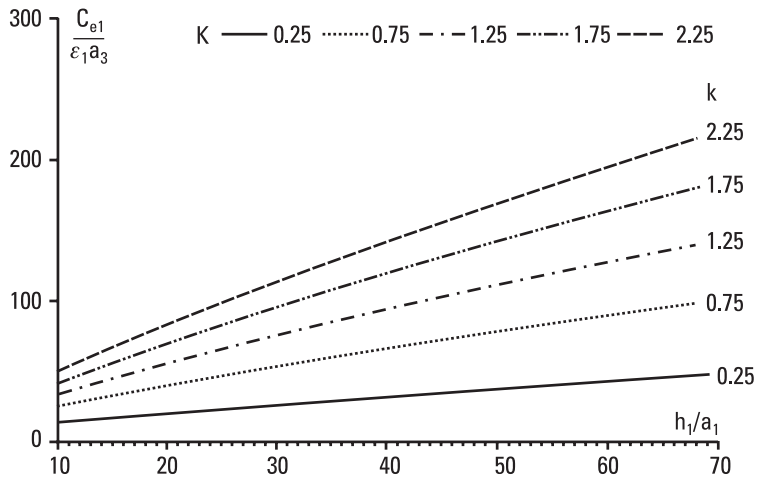


Figure 9.7 Normalized excess capacitance C_{e1} of the upper wire versus h_1/a_1 ratio for $a_5 = 2a_3$ and $k = a_1/a_3$. (*From:* [4]. © 1998 IEEE. Reprinted with permission.)

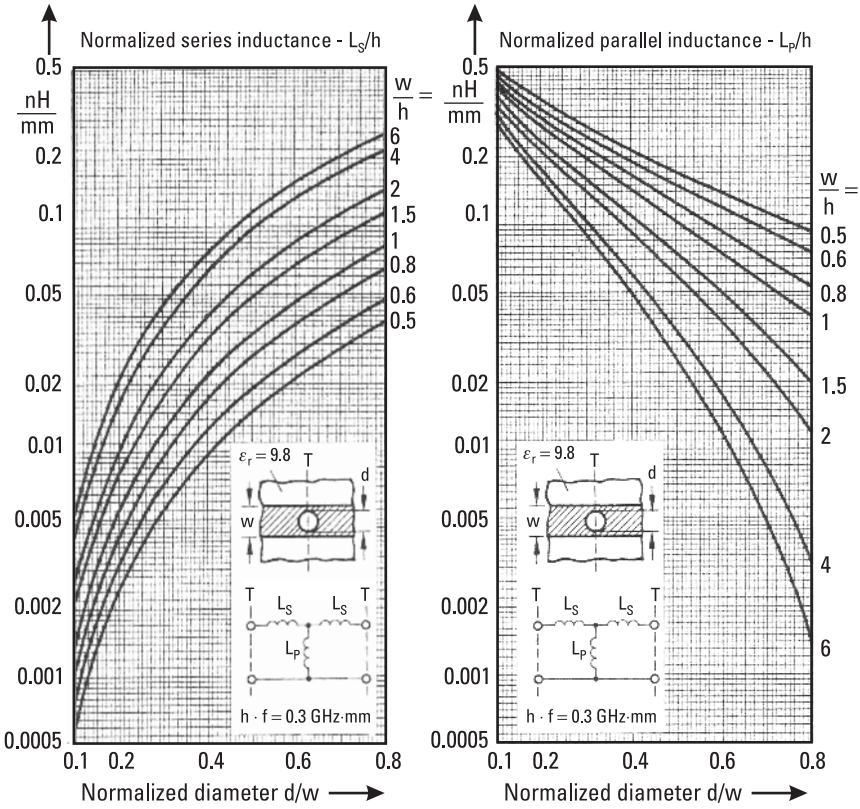


Figure 9.8 Variation of EC model parameter values of a via hole in the microstrip line for series inductance L_s and shunt inductance L_p.

9.2.4 Method of Moments

Single and double via holes were EM simulated using the method of moments. The calculations were performed using Sonnet Software [20] for several line widths over the 2- to 20-GHz bandwidth. The cylindrical hole was approximated by an octagonal hole, and equivalent inductance values were extracted from one-port *S*-parameters. The single via and double via geometries analyzed are shown in Figure 9.9. Dimensions shown are in mils. The substrate used is alumina, $\epsilon_r = 9.8$. The EC model representation is a simple shunt inductor. Figure 9.10(a, b) shows the inductance values of a single via obtained for 15- and 25-mil-thick substrates, respectively.

Figure 9.10(c, d) shows the inductance values of a double via, again for 15- and 25-mil-thick substrates, respectively. Note that, as expected the equivalent inductance for the double via hole is lower than that for a single via hole, but not half due to the mutual coupling as discussed in Chapter 2, which again

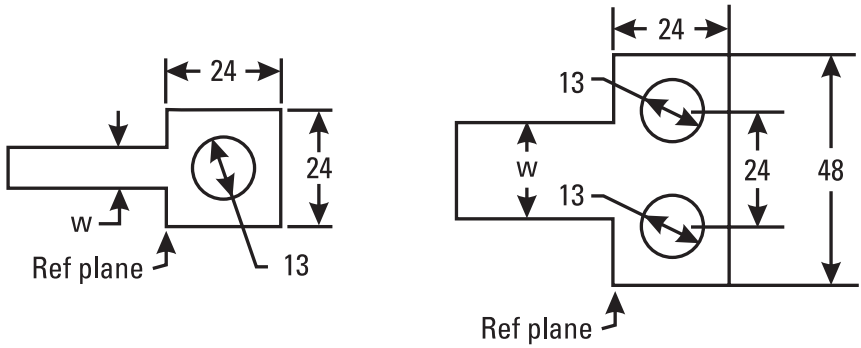


Figure 9.9 Single via and double via configurations.

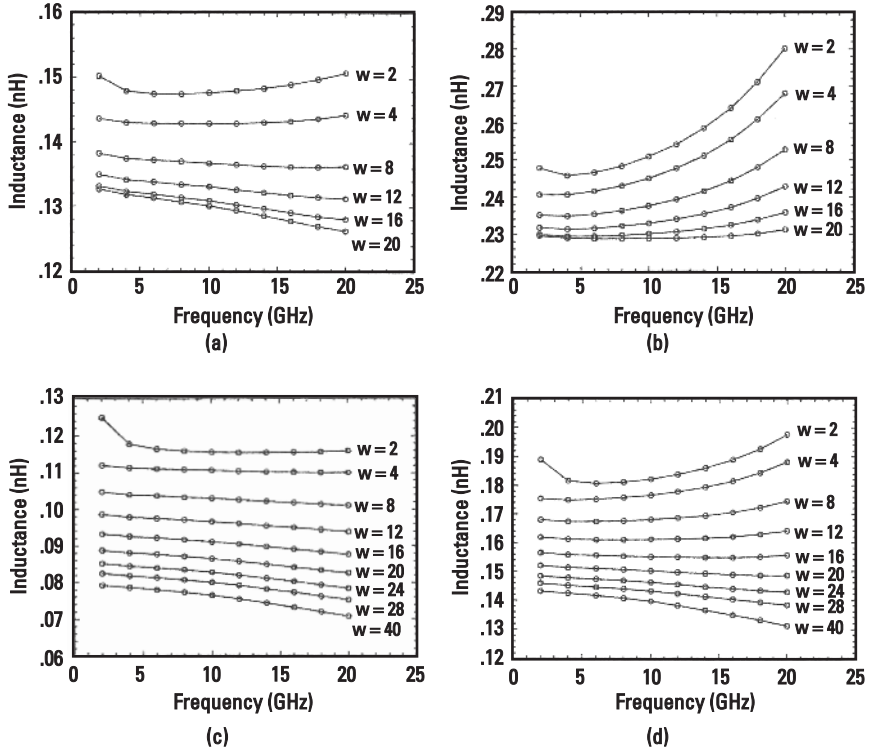


Figure 9.10 Inductance versus frequency: (a) single via, $h = 15$ mil; (b) single via, $h = 25$ mil; (c) double via, $h = 15$ mil; and (d) double via, $h = 25$ mil. (*From:* [20]. © 1992 IEEE. Reprinted with permission.)

depends on the separation between via holes. The sharp increase in equivalent inductance for $W = 2$ mils at 2 GHz is reported to be due to the numerical precision problem in the analysis.

9.2.5 Measurement-Based Model

The measurement-based model of a via hole can be derived using one-port or two-port S-parameters. In this case the via hole structure is represented by a lumped-element EC. Figure 9.11(a) shows the top view of a via hole embedded in the transmission line TRL. The equivalent circuit representation of this element given in Figure 9.11(b) is composed of a series inductance and shunt capacitance associated with the via hole pad and the shunt inductance and

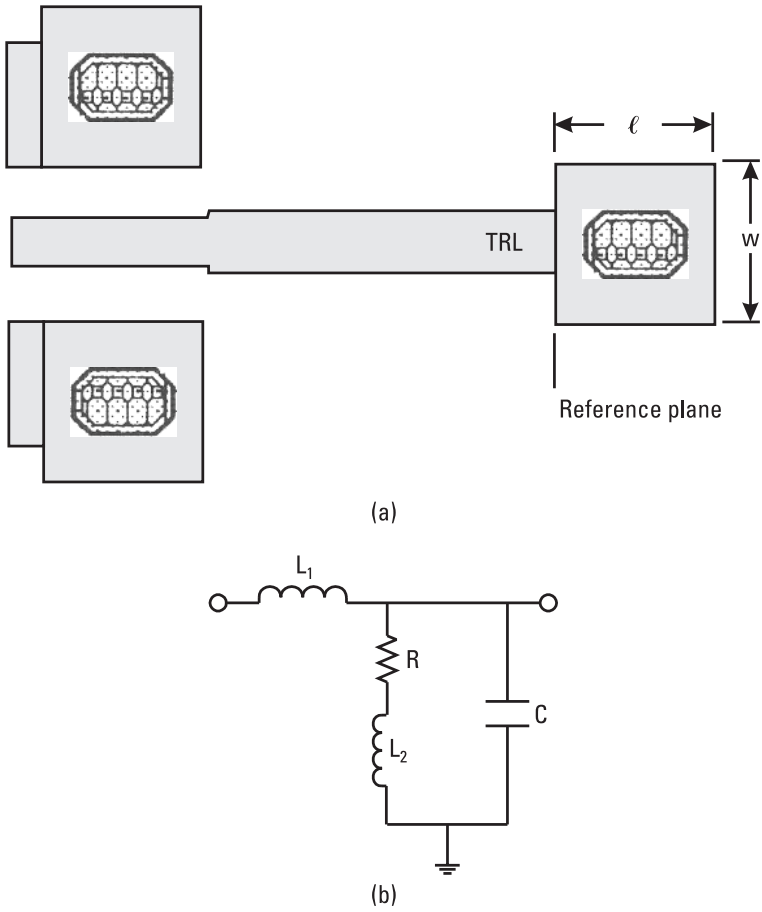


Figure 9.11 (a) Via hole embedded in TRL standard and (b) model of a via hole.

resistance of the metal plug. The comparison between the via hole model and its three measured data sets, shown in Figure 9.12, indicates an excellent correlation. Table 9.2 provides model parameters for two pad dimensions and two substrate thicknesses.

A via hole model has also been validated by comparing the measured and simulated S_{11} data for a 5-pF capacitor terminated by a via hole using a 75-μm-thick GaAs substrate.

9.3 Via Fence

Low-cost RF and microwave systems mandate a higher level of integration and more circuit functions in a smaller package. In other words, one needs to integrate RF/microwave circuits, digital circuits, and interconnect and bias lines in a compact package to lower the volume and cost. When such components are placed in proximity to each other, a fraction of the power present on the

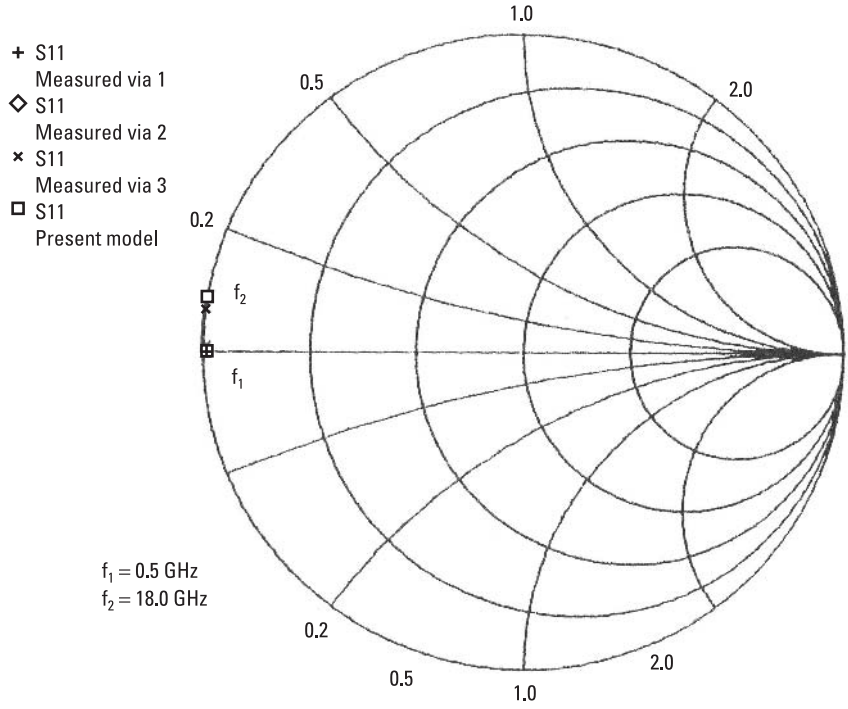


Figure 9.12 Measured versus modeled input reflection coefficient of a via hole. Substrate thickness = 125 μm.

Table 9.2
Physical Dimensions and Equivalent Model Parameters Values for Via Hole of Figure 9.11

Physical Dimensions	**VIA75-1**	**VIA75-2**	**VIA125-1**	**VIA125-2**	**Units**
Width, W	175	225	175	225	μm
Length, ℓ	175	225	175	225	μm
Substrate thickness, h	75	75	125	125	μm
Equivalent Circuit Values	**VIA75-1**	**VIA75-2**	**VIA125-1**	**VIA125-2**	**Units**
Inductance, L_1	0.017	0.023	0.022	0.029	nH
Inductance, L_2	0.003	0.003	0.005	0.005	nH
Resistance, R	0.02	0.02	0.02	0.02	Ω
Shunt capacitance, C	0.09	0.13	0.07	0.10	pF

main structure is coupled to the secondary structure. The power coupled is a function of the physical dimensions of the structure, TEM (transverse electromagnetic) or non-TEM, mode of propagation, the frequency of operation, and the direction of propagation of the primary power. In these structures, there is a continuous coupling between the electromagnetic fields, known as *parasitic coupling* or *cross-talk.* Such parasitic coupling can take place between the distributed matching elements or closely spaced lumped elements, affecting the electrical performance of the circuit in several ways depending on the type of circuit. It may change the frequency response in terms of frequency range and bandwidth and degrade the gain/insertion loss and its flatness, input and output VSWR, and many other characteristics including output power, power-added efficiency, and noise figure. This coupling can also result in the instability of an amplifier circuit or create feedback resulting in a peak or a dip in the measured gain response or a substantial change in a phase-shifter response.

In general, this parasitic coupling is undesirable and an impediment in obtaining an optimal solution in a circuit design. However, this coupling effect can be reduced by using metal-filled via holes known as a *via fence* [21–23]. Via fences provide an electric wall between the fringing fields and are commonly used in single and multilayer ceramic technologies, silicon and GaAs MIC technologies, and *system-on-a package* (SOP) technology. In this structure, connecting via top pads by a strip improves the isolation between the structures by 6 to 10 dB.

To accurately determine such coupling, an electromagnetic simulator such as three-dimensional finite-element method was used [24]. The results of the analysis is for the structure, fabricated in LTCC technology, are shown in Figure 9.13. The parameters for the structure are given in Table 9.3.

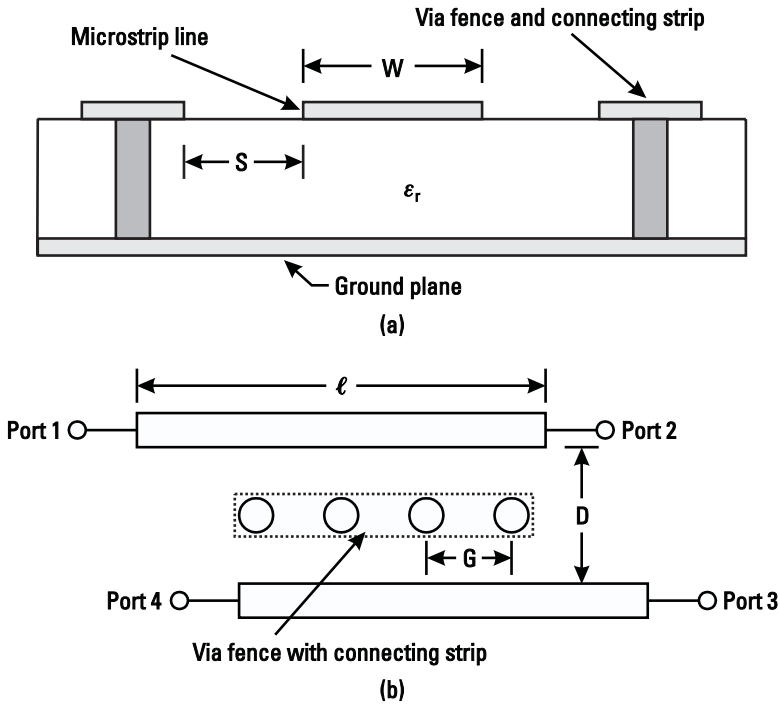


Figure 9.13 Via hole fence: (a) cross-sectional view and (b) four-port circuit configuration.

Table 9.3
Summary of Substrate, Microstrip, and Via Hole Parameters Used to Calculate Isolation Between Two Microstrip Lines in the Via Fence Structure

Substrate:	Glass-ceramic	$\epsilon_r = 5.2$
	Thickness	$h = 0.25$ mm
Microstrip:	Width	$W = 0.414$ mm (50Ω)
	Length	$\ell = 11.7$ mm
	Distance between lines	$D = 1.814$ mm
Via:	Diameter	$d = 0.25$ mm
	Distance between microstrip and via fence	$S = 0.75$ mm

Figure 9.14 shows the calculated forward coupling between two microstrip lines, with and without a via fence, versus frequency. Here, G is the distance between via posts, center to center, and "no strip" means vias are not connected by the strip on the top side. The data show that the via fence with strip improves coupling by about 8 dB, whereas via posts without strip degrade coupling

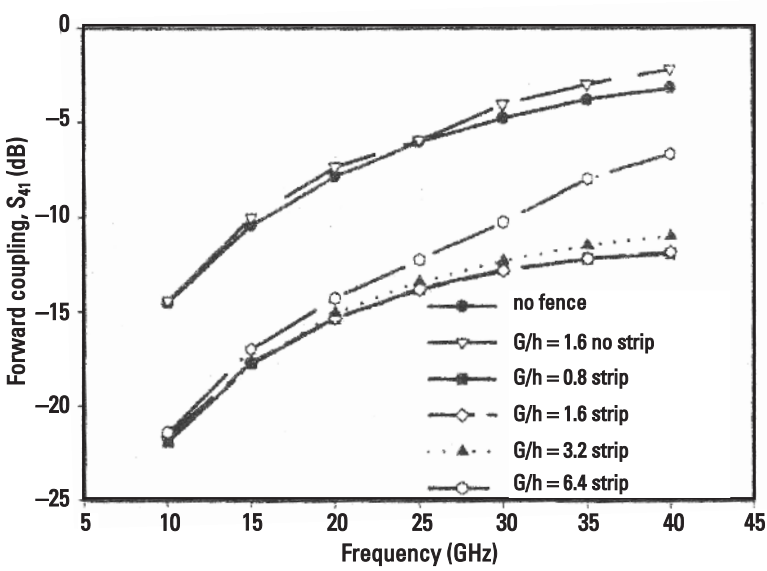


Figure 9.14 Coupling coefficient versus frequency for various G/h values. (*From:* [24]. © 2001 IEEE. Reprinted with permission.)

at high frequencies. Larger spacing between vias also degrades coupling with frequency.

9.3.1 Coupling Between Via Holes

The coupling between two via holes was analyzed using an EM simulator. Figure 9.15(a) shows the structure, where D is the separation between via hole pads. The pad is a square geometry having a side dimension of 165 μm. The substrate is 125-μm-thick GaAs. The coupling between two via holes versus frequency for four separations (15, 100, 200, and 400 μm) is shown in Figure 9.15(b). The coupling for offset via holes, as shown in Figure 9.16(a), was also evaluated. Figure 9.16(b) shows the coupling coefficient versus frequency for four offset S values (40, 80, 165, and 330 μm) and $D = 60$ μm. The coupling is a strong function of distance between via hole plugs and does not depend on their orientations.

9.3.2 Radiation from Via Ground Plug

At low frequencies, a via hole acts as a short; however, as the frequency increases, the reactive component and radiation resistance become significant at high frequencies. Cerri et al. [25] have calculated the radiation resistance using a full-wave analysis. In this case, the via hole is represented by a series combination

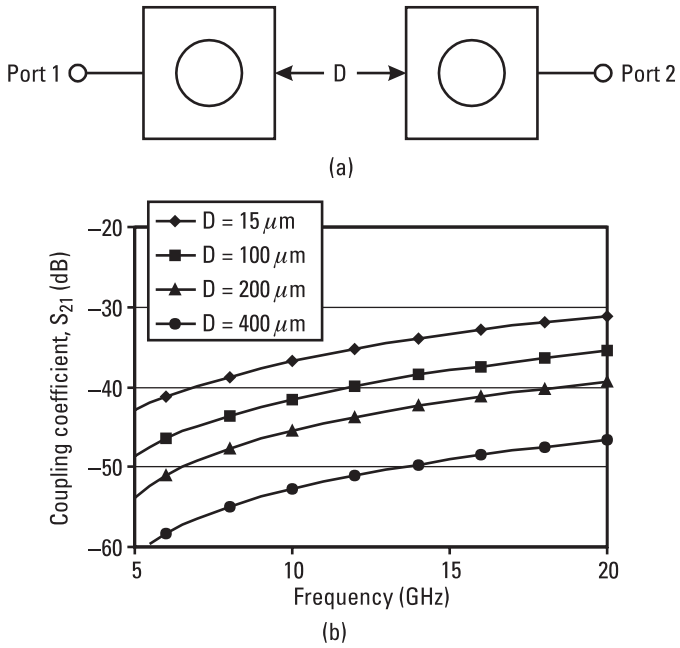


Figure 9.15 (a) Two via hole configuration and (b) simulated coupling coefficient versus frequency.

of an inductor and a radiation resistance. Figure 9.17 shows a plot of calculated frequency dependence of radiation resistance for an 80-μm-diameter via hole. The GaAs substrate thickness was 200 μm. Although the radiation resistance becomes significant at millimeter-wave frequencies, its value below 20 GHz is negligible.

9.4 Plated Heat Sink Via

In MMICs, active devices such as FETs, HEMTs, and HBTs have via hole grounds for source pads and emitter pads, respectively. Such ground connections have appreciable inductance to reduce gain at higher frequencies. To lower source inductance and reduce thermal resistance of FETs, *plated heat sinks* (PHS) are widely used for discrete devices. In this case (shown in Figure 9.18), each source pad is connected to the PHS through the holes underneath these pads.

9.5 Via Hole Layout

When an MMIC chip is mounted on a substrate (alumina, BeO, AlN, and so on), establishing a good ground connection between the back of the chip and

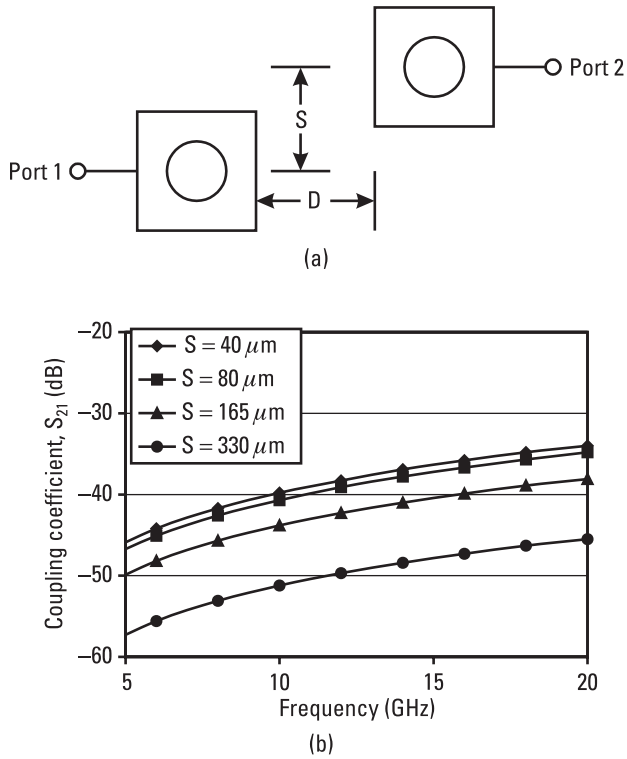


Figure 9.16 (a) Two via holes in offset configuration and (b) simulated coupling coefficient versus frequency.

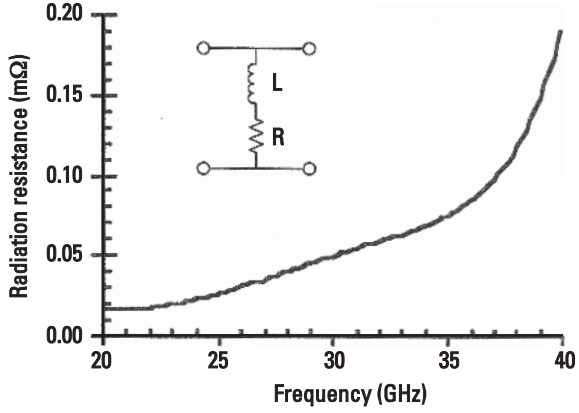


Figure 9.17 Radiation resistance of a via hole.

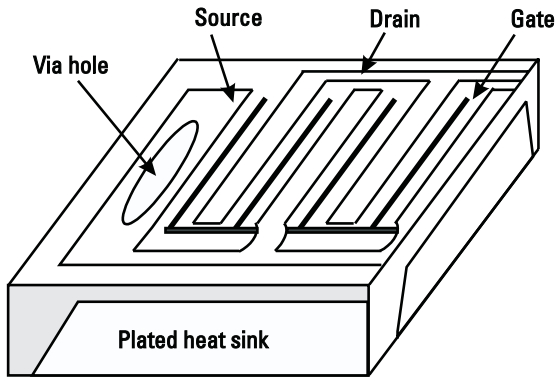


Figure 9.18 PHS geometry.

the back of the substrate is essential. Here the substrate is epoxied/soldered to a conductor or a fixture. A poorly grounded MMIC chip may exhibit reduced performance or spurious oscillations [26]. To minimize these effects, several via holes are used to connect the mounting pad under the footprint of the chip to case ground. The layout of such via holes and their numbers helps greatly in the elimination of resonant modes in the mounting pad. A large number of via holes, permitted by substrate technology and cost, are generally used to ensure the reproduction of the MMIC performance. Several other factors including thinner substrates, larger via hole size, via spacings of less than $\lambda/20$ at the maximum operating frequency, and chips having minimum possible out-of-band gain help in achieving acceptable RF performance and eliminate spurious oscillations.

References

[1] Ferry, D. K., (Ed.), *Gallium Arsenide Technology,* Indianapolis, IN: Howard W. Sams, 1985, Chap. 6.

[2] Goyal, R., (Ed.), *High Frequency Analog Integrated Circuit Design,* New York: John Wiley, 1995, Chap. 4.

[3] Goldfarb, M. E., and R. A. Pucel, "Modeling Via Hole Grounds in Microstrip," *IEEE Microwave Guided Wave Lett.,* June 1991, Vol. 1, pp. 135–137.

[4] Wang, T., R. F. Harrington, and J. Mautz, "Quasi-Static Analysis of a Microstrip Via Through a Hole in a Ground Plane," *IEEE Trans. Microwave Theory Tech.,* June 1988, Vol. 36, pp. 1008–1013.

[5] Rautio, J. C., and R. F. Harrington, "An Electromagnetic Time-Harmonic Analysis of Shielded Microstrip Circuits," *IEEE Trans. Microwave Theory Tech.,* August 1987, Vol. MTT-35, pp. 726–730.

[6] Finch, K. L., and N. G. Alexopoulos, "Shunt Posts in Microstrip Transmission Lines," *IEEE Trans. Microwave Theory Tech.,* November 1990, Vol. 38, pp. 1585–1594.

[7] Maeda S., T. Kashiwa, and I. Fukai, "Full Wave Analysis of Propagation Characteristics of a Through Hole Using the Finite Difference Time-Domain Method," *IEEE Trans. Microwave Theory Tech.,* December 1991, Vol. MTT-39, pp. 2154–2159.

[8] Tsai, W. J., and J. T. Aberle, "Analysis of a Microstrip Line Terminated With a Shorting Pin," *IEEE Trans. Microwave Theory Tech.,* April 1992, Vol. MTT 40, pp. 645–651.

[9] Becker, W. D., P. Harms, and R. Miltra, "Time Domain Electromagnetic Analysis of a Via in a Multilayer Computer Chip Package," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1992, pp. 1129–1232.

[10] Jansen, R. H., "A Full-Wave Electromagnetic Model of Cylindrical and Conical Via Hole Grounds for Use in Interactive MIC/MMIC Design," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1992, pp. 1233–1236.

[11] Sorrentino, R., et al., "Full Wave Modeling of Via-Hole Grounds in Microstrip by Three Dimensional Mode Matching Technique," *IEEE Trans. Microwave Theory Tech.,* December 1992, Vol. MTT-40, pp. 2228–2234.

[12] Visan, S., O. Picon, and V. Fouad Hanna, "3D Characterization of Air Bridges and Via Holes in Conductor-Backed Coplanar Waveguides for MMIC Applications," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1993, pp. 709–712.

[13] Eswarappa, C., and W. J. R. Hoefer, "Time Domain Analysis of shorting Pins in Microstrip Using 3-D SCN TLM," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1993, pp. 917–920.

[14] Cerri, G., M. Mongiardo, and T. Rozzi, "Full-Wave Equivalent Circuit of Via Hole Grounds in Microstrip," *Proc. 23rd European Microwave Conf.,* 1993, pp. 207–208.

[15] Tsai, M. J., et al., "Multiple Arbitrary Shape Via-Hole and Air-Bridge Transitions in Multi-Layered Structures," *IEEE Trans. Microwave Theory Tech.,* Vol. 44, December 1996, pp. 2504–2511.

[16] LaMeres, B. J., and T. S. Kalkur, "Time Domain Analysis of Printed Circuit Board Via," *Microwave J.,* Vol. 43, November 2000, pp. 76–84.

[17] LaMeres, B. J., and T. S. Kalkur, "The Effect of Ground Vias on Changing Signal Layers in a Multilayered PCB," *Microwave Opt. Tech. Lett.,* Vol. 28, February 2001, pp. 257–260.

[18] Sadhir, V. K., I. J. Bahl, and D. A. Willems, "CAD Compatible Accurate Models of Microwave Passive Lumped Elements for MMIC Applications," *Int. J. Microwave Millimeter-Wave Computer-Aided Engineering,* Vol. 4, April 1994, pp. 148–162.

[19] Hoffman, R. K., *Handbook of Microwave Integrated Circuits,* Norwood, MA: Artech House, 1987, Chap. 10.

[20] Swanson, D. G., "Grounding Microstrip Lines with Via Holes," *IEEE Trans. Microwave Theory Tech.,* Vol. 40, August 1992, pp. 1719–1721.

[21] Ponchak, G. E., et al., "The Use of Metal Filled Via Holes for Improving Isolation in LTCC RF and Wireless Multichip Packages," *IEEE Trans. Advanced Packaging,* Vol. 23, February 2000, pp. 88–99.

[22] Gipprich, J. W., "EM Modeling of Via Wall Structures for High Isolation Stripline," *IEEE MTT-S Int. Microwave Symp. Dig.,* San Diego, CA, June 1994, pp. 78–114.

[23] Gipprich, J., and D. Stevens, "Isolation Characteristics of Via Structures in High Density Stripline Packages," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1998.

[24] Ponchak, G. E., et al., "Experimental Verification of the Use of Metal Filled Via Hole Fences for Crosstalk Control of Microstrip Lines in LTCC Packages," *IEEE Trans. Advanced Packaging,* Vol. 24, February 2001, pp. 76–80.

[25] Cerri, G., M. Mongiarzdo, and T. Rozzi, "Radiation from Via-Hole Grounds in Microstrip Lines," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1994, pp. 341–344.

[26] Swanson, D., D. Baker, and M. O'Mahoney, "Connecting MMIC Chips to Ground in a Microstrip Environment," *Microwave J.,* Vol. 36, December 1993, pp. 58–64.

10

Airbridges and Dielectric Crossovers

10.1 Airbridge and Crossover

The primary purpose of airbridges and dielectric crossovers is to provide a cross-connection for two nonconnecting printed transmission-line sections as shown in Figure 10.1. They are also commonly employed in transistors (e.g., to create a nonconnecting crossover between a multiple source and gate or emitter and base), electrodes, spiral inductors and transformers, MIM capacitors (to improve the breakdown voltage), Lange couplers (to connect alternate lines), and *coplanar waveguide* (CPW) based MMICs to connect both ground planes in order to suppress the propagation of the coupled slotline mode.

Airbridges use air as the dielectric between the two conductors, whereas dielectric crossovers employ a layer of low dielectric constant material such as polyimide or BCB. Airbridges and dielectric crossovers have also been used in reducing the shunt capacitance between the conductors and the ground plane in MMIC spiral inductors and transformers. Such structures are called *airbridged inductors* and *transformers.* Low shunt capacitance is a desirable feature of a component to extend the maximum operating frequency.

The airbridge and dielectric crossover allow MICs using multilayer technologies to have one conductor crossing over another. This crossover consists of a metal strap that bridges one or more conductors on the substrate surface. The strap is separated from the bottom conductors by a 1.5- to 3-μm air gap. A good example of airbridge use is in the design of a spiral inductor, which requires a connection to its inner terminal [Figure 10.2(a)]. Depositing photoresist over the conductors to be crossed forms the airbridge. The crossover metal is deposited on the photoresist and plated, after which the photoresist is removed, forming an airbridge. Figure 10.2(b) shows a blowup of the airbridge structure

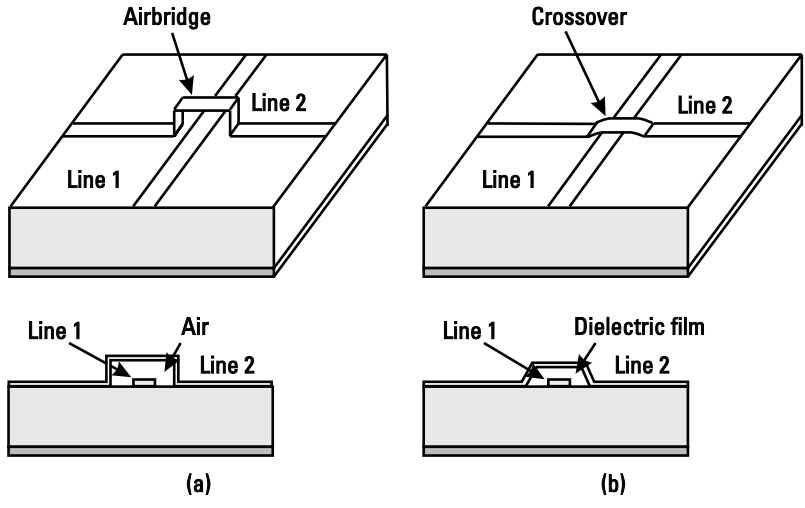


Figure 10.1 Airbridge and crossover configurations: (a) airbridge and (b) crossover.

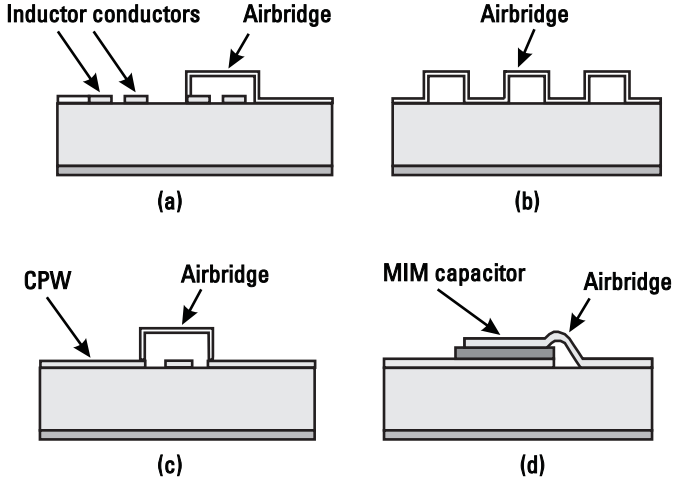


Figure 10.2 Applications of airbridge or crossover: (a) inductor, (b) suspended microstrip, (c) CPW, and (d) capacitor.

used in a suspended coil inductor. Figure 10.2(c, d) shows airbridge applications in CPW line and a MIM capacitor. Multilayer structures are generally fabricated in MMICs using very thin dielectric layers of insulating materials such as silicon nitride ($\epsilon_{rd} \cong 6.7$) and polyimide ($\epsilon_{rd} \cong 3.2$). The dielectric constant of these materials can vary from foundry to foundry depending on the composition used.

10.2 Analysis Techniques

Analyses of airbridges and dielectric crossovers can be carried out by treating them as multilayered structures [1, 2]. Airbridge structures, such as that shown in Figure 10.2(b), can be approximately analyzed using multilayer dielectric microstrip lines, whereas crossover geometry, shown in Figure 10.1(b), is accurately analyzed using three-dimensional EM simulators as described in Chapter 2. Analysis of multilayered dielectric microstrip lines has been performed using quasistatic analyses, such as the variational method [3–5], and full-wave methods including spectral-domain [1, 2, 6–8], *finite-difference time-domain* (FDTD) [9, 10], and finite-difference [11] methods and the method of moments [12].

10.2.1 Quasistatic Method

For the quasistatic analysis of multilayer microstrip transmission lines having two or more dielectric interfaces, the variation method is found to be the simplest. This method requires setting up either the potential function or the Green's function for the geometry under investigation. These functions are derived either by solving a set of algebraic equations obtained by applying the boundary conditions at various interfaces [3–5] or by using the *transverse transmission-line method* [13, 14]. The latter approach is simpler. For the sake of simplicity, the strip conductor is assumed to be infinitely thin.

The boundary conditions and continuity conditions of the structure, shown in Figure 10.3, in the Fourier transform domain are given as follows:

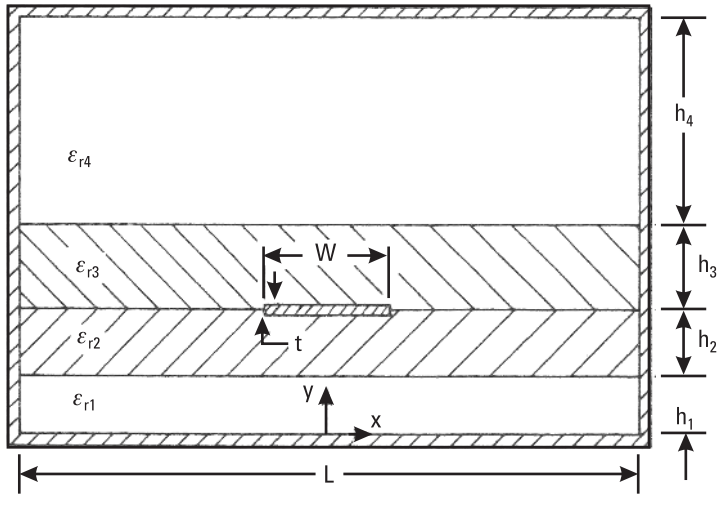


Figure 10.3 Microstrip-like multilayer dielectric transmission-line configuration.

$$\tilde{\phi}(\beta, 0) = 0 \tag{10.1a}$$

$$\tilde{\phi}(\beta, h_4') = 0 \tag{10.1b}$$

$$\tilde{\phi}(\beta, h_1 + 0) = \tilde{\phi}(\beta, h_1 - 0) \tag{10.1c}$$

$$\epsilon_{r1} \frac{d}{dy} \tilde{\phi}(\beta, h_1 + 0) = \epsilon_{r2} \frac{d}{dy} \tilde{\phi}(\beta, h_1 - 0) \tag{10.1d}$$

$$\tilde{\phi}(\beta, h_2' + 0) = \tilde{\phi}(\beta, h_2' - 0) \tag{10.1e}$$

$$\epsilon_{r2} \frac{d}{dy} \tilde{\phi}(\beta, h_2' + 0) = \epsilon_{r3} \frac{d}{dy} \tilde{\phi}(\beta, h_2' - 0) - \frac{\tilde{f}(\beta)}{\epsilon_0} \tag{10.1f}$$

$$\tilde{\phi}(\beta, h_3' + 0) = \tilde{\phi}(\beta, h_3' - 0) \tag{10.1g}$$

$$\epsilon_{r3} \frac{d}{dy} \tilde{\phi}(\beta, h_3' + 0) = \epsilon_{r4} \frac{d}{dy} \tilde{\phi}(\beta, h_3' - 0) \tag{10.1h}$$

and

$$h_2' = h_1 + h_2,\ h_3' = h_1 + h_2 + h_3 \quad \text{and} \quad h_4' = h_1 + h_2 + h_3 + h_4$$

where $\tilde{\phi}$ and $\tilde{f}$ are the Fourier transforms of the potential and charge distribution functions respectively, β is the Fourier transform variable, the h_i values represent the thicknesses of the dielectric sheet materials, and $\epsilon_{ri} = \epsilon_i / \epsilon_0$, where ϵ_0 is the free-space permittivity. Substituting these conditions in the general solution of the Poisson's equation, one obtains the potential distribution on the strip in terms of $\tilde{f}(\beta)$. The variational expression for the line capacitance in the β coordinate can be written as

$$\frac{1}{C} = \frac{1}{2\pi Q^2} \int_{-\infty}^{\infty} \tilde{f}(\beta)\, \tilde{\phi}(\beta, h_2')\, d\beta \tag{10.2}$$

where Q denotes the total charge on the strip conductor and is given by

$$Q = \int_{-\infty}^{\infty} f(x)\, dx \tag{10.3}$$

$$\tilde{f}(\beta) = \int_{-\infty}^{\infty} f(x)\, e^{j\beta x}\, dx \tag{10.4}$$

The function $f(x)$ represents charge distribution on the strip conductor. In the variational method, one can use an approximate trial function for $f(x)$ and incur only a second-order error in (10.2). In the present case, the charge distribution on the strip conductor has been assumed as follows:

$$f(x) = \begin{cases} 1 + \left|\dfrac{2x}{W}\right|^3 & -W/2 < x < W/2 \\ 0 & \text{elsewhere} \end{cases} \tag{10.5}$$

From (10.3), (10.4), and (10.5),

$$\frac{\tilde{f}(\beta)}{Q} = 1.6\left\{\frac{\sin(\beta W/2)}{\beta W/2}\right\} + \frac{2.4}{(\beta W/2)^2} \times \left\{\cos(\beta W/2) - \frac{2\sin(\beta W/2)}{(\beta W/2)} + \frac{\sin^2(\beta W/4)}{(\beta W/4)^2}\right\} \tag{10.6}$$

To solve (10.2), we still need to find the $\tilde{\phi}(\beta, h_2')$ function. The Fourier transforms of the potential function $\tilde{\phi}(\beta, h_2')$ can be determined by solving (10.1a)–(10.1h) or by using a transverse transmission-line approach, which is discussed next. Using the standard procedure for transmission lines as delineated in Figure 10.4, the admittance in the charge plane can be written

$$Y = Y_2 + Y_3 \tag{10.7}$$

where

$$Y_2 = \epsilon_{r2}\,\frac{Y_1 + \epsilon_{r2}\tanh(\beta h_2)}{\epsilon_{r2} + Y_1\tanh(\beta h_2)} \tag{10.8a}$$

$$Y_3 = \epsilon_{r3}\,\frac{Y_4 + \epsilon_{r3}\tanh(\beta h_3)}{\epsilon_{r3} + Y_4\tanh(\beta h_3)} \tag{10.8b}$$

and

$$Y_1 = \epsilon_{r1}\coth(\beta h_1) \tag{10.8c}$$

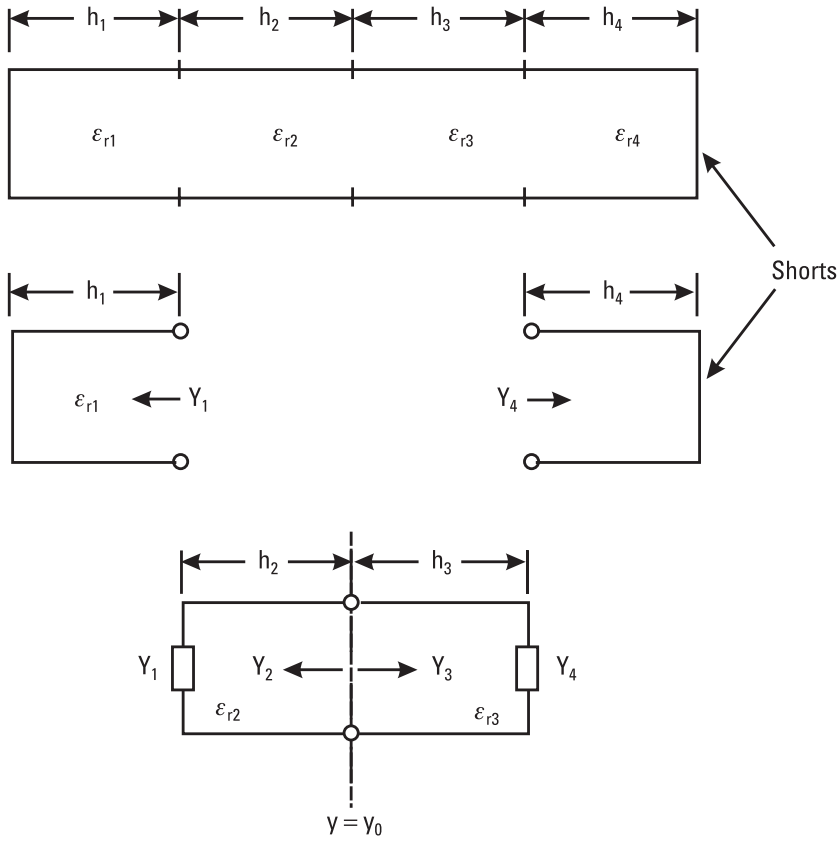


Figure 10.4 Equivalent transmission-line model.

$$Y_4 = \epsilon_{r4} \coth(\beta h_4) \tag{10.8d}$$

For standard open microstrip, $h_2 = h_3 = 0$, $h_4 = \infty$:

$$Y = \epsilon_{r1} \coth(\beta h_1) + 1 \tag{10.9}$$

For shielded microstrip, $h_2 = h_3 = 0$

$$Y = \epsilon_{r1} \coth(\beta h_1) + \epsilon_{r4} \coth(\beta h_4) \tag{10.10}$$

For two-layer open microstrip, $h_3 = 0$, $h_4 = \infty$

$$Y = \epsilon_{r2} \frac{\epsilon_{r1} + \epsilon_{r2} \tanh(\beta h_1) \tanh(\beta h_2)}{\epsilon_{r2} \tanh(\beta h_1) + \epsilon_{r1} \tanh(\beta h_2)} + 1 \tag{10.11}$$

The potential function $\tilde{\phi}$ in terms of the admittance Y is given by

$$\tilde{\phi}(\beta, h_2') = \frac{f(\beta)}{\epsilon_0 \beta Y} \tag{10.12}$$

From (10.2) and (10.9)

$$\frac{1}{C} = \frac{1}{\pi \epsilon_0 Q^2} \int_0^\infty \frac{f^2(\beta)}{\beta Y}\, d\beta \tag{10.13}$$

From (10.11) and (10.13), for a two-layer open microstrip,

$$\frac{1}{C} = \frac{1}{\pi \epsilon_0 Q^2} \int_0^\infty \frac{f^2(\beta)\, d(\beta h)}{\left[\epsilon_{r2} \dfrac{\epsilon_{r1} + \epsilon_{r2} \tanh(\beta h_1) \tanh(\beta h_2)}{\epsilon_{r2} \tanh(\beta h_1) + \epsilon_{r1} \tanh(\beta h_2)} + 1\right](\beta h)} \tag{10.14}$$

Substituting (10.6) in (10.14), the resulting integral can be evaluated using numerical techniques. After evaluating the capacitance C for a unit length of the microstrip with the dielectric layers present and the capacitance C_a when all dielectric layers are replaced by air, the characteristic impedance Z_0 and the effective dielectric constant ϵ_{re} can be determined from these capacitances as follows:

$$Z_0 = \frac{1}{c\sqrt{CC_a}} \tag{10.15a}$$

$$\epsilon_{re} = \frac{C}{C_a} \tag{10.15b}$$

or

$$C = \frac{\sqrt{\epsilon_{re}}}{Z_0 c} \tag{10.16a}$$

$$L = \frac{Z_0 \sqrt{\epsilon_{re}}}{c} \tag{10.16b}$$

where capacitance C and inductance L are per unit length of a microstrip line, and c is the velocity of light. If $c = 3 \times 10^8$ m/s, then C and L are expressed as F/m and H/m, respectively.

Figure 10.5 shows the calculated capacitance and inductance per unit length of a microstrip as a function of strip width for various values of air and polyimide thickness under the conductor. The substrate was 125-μm-thick GaAs ($\epsilon_r = 12.9$) and the gold conductors were 4.5 μm thick. The capacitance reduces significantly even for small thicknesses, whereas the inductance is almost constant.

10.2.2 Full-Wave Analysis

10.2.2.1 Spectral-Domain Techniques

The analysis of a microstrip line, shown in the inset of Figure 10.5(a), was performed using the spectral-domain technique [8]. The simulated results are shown in Figure 10.6 for C and L when the GaAs substrate is 100 μm thick and the separation between the substrate and thin conductor d varies from 0 to 10 μm. The capacitance drops to about 35% of its nonbridged value when the airbridge is about 3 μm high. However, the change in the inductance is very small.

Goldfarb and Tripathi [8] also simulated spiral inductors with and without an airbridge using the spectral-domain technique and revealed their effect on the self-resonant frequency. Two nine-segment inductors, one having and airbridge [Figure 10.2(b)] and the other using the standard process (i.e., inductor pattern placed directly on GaAs substrate), were simulated. The inductor with the airbridge has approximately 50% of its inductor length 3 μm high above the 100-μm-thick GaAs substrate surface. The physical parameters for the inductors were $W = 10$ μm, $S = 5$ μm, outside width = 149 μm, and outside length = 132 μm. The inside port of the inductor was grounded using a via hole. The calculated SRF for the airbridged inductor was 19.7 GHz compared to 18.55 GHz for the standard inductor. This 6.2% increase in the resonant frequency was due to an approximately 12.8% lower shunt capacitance.

10.2.2.2 Method of Moments

The multilayer microstrip was also analyzed using the method of moments [15]. Several multilayer microstrip lines on alumina, GaAs, and high-K substrates were analyzed using the Sonnet EM simulator. Figures 10.7, 10.8, and 10.9 show the characteristic impedance, Z_0, and effective dielectric constant, ϵ_{re}, versus polyimide thickness for $\epsilon_r = 9.9$, 12.9, and 20, respectively. The substrate thickness values for these materials are 380, 75, and 250 μm, respectively. The characteristic impedance increases and ϵ_{re} decreases with increasing polyimide thickness d. For a small value of d, the change in the Z_0 and ϵ_{re} values is large with respect to $d = 0$. As can be noted by using a thin layer of polyimide material, the impedance can be increased by more than 50%, and impedance values as large as 125 to 140Ω can easily be realized on thin substrates.

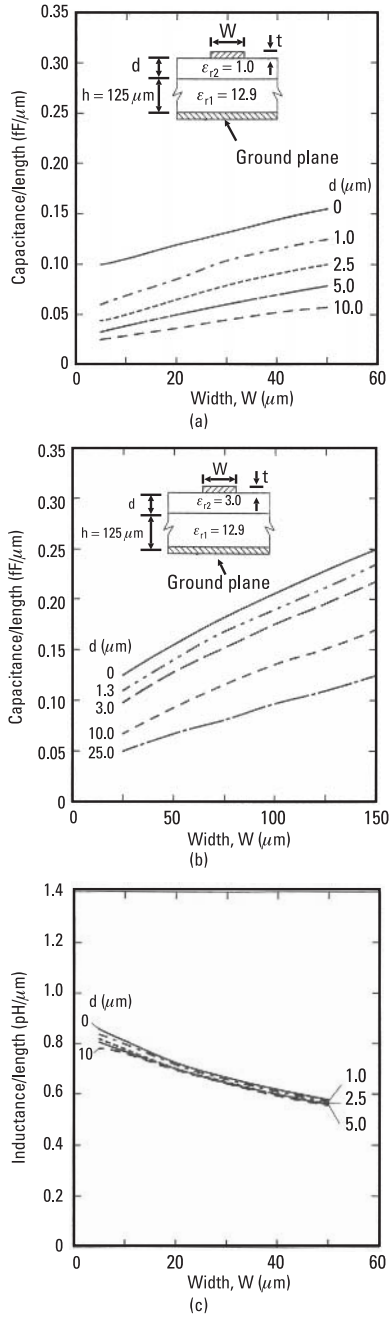


Figure 10.5 Calculated capacitance and inductance per unit length of a multilayer GaAs microstrip of various values of d and W, for $h = 125$ μm and $t = 4.5$ μm: (a) capacitance for airbridge, (b) capacitance for crossover, and (c) inductance for crossover.

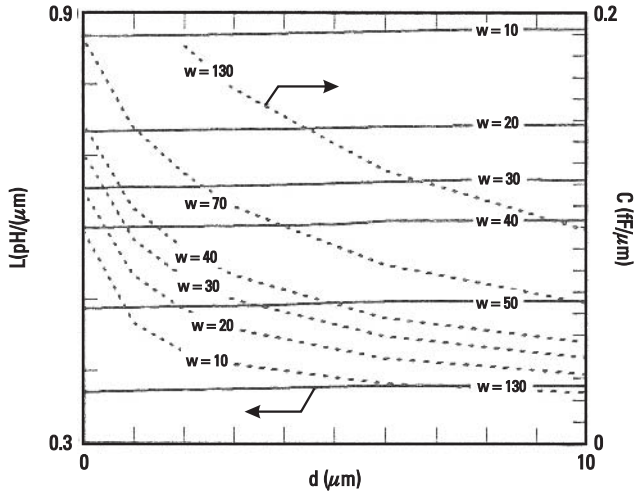


Figure 10.6 Calculated inductance and capacitance per unit length versus airbridge height.

Figure 10.10 shows the calculated capacitance per unit length of a microstrip line versus the polyimide thickness. Even thin layers of low dielectric constant under the microstrip conductors reduce the capacitance significantly. This feature can effectively be used to reduce the parasitic capacitance of a lumped inductor, thereby extending the maximum operating frequency, as discussed in Section 3.2 of Chapter 3 or such microstrip lines can be used in matching networks to tune out the device capacitance over a wider bandwidth.

10.3 Models

Both analytical and measurement techniques have been used to develop equivalent circuit models for the airbridge. These are discussed next.

10.3.1 Analytical Model

A simple representation of an airbridge is the parallel plate capacitance given by

$$C = \frac{\epsilon_0 \epsilon_{rd} A}{d} \tag{10.17}$$

where ϵ_{rd} is the dielectric constant between the plates, A is the overlap area, and d is the separation between the two conductors. A more accurate model for an airbridge in CPW technology is given by [16] and shown in Figure 10.11. Here

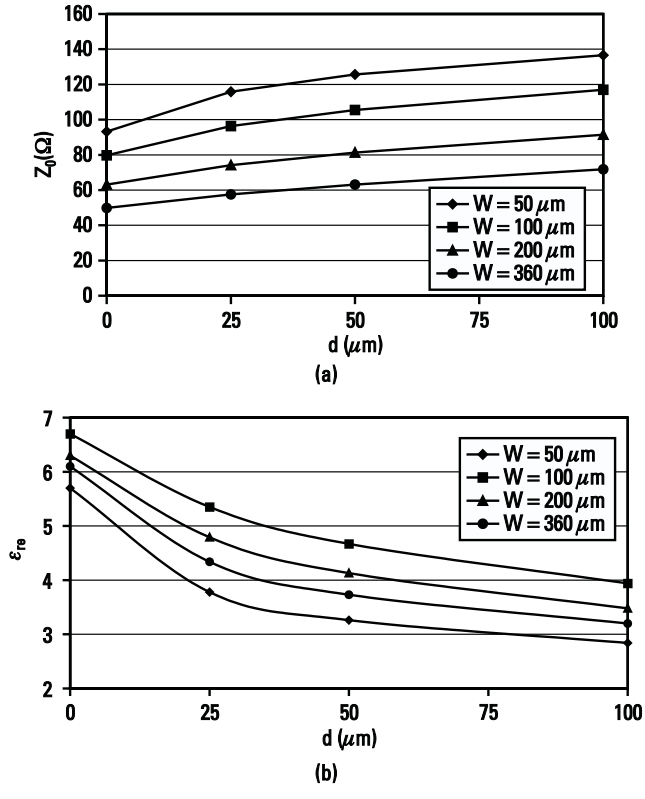


Figure 10.7 Calculated characteristics of multilayer microstrip lines on alumina substrate, $\epsilon_r = 9.9$, $h = 380$ μm, $t = 6$ μm for (a) Z_0 and (b) ϵ_{re}.

$$C = C_p + C_b \tag{10.18a}$$

$$C_p = \frac{0.1219\ell}{\ln\left(\dfrac{29.6}{u} + \sqrt{1 + \left(\dfrac{2}{u}\right)^2}\right)} \tag{10.18b}$$

with $u = W/t$.

$$C_b = 0.101\,\frac{W}{t}\exp\left(-\frac{1.782}{t}\right) \tag{10.18c}$$

where the dimensions are in microns and capacitances are in femtofarads. The inductance L can be evaluated using (2.13) from Chapter 2 with conductor width W and length $\ell/2$.

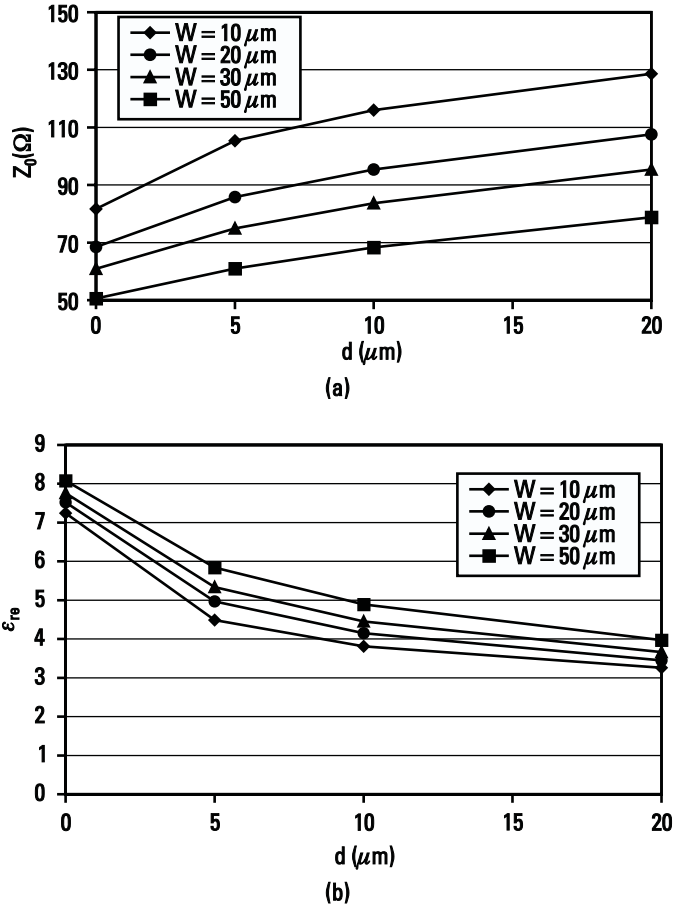


Figure 10.8 Calculated characteristics of multilayer microstrip lines on GaAs substrate, $\epsilon_r = 12.9$, $h = 75$ μm, $t = 4.5$ μm for (a) Z_0 and (b) ϵ_{re}.

10.3.2 Measurement-Based Model

The critical parameter in the airbridge model is the coupling between the two conductors. An airbridge can be simply modeled by measuring *S*-parameters. Unfortunately, this technique requires a four-port measurement, which is difficult with on-wafer testing. An indirect method for modeling an airbridge using a short-circuited $\lambda/4$ resonator coupled to a microstrip feed line through an airbridge, as shown in Figure 10.12(b), was used [17]. This technique works well because the small capacitance results in a light loading of the resonator, which increases its resonant frequency. Therefore, the two-port transmission response contains a sharp, easily observable notch at the resonant frequency of the quarterwave structure. The value of the coupling capacitance can easily be

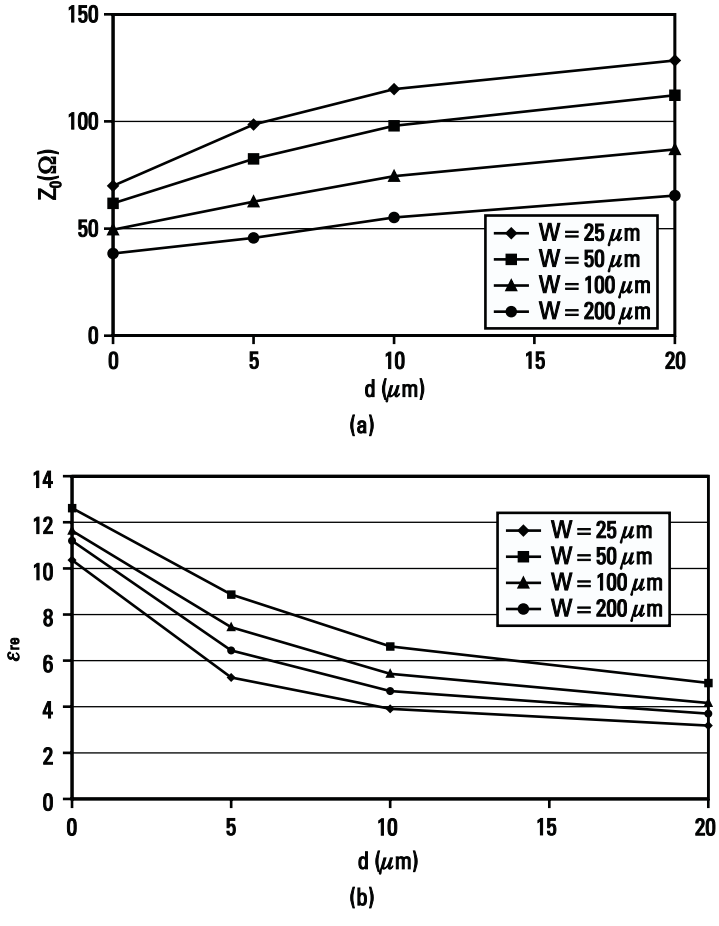


Figure 10.9 Calculated characteristics of multilayer microstrip lines on high-K substrate, $\epsilon_r = 20$, $h = 250$ μm, $t = 6$ μm for (a) Z_0 and (b) ϵ_{re}.

ascertained by calculating the frequency shift in the resonant frequency caused by the additional airbridge capacitance. The model parameters are extracted by computer optimization using conventional circuit analysis as discussed in Chapter 2.

This technique was used to model two airbridge structures on a 125-μm-thick GaAs substrate where an 88-μm-wide line (50Ω) crossed over an 88-μm-wide line and an 88-μm-wide line crossed over a 20-μm-wide line (80Ω). Figure 10.13(a) shows the EC model used to represent the airbridge crossover, and Figure 10.13(b) compares the measured and simulated performance for the 20-μm-wide line airbridge. Table 10.1 lists the model parameter values obtained for the GaAs IC process [17].

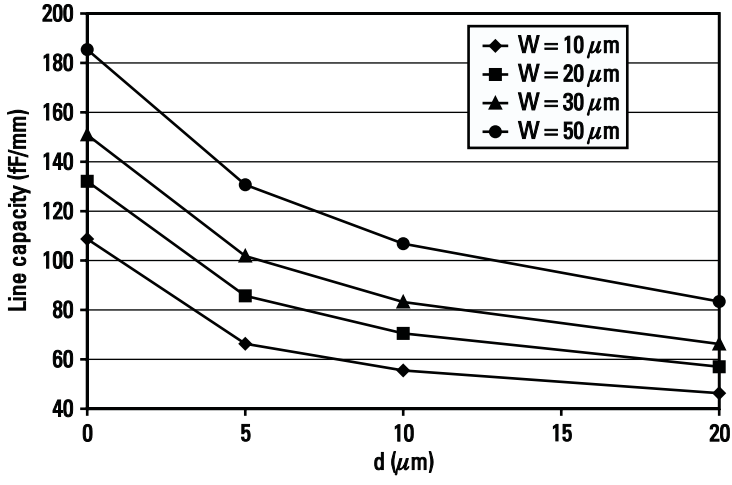


Figure 10.10 Calculated capacitance per unit length of a multilayer GaAs microstrip for various values of d and W, with $h = 75$ μm and $t = 4.5$ μm. Reduction in capacitance is as large as 60%.

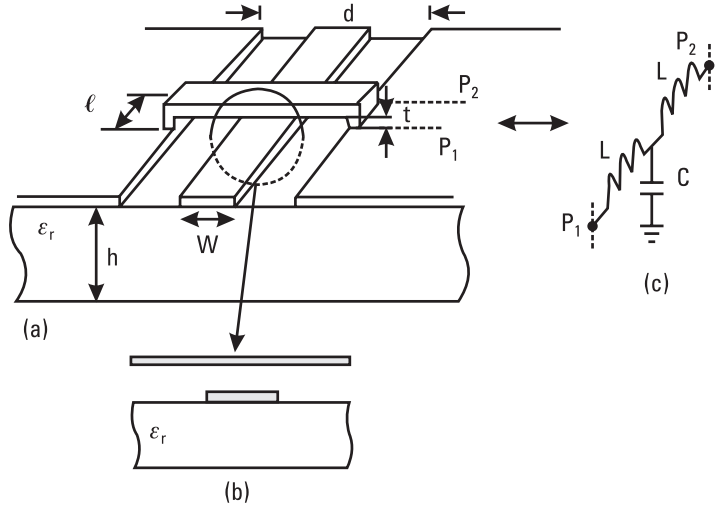


Figure 10.11 (a) Geometry of a coplanar airbridge, (b) airbridge cross-section, and (c) EC model.

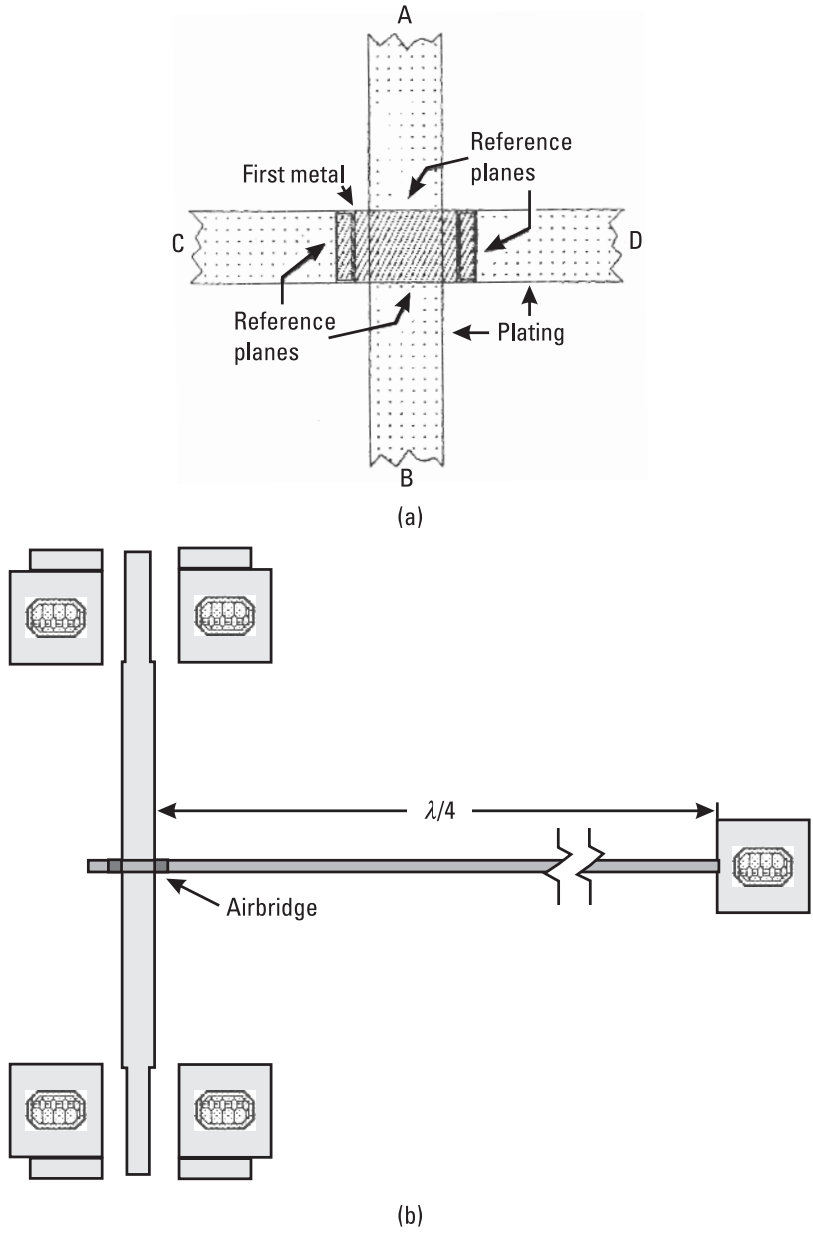


Figure 10.12 (a) A top view of the airbridge crossover and (b) physical layout of the test structure used for characterizing an airbridge crossover.

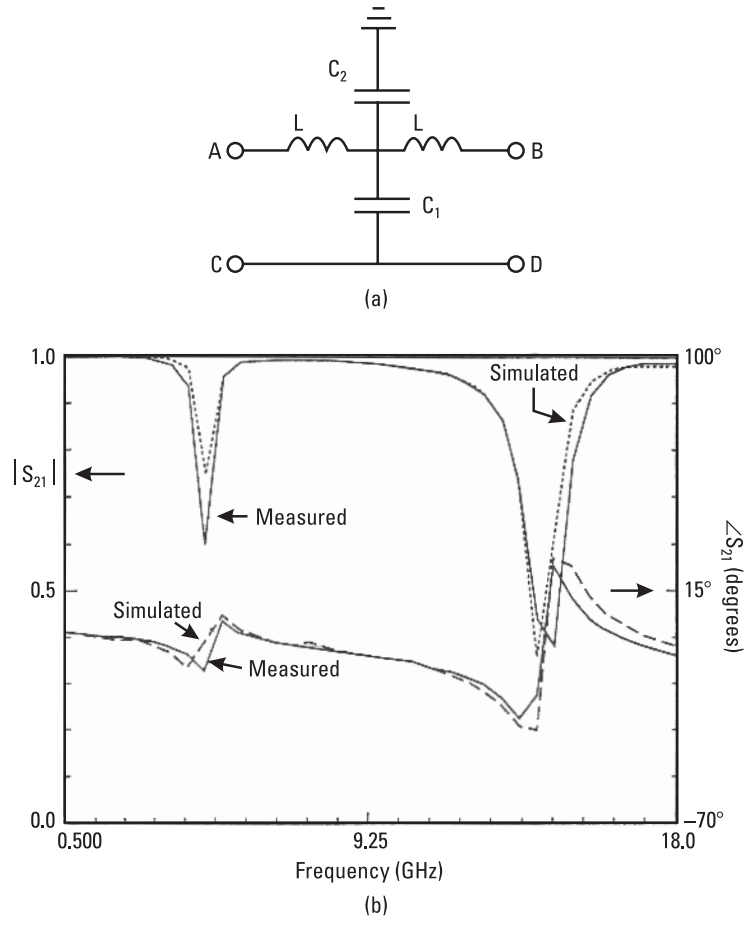


Figure 10.13 (a) Equivalent circuit model of the airbridge crossover and (b) measured and simulated performance of a 20-μm-wide line airbridge.

Table 10.1
Physical Dimensions and Equivalent Model Values for Two Airbridge Geometries

Parameter	AIRBRG1	AIRBRG2	Units
Width of lower line, W_1	88	20	μm
Width of overlay, W_2	88	88	μm
Substrate thickness, h	125	125	μm
Series inductance, L	0.004	0.0025	nH
Coupling capacitance, C_1	0.45	0.115	pF
Capacitance to ground, C_2	0.005	0.0005	pF

References

[1] Itoh, T., *Analysis Methods for Electromagnetic Wave Problems,* Norwood, MA: Artech House, 1990.

[2] Gupta, K. C., et al., *Microstrip Lines and Slotlines,* 2nd ed., Norwood, MA: Artech House, 1996.

[3] Yamashita, E., "Variational Method for the Analysis of Microstrip-Like Transmission Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-16, August 1968, pp. 529–535.

[4] Yamashita, E., and R. Mitra, "Variational Method for the Analysis of Transmission Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-16, April 1968, pp. 251–256.

[5] Bahl, I. J., and S. S. Stuchly, "Analysis of Microstrip Covered with Lossy Dielectric," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-28, February 1980, pp. 104–109.

[6] Das, N. K., and D. M. Pozar, "Generalized Spectral Domain Green's Function for Multilayer Dielectric Substrates with Applications to Multilayer Transmission Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-35, March 1987, pp. 326–335.

[7] Finlay, H. J., et al., "Accurate Characterization and Modeling of Transmission Lines for GaAs MMICs," *IEEE Trans. Microwave Theory Tech.,* Vol. 36, June 1988, pp. 961–967.

[8] Goldfarb, M. E., and V. K. Tripathi, "The Effect of Air Bridge Height on the Propagation Characteristics of Microstrip," *IEEE Microwave Guide Wave Lett.,* Vol. 1, October 1991, pp. 273–274.

[9] Hotta, M., Y. Qiam, and T. Itoh, "Resonant Coupling Type Microstrip Line Interconnect Using a Bonding Ribbon and Dielectric Pad," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1998, pp. 797–800.

[10] Visan, S., O. Picon, and V. Fouad Hanna, "3D Characterization of Air Bridges and Via Holes in Conductor-Backed Coplanar Waveguides for MMIC Applications," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1993, pp. 709–712.

[11] Beilenhoff, K., W. Henrich, and H. L. Hartnagel, "The Scattering Behavior of Air Bridges in Coplanar MMIC's," *European Microwave Conf. Dig.,* 1991, pp. 1131–1135.

[12] Rautio, J. C., and R. F. Harrington, "An Electromagnetic Time-Harmonic Analysis of Shielded Microstrip Circuits," *IEEE Trans. Microwave Theory Trans.,* Vol. MTT-35, August 1987, pp. 726–730.

[13] Champagne, K., M. Ahmadpanah, and J. L. Guirand, "A Simple Method for Determining the Green's Function for a Large Class of MIC Lines Having Multilayered Dielectric Structures," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-26, February 1978, pp. 82–87.

[14] Bhat, B., and S. K. Koul, "United Approach to Solve a Class of Strip and Microstrip-Like Transmission Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-30, May 1982, pp. 679–686.

[15] Bahl, I. J., "High-Q and Low-Loss Matching Network Elements for RF and Microwave Circuits," *IEEE Microwave Magazine,* Vol. 2, September 2000, pp. 64–73.

[16] Bessemoulin, A., et al., "A Simple Airbridge Analytical Model in Coplanar Waveguides for MMIC Applications," *Microwave Optical Tech. Lett.,* Vol. 17, March 1998, pp. 265–267.

[17] Sadhir, V. K., I. J. Bahl, and D. A. Willems, "CAD Compatible Accurate Models of Microwave Passive Lumped Elements for MMIC Applications," *Int. J. Microwave and Millimeter-Wave Computer-Aided Engineering,* Vol. 4, April 1994, pp. 148–162.

11

Transformers and Baluns

Inductor transformers are employed in RF and microwave circuits for various applications including impedance matching, power dividers/combiners, double balanced mixers, power amplifiers, signal coupling, and phase shifting. A transformer at RF frequencies consists of two or more mutually coupled coils of wires wrapped around a common core. When an RF signal is applied across input terminals of a coil also known as the *primary coil,* it induces magnetic fields in all other coupled coils, known as *secondary coils,* and producing RF voltages at the terminals of the coupled coils. Classical coil transformers used at low and radio frequencies can be realized in the printed circuit form by hybrid and monolithic techniques in the microwave frequency range. A major challenge in the printed coil transformers is that of maintaining low parasitic capacitances and series resistances, in order to operate these components at higher frequencies with low insertion loss. The transformers can be two-, three-, or four-port components. The three-port transformers may have 0°, 90°, or 180° phase difference at the output ports. The treatment of such transformers can be found in several books [1–7].

An inductor transformer's frequency response is limited to low frequencies due to winding lengths, inductive reactance, leakage inductance, losses, and associated parasitic capacitances. Using ferrite cores with large permeabilities and minimizing losses and parasitic capacitance can extend the frequency of operation. The use of such transformers has been reported up to 4 GHz.

In this chapter, we describe the basic theory of inductor transformers and briefly discuss the various types of such transformers.

11.1 Basic Theory

11.1.1 Parameters Definition

11.1.1.1 Turns Ratio

Transformers are designated by an impedance ratio, for example, $1{:}n^2$ where n is the number of turns ratio. In this case, the secondary impedance is n^2 times primary impedance. When $n > 1$, the transformer is known as a *step-up transformer* and the secondary impedance is greater than the primary impedance. The transformers turn ratio is $1{:}n$. For example, for a 1:4 impedance ratio transformer, the turn ratio is 1:2.

When the primary impedance is n^2 times secondary impedance and $n > 1$, the transformer is known as a *step-down transformer*. Figure 11.1 shows both step-up and step-down transformers for $n > 1$.

11.1.1.2 Magnetic Coupling

The magnitude of the magnetic coupling between the primary and secondary windings of a transformer is designated by the magnetic coupling coefficient k, given by

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{11.1}$$

where M is the mutual inductance between the primary and secondary windings having self-inductance of L_1 and L_2, respectively. The preceding equation is derived in the next section.

11.1.1.3 Ideal Transformers

An ideal transformer as shown in Figure 11.1 is characterized by one parameter, the turn ratio n.

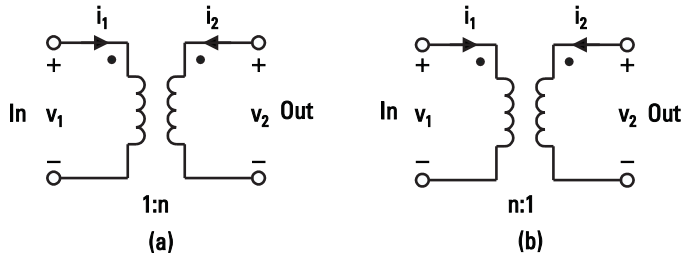


Figure 11.1 (a) Step-up and (b) step-down transformer configurations.

11.1.2 Analysis of Transformers

Consider Figure 11.2(a), which shows various quantities, input and output currents, and voltages. By taking into account the effect of the induced voltage through mutual coupling, one can write

$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} = j\omega L_1 i_1 + j\omega M i_2 \tag{11.2}$$

$$v_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} = j\omega M i_1 + j\omega L_2 i_2 \tag{11.3}$$

The ratio of the input voltage induced by a time-varying current in the output of a transformer to the voltage across the output winding is known as coupling k_1. When $i_1 = 0$, from (11.2) and (11.3), we obtain

$$k_1 = \frac{v_1}{v_2} = \frac{M}{L_2}$$

Similarly, when $i_2 = 0$,

$$k_2 = \frac{v_2}{v_1} = \frac{M}{L_1}$$

The geometric mean of these two quantities is given by

$$k = \sqrt{k_1 k_2} = \frac{M}{\sqrt{L_1 L_2}}$$

and is called the *coupling coefficient.* The value of k is always positive and real. Multiplying (11.2) by i_1 and (11.3) by i_2, and adding the two equations, we get

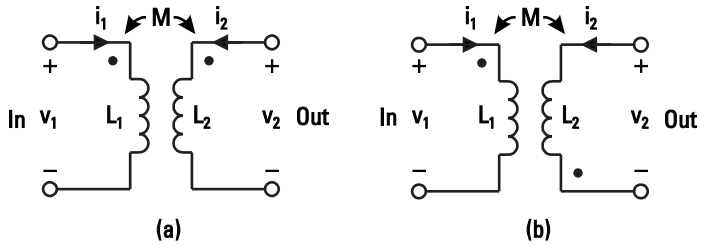


Figure 11.2 Simple transformer configurations: (a) $M > 0$ and (b) $M < 0$.

$$v_1 i_1 + v_2 i_2 = j\omega[L_1 i_1^2 + L_2 i_2^2 + 2Mi_1 i_2] \tag{11.4a}$$

or

$$(v_1 i_1 + v_2 i_2)/2j\omega = \frac{1}{2}[L_1 i_1^2 + L_2 i_2^2 + 2Mi_1 i_2] \tag{11.4b}$$

The term on the right-hand side represents the total magnetic energy stored in the transformer and is given by

$$W_m = \frac{1}{2}[L_1 i_1^2 + L_2 i_2^2 + 2Mi_1 i_2] \tag{11.5}$$

The stored energy is always positive. Therefore,

$$L_1 i_1^2 + L_2 i_2^2 + 2Mi_1 i_2 \geq 0 \tag{11.6}$$

Next we show that $k \leq 1$ and $M \leq \sqrt{L_1 L_2}$. In (11.6) the first two terms are always positive. We assume that the third term is negative when currents i_1 and i_2 flow in opposite directions and M is positive. Under this condition, we can write

$$i_2 = -ai_1 \tag{11.7}$$

where a is a positive quantity. From (11.6) and (11.7),

$$L_1 - 2Ma + L_2 a^2 \geq 0 \tag{11.8}$$

and this quadratic equation has two roots given by

$$a_{1,2} = \frac{1}{L_2}\left(M \pm \sqrt{M^2 - L_1 L_2}\right) \tag{11.9}$$

The roots are real when $M^2 - L_1 L_2 > 0$ and complex when $M^2 - L_1 L_2 < 0$. We discuss these two conditions next.

1. For $M^2 - L_1 L_2 > 0$: Under this condition, the values of roots a_1 and a_2 lie between 0 and $2M/L_2$. Let the root value be $\frac{1}{L_2}(M + b)$ where b is a positive or negative quantity. Substituting $a = \frac{1}{L_2}(M + b)$ in (11.8), we get

$$L_1 - \frac{2M}{L_2}(M + b) + L_2 \frac{1}{L_2^2}(M + b)^2 \geq 0$$

$$L_1 L_2 - 2M(M + b) + (M + b)^2 \geq 0$$

$$L_1 L_2 + b^2 - M^2 \geq 0$$

or

$$M^2 - L_1 L_2 - b^2 \leq 0 \tag{11.10}$$

which is not possible because b may be 0 and $M^2 - L_1 L_2 > 0$ is the condition we started with. Hence $M^2 - L_1 L_2$ cannot be positive.

2. For $M^2 - L_1 L_2 < 0$: Let us look at the second condition in which $M^2 - L_1 L_2 < 0$. In this case roots a_1 and a_2 become complex and can be written as

$$a_{1,2} = \frac{1}{L_2}(M \pm jb) \tag{11.11}$$

Substituting these roots in (11.8),

$$L_1 L_2 - M^2 + b^2 > 0$$

or

$$M^2 - L_1 L_2 - b^2 < 0 \tag{11.12}$$

Because $M^2 - L_1 L_2 < 0$ and b is a positive quantity, (11.12) is valid, and the only valid possibility is

$$M^2 - L_1 L_2 < 0$$

or

$$M \leq \sqrt{L_1 L_2}$$

Because $M = k\sqrt{L_1 L_2}$, then $k \leq 1$ (i.e., the coupling coefficient is always less than unity).

So far we have discussed a positive mutual coupling case. When the input and output currents are flowing in opposite directions, the mutual coupling becomes negative and is represented as shown in Figure 11.2(b).

11.1.3 Ideal Transformers

Referring to Figure 11.1(b), one can write the following relations:

$$Z_1 = \frac{v_1}{i_1} = n^2 \qquad Z_2 = n^2 \frac{v_2}{i_2} \tag{11.13}$$

$$i_2 = ni_1 \quad \text{or} \quad i_1 = \frac{1}{n} i_2 \tag{11.14}$$

$$v_2 = \frac{1}{n} v_1 \quad \text{or} \quad v_1 = nv_2 \tag{11.15}$$

Using (11.14) in (11.2) and (11.3), we get

$$\frac{v_1}{i_1} = j\omega(L_1 + Mn) \tag{11.16a}$$

$$\frac{v_2}{i_2} = j\omega\left(L_2 + \frac{M}{n}\right) \tag{11.16b}$$

From (11.13) and (11.16),

$$n = \sqrt{\frac{L_1}{L_2}} \tag{11.17}$$

From (11.1) and (11.17),

$$k = \frac{nM}{L_1} = \frac{M}{nL_2} \tag{11.18}$$

For an ideal transformer, $k = 1$ and $M = \sqrt{L_1 L_2}$,

$$M = \frac{L_1}{n} = nL_2 \tag{11.19}$$

11.1.4 Equivalent Circuit Representation

From (11.2), (11.3), and (11.19), the Z-matrix for positive mutual coupling can be written

$$[Z]^{+} = j\omega \begin{bmatrix} L_1 & M \\ M & L_2 \end{bmatrix} = j\omega M \begin{bmatrix} n & 1 \\ 1 & \frac{1}{n} \end{bmatrix} \tag{11.20}$$

Similarly for negative mutual coupling, the Z-matrix becomes

$$[Z]^{-} = j\omega \begin{bmatrix} L_1 & -M \\ -M & L_2 \end{bmatrix} = j\omega M \begin{bmatrix} n & -1 \\ -1 & \frac{1}{n} \end{bmatrix} \tag{11.21}$$

T-Equivalent Circuit

In the T-equivalent circuit case shown in Figure 11.3(a), the relationships between T-equivalent circuit elements Z_1, Z_2, and Z_3 and Z-matrix elements are as follows:

$$Z_1 = Z_{11} - Z_{21} \tag{11.22a}$$

$$Z_2 = Z_{22} - Z_{21} \tag{11.22b}$$

$$Z_3 = Z_{21} \tag{11.22c}$$

Using these relations, T-equivalent circuits for Figure 11.2(a, b) become like those shown in Figure 11.3(b, c), respectively. Similarly, one can express these equivalent circuit expressions in the pi configuration. The two series inductances represent the leakage flux and the shunt inductance is known as the magnetizing inductance. These T-equivalent circuits do not show any isolation

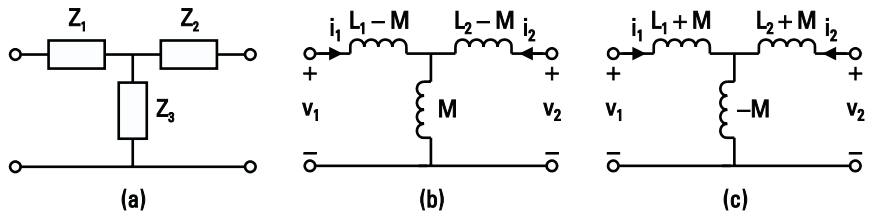


Figure 11.3 T-equivalent circuit configurations: (a) Z impedances, (b) transformer with $M > 0$, and (c) transformer with $M < 0$.

between the two input and output ports as desired from a transformer. An ideal transformer with a turns ratio of n can be easily added at the output of these T-equivalent circuits. The modified version of Figure 11.3(b) with a transformer at the output is shown in Figure 11.4(a). In this case the V-I relationships become

$$v_2 = \frac{1}{n} v_2' \tag{11.23a}$$

$$i_2 = n i_2' \tag{11.23b}$$

where i_2' and v_2' are the primary current and voltage of the added transformer.

Using (11.23) in (11.2) and (11.3),

$$v_1 = j\omega L_1 i_1 + j\omega n M i_2' \tag{11.24a}$$

$$v_2' = j\omega n M i_1 + j\omega n^2 L_2 i_2' \tag{11.24b}$$

Again repeating the foregoing process, the modified T-equivalent circuit parameters become like those shown in Figure 11.4(a). Now for any real value of n, the equivalent circuits shown in Figures 11.3(b) and 11.4(a) are electrically identical. For example, when $n = 1$, the T-equivalent circuit shown in Figure 11.4(a) becomes identical to that shown in Figure 11.3(b). Using the relations

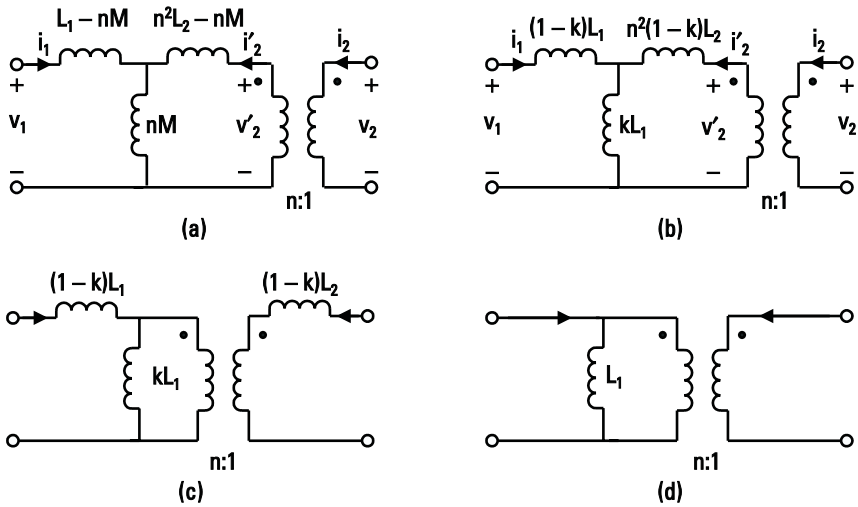


Figure 11.4 (a–d) Equivalent circuits of a transformer.

given in (11.18), the EC shown in Figure 11.4(a) can also be represented as shown in Figure 11.4(b, c). Because $n = \sqrt{L_1/L_2}$, a general transformer can be represented by three parameters L_1, L_2 and M or L_1, k, and n. In the case of perfect coupling, $k = 1$, Figure 11.4(b, c) reduce to Figure 11.4(d). In this case the transformer is called a *perfect transformer* and is characterized by only two parameters, L_1 and n. Figure 11.4(d) is also known as a low-frequency EC representation of a transformer.

11.1.5 Equivalent Circuit of a Practical Transformer

In a practical transformer, one must include the effect of leakage flux, the finite value of the magnetizing inductance, losses (winding conductor losses and core hysteresis and eddy current losses), and the effect of signal power level, frequency, temperature, and parasitic capacitances. An equivalent circuit for a practical transformer is shown in Figure 11.5, where R_1 and R_2 are the series resistances of the primary and secondary windings, and R_c represents the loss in the core. The capacitances C_1', C_2', and C_{12}' are due to parasitic capacitances of the primary (C_1), secondary (C_2), and interwindings (C_{12}), respectively, and they are either calculated using EM simulators or obtained by measurements. The relationship between these capacitances are given by [8].

$$C_1' = C_1 + C_{12}\left(1 - \frac{1}{n}\right) \tag{11.25}$$

$$C_{12}' = \frac{C_{12}}{n} \tag{11.26}$$

$$C_2' = \frac{C_2}{n^2} + C_{12}\left(\frac{1}{n} - 1\right) \tag{11.27}$$

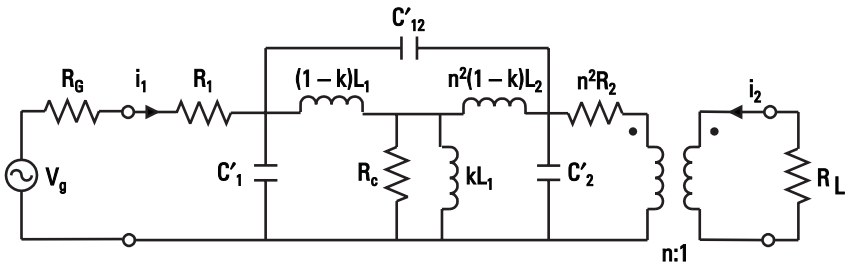


Figure 11.5 Equivalent circuit of a practical transformer.

As a first-order approximation, C_1', C_2', and C_{12}' and nonlinearities can be neglected. The components $(1-k)L_1$ and $n^2(1-k)L_2$ are known as the *leakage inductances* of the primary and secondary windings, respectively, and can be minimized by using bifilar windings, that is, coils that are wound side by side. The resistances R_1 and R_2 can be made small compared to the R_G and R_L values, by using low-resistance wires.

11.1.6 Wideband Impedance Matching Transformers

Wideband impedance matching (up to decade bandwidth) is possible [5] provided that the parasitic capacitances are negligible and the coupling between the windings is strong. For $k \cong 1$ and ignoring R_c and parasitic capacitances, the equivalent circuit shown in Figure 11.5 can be simplified as shown in Figure 11.6.

11.1.6.1 Low Cutoff Frequency

The transfer function for the network, when R_1 and R_2 are neglected and $R_G = n^2 R_L$, is given by

$$H(j\omega) = \frac{j\omega L_1 \| R_G}{j\omega L_1 \| R_G + R_G} = \frac{j\omega L_1 R_G}{2j\omega L_1 R_G + R_G^2} \tag{11.28}$$

where $A \| B$ denotes parallel combination of impedances A and B. The 3-dB low cutoff frequency ω_L is obtained from the magnitude of the pole location, that is, from

$$2\omega_L L_1 R_G = R_G^2$$

or

$$\omega_L = \frac{R_G}{2L_1} \tag{11.29}$$

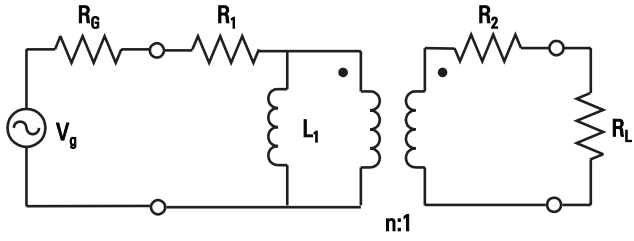


Figure 11.6 Simplified equivalent circuit of a practical transformer.

From (11.17) and (11.29), the value of L_2 is calculated as

$$L_2 = \frac{R_L}{R_G} L_1 = \frac{R_L}{2\omega_L} \tag{11.30}$$

11.1.6.2 Low and High Cutoff Frequencies

Now consider the transformer's equivalent circuit of Figure 11.3(b), but modified as shown in Figure 11.7. In this, the 3-dB bandwidth of a transformer can be obtained by finding its poles. The circuit has two poles, which can be obtained by equating the impedances in either of the two loops to 0. This equation is given by [5]

$$[j\omega L_1(1 + k) + R'_G][j\omega L_1(1 - k) + R'_G] = 0$$

where $R'_G = R_G + R_1$ and k is given by (11.1). The low and high cutoff frequencies are as follows:

$$2\pi f_L = \omega_L = R'_G/[L_1(1 + k)] \tag{11.31a}$$

$$2\pi f_H = \omega_H = R'_G/[L_1(1 - k)] \tag{11.31b}$$

Equation (11.31a) is the same as (11.29) when $R_1 = 0$ and $k = 1$. The relative bandwidth of the transformer is given by

$$\frac{f_H}{f_L} = \frac{1 + k}{1 - k} \cong \frac{2}{1 - k} \tag{11.32}$$

Example

Determine transformer parameters L_1, L_2, and k to transform a source impedance of 50Ω to a load impedance of 10Ω over 200 to 1,000 MHz by ignoring losses and capacitances. In such a case,

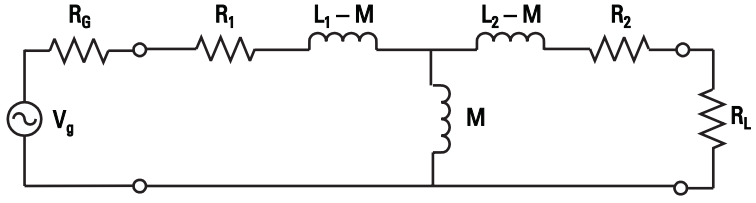


Figure 11.7 A T-section equivalent circuit of a practical transformer.

$$R_G = 50\Omega,\ R_L = 10\Omega$$

$$\omega_H/\omega_L = 1{,}000/200 = 5$$

From (11.30),

$$\frac{L_2}{L_1} = \frac{R_L}{R_G} = \frac{10}{50} = 0.2$$

From (11.32), $k = 0.67$. From (11.31a),

$$\omega_L = 2\pi \times 200 \times 10^6 = \frac{50}{L_1(1 + 0.67)}$$

or $L_1 = 23.8$ nH and $L_2 = 4.8$ nH.

11.1.6.3 Single-Tuned Transformer

A configuration of a single-tuned transformer is shown in Figure 11.8, where C is the total capacitance, including parasitic capacitance, of the primary winding. The transfer function of this network when R_L is transformed at the input side as $R_G = n^2 R_L$, is given by

$$H(j\omega) = \frac{j\omega L_1}{-\omega^2 L_1 C R_G + 2j\omega L_1 + R_G} \tag{11.33a}$$

When $\omega_0^2 L_1 C = 1$, where ω_0 is the parallel resonant frequency,

$$H(j\omega) = \frac{1}{2} \tag{11.33b}$$

that is, all of the power available from the generator is delivered to the load. For a parallel tuned circuit, the quality factor Q is given by

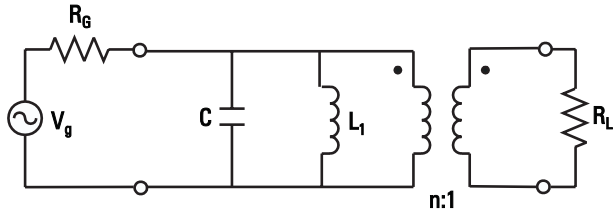


Figure 11.8 Simplified equivalent circuit of a single-tuned transformer.

$$Q = \frac{R_G/2}{\omega_0 L_1}$$

or

$$L_1 = \frac{R_G}{2\omega_0 Q} \tag{11.34a}$$

and

$$C = \frac{1}{\omega_0^2 L_1} \tag{11.34b}$$

Assuming strong coupling, the value of L_2 is calculated from (11.30).

11.1.6.4 Double-Tuned Transformers

A single-tuned transformer has a narrow bandwidth of operation. To enhance the bandwidth of a transformer, a double-tuned circuit is implemented, which allows matching of the source impedance to the load impedance at two closely spaced frequencies. In this case, the second tuned circuit is placed in the secondary. Analysis of such circuits is similar to that of a single-tuned transformer. The tuned circuits can also be of the series type as discussed by Abrie [5].

11.1.7 Types of Transformers

Coupled coil transformers can be classified based on the number of ports or their fabrication. In addition to conventional two-port transformers, they can be three-port circuits as baluns or power splitters, or four-port directional couplers. They can be fabricated by employing conventional wire-wound techniques using an air core, ferrite, or printed circuit technologies including hybrid, Si monolithic, or GaAs monolithic. These are discussed in the following sections.

11.2 Wire-Wrapped Transformers

Several types of inductors using wires were described in Chapter 4. This section is an extension of the topics discussed by treating coils or solenoids as transformers.

11.2.1 Tapped Coil Transformers

The tapped coil transformer shown in Figure 11.9 is a commonly used narrowband impedance matching circuit. It consists of two coupled coils having

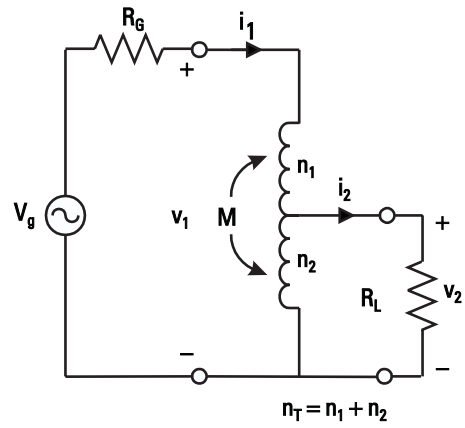


Figure 11.9 Tapped coil transformer topology.

a number of turns n_1 in the upper section and n_2 in the lower section. The inductance of these sections can be written using (4.11) as follows:

$$L_1 = \frac{4\mu_r(\pi R n_1)^2}{n_1 \ell_T / n_T + 0.9R} \quad \text{(nH)} \tag{11.35a}$$

$$L_2 = \frac{4\mu_r(\pi R n_2)^2}{n_2 \ell_T / n_T + 0.9R} \quad \text{(nH)} \tag{11.35b}$$

where $n_T = n_1 + n_2$, R is the mean radius of the coil, ℓ_T is the total length of the coil, μ_r is the relative permeability of the core, and the dimensions are in centimeters. The total inductance L_T is given by

$$L_T = \frac{4\mu_r(\pi R n_T)^2}{\ell_T + 0.9R} \quad \text{(nH)} \tag{11.36a}$$

and can also be written as

$$L_T = L_1 + L_2 + 2M \tag{11.36b}$$

where M is the mutual coupling between the two-coupled sections. From (11.1) and (11.36b), the magnetic coupling coefficient is given by

$$k = \frac{[L_T - L_1 - L_2]}{\lfloor 2(L_1 L_2)^{1/2} \rfloor} \tag{11.36c}$$

Table 11.1 shows the coupling factor for various ℓ_T/R ratio values [5]. The coupling coefficient is not as strong as for conventional transformers and also a weak function of the relative position of the tap point. From Figure 11.9,

$$v_1 = j\omega(L_1 + L_2 + 2M)\,i_1 - j\omega(L_2 + M)\,i_2 \tag{11.37a}$$

$$0 = -j\omega(L_2 + M)\,i_1 + (j\omega L_2 + R_L)\,i_2 \tag{11.37b}$$

Eliminating i_2, the input impedance is given by

$$Z_{in} = \frac{v_1}{i_1} = \frac{\omega^2(L_2 + M)^2 R_L}{(\omega L_2)^2 + R_L^2} + j\omega\left[L_T - \frac{\omega^2(L_2 + M)^2 L_2}{(\omega L_2)^2 + R_L^2}\right] \tag{11.38a}$$

When $k \cong 1$, $M \cong \sqrt{L_1 L_2}$

$$Z_{\text{in}} = \frac{\omega^2 L_2 R_L\left(\sqrt{L_1} + \sqrt{L_2}\right)^2}{(\omega L_2)^2 + R_L^2} + j\omega\left[L_T - \frac{\omega^2 L_2^2\left(\sqrt{L_1} + \sqrt{L_2}\right)^2}{(\omega L_2)^2 + R_L^2}\right] \tag{11.38b}$$

If L_T, L_2, and M are selected so that the imaginary part is almost negligible, then in this case

$$Z_{\text{in}} = R_L L_T / L_2 \tag{11.39a}$$

Under matched conditions,

$$R_G = R_L L_T / L_2 \tag{11.39b}$$

Table 11.1
Coupling Coefficient of the Tapped Coil as a Function of the ℓ_T/R Ratio of the Coil and the Relative Position of the Tap Point

n_1/n_T	$\ell_T/R = 1$	$\ell_T/R = 1.5$	$\ell_T/R = 2$	$\ell_T/R = 3$	$\ell_T/R = 4$	$\ell_T/R = 5$
0.1	0.543	0.449	0.386	0.304	0.253	0.218
0.2	0.535	0.438	0.372	0.288	0.235	0.200
0.3	0.530	0.431	0.363	0.277	0.225	0.189
0.4	0.529	0.426	0.358	0.272	0.219	0.183
0.5	0.526	0.425	0.357	0.270	0.217	0.182

The input reflection coefficient is given by

$$\rho = \frac{R_G - Z_{\text{in}}}{R_G + Z_{\text{in}}} \tag{11.40}$$

The design of tapped coil transformers is discussed in detail by Abrie [5].

11.2.2 Bond Wire Transformer

A high-frequency wideband vertically integrated transformer using bond wires for MMIC applications has been developed [9]. Figure 11.10 shows the SEM photograph of the 1:1 transformer, which consists of three turns in the primary as well as in the secondary windings. The transformer was fabricated on a 600-μm-thick semi-insulating substrate. On the substrate, the gold conductor (1 μm thick) track has a width of 80 μm and spacing of 20 μm. The fine-pitch automatic ball-bonding machine was used for fabricating the individual bond wire loops. The wire diameter, the bonding pitch, and the height of bond wire loops were 25, 100, and 340 μm, respectively. The bonding pads are 80×80 μm.

The transformer was tested using on-wafer RF probes. The measured insertion loss was about 0.43 dB at 11 GHz and the 1-dB bandwidth was from 9.4 to 14.1 GHz. The measured return loss was better than 7 dB over the 1-dB bandwidth.

11.3 Transmission-Line Transformers

The leakage inductance and parasitic capacitances between the two windings and between the turns of each winding restrict the high-frequency operation

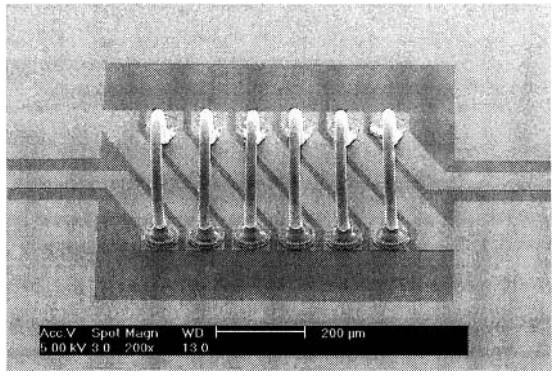


Figure 11.10 Photograph of a 1:1 three-turn bond wire transformer. (*From:* [9]. © 2000 IEEE. Reprinted with permission.)

of a conventional magnetically coupled coil transformer (see Section 11.2). If the leakage inductance and the parasitic capacitance are absorbed into the characteristic impedance of a transmission line so that $Z_0 = \sqrt{L/C}$ or are used to form an equivalent transmission line, the frequency of operation of such transformers can be extended to higher frequencies because transmission lines can be used up to very high frequencies. Transmission-line transformers have been extensively discussed in the literature [4–7, 10–18]. A simple analysis and salient features of such transformers are described in this section.

The important characteristics of a transmission-line transformer can be derived by considering a 1:4 transformer using lossless twin wires [7] as shown in Figure 11.11. All voltages and currents have their usual meanings. The transmission lines are designed to have balanced (odd-mode) currents and have their own ground. The two different transmission lines are not electromagnetically coupled and their lengths are typically less than $\lambda/8$.

The input (port 1) voltage V_1 and current I_1, can be expressed in terms of output (port 2) voltage V_2 and current I_2, using the following relations:

$$V_1 = V_2 \cos\theta + jZ_0 I_2 \sin\theta \tag{11.41a}$$

$$I_1 = I_2 \cos\theta + j\frac{V_2}{Z_0}\sin\theta \tag{11.41b}$$

where θ and Z_0 are the electrical length and the characteristic impedance of the line, respectively. From Figure 11.11,

$$V_g = (I_1 + I_2)R_G + V_1 \tag{11.42a}$$

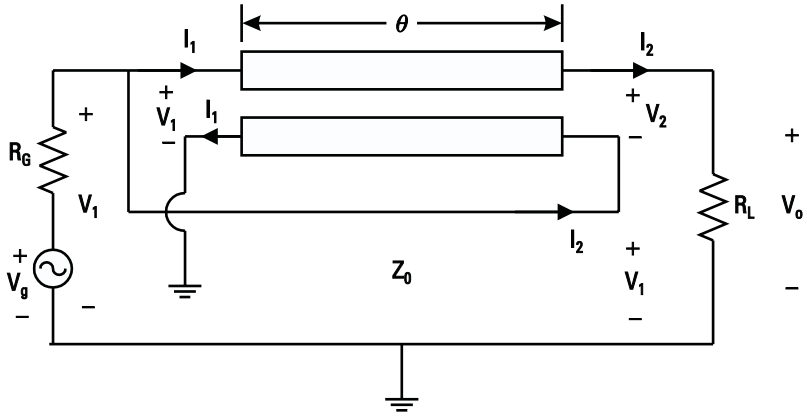


Figure 11.11 A 1:4 transmission-line transformer configuration.

or

$$V_g = (I_1 + I_2)R_G + I_2R_L - V_2 \tag{11.42b}$$

as

$$V_O = V_1 + V_2 = I_2R_L \tag{11.43}$$

Eliminating V_1 from (11.41a) and rearranging (11.41b) and (11.42b), we get three equations in terms of I_1, I_2, and V_2 as given here:

$$V_G = I_1R_G + I_2(R_G + R_L) - V_2 \tag{11.44a}$$

$$0 = 0I_1 + I_2(jZ_0 \sin\theta - R_L) + V_2(1 + \cos\theta) \tag{11.44b}$$

$$0 = I_1 - I_2\cos\theta - j\frac{V_2}{Z_0}\sin\theta \tag{11.44c}$$

From (11.44), the output current I_2 is

$$I_2 = \frac{V_G(1 + \cos\theta)}{2R_G(1 + \cos\theta) + R_L\cos\theta + j\sin\theta\left(\dfrac{R_GR_L}{Z_0} + Z_0\right)} \tag{11.45}$$

Maximum power available from the generator is

$$P_{\text{in}} = \frac{V_g^2}{4R_G} \tag{11.46}$$

and the power delivered to the load is

$$P_o = |I_2|^2R_L = \frac{|V_g|^2(1 + \cos\theta)^2R_L}{[2R_G(1 + \cos\theta) + R_L\cos\theta]^2 + \left[\sin\theta\left(\dfrac{R_GR_L}{Z_0} + Z_0\right)\right]^2} \tag{11.47}$$

The optimum load can be obtained by maximizing P_o with respect to R_L or $dP_o/dR_L = 0$. In the limiting case when θ is very small, $R_L = 4R_G$. The optimum characteristic impedance is found to be $Z_0 = 2R_G$ when $dP_o/dZ_0 = 0$.

Substituting $Z_0 = 2R_G$ and $R_L = 4R_G$ in (11.47) and from (11.46) and (11.47), we get

$$P_o/P_{\text{in}} = \frac{4(1 + \cos\ \theta)^2}{(1 + 3\ \cos\ \theta)^2 + 4\ \sin^2\ \theta} \tag{11.48}$$

When $\theta \cong 0$, $P_o/P_{\text{in}} \cong 1$ and demonstrates the operation of a transformer. For

$$\theta = \beta\ell = 2\pi/\lambda \times 0.1\lambda = 36°, \quad P_o/P_{\text{in}} = 0.934 \text{ or } -0.3 \text{ dB}$$

Figure 11.12 shows schematics of several other transformers. For example, in Figure 11.12(c), input current from the generator splits into four current paths and the voltage on the load side sums up to four times the input voltage, giving rise to a 1:16 impedance transformation ratio. Figure 11.12(d) shows the 1:4 transformer in the loop form. Thus, transmission-line transformers can be formed in the solenoid form or wrapped around a magnetic core.

In the design of such transformers the selection of a suitable configuration that provides the required impedance transformation ratio over the desired frequency range is very important. The next step is to determine the required characteristic impedance followed by the selection of the transmission medium.

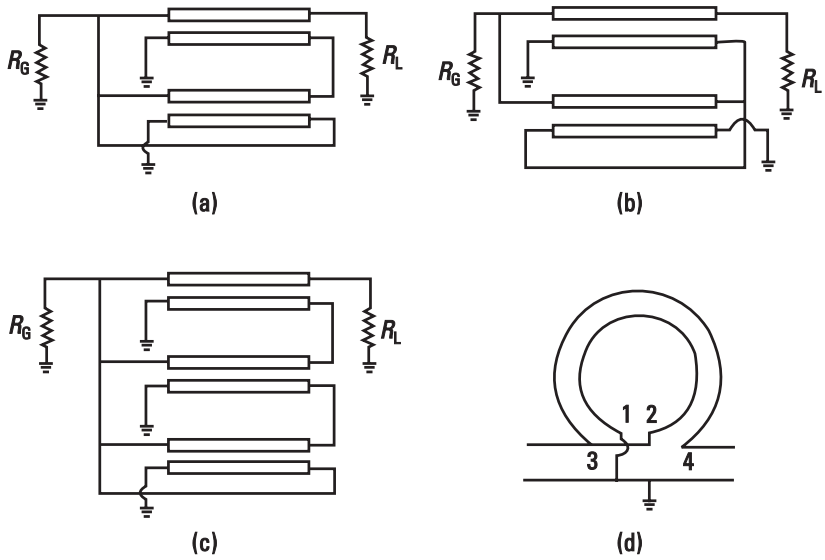


Figure 11.12 Schematic of transmission-line transformers: (a) 1:9, (b) 4:9, (c) 1:16, and (d) coiled 1:4 [shown in Figure 11.13(c)].

Preserving the characteristics of the transmission line during transformer fabrication is critical to maintaining a transformer's high-frequency response. Twisted insulated wires can be used to produce characteristic impedances in the range of 10 to 200Ω [11]. Thin wires and large spacing result in a high characteristic impedance, whereas thick wires and close spacing are suitable for low characteristic impedance. Semirigid coaxial cable with the required characteristic impedance is the most desirable transmission line. Figure 11.13 shows configurations for four basic 1:4 transformers.

11.4 Ferrite Transformers

The properties of ferrite materials and the shape of the core affect the performance of a coil transformer. Both toroid and binocular (two-hole) cores are commonly used in broadband RF transformers. However, a binocular is preferred to a toroid core, because it provides a higher inductance for a given winding length. The maximum frequency of operation of a ferrite core transformer is limited to about 2 GHz due to their leakage inductance, core losses, and parasitic capacitances.

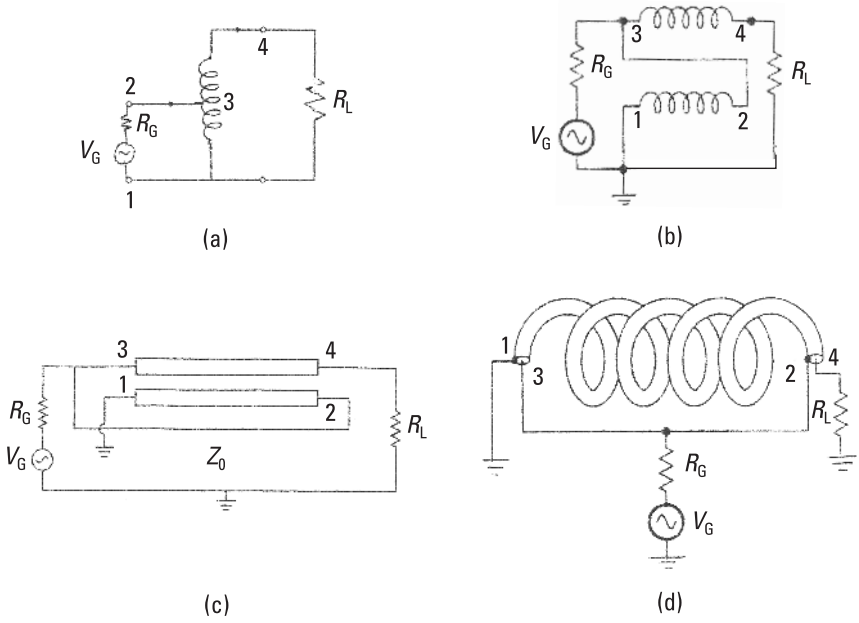


Figure 11.13 Four basic transmission-line transformers with 1:4 configurations: (a) autotransformer, (b) general transmission line, (c) twin wire topology, and (d) coaxial cable schematic.

Figure 11.14 shows several types of 4:1 ferrite transmission-line transformers. At the input, two currents are summed to obtain twice the current, and at the output, two voltages are added to get twice the voltage, thus achieving a 4:1 impedance ratio. The coaxial cable or closely spaced parallel insulated wires are wrapped around the ferrite core so that that the phase delay between terminals 2 and 3 is minimized and the transmission-line properties are maintained at higher frequencies. Among all of the transformer configurations, the brass tube topology is somewhat different. In this case, a binocular (two-hole) core, or two stacked toroids placed side by side, is used. A brass (nonmagnetic) tube is passed through each hole and both tubes are connected at one end to form a single turn primary. The secondary winding is formed by coaxial cables or wires running two times through the tubes. In the case of coaxial cables, the outer conductors are connected to tubes. The current flowing through the tube is equal to the sum of the currents in the two wires flowing in the opposite direction, preserving the voltage and current relationships required for transmission-line operation.

The design of such transformers starts with the selection of a configuration providing the required impedance transformation over the desired frequency range. Next comes the choice of a ferrite core. At higher power levels, the ferrite cores introduce nonlinear operation due to saturation of the magnetic flux density. This gives rise to harmonic generation and higher loss in the transformer. Therefore, it is very desirable to keep the operating flux density well below the saturation level.

The voltage across the input of a transformer having an inductance L and carrying an rms current I is given by

$$V = L\frac{dI}{dt} = j\omega LI \tag{11.49}$$

Using (2.1) and (11.49),

$$V = j\omega I\Phi = j\omega nAB \tag{11.50}$$

where n is the number of turns in the primary and B is the magnetic flux density. If $V_{\max}$ is the maximum allowed voltage at the input of the transformer before saturation, the maximum magnetic flux density $B_{\max}$ is given by

$$B_{\max} = \frac{V_{\max}}{\omega nA} \quad (\text{Wb/m}^2) \tag{11.51}$$

where the cross-sectional area A of the core is in square meters. The maximum flux levels for core saturation are generally given in the manufacturer's data.

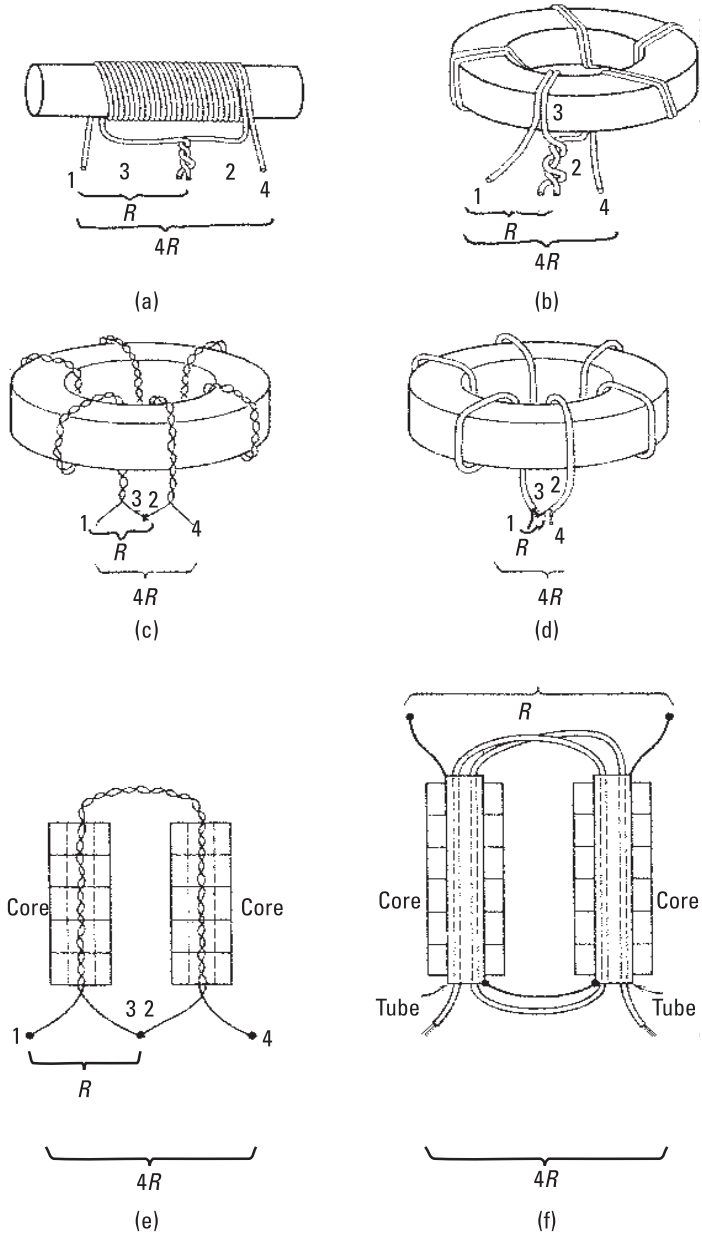


Figure 11.14 Ferrite transmission-line transformers: (a) twin wire around cylindrical rod core, (b) twin wire around toroid, (c) twisted wire around toroid, (d) coaxial cable around toroid, (e) twisted wire through stacked core, and (f) brass tube.

In the case of a stacked toroid core, the maximum flux density is given by

$$B_{\max} = \frac{V_{\max}}{\omega n N A} \tag{11.52}$$

where N is the number of cores and A is the cross-sectional area of a single toroid.

11.5 Parallel Conductor Winding Transformers on Si Substrate

In this transformer, the magnetic coupling between the interwound parallel conductors is used to realize such transformers [19]. Both the primary ($P\overline{P}$) and secondary ($S\overline{S}$) windings lie in the same plane. Figure 11.15(a) shows the top and cross-sectional views of a parallel conductor winding transformer. The structure is asymmetrical and the transformer turns ratio n is not equal to one, that is, the primary and secondary windings self-inductances are not equal.

A planar symmetrical transformer using interwound winding as shown in Figure 11.15(b) was realized. For a given number of turns, the electrical characteristics of the primary and secondary windings are identical. In this configuration, the primary and secondary terminals are located opposite each other, a desirable feature for easy circuit connections.

The third type of planar transformers is of a concentric spiral type as shown in Figure 11.15(c). In this topology, the primary winding lies in the center and the secondary winding is around it. In this configuration, the mutual couplings between the turns enhance the self-inductance of each winding instead of strengthening mutual coupling between the windings. Therefore, concentric-type transformers have a lower coupling coefficient ($\cong$ 0.4–0.6) compared to the first two transformers ($k \cong 0.7$–0.9) and are very asymmetrical. Such transformers have limited usage.

The fourth type of transformer is the stack or multiconductor layer type shown in Figure 11.15(d), also known as an overlay or quasi-broadside coupled transformer. This structure has the highest coupling coefficient ($k \cong 0.8$–0.95) due to both edge and broadside magnetic coupling and compact size. The structure is electrically asymmetric due to the different parasitic resistances and capacitances for each winding. Another disadvantage of this topology is its large parallel plate capacitance between the windings, which limits its frequency of operation. By creating an offset between the windings, the parallel plate capacitance effect can be reduced.

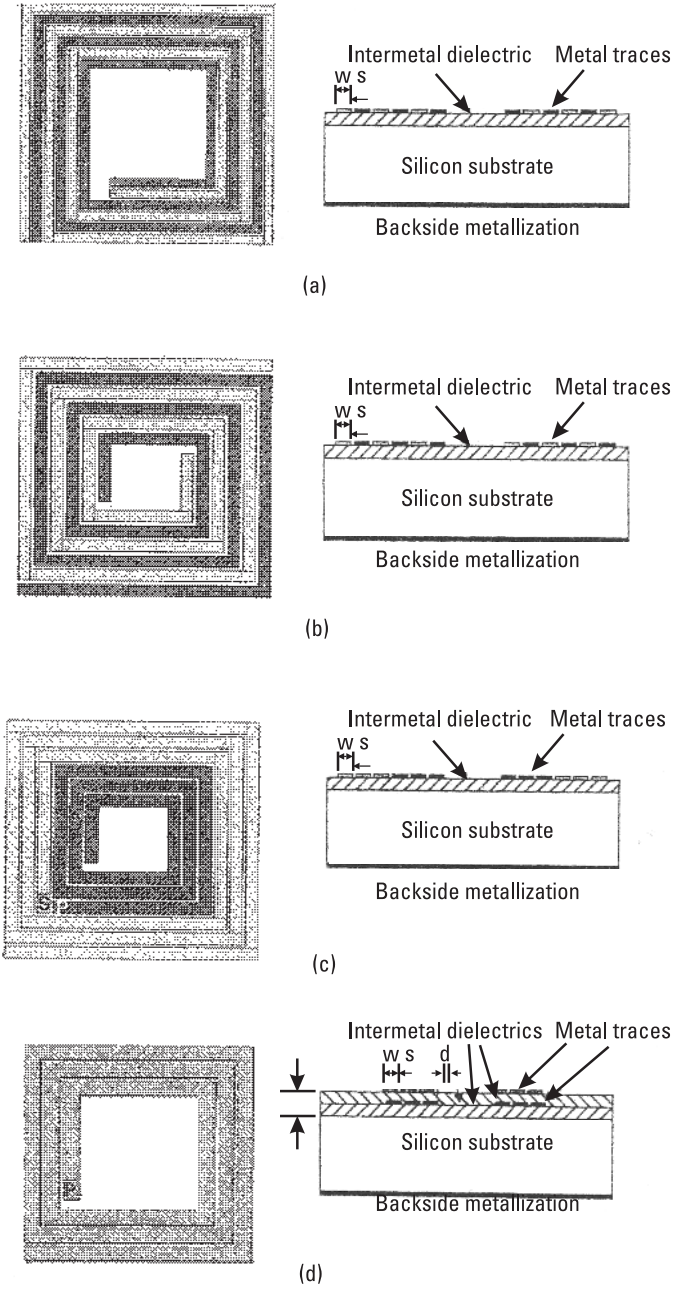


Figure 11.15 Parallel conductor winding transformer configurations on Si substrate: (a) parallel conductor, (b) interwound, (c) concentric spiral, and (d) overlay or stacked. (*From:* [19]. © 2000 IEEE. Reprinted with permission.)

Among several types of planar transformers, stacked-type transformers in Si technology are becoming more popular due to their compact size. Their electrical performance can be further improved by employing thick conductors, thick low dielectric constant intermetal layers such as BCB or polyimide, and multilayers.

11.6 Spiral Transformers on GaAs Substrate

Classical coil transformers used at low and radio frequencies can be realized by hybrid and monolithic technologies in the microwave frequency range. A major challenge in the printed coil transformers is to reduce the parasitic capacitance and series resistance in order to operate these components at higher frequencies, with low insertion loss. The transformers can be two-, three-, or four-port components. The three-port transformers may have 0°, 90°, or 180° phase difference at the output ports.

Rectangular spiral transformers fabricated using GaAs MMIC technology have been reported in the literature [20–24]. In active circuits, their impedance transformer ratio and inductance values are used for impedance transformation and resonating out the active device's capacitance, respectively. Figure 11.16 shows the physical layout of a two-conductor transformer consisting of a series of turns of thin, metallized conductors placed on a dielectric substrate (not shown). The characterization of this structure is not straightforward; however, a multiconductor coupled microstrip line analysis [25, 26] can be used to approximately determine its parameters. A more accurate characterization of this transformer can only be achieved by using full-wave and comprehensive circuit simulators such as EM CAD tools.

The twin coil four-port rectangular spiral transformer [21, 23] shown in Figure 11.16 has a ground ring around it. The dimensions of the transformer are outside ring = 1,020 × 710 μm, conductor thickness = 1 μm, GaAs (ϵ_r = 12.9) substrate thickness = 250 μm, dielectric crossover height = 1.3 μm, overlay dielectric ϵ_r = 6.8, conductor width = 20 μm, and conductor gap = 6 μm. Figure 11.17 shows a comparison between the measured and simulated S_{11} and S_{21} response of this transformer when ports 3 and 4 are short circuited as shown in Figure 11.16. The simulated performance was obtained using an electromagnetic simulator.

As shown in Figure 11.17, S_{21} has a sharp null at 6 GHz, which occurs because of the $\lambda/4$ short-circuited secondary coil at that frequency. In this case, maximum current flows through the grounded port 4 and negligible current flows through port 2. Thus, power flowing into the load at port 2 is negligible and results in a null in the S_{21} response. Below 6 GHz, the current in the spiral conductors is nearly constant and the power transfer is provided by magnetic

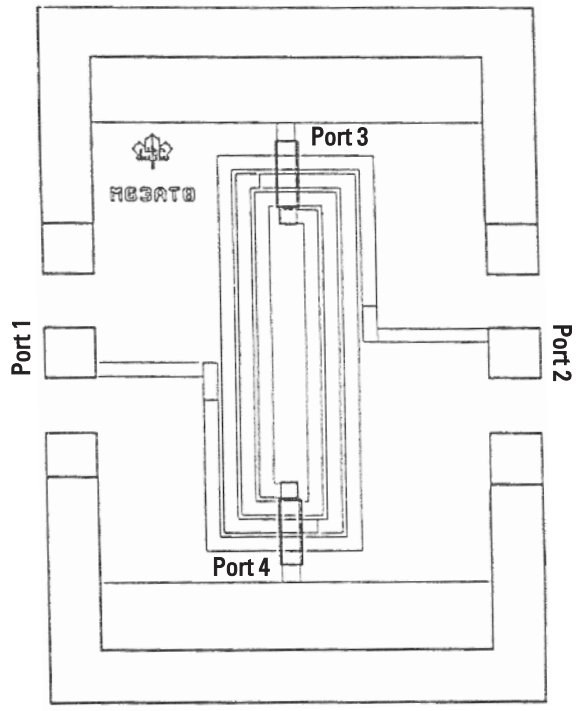


Figure 11.16 The spiral transformer example. (*From:* [21]. © 1989 IEEE. Reprinted with permission.)

coupling similar to that in classical coil transformers. Above 6 GHz, however, the spiral conductors are electrically long and the current distribution along the conductors has less of a standing-wave nature. Their behavior becomes closer to that of coupled transmission lines supporting both magnetic and electric coupling.

When ports 3 and 4 are terminated in 50Ω loads, the measured two-port response of the transformer is shown in Figure 11.18, which shows a gradual increase of S_{11} and S_{21}. Because in this case there are no standing waves, the power transfer from primary to secondary occurs gradually from magnetic to combined magnetic and electric coupling. However, 50-Ω terminating loads result in a higher loss in the transformer.

The preceding examples show that efficient power transfer in a two-port transformer occurs at high frequencies through both magnetic and electric coupling. At such frequencies, the spiral conductors are longer than $\lambda/4$. This does not permit grounding of the center tap of the secondary spiral conductor to obtain a balanced output at ports 2 and 3. On the other hand, at low frequencies, a center tap is possible; as in classical transformers, however, power

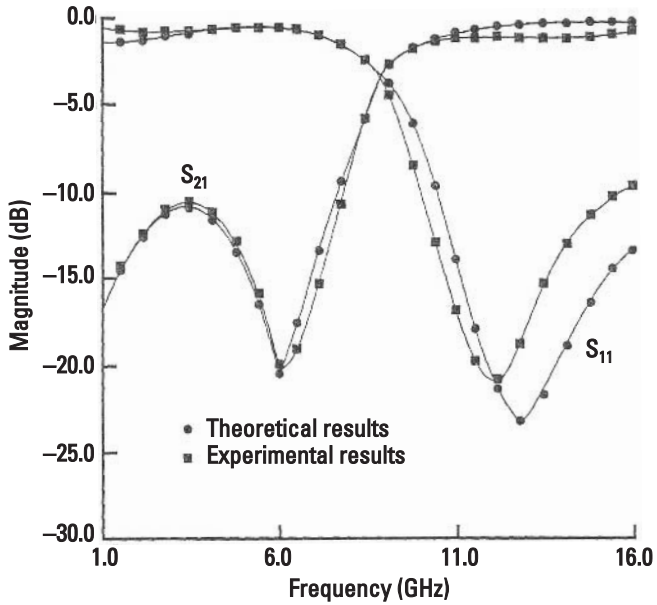


Figure 11.17 The $|S_{11}|$ and $|S_{21}|$ responses of the two-port configuration of the transformer in Figure 11.16.

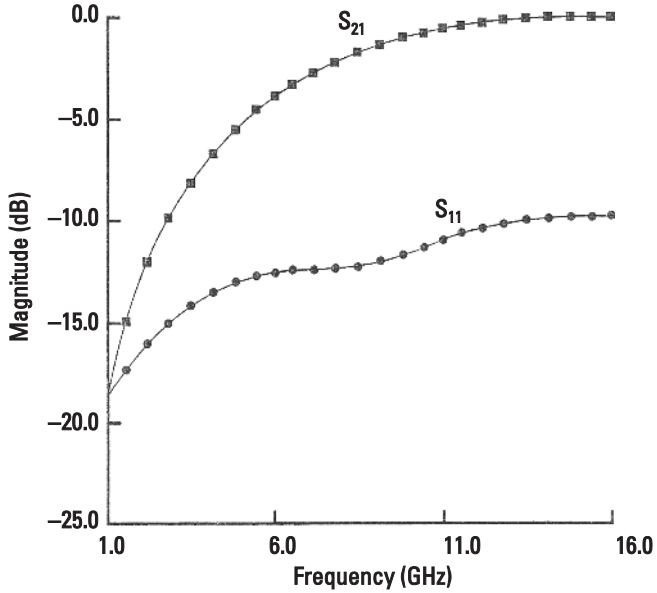


Figure 11.18 The $|S_{11}|$ and $|S_{21}|$ responses of the four-port configuration, constructed by adding 50-Ω series resistors to ports 3 and 4 in Figure 11.16.

transfer is inefficient as shown in Figure 11.18. The power transfer can be improved by making these transformers electrically small, minimizing the parasitic capacitances, and increasing the number of tightly coupled turns of the spirals, while maintaining the same spiral length.

Efficient power transfer can also be obtained by using more than two coils in a transformer as shown in Figure 11.19. Figure 11.20(a) shows a photograph of this structure, known as a *triformer,* having 1.5 turns and fabricated on GaAs using conductor width and spacing of 5 μm [22] and designed as a two-port matching network. Here ports 1, 3, 4, and 5 are grounded and ports 2 and 6 are input and output ports, respectively. An electrical equivalent circuit is shown in Figure 11.20(b). TRL denotes on-wafer probe pads. The triformer structure can be used in the realization of wideband baluns discussed next.

11.6.1 Triformer Balun

A triformer balun that is a rectangular-spiral-shaped inductor using three coupled lines has been developed for MMIC applications [22]. The balun was designed using the multiconductor coupled-line transformer chain matrix method. However, this structure can be accurately analyzed using EM simulators. The physical layout, equivalent circuit, and microphotograph of a one-turn triformer are shown in Figure 11.21. Here ports 3, 4, and 5 are grounded, port 2 is input, and ports 1 and 6 are the outputs. The output ports have 180° phase difference. The structure was fabricated on a GaAs (ϵ_r = 12.9) substrate with a 2-μm conductor thickness, a 10-μm conductor width, and 5-μm spacing between the conductors. The gold conductors have a metal resistivity of 0.03 Ω-μm, and the substrate thickness is 100 μm. Measured and simulated performance of the triformer is shown in Figure 11.22. The differential phase shift between output ports 1 and 6 remains constant at about 182°. A major shortcoming of

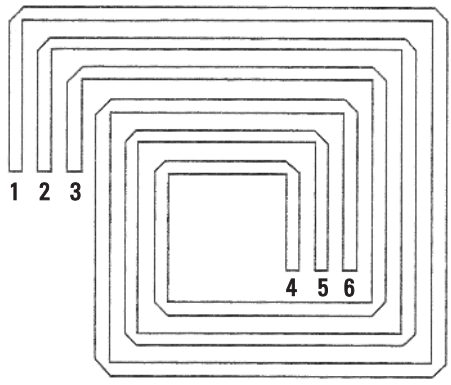


Figure 11.19 Schematic of a 1.5-turn rectangular spiral transformer.

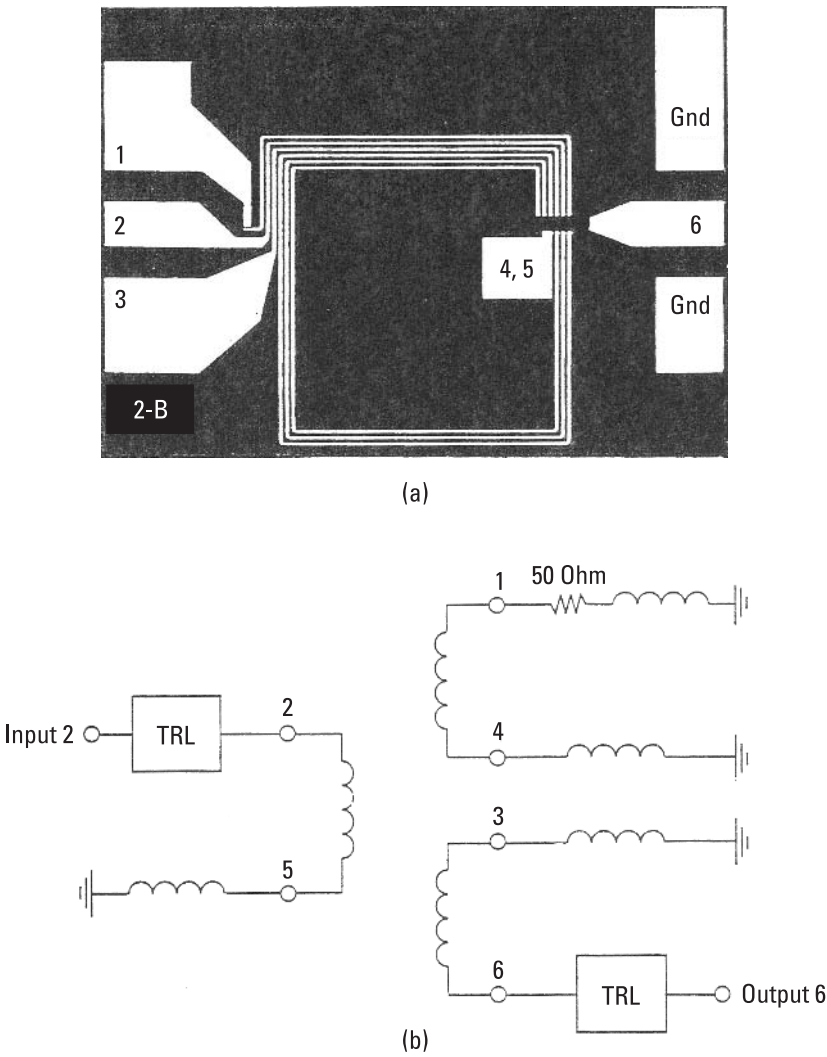


Figure 11.20 (a) Photograph of a 1.5-turn MMIC triformer and (b) two-port equivalent circuit of the triformer. (*From:* [22]. © 1989 IEEE. Reprinted with permission.)

this approach is the loss in the structure because of the thin substrate and narrow conductor width. This can be overcome to some extent by printing thick lines on thick alumina substrates.

11.6.2 Planar-Transformer Balun

The planar-transformer balun consists of two oppositely wrapped twin-coil transformers connected in series. In this configuration, one of the two outer

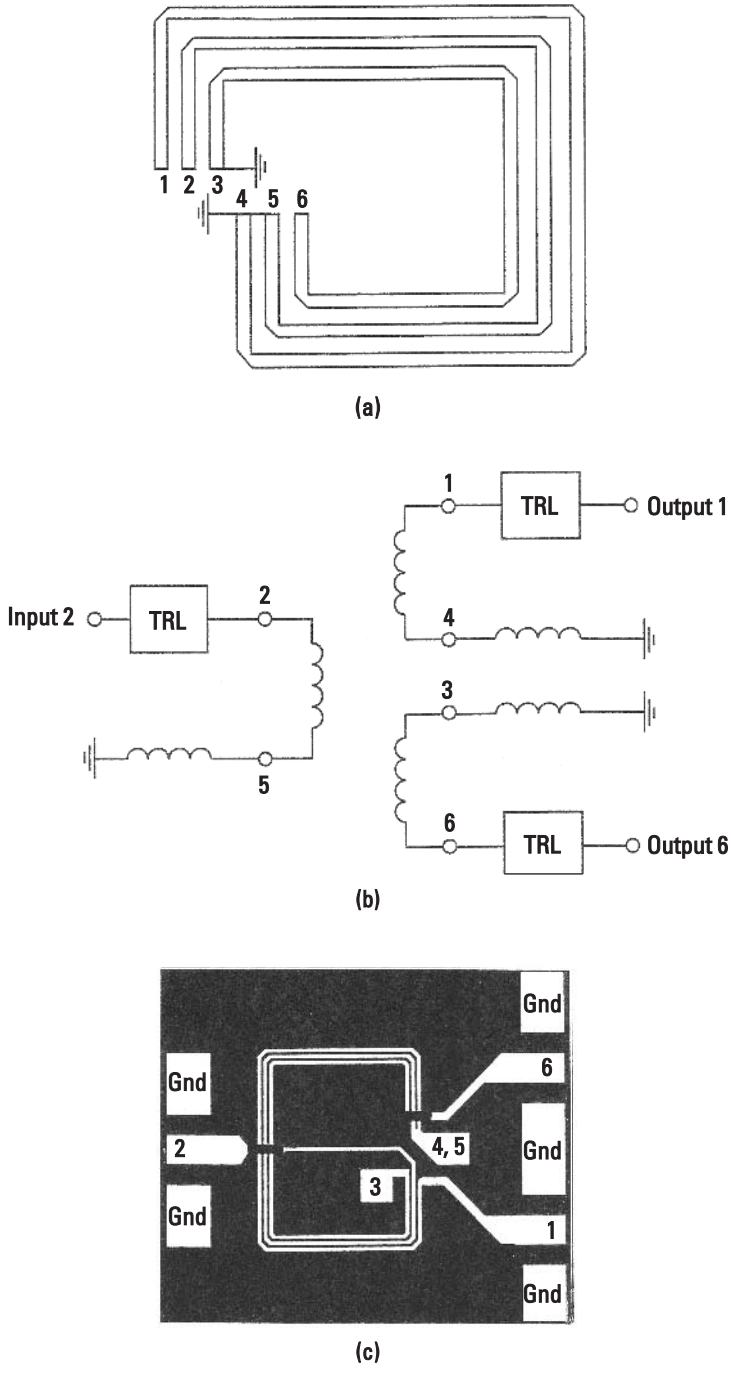


Figure 11.21 Multiconductor coupled line triformer: (a) physical layout, (b) equivalent circuit, and (c) microphotograph. (*From:* [22]. © 1989 IEEE. Reprinted with permission.)

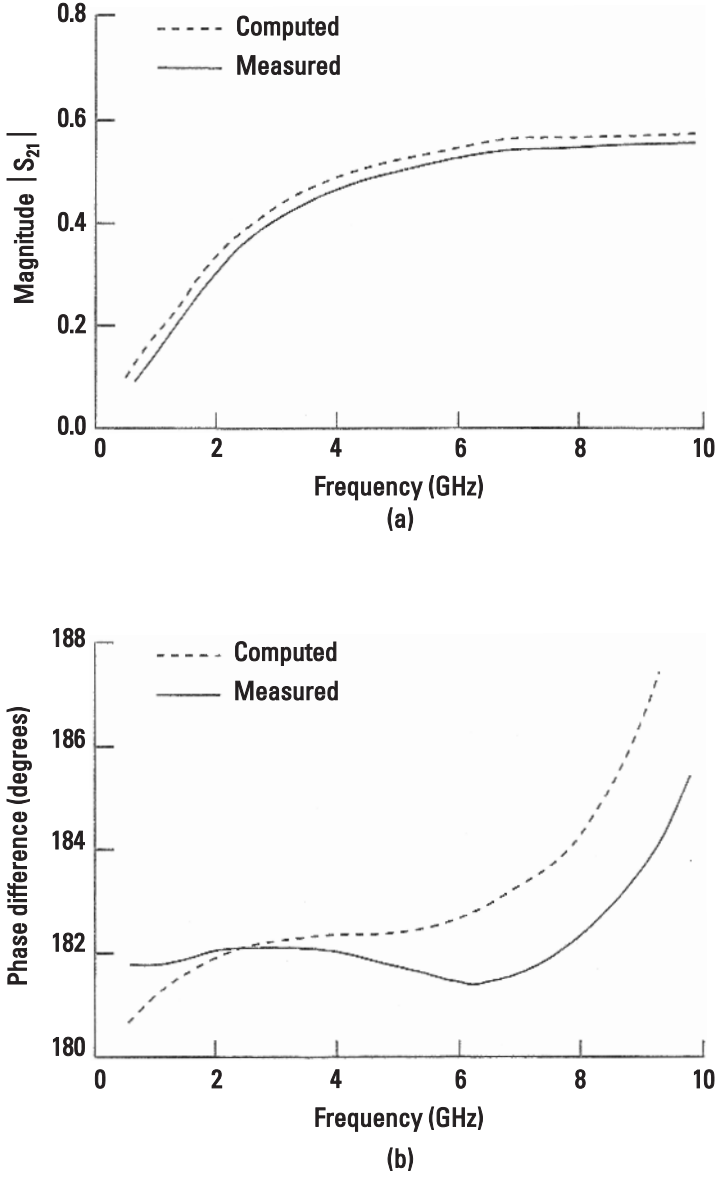


Figure 11.22 Comparison of computed and measured S-parameters: (a) magnitude and (b) differential phase shift. (*From:* [22]. © 1989 IEEE. Reprinted with permission.)

terminals in the primary coil and the inner common terminal in the secondary coil are grounded as shown in Figure 11.23 [24]. Figure 11.23(a) shows the equivalent circuit, and Figure 11.23(b) is a layout of the balun using rectangular spiral transformers. The chip measures about 1.5 mm^2, which demonstrates the compactness of this approach.

The resonant frequency of the coil transformers due to interturn and other parasitic capacitances with the ground limits the performance and bandwidth of this type of balun. Usually the balun is operated below the resonance frequency. The lower frequency bound of the bandwidth is set by the inductance, and the upper frequency bound is set by the resonance frequency of the coil. The bandwidth can be increased either by increasing the resonance frequency while maintaining the same inductance or by increasing the inductance while maintaining the resonance frequency. The resonance frequency can be increased by reducing the interturn and parasitic capacitances by employing thick and low-dielectric constant substrates and airbridges in the coil. In addition, the inductance can be increased by optimizing the area-to-length ratio.

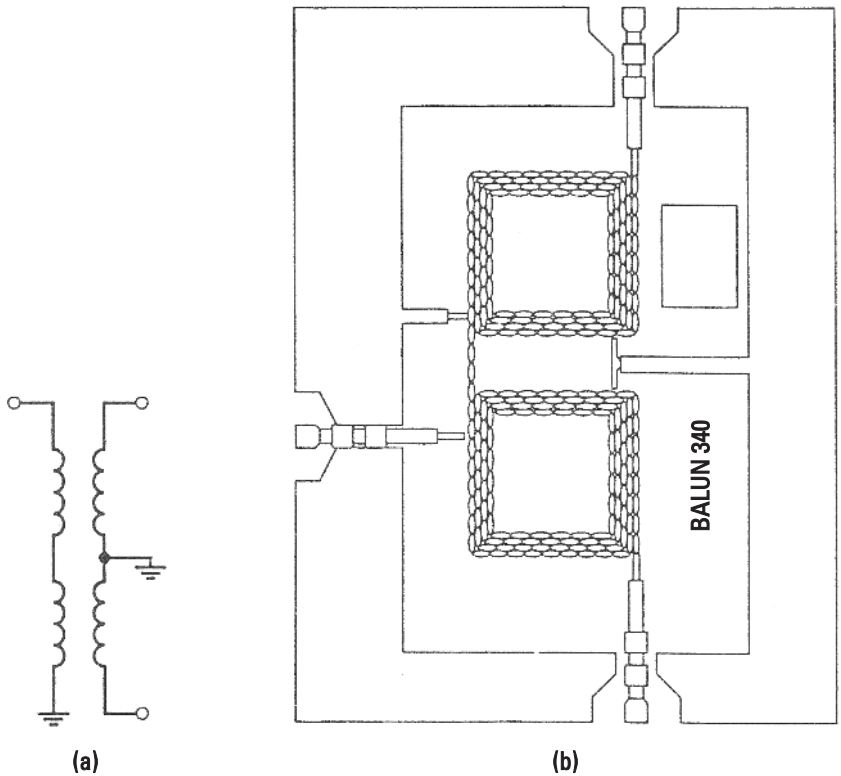


Figure 11.23 (a) Simplified circuit diagram and (b) photograph of a rectangular spiral transformer balun. (*From:* [24]. © 1991 IEEE. Reprinted with permission.)

Figure 11.24 shows the simulated and measured performance of a planar-transformer balun. The amplitude and phase imbalances between the two balanced ports are less than 1.5 dB and 10 degrees, respectively, over the 1.5- to 6.5-GHz frequency band. The simulated results shown were obtained using EM analysis.

We have described several kinds of transformers in this chapter. The selection of a particular type depends on the application, performance, and cost limitations.

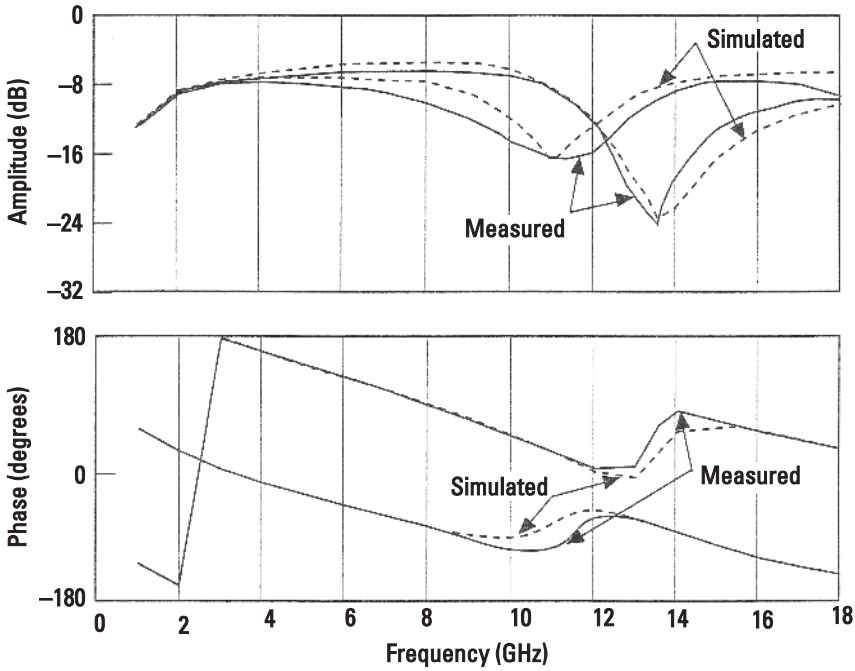


Figure 11.24 Comparison between simulated and measured performances of a planar-transformer balun. (*From:* [24]. © 1991 IEEE. Reprinted with permission.)

References

[1] Balabanian, N., *Fundamentals of Circuit Theory,* Boston, MA: Allyn and Bacon, 1961.

[2] *RF Transformer Designer's Guide,* Brooklyn, NY: Mini Circuits.

[3] van der Puije, P. D., *Telecommunication Circuit Design,* New York: John Wiley, 1992.

[4] Sevick, J., *Transmission Line Transformers,* Atlanta, GA: Noble Publishing, 1996.

[5] Abrie, P. D., *Design of RF and Microwave Amplifiers and Oscillators,* Norwood, MA: Artech House, 1999.

[6] Mongia, R., I. Bahl, and P. Bhartia, *RF and Microwave Coupled-Line Circuits,* Norwood, MA: Artech House, 1999, Chaps. 10, 11.

[7] Davis, W. A., and K. K. Agarwal, *Radio Frequency Circuit Design,* New York: John Wiley, 2001.

[8] Trask, C., "Wideband Transformers: An Intuitive Approach to Models, Characterizations and Design," *Applied Microwave Wireless,* November 2001, pp. 30–41.

[9] Song, B. W., S. J. Kim, and H. Y. Lee, "Vertical Integrated Transformers Using Bondwires for MMICs," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2000, pp. 1341-1344.

[10] Niclas, K. B., R. R. Pereira, and A. P. Chang, "Transmission Lines Accurately Model Autotransformers," *Microwaves and RF,* Vol. 31, November 1992, pp. 67–75.

[11] Krauss, H. L., C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering,* New York: John Wiley, 1980, Chap. 12.

[12] Rotholz, E., "Transmission-Line Transformers," *IEEE Trans. Microwave Theory Tech.,* Volume MTT-29, April 1981, pp. 327–331.

[13] Martin, M., "Ferrite Transformers Minimize Losses in RF Amplifiers," *Microwave and RF,* Vol. 29, May 1990, pp. 117–126.

[14] MacDonald, M., "Design Broadband Passive Components with Ferrites," *Microwaves and RF,* Vol. 32, October 1993, pp. 81–132.

[15] McClure, D. A., "Broadband Transmission-Line Transformer Family Matches a Wide Range of Impedances," *RF Design,* February 1994, pp. 62–66.

[16] Hamilton, N., "RF Transformers Part I: The Windings," *RF Design,* June 1995, pp. 36–44.

[17] Carpentieri, E., "Model Characterizes Transmission-Line Transformers," *Microwaves and RF,* Vol. 35, November 1996, pp. 73–80.

[18] Carpentieri, E., "Equations Model Transmission-Line Transformers," *Microwaves and RF,* Vol. 36, June 1997, pp. 94–98.

[19] Long, J. R., "Monolithic Transformers for Silicon RF IC Design," *IEEE J. Solid-State Circuits,* Vol. 35, September 2000, pp. 1368–1381.

[20] Ferguson, D., et al., "Transformer Coupled High-Density Circuit Technique for MMIC," *IEEE GaAs IC Symp. Dig.,* 1984, pp. 34–36.

[21] Howard, G. E., et al., "The Power Transfer Mechanism of MMIC Spiral Transformers and Adjacent Spiral Inductors," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1989, pp. 1251–1254.

[22] Boulouard, A., and M. LeRouzic, "Analysis of Rectangular Spiral Transformers for MMIC Applications," *IEEE Trans. Microwave Theory Tech.,* Vol. 37, August 1989, pp. 1257–1260.

[23] Chow, Y. L., G. E. Howard, and M. G. Stubbs, "On the Interaction of the MMIC and its Packaging," *IEEE Trans. Microwave Theory Tech.,* Vol. 40, August 1992, pp. 1716–1719.

[24] Chen, T-H, et al., "Broadband Monolithic Passive Baluns and Monolithic Double-Balanced Mixer," *IEEE Trans. Microwave Theory Tech.,* Vol. 39, December 1991, pp. 1980–1986.

[25] Marx, K. D., "Propagation Modes, Equivalent Circuits, and Characteristic Terminations for Multiconductor Transmission Lines with Inhomogeneous Dielectrics," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-21, July 1973, pp. 450–457.

[26] Djordjevic, A., et al., *Matrix Parameters for Multiconductor Transmission Lines,* Norwood, MA: Artech House, 1989.

12

Lumped-Element Circuits

Lumped elements have been in use in microwave circuits for more than 30 years. This chapter deals exclusively with these circuits where lumped elements, in addition to size reduction, provide distinct benefits in terms of bandwidth and electrical performance. Such circuits are classified into two categories: passive circuits and control circuits, as discussed in this chapter.

12.1 Passive Circuits

12.1.1 Filters

The basic theory of filters [1–10] is based on a combination of lumped elements such as inductors and capacitors as shown in Figure 12.1. This configuration is a lowpass filter, and we can develop a prototype design with 1-Ω input–output impedance and a 1-rad cutoff frequency. From here, it is simply a matter of scaling the g values for various elements to obtain the desired frequency response and insertion loss. In addition, other filter types such as highpass, bandpass, and band-stop merely require a transformation in addition to the scaling to obtain the desired characteristics.

At RF frequencies and the lower end of the microwave frequency band, filters have been realized using lumped elements (chip/coil inductors and parallel plate chip capacitors) and employ printed circuit techniques or PCBs to connect them. Several hybrid MIC technologies such as thin film, thick film, and cofired ceramic are being used to develop such circuits. Lumped-element filters can be implemented easily, and using currently available surface-mounted components one can meet size and cost targets in high-volume production. Due to the low

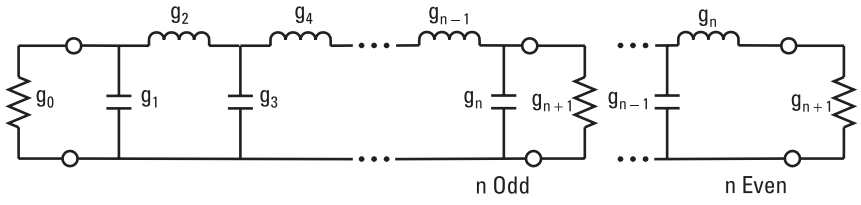


Figure 12.1 Lowpass filter prototype.

Q of inductors and capacitors, it is not possible to realize narrowband filters using MIC or MMIC technologies for some wireless applications.

The temperature sensitivity of lumped capacitors is far greater than the temperature variation in inductors. Therefore, the lumped-element filter's performance over temperature is mainly evaluated by the temperature coefficient of the capacitors [11]. The temperature sensitivity in such filters is minimized either by using only suitably designed coil inductors in which the shunt capacitance is contained in the self-resonance of the coil or thermally stable discrete capacitors.

12.1.1.1 Ceramic Lumped-Element Filters

A five-pole elliptic lowpass filter was developed [12] using thick-film printed inductors and discrete capacitors. The design goals were $f_c = 150$ MHz, passband ripple less than 1 dB, stop-band attenuation less than 40 dB at $1.5f_c$ and return loss greater than 20 dB. Figure 12.2(a) shows the design values, in which the nearest available standard values of the capacitors were used. The inductors were printed on 25-mil alumina substrate $\epsilon_r = 9.6$. Figure 12.2(b) shows the physical layout of this lowpass filter. Figure 12.3 compares the measured and simulated performance.

12.1.1.2 Superconducting Lumped-Element Filters

Conventionally, a low-loss narrowband filter having bandwidth on the order of 1% cannot be designed using a lumped-element approach due to its low Q values. However, such filters can be realized using *high-temperature superconductor* (HTS) substrates. A third-order bandpass filter with a center frequency of 1.78 GHz and 0.84% fractional bandwidth was designed and fabricated using HTS thin-film lumped elements [13]. Figure 12.4(a) shows its schematic and Figure 12.4(b) shows the layout. The filter was patterned using single-sided YBCO film on a MgO substrate. All sides, including the bottom of the substrate and the inner ends of spirals and capacitors bonding pads, were covered with silver. Components were wired together using 40-μm-diameter gold wires and ultrasonic bonding.

Figure 12.5 shows the measured response of the filter operating at 20K. The two sets of data represent results obtained with one and two wires per

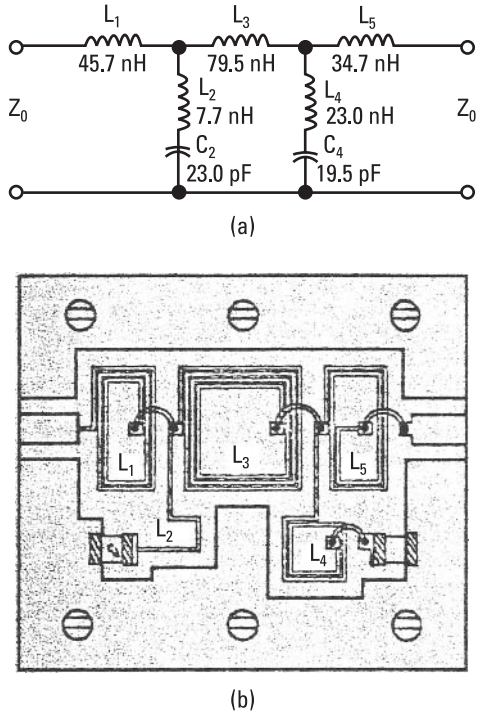


Figure 12.2 Five-pole lowpass elliptic filter: (a) schematic and (b) physical layout.

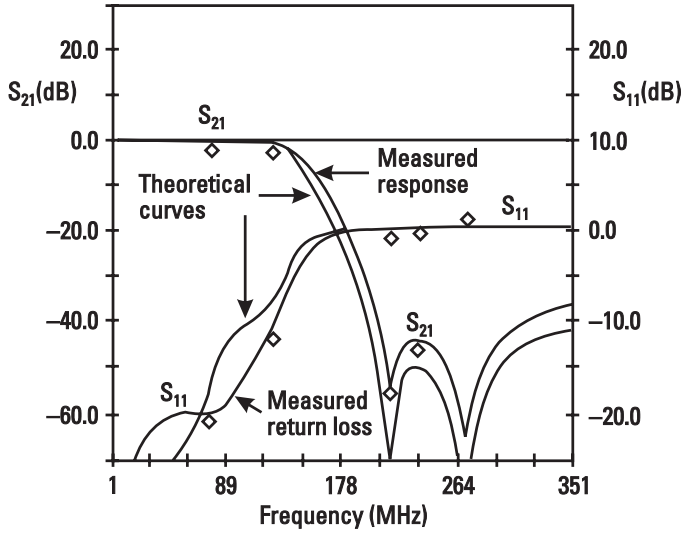


Figure 12.3 Simulated and measured performance of the lumped-element based five-pole lowpass elliptic filter.

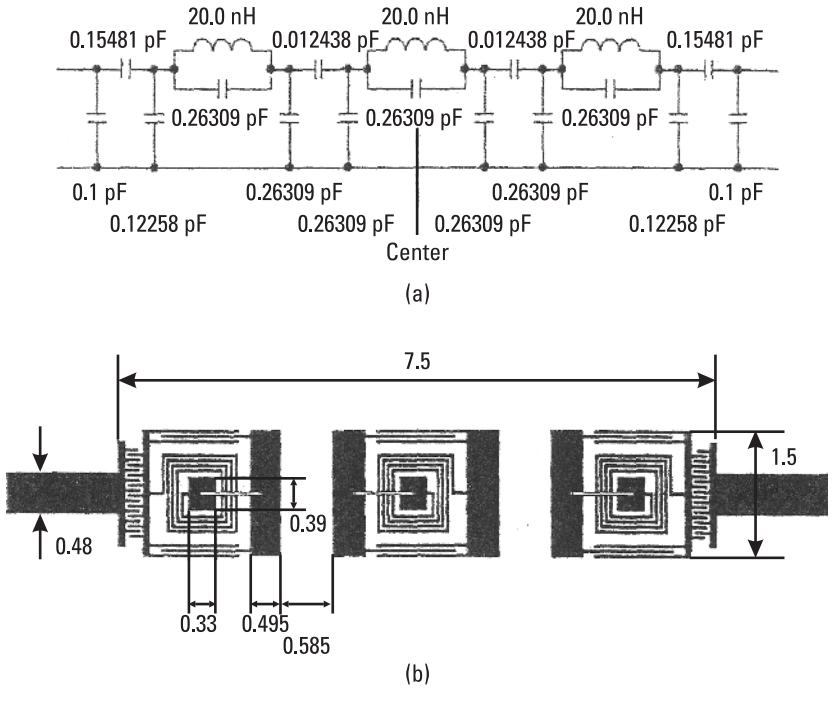


Figure 12.4 Lumped-element three-pole bandpass filter: (a) schematic and (b) physical layout. All dimensions are in millimeters. (*From:* [13]. © 2001 John Wiley. Reprinted with permission.)

connection. Measured insertion loss was about 1.5 dB at 1.725 GHz over 0.84% fractional bandwidth. The difference between the simulated and measured center frequency was attributed to substrate properties and etching accuracy.

Ong et al. [14] have reported a HTS bandpass filter using a dual-spiral resonator approach.

12.1.2 Hybrids and Couplers

Hybrids and couplers are indispensable components in the rapidly growing applications of microwaves in electronic warfare, radar, and communication systems. These circuits are often used in frequency discriminators, balanced amplifiers, balanced mixers, automatic level controls, and many other wireless applications. Hybrids are realized by directly connecting circuit elements, whereas couplers are realized using sections of transmission lines placed in proximity. They have four ports and have matched characteristics at all four ports; that is, over the specified frequency range the reflection coefficients are very small, usually less than 0.1, which makes them very suitable for insertion

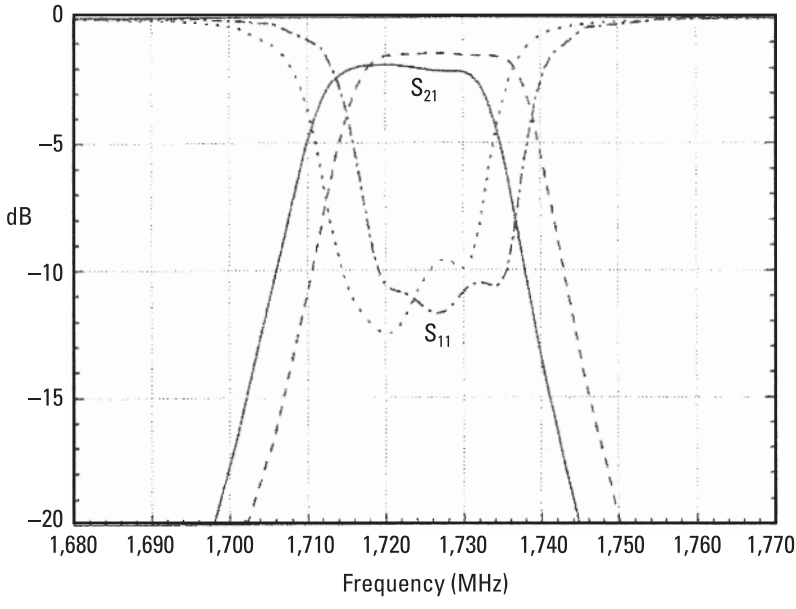


Figure 12.5 Measured performance of the three-pole bandpass filter with one wire connection (solid line: S_{21}; dotted line: S_{11}) and two wire connection (dashed line: S_{21}; dashed-dotted line: S_{11}). (*From:* [13]. © 2001 John Wiley. Reprinted with permission.)

in a circuit or subsystem. The theory of these couplers is well described in the literature [1, 4, 7, 8, 15–20]. In this section, design equations are given, and design methods for several couplers are described.

12.1.2.1 Parameter Definition

A hybrid or directional coupler can in principle be represented as a multiport network, as shown in Figure 12.6. The structure has four ports: input, direct, coupled, and isolated. If P_1 is the power fed into port 1 (which is matched to the generator impedance) and P_2, P_3, and P_4 are the powers available at ports 2, 3, and 4, respectively (while each of the ports is terminated by its characteristic

Figure 12.6 Four-port network.

impedance), the two most important parameters that describe the performance of this network are its coupling factor and directivity, defined as follows:

$$\text{Coupling factor (dB)} = C = 10 \log \frac{P_1}{P_3} \tag{12.1a}$$

$$\text{Directivity (dB)} = D = 10 \log \frac{P_3}{P_4} \tag{12.1b}$$

The isolation and transmitted power are given by

$$\text{Isolation (dB)} = I = 10 \log \frac{P_1}{P_4} = D + C \tag{12.2a}$$

$$\text{Transmitted power (dB)} = T = 10 \log \frac{P_2}{P_1} \tag{12.2b}$$

As a general rule, the performance of these circuits is specified in terms of coupling, directivity, and the terminating impedance at the center frequency of the operating frequency band. Usually, the isolated port is terminated in a matched load. Normally coupling, directivity, and isolation are expressed in decibels and are positive quantities. For many applications, a single-section coupler has an inadequate bandwidth. A multisection design that is a cascaded combination of more than one single-section coupler results in a larger bandwidth. The number of sections to be used depends on the tolerable insertion loss, bandwidth, and the available physical space.

12.1.2.2 90° Hybrid

The 90° hybrids use directly connected circuit elements and can be implemented either using a distributed approach or lumped elements. Because the design of the lumped-element hybrid is derived from the distributed configuration, both approaches are briefly described next.

The branch-line type of hybrid shown in Figure 12.7 is one of the simplest structures for a 90° hybrid in which the circumference is an odd multiple of λ. The geometry is readily realizable in any transmission medium. Branch-line hybrids have narrow bandwidths—on the order of 10%. As shown in Figure 12.7, the two quarter-wavelength-long sections spaced one-quarter wavelength apart divide the input signal from port 1 so that no signal appears at port 4. The signals appearing at ports 2 and 3 are equal in magnitude, but out of phase by 90°. The coupling factor is determined by the ratio of the impedance of the shunt (Z_p) and series (Z_r) arms and is optimized to maintain proper match

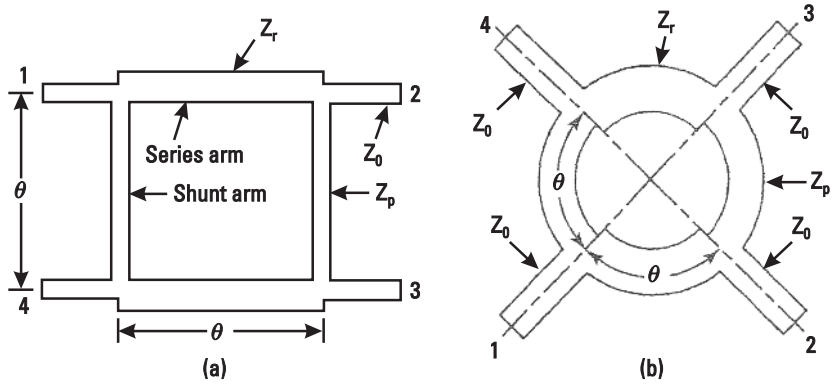


Figure 12.7 (a, b) A 90° hybrid configuration.

over the required bandwidth. In terms of Z_r and Z_p, the scattering parameters of a branch-line coupler are given by

$$S_{21} = -j\frac{Z_r}{Z_0}, \quad S_{31} = -\frac{Z_r}{Z_p}, \quad S_{41} = 0 \tag{12.3a}$$

For a 90° lossless matched hybrid, the following conditions hold:

$$|S_{21}|^2 + |S_{31}|^2 = 1$$

or

$$\left|\frac{Z_r}{Z_0}\right|^2 + \left|\frac{Z_r}{Z_p}\right|^2 = 1 \tag{12.3b}$$

For 3-dB coupling, the characteristic impedances of the shunt and series arms are Z_0 and $Z_0/\sqrt{2}$, respectively, for optimum performance of the coupler, with Z_0 being the characteristic impedance of the input and output ports. For most applications $Z_0 = 50\Omega$, thus shunt and series arms lines have characteristic impedances of 50Ω and 35.36Ω, respectively.

In MMICs, lumped capacitors can be easily realized and have become attractive in reducing the size of passive components. Reduced-size branch-line hybrids that use only lumped capacitors and small sections of transmission lines (smaller than $\lambda_g/4$) have also been reported [21]. The size of these hybrids is about 80% smaller than those for conventional hybrids and is therefore quite suitable for MMICs.

The lumped element 90° hybrid can be realized in either a *pi* or *tee* equivalent network. In MMICs, a pi network is preferred to a tee network because it uses fewer inductor elements with lower Q and occupies more space. The bandwidth of these couplers can be increased by using more sections of pi or tee equivalent networks, that is, two sections of 45° or three sections of 30°, to realize 90° sections or by properly selecting highpass and lowpass networks [22, 23]. Generally two to three sections are sufficient to realize a broadband 90° hybrid.

In the lumped-element implementation, each transmission line shown in Figure 12.7 is replaced by an equivalent pi lumped-element network as shown in Figure 12.8. The values of lumped elements are obtained by equating *ABCD*-matrix parameters for both these structures. The *ABCD*-matrix of a lossless transmission line section of characteristic impedance Z_r and electrical length θ is given by

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{bmatrix} \cos\theta & jZ_r \sin\theta \\ j\dfrac{1}{Z_r}\sin\theta & \cos\theta \end{bmatrix} \tag{12.4}$$

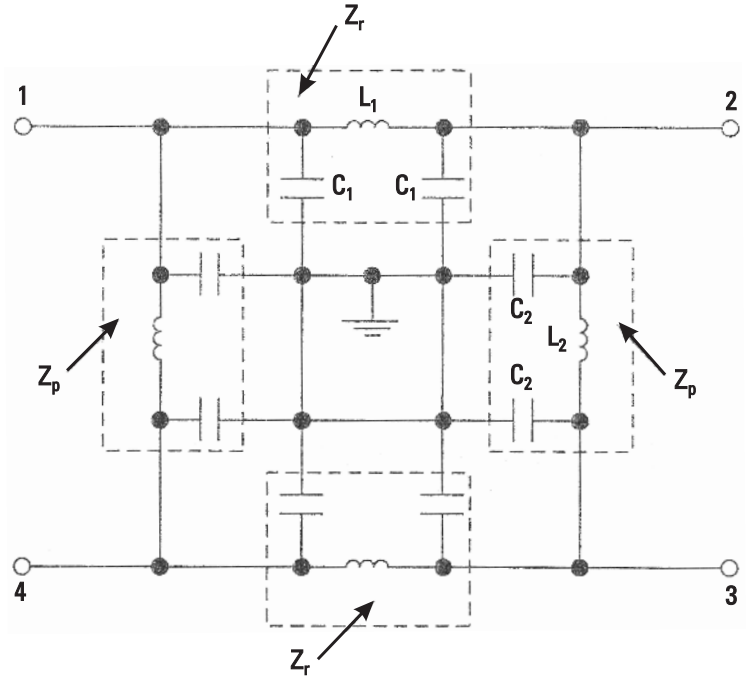


Figure 12.8 Lumped-element EC model for the 90° hybrid shown in Figure 12.7.

The *ABCD*-matrix of any of the pi networks shown in Figure 12.8 is given by

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C_1 & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_1 & 1 \end{bmatrix} \tag{12.5}$$

$$= \begin{bmatrix} 1 - \omega^2 L_1 C_1 & j\omega L_1 \\ j\omega C_1 (2 - \omega^2 L_1 C_1) & 1 - \omega^2 L_1 C_1 \end{bmatrix}$$

Equating the matrix elements in (12.4) and (12.5), we get

$$\cos\ \theta = 1 - \omega^2 L_1 C_1, \quad \theta = \cos^{-1}(1 - \omega^2 L_1 C_1) \tag{12.6a}$$

$$Z_r \sin\ \theta = \omega L_1 \tag{12.6b}$$

$$\frac{1}{Z_r} \sin\ \theta = \omega C_1 (2 - \omega^2 L_1 C_1) \tag{12.6c}$$

$$\frac{1}{Z_r} = \sqrt{\frac{2C_1}{L_1} - (\omega C_1)^2} \tag{12.6d}$$

or

$$L_1 = \frac{Z_r \sin\ \theta}{\omega} \tag{12.7a}$$

$$C_1 = \frac{1}{\omega Z_r} \sqrt{\frac{1 - \cos\ \theta}{1 + \cos\ \theta}} \tag{12.7b}$$

Similarly, for the shunt line,

$$L_2 = \frac{Z_p \sin\ \theta}{\omega} \tag{12.8a}$$

$$C_2 = \frac{1}{\omega Z_p} \sqrt{\frac{1 - \cos\ \theta}{1 + \cos\ \theta}} \tag{12.8b}$$

When $\theta = 90°$, element values become

$$L_1 = \frac{Z_r}{\omega},\ L_2 = \frac{Z_p}{\omega},\ C_t = C_1 + C_2 = \frac{1}{\omega}\left(\frac{1}{Z_r} + \frac{1}{Z_p}\right) \tag{12.8c}$$

The analysis just presented does not include losses and other lumped-element parasitic effects. Typical lumped-element values for a 900-MHz coupler designed for 50-Ω terminal impedance are $L_1 = 6.3$ nH, $L_2 = 8.8$ nH, and $C_t = 8.5$ pF. Over 900 ± 45 MHz the calculated value of amplitude unbalance and the phase difference between the output ports are ±0.2 dB and 90 ± 2°, respectively. Lumped-element quadrature hybrids with low insertion loss and wide bandwidth have been developed using a micromachining process [24].

12.1.2.3 Rat-Race Hybrid

Rat-race hybrid couplers, like 90° hybrids, use directly connected circuit elements and can be realized either using a distributed approach or lumped elements. Both techniques are briefly discussed next.

The rat-race hybrid is a special kind of branch-line coupler in which the circumference is an odd multiple of 1.5λ. As a result, the phase difference between the two outputs is 180°. The simplest version of this circuit is shown in Figure 12.9. Ports 1–2, 2–3, and 3–4 are separated by 90°, and port 1 and port 4 are three-quarter wavelengths away from each other. Because the characteristic impedance of each line is Z_0 and in the ring is $\sqrt{2}Z_0$, and the phase relationships shown in the structure, any power fed into port 3 splits equally into two parts that add up in phase at ports 2 and 4, and out of phase at port 1. As a result, port 1 is isolated from the input. Similarly, power fed at port 1 divides equally between ports 2 and 4 with 180° phase difference, and port 3 remains isolated.

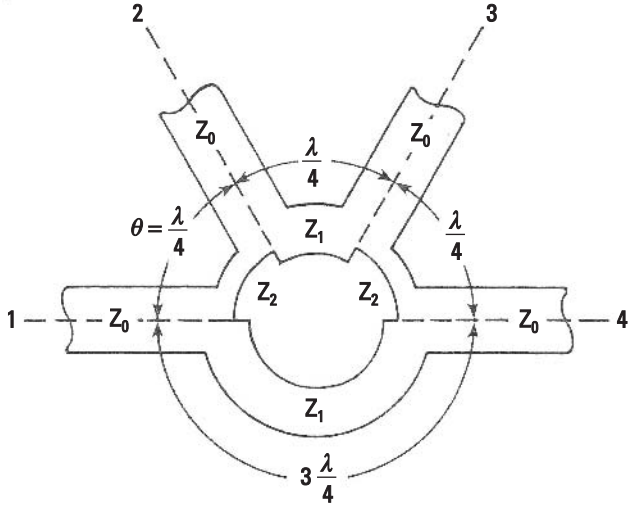


Figure 12.9 Rat-race hybrid configuration.

At the center frequency, the scattering parameters for a matched, lossless hybrid in terms of Z_1 and Z_2 (Figure 12.9) are given by

$$S_{21} = -j\frac{Z_0}{Z_2} \tag{12.9a}$$

$$S_{41} = j\frac{Z_0}{Z_1} \tag{12.9b}$$

$$S_{31} = 0 \tag{12.9c}$$

$$|S_{21}|^2 + |S_{41}|^2 = 1 \tag{12.9d}$$

The rat-race hybrid has a bandwidth (>20%) wider than that of a 90° hybrid.

The design of a lumped-element rat-race hybrid is similar to that of the lumped-element 90° hybrid described in the previous section. A lumped-element EC model for the 180° hybrid is shown in Figure 12.10. Three 90° sections are replaced by lowpass pi networks and the 270° (or −90°) section is replaced by an equivalent highpass tee network [25]. Following the same procedure as described for the 90° hybrid, the lumped elements for the pi section can be expressed as follows:

$$L_1 = \frac{\sqrt{2}Z_0 \sin\theta}{\omega} \tag{12.10a}$$

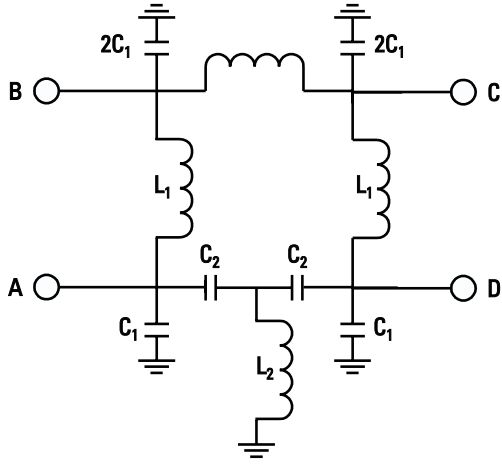


Figure 12.10 The lumped-element EC model for the 180° hybrid.

$$C_1 = \frac{1}{\sqrt{2}Z_0\omega}\sqrt{\frac{1-\cos\theta}{1+\cos\theta}} \tag{12.10b}$$

For the tee network, the *ABCD*-matrix is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{-j}{\omega C_2} \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \frac{-j}{\omega L_2} & 1 \end{bmatrix}\begin{bmatrix} 1 & \frac{-j}{\omega C_2} \\ 0 & 1 \end{bmatrix} \tag{12.11}$$

$$= \begin{bmatrix} 1-\frac{1}{\omega^2 L_2 C_2} & \frac{-j}{\omega C_2}\left(2-\frac{1}{\omega^2 L_2 C_2}\right) \\ \frac{-j}{\omega L_2} & 1-\frac{1}{\omega^2 L_2 C_2} \end{bmatrix}$$

Equating the matrix elements in (12.4) and (12.11), and using $Z_r = \sqrt{2}Z_0$,

$$L_2 = \frac{-\sqrt{2}Z_0}{\omega \sin\theta} \tag{12.12a}$$

$$C_2 = \frac{1}{\sqrt{2}Z_0\omega}\sqrt{\frac{1+\cos\theta}{1-\cos\theta}} \tag{12.12b}$$

when $\theta = 270°$ or $-90°$, element values for a 50-Ω system become $L_1 = L_2 = 11.25/f$ nH, and $C_1 = C_2 = 2.25/f$ pF, where f is the center frequency in gigahertz.

12.1.2.4 Directional Couplers

When two unshielded transmission lines as shown in Figure 12.11 are placed in proximity to each other, a fraction of the power present on the main line is coupled to the secondary line. The power coupled is a function of the physical dimensions of the structure, the frequency of operation, and the direction of propagation of the primary power. In these structures, continuous coupling is realized between the electromagnetic fields of the two lines, also known as parasitic coupling. If the coupled lines are of the TEM type (striplines), the power coupled to port 2 is through a backward wave, and the structure is called a *backward-wave directional coupler.* In such couplers ports 2, 3, and 4 are known as coupled, isolated, and direct ports, respectively. The phase difference between ports 1 and 2 and between ports 1 and 4 are 0 and 90°, respectively.

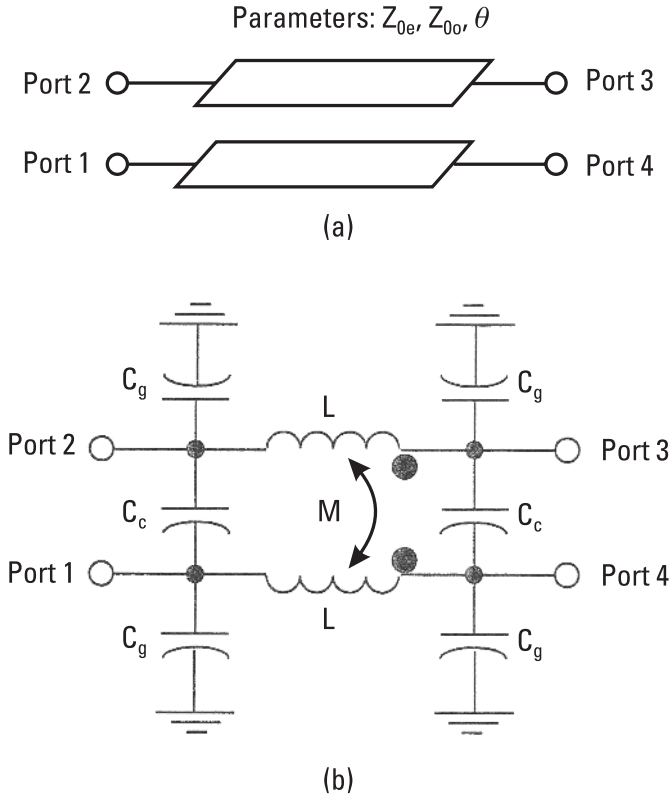


Figure 12.11 (a) Two-conductor microstrip coupled transmission lines and (b) lumped-element model.

The design equations for the TEM coupler shown in Figure 12.11(a) are summarized in the following at the center frequency of the band:

$$\theta_c = \theta_e = \theta_0 = \pi/2, \quad Z_0^2 = Z_{0e} Z_{0o} \tag{12.13a}$$

$$C = -20 \log \left| \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \right| \quad \text{dB} \tag{12.13b}$$

$$Z_{0e} = Z_0 \left(\frac{1 + 10^{-C/20}}{1 - 10^{-C/20}} \right)^{1/2} \tag{12.14a}$$

$$Z_{0o} = Z_0 \left(\frac{1 - 10^{-C/20}}{1 + 10^{-C/20}} \right)^{1/2} \tag{12.14b}$$

where subscripts e and o denote even and odd mode, C is the coupling coefficient expressed in decibels with positive sign, and Z_0 is the terminating impedance. To maximize the effective usable bandwidth, it is often desirable to overcouple at the design frequency, thus permitting a plus and minus tolerance across the frequency range.

Several existing coupler configurations have been transformed into new layouts to meet size target values. Some of these new configurations such as lumped-element couplers [26] and spiral directional couplers [27] are briefly described next.

12.1.2.5 Lumped-Element Couplers

The coupler shown in Figure 12.11(a) can be modeled as a lumped-element EC as shown in Figure 12.11(b). The values for L, M, C_g, and C_c in terms of Z_{0e}, Z_{0o}, and θ are obtained as follows [26]:

$$L = \frac{(Z_{0e} + Z_{0o})\ \sin\ \theta}{4\pi f_0}, \quad C_g = \frac{\tan(\theta/2)}{Z_{0e} 2\pi f_0} \tag{12.15a}$$

$$M = \frac{(Z_{0e} - Z_{0o})\ \sin\ \theta}{4\pi f_0}, \quad C_c = \left(\frac{1}{Z_{0o}} - \frac{1}{Z_{0e}}\right) \frac{\tan(\theta/2)}{4\pi f_0} \tag{12.15b}$$

where f_0 is the center frequency and $\theta = 90°$ at f_0. For a given coupling, using (12.14), the values of Z_{0e} and Z_{0o} are determined and then lumped-element values are calculated using (12.15). The self and mutual inductors are realized using a spiral inductor transformer, and the capacitors C_g and C_c are of the MIM type and their partial values are also included in the transformer's parasitics.

12.1.2.6 Spiral Directional Couplers

To obtain a small-size directional coupler with tight coupling, a coupled structure in the spiral shape (also known as a *spiral coupler*) is realized. Printing the spiral conductor on high dielectric constant materials further reduces the size of the coupler. In this case tight coupling is achieved by using loosely coupled parallel-coupled microstrip lines placed in proximity with the spiral configuration. This structure, as shown in Figure 12.12, uses two turns and resembles a multiconductor structure. Design details of such couplers and their modifications are given in [27], and are briefly summarized here. However, accurate design of such structures is only possible by using EM simulators.

As reported in [27], the total length of the coupled line, on the alumina substrate, along its track is $\lambda_0/8$, where λ_0 is the free-space wavelength at the center frequency and $D \cong \lambda_0/64 + 4W + 4.5S$. Parameters D, W, and S are shown in Figure 12.12. Longer lengths result in tighter couplings. The typical line width W and spacing S are approximately 500 and 40 μm, respectively,

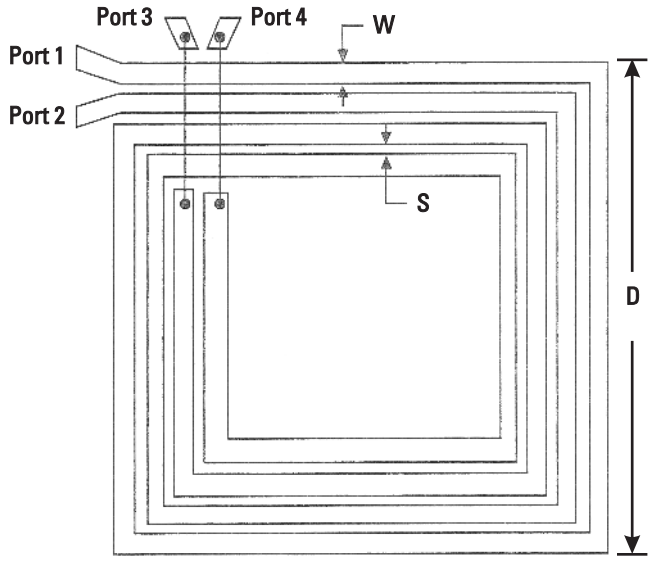


Figure 12.12 Top conductor layout of a two-turn spiral coupler.

for a 0.635-mm-thick alumina ($\epsilon_r = 9.6$) substrate. In the spiral configuration, coupling is not a strong function of spacing between the conductors. The conductors were about 5 μm thick. Measured coupled power, direct power, return loss, and isolation for the two-turn spiral coupler were approximately −3.5, −3.5, 22, and 18 dB, respectively.

12.1.2.7 Transformer Directional Couplers

Simple and inexpensive broadband RF directional couplers are based on coil transformers [28–30]. Figure 12.13 shows the schematic of a directional coupler in which two identical transformers wound on magnetically isolated cores are used. The primary and secondary inductances of each transformer are denoted by L_1 and L_2, respectively. Ports A, B, C, and D are referred to as input,

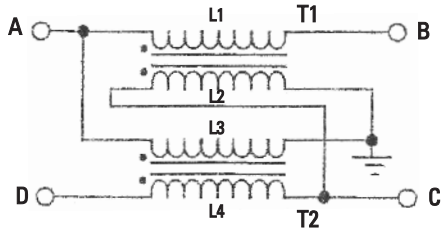


Figure 12.13 Broadband RF directional coupler schematic.

coupled, isolated, and direct ports, respectively. The analysis of such a coupler can be carried out by using its equivalent circuit, as shown in Figure 12.14, in which ports A, B, C, and D are terminated in Z_0, Z_b, Z_c, and Z_d, respectively. The inductive coupling between the primary and secondary is represented by $M = k\sqrt{L_1 L_2}$, where k is the coupling coefficient as discussed in Chapter 11. The expressions for coupling coefficients are derived using the Kirchhoff's voltage loop equations:

$$\text{Loop 1: } -V_{in} + I_1(Z_0 + Z_b + j\omega L_1) + I_2 Z_0 + I_3 j\omega M = 0 \tag{12.16a}$$

$$\text{Loop 2: } -V_{in} + I_1 Z_0 + I_2(Z_0 + j\omega L_2) - I_4 j\omega M = 0 \tag{12.16b}$$

$$\text{Loop 3: } I_1 j\omega M + I_3(Z_c + j\omega L_2) + I_4 Z_c = 0 \tag{12.16c}$$

$$\text{Loop 4: } -I_2 j\omega M + I_3 Z_c + I_4(Z_d + Z_c + j\omega L_1) = 0 \tag{12.16d}$$

By solving the preceding equations for $Z_b = Z_c = Z_d = Z_0$, we obtain

$$I_a = I_1 + I_2 = \left(\frac{V_{\text{in}}}{Z_0}\right)\left(\frac{L_1 + L_2}{L_1 + 2L_2}\right) \tag{12.17a}$$

$$I_b = I_1 = \left(\frac{V_{\text{in}}}{Z_0}\right)\left(\frac{L_2}{L_1 + 2L_2}\right) \tag{12.17b}$$

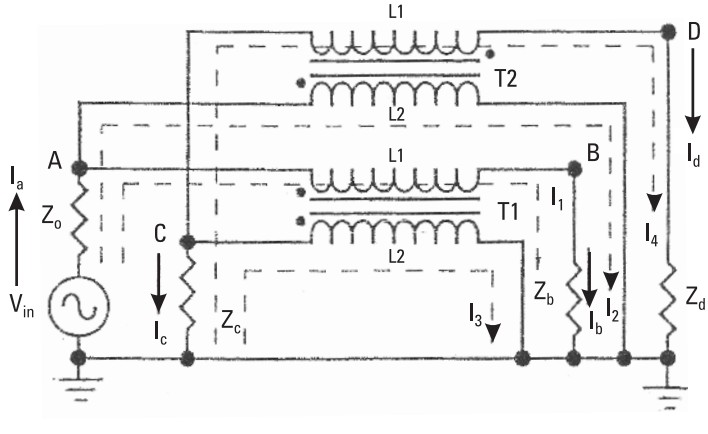


Figure 12.14 Equivalent circuit of the broadband directional coupler.

$$I_c = -(I_3 + I_4) = 0 \tag{12.17c}$$

$$I_d = I_4 = \left(\frac{V_{\text{in}}}{Z_0}\right)\left(\frac{M}{L_1 + 2L_2}\right) \tag{12.17d}$$

Voltage at each port can be written as

$$V_a = Z_0 I_a - V_{\text{in}} = \frac{V_{\text{in}} L_2}{L_1 + 2L_2} \tag{12.18a}$$

$$V_b = \frac{V_{\text{in}} L_2}{L_1 + 2L_2} \tag{12.18b}$$

$$V_c = 0 \tag{12.18c}$$

$$V_d = \frac{V_{\text{in}} M}{L_1 + 2L_2} \tag{12.18d}$$

Impedances looking into the three ports are given by

$$Z_a = \frac{V_a}{I_a} = Z_0\left(\frac{L_2}{L_1 + L_2}\right) \tag{12.19a}$$

$$Z_b = \frac{V_b}{I_b} = Z_0 \tag{12.19b}$$

$$Z_d = \frac{V_d}{I_d} = Z_0 \tag{12.19c}$$

The preceding equations show that except for the input port, all other ports are matched. The reflection coefficient at the input is given by

$$\rho = \frac{Z_0 - Z_a}{Z_0 + Z_a} = \frac{L_1}{L_1 + 2L_2} \tag{12.20}$$

Therefore, for the input port to be matched, $L_2 >> L_1$. When $L_1 = L_2$, ρ is 0.33 (VSWR = 2:1).

The power levels at various ports are given by:

$$P_a = V_a I_a = \left(\frac{V_{\text{in}}^2}{Z_0}\right) L_2 \left(\frac{L_1 + L_2}{(L_1 + 2L_2)^2}\right) \tag{12.21a}$$

$$P_b = \frac{V_b^2}{Z_0} = \left(\frac{V_{\text{in}}^2}{Z_0}\right)\left(\frac{L_2^2}{(L_1 + 2L_2)^2}\right) \tag{12.21b}$$

$$P_c = 0 \tag{12.21c}$$

$$P_d = \frac{V_d^2}{Z_0} = \left(\frac{V_{\text{in}}^2}{Z_0}\right)\left(\frac{L_1 L_2}{(L_1 + 2L_2)^2}\right) \tag{12.21d}$$

The relative coupled and direct power levels with respect to P_a are expressed as

$$P_{ba} = \frac{L_2}{L_1 + L_2} \tag{12.22a}$$

$$P_{da} = \frac{L_1}{L_1 + L_2} \tag{12.22b}$$

Table 12.1 summarizes the performance for various coupling coefficients for transformer directional couplers. Figure 12.15 shows a typical construction for a transformer directional coupler. Toroidal-based couplers have an operating frequency up to 1 GHz and bandwidths up to two decades [28].

12.1.3 Power Dividers/Combiners

Power dividers are commonly used in power amplifiers, mixers, active circulators, measurement systems, and phased-array antennas. In this section we discuss

Table 12.1
Simulated Performance for Various Transformer Directional Couplers

Turn Ratio N	L_2/L_1	Z_a/Z_0	P_{ba} (dB)	P_{da} (dB)	Input VSWR
1	1	0.500	–3.01	–3.01	2.00:1
2	4	0.800	–0.97	–6.99	1.25:1
3	9	0.900	–0.46	–10.00	1.11:1
4	16	0.940	–0.26	–12.30	1.06:1
5	25	0.960	–0.17	–14.10	1.04:1
6	36	0.973	–0.12	–15.70	1.03:1
8	64	0.984	–0.07	–18.30	1.02:1
10	100	0.990	–0.04	–20.00	1.01:1
12	144	0.993	–0.03	–21.60	1.01:1
15	225	0.996	–0.02	–23.50	1.00:1

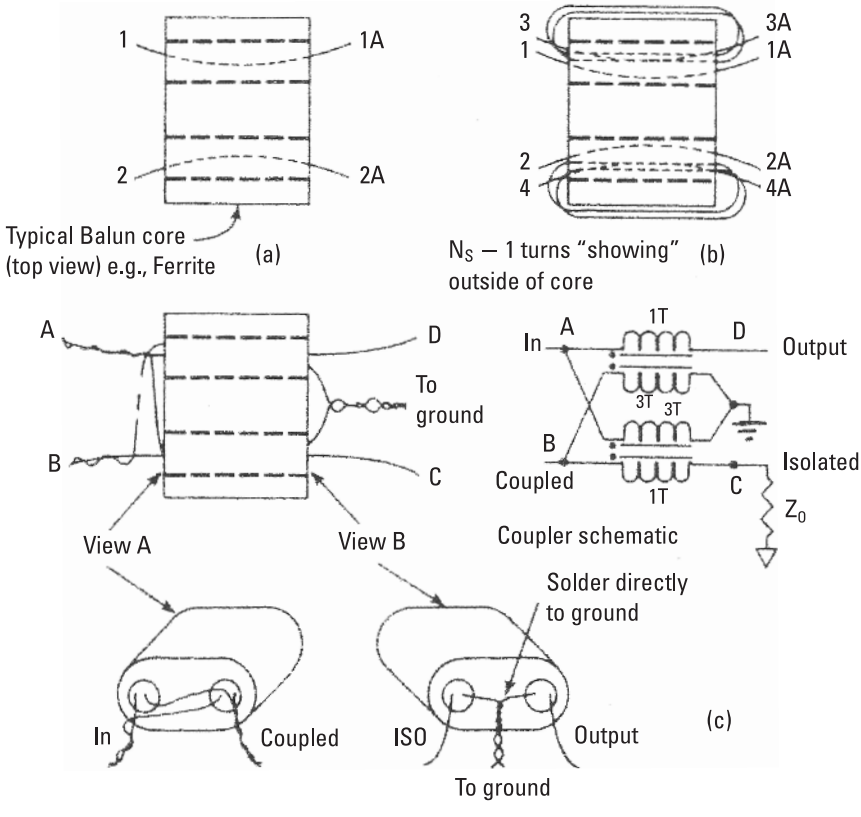


Figure 12.15 (a–c) Typical winding of a broadband 10-dB RF coupler. The number of turns in the primary and secondary are one and three, respectively.

three-port power splitters/combiners, among which the Wilkinson power divider is the most popular. A Wilkinson power divider [31, 32], also known as a two-way power splitter, offers broad bandwidth and equal phase characteristics at each of its output ports. Figure 12.16 shows its schematic diagram. The isolation between the output port is obtained by terminating the output ports by a series resistor. Each of the quarter-wave lines shown in Figure 12.16 has the characteristic impedance of $\sqrt{2}Z_0$ and the termination resistor has the value of $2Z_0\ \Omega$, Z_0 being the system impedance. A Wilkinson power divider offers a bandwidth of about one octave. The performance of this divider can be further improved, depending on the availability of space, by the addition of a $\lambda/4$ transformer in front of the power-division step. The use of multisections makes it possible to obtain a decade bandwidth. These power dividers can be designed to be unequal power splitters by modifying the characteristic impedances of the $\lambda/4$ sections and isolation resistor values [4, 8].

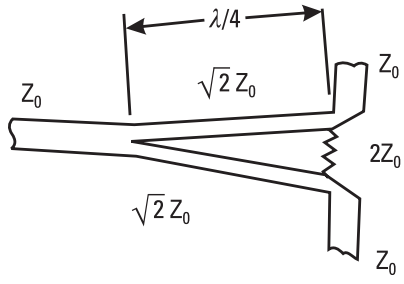


Figure 12.16 Wilkinson divider configuration.

The design of lumped-element power dividers [33, 34] is similar to 90° and 180° hybrids; that is, the $\lambda/4$ sections are replaced by equivalent LC networks. Figure 12.17 shows a lumped-element version of a two-way power divider using pi equivalent lowpass LC networks.

Table 12.2 summarizes the values of LC elements for the pi and tee equivalent lowpass and highpass LC networks. Here $Z_r = \sqrt{2}Z_0$ and $\theta = \pi/2$. Typical lumped-element values for a divider shown in Figure 12.17 designed at 1 GHz for 50Ω terminal impedance are L = 11.25 nH, C = 2.25 pF, and R = 100Ω. Again the simple equations included in Table 12.2 do not include losses and parasitic effects.

12.1.4 Matching Networks

Matching networks for RF and microwave circuits are generally designed to provide a specified electrical performance over the required bandwidth. To realize compact circuits, lumped-element matching networks are utilized to transform the device impedance to 50Ω. At RF frequencies lumped discrete

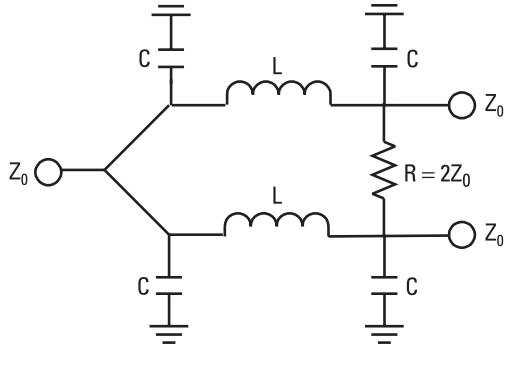
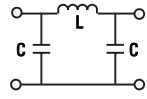
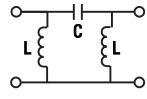
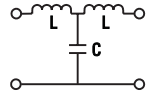
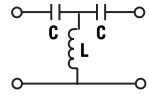


Figure 12.17 Lumped-element EC model for the two-way power divider.

Table 12.2
LC Element Values of Several Networks

Configuration		Element Values
"pi" lowpass		$L = \frac{\sqrt{2}Z_0 \sin\theta}{\omega}$ $C = \frac{1}{\sqrt{2}Z_0\omega}\sqrt{\frac{1-\cos\theta}{1+\cos\theta}}$
"pi" highpass		$L = \frac{\sqrt{2}Z_0}{\omega}\sqrt{\frac{1+\cos\theta}{1-\cos\theta}}$ $C = \frac{1}{\sqrt{2}Z_0\omega\sin\theta}$
"tee" lowpass		$L = \frac{\sqrt{2}Z_0}{\omega}\sqrt{\frac{1-\cos\theta}{1+\cos\theta}}$ $C = \frac{\sin\theta}{\omega\sqrt{2}Z_0}$
"tee" highpass		$L = \frac{\sqrt{2}Z_0}{\omega\sin\theta}$ $C = \frac{1}{\sqrt{2}Z_0\omega}\sqrt{\frac{1+\cos\theta}{1-\cos\theta}}$

spiral inductors, MIM capacitors, and thin-film resistors are primarily used in matching networks. Lumped-element circuits that have lower Q than distributed circuits have the advantage of smaller size, lower cost, and wide bandwidth characteristics. These are especially suitable for MMICs and for broadband hybrid MICs in which "real estate" requirements are of prime importance. Impedance transformations on the order of 20:1 can be easily accomplished using the lumped-element approach. Therefore, high-power devices that have very low impedance values can easily be tuned with large impedance transformers realized using lumped elements. At low frequencies (below C-band), MMICs designed using lumped inductors and capacitors have an order of magnitude smaller die size compared to ICs designed using distributed matching elements such as microstrip lines.

Lowpass matching networks in amplifiers provide good rejection for high-frequency spurious and harmonic frequencies but have a tendency toward high

gain (and, hence, instability) at very low frequencies. Thus, in multistage amplifiers, a combination of bandpass at the input stage and interstages and lowpass at the output stage will produce the required frequency response. This section describes various *LC* configurations suitable for designing matching networks.

An impedance can be represented by a parallel combination of a resistance and a reactance or an equivalent series combination of a resistance and reactance as shown in Figure 12.18. Thus, one can convert a parallel network to an equivalent series network using the following relations:

$$R_S = R_P X_P^2/(R_P^2 + X_P^2) \tag{12.23a}$$

$$X_S = X_P R_P^2/(R_P^2 + X_P^2) \tag{12.23b}$$

Similarly, a series network can be converted into a parallel network using the following equations:

$$R_P = (R_S^2 + X_S^2)/R_S \tag{12.24a}$$

$$X_P = (R_S^2 + X_S^2)/X_S \tag{12.24b}$$

12.1.4.1 L-Network

Inductors and capacitors connected in an L-section configuration are widely used as impedance-matching circuit elements. As shown in Figure 12.19, eight possible arrangements of inductors and capacitors can be utilized. The range

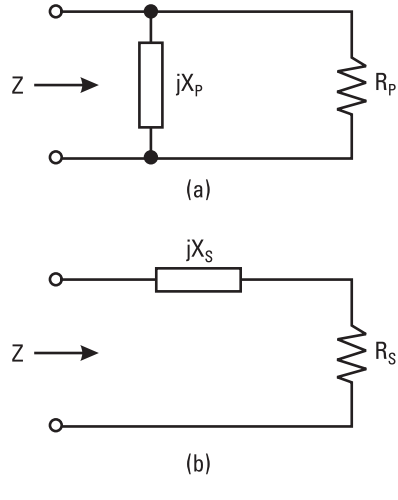


Figure 12.18 (a) Parallel and (b) series representations of an impedance.

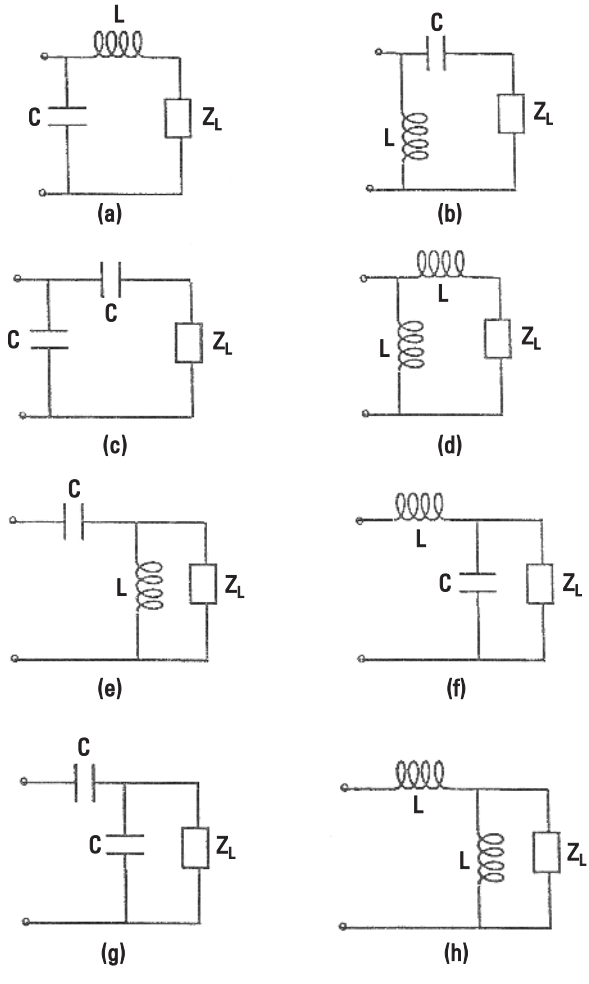


Figure 12.19 (a–h) Eight topologies of lumped-element matching networks.

of impedance transformation depends on the value of the original inductors or capacitors in the L-configuration. Rearranging (12.24a), we get

$$\frac{R_P}{R_S} = 1 + Q^2, \quad \text{where } Q = X_S/R_S \tag{12.25}$$

When a reactance X_S is added in series with a resistor R_S, and converted to an equivalent parallel combination, the resistance increases by a $1 + Q^2$ factor. Conversely, when a reactance X_P is added in parallel with a resistor R_P, and converted to an equivalent series combination, the resistance decreases.

These properties of network conversion are used to design L-section matching networks.

Two basic topologies of L-section matching networks are shown in Figure 12.20. These networks consist of purely reactive elements. The impedances Z_{SE} and Z_{SH} of the series (reactance) and shunt (susceptance) elements are represented by jX and jB, respectively. Consider a design problem where the complex load impedance Z_L (= $R_L + jX_L$) is required to be transformed to a real impedance Z_{IN} (= Z_0).

When $R_L < Z_0$, the configuration in Figure 12.20(a) is used and

$$Z_{\text{in}} = Z_0 = \left[jB + \frac{1}{R_L + j(X + X_L)} \right]^{-1} \tag{12.26}$$

By equating real and imaginary parts,

$$X = \pm\sqrt{R_L(Z_0 - R_L)} - X_L \tag{12.27a}$$

$$B = \pm\frac{\sqrt{(Z_o - R_L)/R_L}}{Z_0} \tag{12.27b}$$

The positive and negative signs imply that there are two possible solutions. Positive reactance corresponds to an inductor and negative reactance implies a capacitor. Similarly, a positive susceptance corresponds to a capacitor and a negative susceptance implies an inductor.

If $R_L > Z_0$, the configuration in Figure 12.20(b) is used and

$$Z_{\text{in}} = Z_0 = jX + \frac{1}{jB + (R_L + jX_L)^{-1}} \tag{12.28}$$

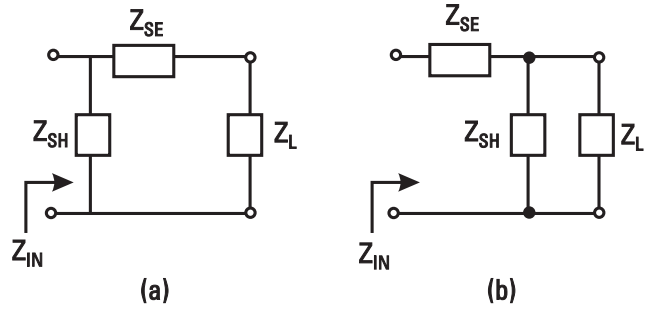


Figure 12.20 (a, b) Two basic configurations of L-shaped lumped-element matching networks.

Again, by equating real and imaginary parts,

$$B = \frac{X_L \pm \sqrt{R_L/Z_0}\sqrt{R_L^2 + X_L^2 - Z_0 R_L}}{R_L^2 + X_L^2} \tag{12.29a}$$

$$X = \frac{1}{B} + \frac{X_L Z_0}{R_L} - \frac{Z_0}{BR_L} \tag{12.29b}$$

Again, there are two possible solutions. Once the values of X and B are determined, one could proceed to calculate the values of the lumped elements needed at the design frequency.

12.1.4.2 Tee and Pi Networks

To get a larger bandwidth and realize large impedance ratios, more elements are required in the matching networks. The tee and pi arrangements of lumped elements, shown in Figure 12.21, are commonly used. Such arrangements are simply considered back-to-back L-section networks. The addition of one more element to the simple L-section matching circuit gives the designer much greater control over the bandwidth and also permits the use of more practical circuit elements. The circuit configurations and circuit element values [35] are given in Figure 12.21 where

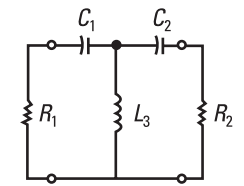
$$M = \frac{R_2}{R_1} > 1 \quad \text{and} \quad N > M \tag{12.30}$$

and where M is the impedance transformation ratio and N is a variable. By properly selecting N, a compromise is obtained in terms of bandwidth and realizable circuit element values. For more details the readers are referred to recently published books [36, 37].

12.1.5 Lumped-Element Biasing Circuit

Solid-state devices require low frequency and dc bias circuitry that must be separated from the RF circuit. In other words, when a bias voltage is applied to the device, the RF energy should not leak through the bias port. In practice, many biasing circuits are used [20]. Lumped-element biasing circuits are described in this section. The circuit performance is discussed by calculating the VSWR response of these circuits. The desirable features of these biasing circuits are small RF leakage and broad bandwidth characteristics.

A shunt coil inductor, L, also known as an RF choke, is used as a biasing element while a series capacitor C is used to isolate the bias voltage applied to

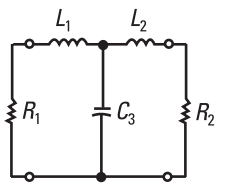


$$C_1 = \left(\omega_0 R_1 \sqrt{N-1}\right)^{-1}$$

$$C_2 = \left(\omega_0 R_2 \sqrt{\frac{N}{M}-1}\right)^{-1}$$

$$L_3 = \frac{NR_1}{\omega_0\left(\sqrt{N-1}+\sqrt{\frac{N}{M}-1}\right)}$$

(a)

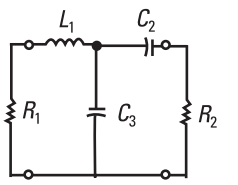


$$L_1 = R_1 \frac{\sqrt{N-1}}{\omega_0}$$

$$L_2 = R_2 \frac{\sqrt{\frac{N}{M}-1}}{\omega_0}$$

$$C_3 = \frac{\sqrt{N-1}+\sqrt{\frac{N}{M}-1}}{\omega_0 N R_1}$$

(b)

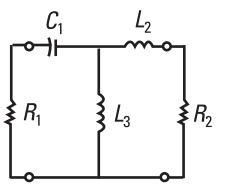


$$L_1 = R_1 \frac{\sqrt{N-1}}{\omega_0}$$

$$C_2 = \left(\omega_0 R_2 \sqrt{\frac{N}{M}-1}\right)^{-1}$$

$$C_3 = \frac{\sqrt{N-1}+\sqrt{\frac{N}{M}-1}}{\omega_0 N R_1}$$

(c)



$$C_1 = \left(\omega_0 R_1 \sqrt{N-1}\right)^{-1}$$

$$L_2 = R_2 \frac{\sqrt{\frac{N}{M}-1}}{\omega_0}$$

$$L_3 = \frac{NR_1}{\omega_0\left(\sqrt{N-1}-\sqrt{\frac{N}{M}-1}\right)}$$

(d)

Figure 12.21 (a–d) T-section matching configurations.

various circuits. Shunt inductor and series capacitor circuits are shown in the inset of Figure 12.22. The normalized admittance of the coil and normalized impedance of the capacitor backed by a 50-Ω matched element are given by

$$y = 1 - j\frac{Z_0}{\omega L} \tag{12.31}$$

$$z = 1 - j\frac{1}{\omega C Z_0} \tag{12.32}$$

If $y = z$, that is, $Z_0^2 = L/C$, the both elements will have an equal VSWR at all frequencies. The VSWR in each case can be written

$$\text{VSWR} = \big(1 + |\rho|\big)/\big(1 - |\rho|\big) \tag{12.33}$$

where

$$|\rho| = \frac{Z_0/\omega L}{[4 + (Z_0/\omega L)^2]^{1/2}} \quad \text{for a shunt coil} \tag{12.34a}$$

$$= \frac{1/\omega C Z_0}{[4 + (1/\omega C Z_0)^2]^{1/2}} \quad \text{for a series capacitor} \tag{12.34b}$$

The *insertion loss* (IL) of a reactive discontinuity having a VSWR, S, is given by

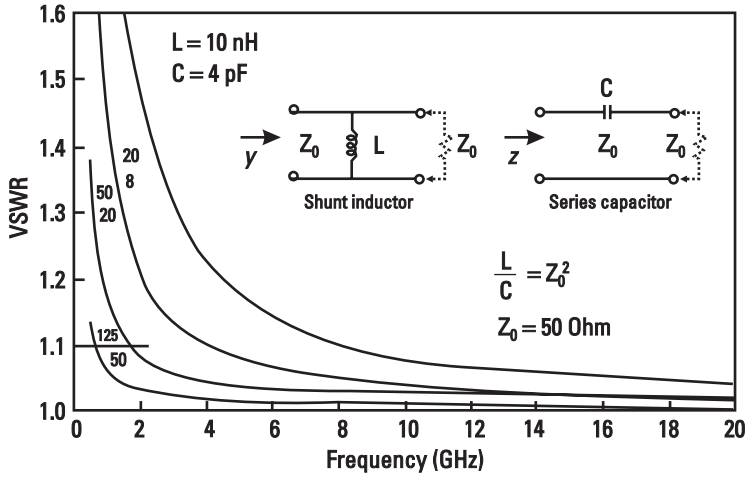


Figure 12.22 *L* and *C* biasing networks and their responses.

$$\text{IL} = 20 \log\left(\frac{S+1}{2\sqrt{S}}\right) \tag{12.35}$$

Variation of VSWR corresponding to these elements is shown in Figure 12.22. Higher values of L or C have a lower VSWR. When both of these elements are used simultaneously, the elements should be connected at the same plane. The normalized admittance of the capacitor, which is backed by a 50-Ω matched line, becomes

$$y_c = \frac{1 + j\dfrac{1}{\omega C Z_0}}{1 + \dfrac{1}{(\omega C Z_0)^2}} \tag{12.36}$$

This admittance will add to the admittance of the inductor ($y_L = -jZ_0/\omega L$). The total admittance y_t is given by

$$y_t = y_c + y_L \tag{12.37}$$

When $\omega C Z_0 >> 1$

$$y_t = 1 + j\left(\frac{1}{\omega C Z_0} - \frac{Z_0}{\omega L}\right) \tag{12.38}$$

If $Z_0^2 = L/C$, $y_t = 1$. Thus, the VSWR will be unity and also independent of frequency as long as L and C are independent of frequency.

12.2 Control Circuits

Semiconductor control circuits, such as switches, phase shifters, attenuators, and modulators, have been used extensively in radar, communication systems, electronic warfare, wireless applications, instruments, and other systems for controlling the signal flow or to adjust the phase and amplitude of the signal. At RF, microwave, and millimeter-wave frequencies, many of the problems of bandwidth, switching speed, power handling, high dynamic range, low voltage operations, and high operating frequency have already been solved. An excellent overview of control circuits and switching devices can be found in [7, 15, 17, 38–43]. Here only switches, phase shifters, and attenuators having unique performance when designed using lumped elements are described.

12.2.1 Switches

In microwave systems, the transmitter and receiver section is called a *transceiver.* Transceivers have different requirements for switches including low and high power, narrowband and broadband, and high isolation. Lumped elements play an important role in achieving broad bandwidths, high isolation, and high power levels in RF/microwave switches. Examples of high isolation and high-power switches are discussed next.

12.2.1.1 High Isolation Switches

Several techniques are available for improving the isolation of switches, including the use of low "off" state capacitance FETs [44], distributed with tuning inductors [7, Chapter 12], and achieving band-rejection filter in the operating frequency range [45]. Basically, in these schemes either the off state capacitance of the switching device is tuned out or its effect is minimized. In all of these methods, the insertion loss of the switches more or less remains the same. Figure 12.23 shows a simplified version of a *single-pole single-throw* (SPST) switch using a band-rejection filter technique to improve the isolation in the operating frequency band. FETs 1, 2, and 3 constitute a conventional SPST switch, and the T-shaped R-C-R network is added to improve the isolation in the off state. To a first-order approximation, the element values of the R-C-R network can be calculated from the transistor's "on" state resistance and off state capacitance using the following equations [45]:

$$f_0 = \frac{1}{2\pi\sqrt{2C_{\text{off1}}\,C_{\text{off3}}R_{\text{on2}}R}} \tag{12.39a}$$

$$RC = 2R_{\text{on2}} \cdot (C_{\text{off1}} + C_{\text{off3}}) \tag{12.39b}$$

where R_{onx} and C_{offx} are the on resistance and off capacitance of the xth switching device, respectively. Here f_0 is the center frequency of the operating band and the switch is assumed to be terminated into a 50-Ω input–output impedance. With this method, the isolation was improved by more than 15 dB over about a 20% bandwidth in the C-band [45].

12.2.1.2 High-Power Switches

For several communication and radar applications, one needs high-power handling switches. The maximum power-handling capacity of switches depends on the maximum voltage that can be applied safely to the device in the off state and the maximum current limit of the FET in the on state. The maximum power, P_{max}, that can be transmitted for a shunt FET switch is given by

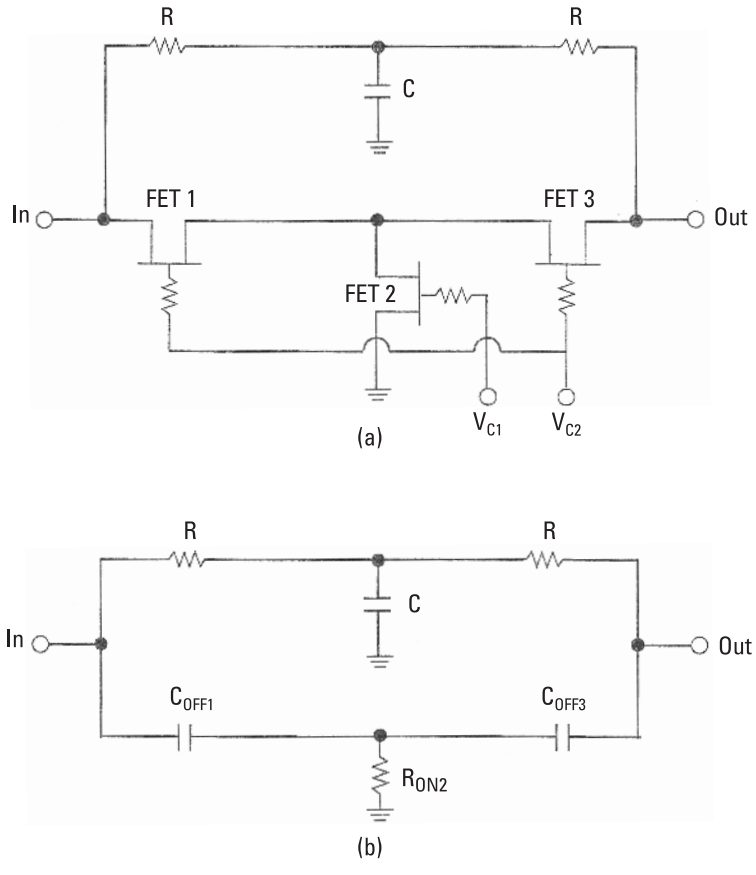


Figure 12.23 (a) Circuit configuration of the improved isolation FET switch and (b) its equivalent in the off state.

$$P_{\max} = \frac{(V_B - V_p)^2}{2Z_0} \tag{12.40}$$

For low-voltage applications, where the breakdown voltage is much greater than the control voltage V_c, the maximum power is given by

$$P_{\max} = \frac{2(V_c - V_p)^2}{Z_0} \tag{12.41}$$

where V_p is the pinch-off voltage of the device, V_B is the breakdown voltage between the gate and drain terminals, and Z_0 is the impedance level the shunt FET sees in its off state. Both V_c and V_p are positive quantities. When the

shunt FET is in the on state, there is no voltage at the gate terminal. The maximum power capacity is determined by the short-circuited current, which is equal to the maximum drain-source current (I_{dss}) of the FET or HEMT and is proportional to the gate periphery. Again, if Z_0 is the impedance level that the switch FET sees in its low impedance state, then the maximum power-handling capacity is given by

$$P_{max} = \frac{1}{2} I_{dss}^2 Z_0$$

or

$$I_{dss} = \sqrt{\frac{2P_{max}}{Z_0}} \tag{12.42}$$

Equations (12.40) and (12.42) are used to design switching FETs for high-power operation. Based on the maximum power requirements and a given breakdown voltage, the gate periphery of the FET is selected. Based on (12.40) and (12.42), available bias voltages and breakdown voltage, conventional switches can handle up to a few watts. Several methods have been discussed [43] to improve the power-handling capability of FET switches using low-power switching FETs. These techniques include (1) impedance transformation, (2) stacked FETs, and (3) *LC* resonant circuits. The impedance transformation technique that uses two $\lambda/4$ transformers occupy a considerably large area on GaAs chips. One can reduce the chip size by using lumped-element-based transformers; however, both impedance transformation and stacked FET techniques require FETs with large pinch-off voltages and high breakdown voltages. To overcome these limitations, a novel technique known as *LC*-resonant was introduced by Tokumitsu et al. [46]. This works well at low supply voltages and does not require high breakdown voltage FETs.

Figure 12.24 shows a conventional series/shunt FET *transmit/receive* (T/R) switch and *LC*-resonant circuit configuration. In an *LC*-resonant circuit switch configuration, the shunt FET (SW-a) in the transmitting path and series FET (SW-c) in the receiving path in Figure 12.24(a) are replaced with a combination of FETs and an *LC*-resonant circuit as shown in Figure 12.24(c). In Figure 12.24(b) each box is equivalent to an *LC*-resonant circuit. The *LC*-resonant circuit consists of spiral inductors and MIM capacitors. In Figure 12.24(c), the capacitance C_s represents the FET's total capacitance in the off state. When the FETs are in the on state, the switch between 1 and 2 is in the off state because of the parallel resonance of inductor L_1 and capacitance C_1. Conversely, the switch between 1 and 2 is in the on state when the FETs are in the off state, due to the series resonance of inductor L_1 and C_2 shunted by C_s.

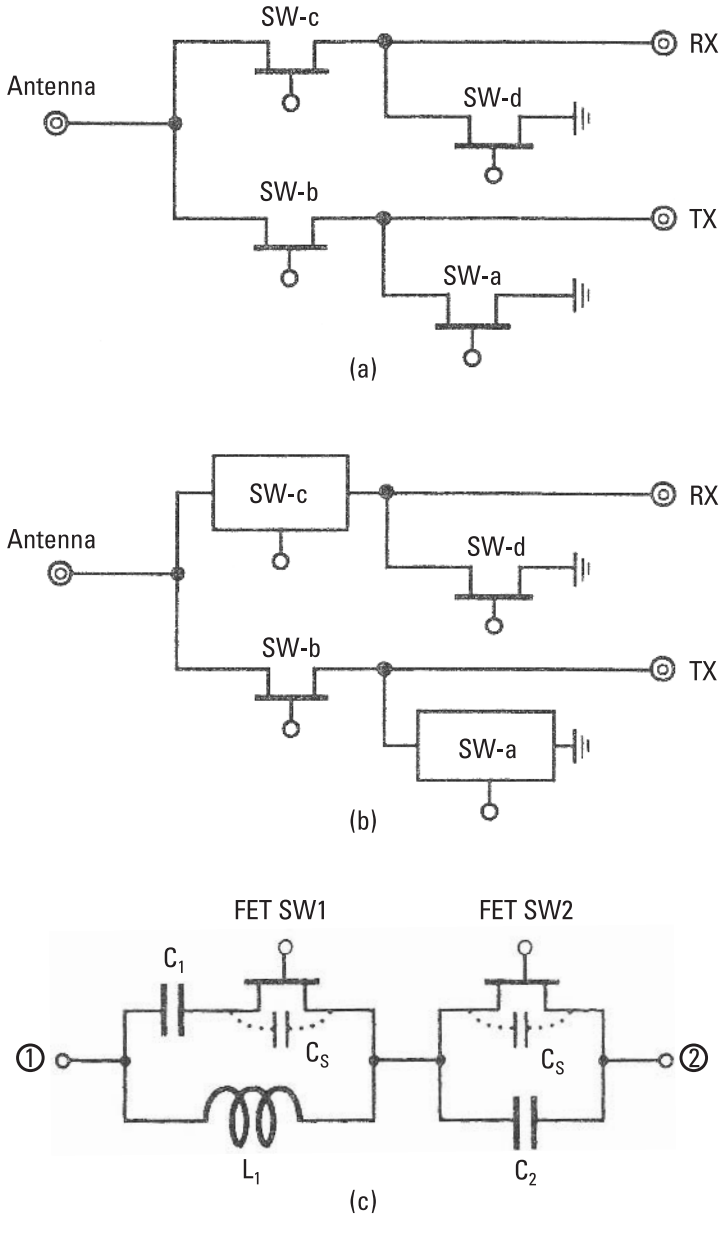


Figure 12.24 Typical T/R switch configurations for (a) conventional and (b) improved power-handling configuration; (c) SW-a/SW-c using the *LC*-resonant circuit technique.

Thus, in this scheme the FET switchable *LC* resonator uses a reverse control voltage scheme, that is, the FET switchable *LC* resonator is off when the FET devices are on and vice versa. Thus, this technique uses a unique scheme of biasing T/R switches—only one control line for both transmitting and receiving modes because all FETs will be on for the transmitting mode and off for the receiving mode. In the transmit mode, $P_{\max}$ and the linearity of *LC*-resonant circuit-based switches can be enhanced by increasing the gate periphery of FETs.

The $P_{\max}$ of this scheme is given by

$$P_{\max} = \frac{Z_0}{2}\left(\frac{I_{\text{dss}}}{Q_L}\right)^2 \tag{12.43}$$

where Z_0, I_{dss}, and Q_L are the system impedance, drain-source saturation current of the FET devices, and loaded Q of the T/R switch in the transmit mode, respectively. Figure 12.25 compares $P_{\max}$ for this scheme and stacked FET technique, where the pinch-off voltage is −1V and the control voltage is 0V/−2V. The *LC*-resonant circuit technique shows great potential for high-power operation for large gate periphery FETs.

Figure 12.26 shows a T/R switch schematic and a photograph of a MMIC chip. The *LC* resonators are placed where a large RF voltage is applied in the transmitting mode. There is one shunt FET in the receiver arm and two series FETs in the shunt branch of the transmitting arm. All FETs have 0.48-mm gate peripheries and 0V/−2V as the control voltage. The design trade-offs are the FET gate periphery (W_g), FET off capacitance C_{so} (pF/mm), and the

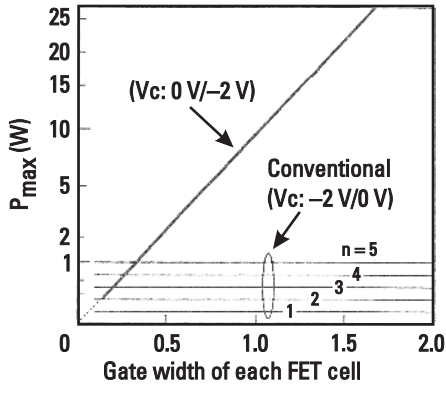


Figure 12.25 Maximum transmitting power comparison between the proposed *LC*-resonant T/R switch and conventional series/shunt FET T/R switches where I_{dss} = 0.2 A/mm, V_p = –1V, and Q_L = 0.44.

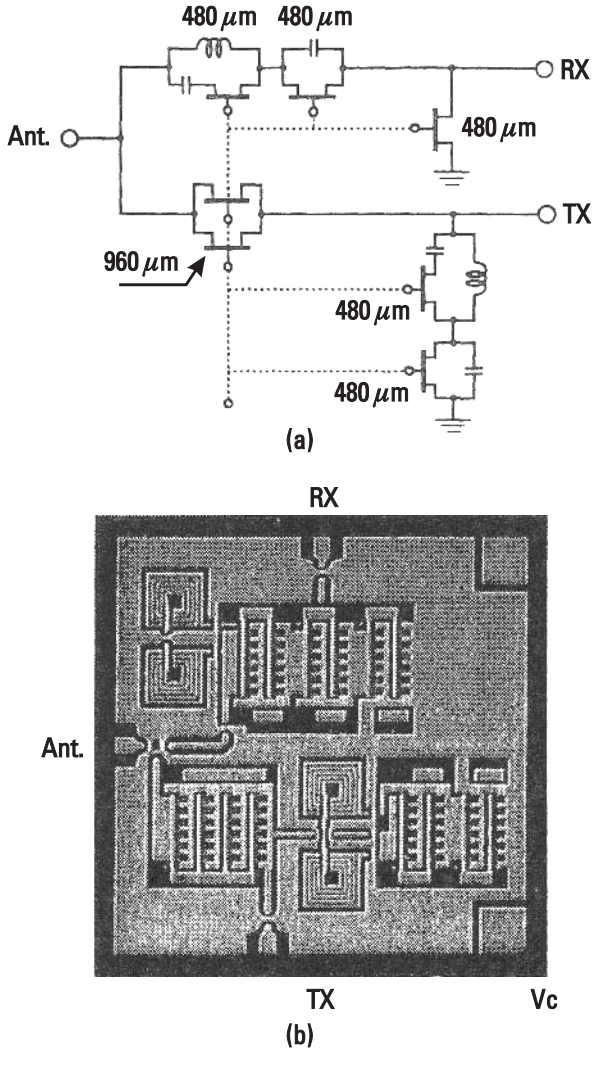


Figure 12.26 (a) Circuit topology and (b) MMIC photograph of an *LC*-resonant T/R switch, which measures only 2 × 2 mm in chip size. (*From:* [46]. © 1995 IEEE. Reprinted with permission.)

bandwidth balance between the transmitting and receiving arms. A simple design equation, relating these quantities, is given by [46]

$$W_{g\max}\ (\text{mm}) = 1.4[f_0\ (\text{GHz}) \cdot C_{so}\ (\text{pF/mm})]^{-1} \qquad (12.44)$$

where f_0 is the center frequency of operation and the system's impedance (Z_0) is 50Ω.

Figure 12.27 shows the measured output power/tone and third *intermodulation rejection* (IMR) as a function of input power. The measured insertion loss and isolation at about 2 GHz were better than 2 and 30 dB, respectively. The measured rise/fall times characteristics were similar to those for conventional T/R switches.

12.2.2 Phase Shifters

One of the important elements in a T/R module is the programmable multibit phase shifter. The scanning of the beam in phased-array radars is achieved by changing the phase of the RF signal fed to or received from each radiating element. For beam steering, programmable bidirectional phase shifters are required to adaptively adjust the transceiver phase in both the transmitting and the receiving modes.

The four main types of solid-state digitally controlled phase shifters are switched line, reflection, loaded line, and lowpass/highpass, as shown in Figure 12.28. The first three types can be realized using both distributed and lumped elements, while the lowpass/highpass topology uses only lumped elements. The lowpass/highpass phase shifter configuration is very suitable for narrowband and broadband and compact size applications. Here the digital phase shift is realized by using the phase lag property of the lowpass network and phase lead characteristic of the highpass network, which are connected between two SPDT switches. The small bits are of an embedded-FET type, where the FET's reactances become part of the phase shifting lowpass/highpass networks.

Generally, the digital bits in a multibit phase shifter have binary values; that is, 4-bit and 5-bit phase shifters have 180°, 90°, 45°, 22.5° bits and 180°, 90°, 45°, 22.5°, 11.25° bits, respectively. Several different topologies have been

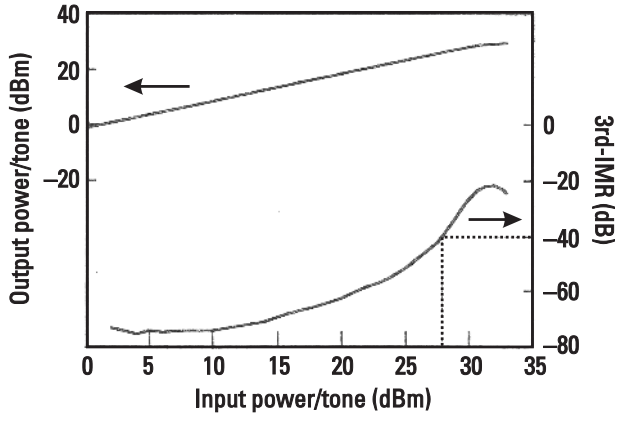


Figure 12.27 Linearity of the improved power-handling capability of an *LC*-resonant T/R switch.

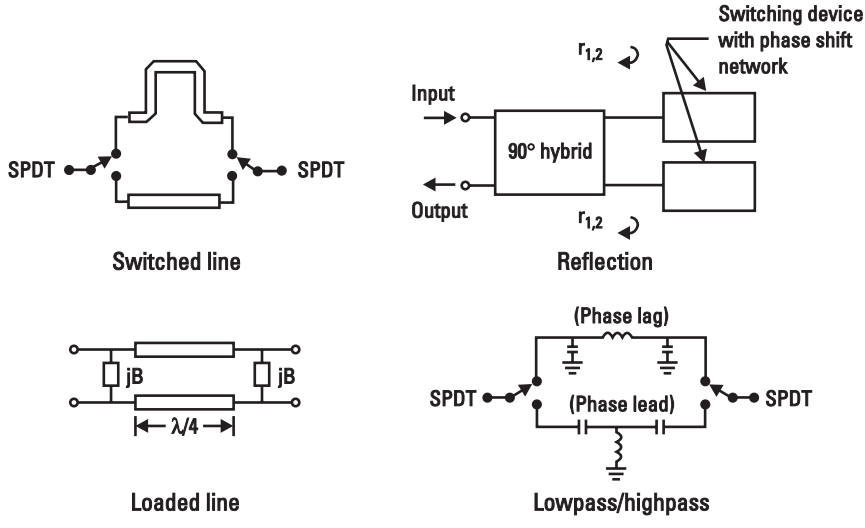


Figure 12.28 Four basic phase shifter configurations.

reported in the literature [47–51]. The 180° bit is commonly designed using a switched lowpass/highpass topology as shown in Figure 12.29(a). The simplest topology for 90° and smaller bits is shown in Figure 12.29(b).

Assuming ideal switches, for 180° bit, the values of L_1, C_1 and L_2, C_2 for a 50-Ω system are calculated from (12.7) and Table 12.2, respectively. These values are

$$L_1 = L_2 = \frac{50}{2\pi f}, \quad C_1 = C_2 = \frac{1}{50 \times 2\pi f} \tag{12.45}$$

The first-order equation for circuit elements for 90° and lower bits can be derived as follows: When FET 1 is in the on state, FET 2 is in the off state, and the value of L_p is selected to parallel resonate out the off-state capacitance of FET 2, the circuit is simplified to a single series on-resistance of FET 1. Thus, in the reference state, the phase shifter has an insertion loss that depends on the FET 1 size and approximately zero insertion phase. On the other hand, when FET 1 is in the off state and FET 2 is in the on state, Figure 12.29(b) is reduced to the equivalent circuit shown in Figure 12.30. Here the total capacitance C_T is given by

$$C_T = C_S + C_{\text{off1}} \tag{12.46}$$

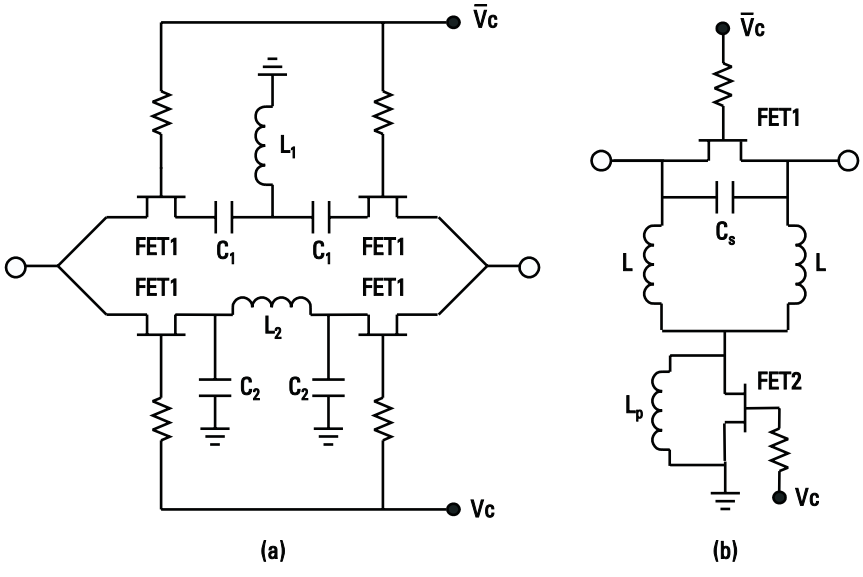


Figure 12.29 Schematics for multibit phase shifters: (a) 180° bit and (b) 90°, 45°, and 22.5° bits.

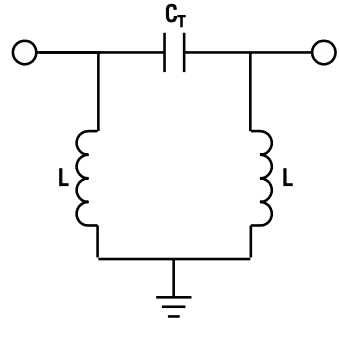


Figure 12.30 Pi *LC* representation.

where C_{off1} is the off-state capacitance of FET 1. When the system impedance is Z_0 and under matched conditions, the values of L and C_T using Table 12.2 can be expressed as follows:

$$L = \frac{Z_0}{\omega}\sqrt{\frac{1+\cos\theta}{1-\cos\theta}} = \frac{Z_0}{\omega\tan(\theta/2)} \tag{12.47}$$

$$C_T = \frac{1}{\omega Z_0 \sin\theta} \tag{12.48}$$

where θ is the insertion phase. Thus, for a given phase shift, the values of C_s and L are determined using (12.46), (12.47), and (12.48).

12.2.3 Digital Attenuator

Digital multibit attenuators offer precise attenuation ranges, good linearity, good thermal stability, and high power-handling capability. The multibit attenuators are realized using a tee attenuator topology in which the switching FETs become an integral part of the attenuator configuration. This results in compact size and low insertion loss. In a 6-bit attenuator, the small, that is, 0.5-, 1-, and 2-dB, bits are generally realized using a topology like that shown in Figure 12.31(a), whereas 4- and 8-dB bits use the topology shown in Figure 12.31(b). The 16-dB bit will basically use two 8-dB bits. The RC network shown in Figure 12.31 is optimized to maintain the attenuator's linearity and a good VSWR. The combination of thin-film resistors, active resistors, and the FETs parasitic resistance are used to set the attenuation value of each bit.

In addition to the tee configuration, pi and bridged-tee topologies, as summarized in Table 12.3, are also used.

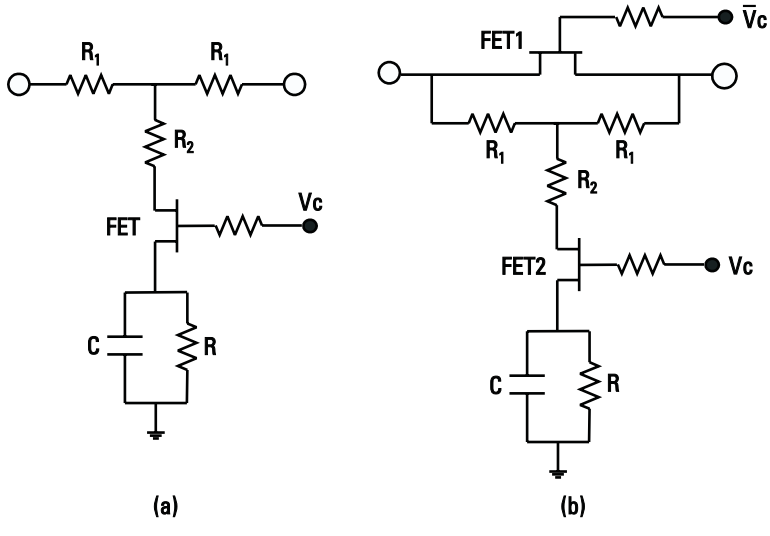
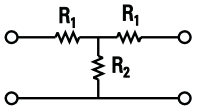
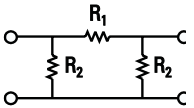
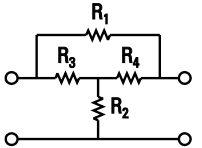


Figure 12.31 Schematic for multibit attenuators: (a) 0.5-, 1-, and 2-dB bits and (b) 4- and 8-dB bits.

Table 12.3
Characteristics of Tee, Pi, and Bridged-tee Attenuators

	Tee		**Pi**		**Bridged-Tee**	
Configuration						
Matching conditions	$Z_0^2 = R_1^2 + 2R_1R_2$		$Z_0^2 = \dfrac{R_2^2}{1 + 2R_2/R_1}$		$R_3 = R_4 = Z_0$ $Z_0^2 = R_1R_2$	
Attenuation at matching	$A = \dfrac{V_0}{V_1} = \dfrac{R_2}{R_1 + R_2 + Z_0}$		$A = \dfrac{V_0}{V_1} = \dfrac{R_2Z_0}{R_1R_2 + Z_0(R_1 + R_2)}$		$A = \dfrac{R_2}{Z_0 + R_2}$ $A = \dfrac{Z_0}{Z_0 + R_1}$	
Attenuation (dB)	R_1 **(Ω)**	R_2 **(Ω)**	R_1 **(Ω)**	R_2 **(Ω)**	R_1 **(Ω)**	R_2 **(Ω)**
0.5	1.4	868	2.9	1,737	3	843
1	2.9	433	5.8	869	6	409
3	8.5	142	17.6	292	20	120
5	14	82	31	179	39	64
10	26	35	71	96	108	23
15	35	18.4	136	72	231	10.8

References

[1] Matthaei, G. L., L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks and Coupling Structures,* New York: McGraw-Hill, 1964.

[2] Skwirzynski, J. K., *Design Theory and Data for Electrical Filters,* London: Van Nostrand, 1965.

[3] Zverev, A. I., *Handbook of Filter Synthesis,* New York: John Wiley, 1967.

[4] Howe, Jr., H., *Stripline Circuit Design,* Dedham, MA: Artech House, 1974.

[5] Rhodes, J. D., *Theory of Electrical Filters,* New York: John Wiley, 1976.

[6] Malherbe, J. A. G., *Microwave Transmission Line Filters,* Dedham, MA: Artech House, 1979.

[7] Bahl, I. J., and P. Bhartia, *Microwave Solid State Circuit Design,* New York: John Wiley, 1988, Chap. 6.

[8] Chang, K., (Ed.), *Handbook of Microwave and Optical Components,* Vol. 1, New York: John Wiley, 1989.

[9] Rhea, R. W., *HF Filter Design and Computer Simulation,* Atlanta, GA: Noble Publishing, 1994.

[10] Hong, J.-S., and M. J. Lancaster, *Microstrip Filters for RF/Microwave Applications,* New York: John Wiley, 2001.

[11] Levy, R., "Design Considerations for Lumped-Element Microwave Filters," *Microwave J.,* Vol. 31, February 1988, pp. 183–192.

[12] Dayal, H., and Q. Le, "Printed Inductors on Alumina Substrates," *IEEE Microwave Magazine,* Vol. 2, June 2001, pp. 78–86.

[13] Barinov, A. E., et al., "Superconducting Lumped-Element Filter with Spiral Inductors," *Microwave Opt. Lett.,* Vol. 29, April 2001, pp. 94–95.

[14] Ong, C. K., et al., "High-Temperature Superconducting Bandpass Spiral Filters," *IEEE Microwave Guided Wave Lett.,* Vol. 9, October 1999, pp. 407–409.

[15] Bhartia, P., and I. J. Bahl, *Millimeter Wave Engineering and Applications,* New York: John Wiley, 1984, Chap. 7.

[16] Levy, R., *Directional Couplers in Advances in Microwaves,* Vol. 1, New York: Academic Press, 1966, pp. 184–191.

[17] Davis, W. A., *Microwave Semiconductor Circuit Design,* New York: Van Nostrand Reinhold, 1983.

[18] Malherbe, J. A. G., *Microwave Transmission Line Couplers,* Norwood, MA: Artech House, 1988.

[19] Uysal, S., *Nonuniform Line Microstrip Directional Couplers and Filters,* Norwood, MA: Artech House, 1993.

[20] Mongia, R., I. Bahl, and P. Bhartia, *RF and Microwave Coupled-Line Circuits,* Norwood, MA: Artech House, 1999.

[21] Hirota, T., A. Minakawa, and M. Muraguchi, "Reduced-Size Branch-Line and Rat-Race Hybrids for Uniplanar MMICs," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-38, March 1990, pp. 270–275.

[22] Coulton, M., et al., "Status of Lumped Elements in Microwave Integrated Circuit—Present and Future," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-19, July 1991, pp. 588–599.

[23] Fusco, V. F., and S. B. D. O'Caireallain, "Lumped Element Hybrid Networks for GaAs MMICs," *Microwave Optical Tech. Lett.,* Vol. 2, January 1989, pp. 19–23.

[24] Lu, L. H., et al., "Design and Implementation of Micromachined Lumped Quadrature (90°) Hybrids," *IEEE MTT-S Int. Microwave Symp. Dig.,* 2001, pp. 1285–1288.

[25] Parisi, S. J., "A Lumped Element Rat Race Coupler," *Applied Microwave,* August/September 1989, pp. 84–93.

[26] Hagerheiden, J., M. Ciminera, and G. Jue, "Improved Planar Spiral Transformer Theory Applied to a Miniature Lumped Element Quadrature Hybrid," *IEEE Trans. Microwave Theory Tech.,* Vol. 45, April 1997, pp. 543–545.

[27] Shibata, K., "Microstrip Spiral Directional Coupler," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-29, July 1981, pp. 680–689.

[28] McWhorter, M., "Broadband RF Transformer Directional Couplers," *RF Design,* July 1991, pp. 59–61.

[29] Ellis, M. G., "RF Directional Couplers," *RF Design,* February 1997, pp. 30–43.

[30] Directional Couplers, Brooklyn, NY: Mini-Circuits.

[31] Wilkinson, E. J., "An N-Way Hybrid Power Divider," *IRE Trans. Microwave Theory Tech.,* Vol. MTT-8, January 1960, pp. 116–118.

[32] Parad, L. I., and R. L. Moynihan, "Split-Tee Power Divider," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-13, January 1965, pp. 91–95.

[33] Kopp, B., "Asymmetric Lumped Element Power Splitters," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1989, pp. 333–336.

[34] Staudinger, J., "Wide Bandwidth MMIC Power Dividers: Implementation and a Practical Design Technique," *Microwave J.,* Vol. 33, February 1990, pp. 73–90.

[35] Chakmanlan, J. S., "Control VSWR Bandwidth in T-Section Networks," *Microwaves,* Vol. 20, July 1981, pp. 87–94.

[36] Abrie, P. D., *Design of RF and Microwave Amplifiers and Oscillators,* Norwood, MA: Artech House, 1999, Chap. 7.

[37] Davis, W. A., and K. K. Agarwal, *Radio Frequency Circuit Design,* New York: John Wiley, 2001.

[38] White, J. F., *Microwave Semiconductor Engineering,* New York: Van Nostrand Reinhold, 1982.

[39] Wolff, E. A., and R. Kaul, *Microwave Engineering and Systems Applications,* New York: John Wiley, 1988, Chap. 12.

[40] Chang, K., (Ed), *Handbook of Microwave and Optical Components,* Vol. 2, New York: John Wiley, 1990, Chaps. 4 and 5.

[41] Chang, K., *Microwave Solid-State Circuits and Applications,* New York: John Wiley, 1997.

[42] Sharma, A. K., "Solid-State Control Devices: State of the Art," *Microwave J.,* September 1989, pp. 95–112.

[43] Chang, K., I. Bahl, and V. Nair, *RF and Microwave Circuit and Component Design for Wireless Systems,* New York: John Wiley, 2002, Chap. 7.

[44] Blackwell, D. A., D. E. Dawson, and D. C. Buck, "X-Band MMIC Switch with 70 dB Isolation and 0.5 dB Insertion Loss," *Microwave J.,* 1995, pp. 97–98.

[45] Imai, N., A. Minakawa, and H. Ozaki, "Novel High-Isolation FET Switches," *IEEE Trans. Microwave Theory Tech.,* Vol. 44, May 1996, pp. 685–691.

[46] Tokumitsu, T., I. Toyoda, and M. Aikawa, "A Low-Voltage, High-Power T/R Switch MMIC Using LC Resonators," *IEEE Trans. Microwave Theory Tech.,* Vol. 43, May 1995, pp. 997–1003.

[47] Ayasli, Y., et al., "Wide-Band Monolithic Phase Shifter," *IEEE Trans. Microwave Theory Tech.,* Vol. 32, December 1984, pp. 1710–1714.

[48] Moye, C., G. Sakamoto, and M. Brand, "A Compact Broadband, Six-Bit MMIC Phasor with Integrated Digital Drivers," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.,* 1990, pp. 123–126.

[49] Krafcsik, D. M., et al., "A Low-Loss X-Band 6-Bit MMIC Phase Shifter Using MESFET Switches," *GOMAC Dig.,* 1991, pp. 355–358.

[50] Wallace, J., H. Redd, and R. Furlow, "Low Cost MMIC DBS Chip Sets for Phased Array Applications," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1999, pp. 677–680.

[51] Campbell, C. F., and S. A. Brown, "A Compact 5-Bit Phase Shifter MMIC for K-Band Satellite Communication Systems," *IEEE Trans. Microwave Theory Tech.,* Vol. 48, December 2000, pp. 2652–2656.

13

Fabrication Technologies

13.1 Introduction

Since the early 1950s, after the invention of planar transmission lines such as striplines and microstrip lines, work on microwave planar printed circuits and lumped elements at microwave frequencies began. As several microwave functions were miniaturized and batch fabricated for large-volume production, this brought about a revolution in the microwave industry. Early work on planar printed circuits served as the seed for the successful introduction of hybrid MICs. Several factors contributed to the success of MIC technology including the availability of good quality-polished alumina substrates, the evolution of cost-effective processes for thin-film metallization and high resolution photoetching, the development of alumina drilling and cutting tools, and the proliferation of good-quality GaAs *metal-semiconductor field-effect transistors* (MESFETs or simply FETs).

MIC technology has steadily improved in the areas of modeling, automatic manufacturing, multilayer production, and cost effectiveness. During the past 30 years, MIC technology has played a key role in the growth of microwave applications. Several MIC manufacturing technologies [1–4] are being used to reduce product size and component count and cost. These include thin- and thick-film hybrids and low- and high-temperature cofired ceramic technologies.

Building on the success of MIC technology, a new microwave GaAs semiconductor based technology, the MMIC, was introduced in the mid-1970s. Unlike MICs, in MMICs all active and passive circuit elements and interconnections are formed together on the surface of a semi-insulating substrate (usually gallium arsenide). MMICs are low cost and provide improved reliability and

reproducibility, small size, low weight, broadband performance, circuit design flexibility, and multifunction performance on a single chip.

During the past 10 years, microwave technology has gone through a significant evolution to meet necessary requirements for lower cost solutions, circuit miniaturization, higher levels of integration, improved reliability, lower power consumption, low-voltage operation, and high-volume applications. Component size and weight are prime factors in the design of electronic systems for satellite communications, *phased-array radar* (PAR), electronic warfare, and other airborne applications. High-volume and low- cost considerations drive the PAR and consumer electronics markets. MMICs are the key to meeting the above requirements.

This chapter describes lumped-element circuit fabrication technologies for RF and microwave applications, including PCBs, *microwave printed circuits* (MPCs), thin films, thick films, cofired ceramics, and MICs. Their salient features such as materials, fabrication and cost are reviewed and compared.

13.1.1 Materials

The basic materials for fabricating printed circuits and MICs, in general, are divided into four categories:

1. *Substrate materials:* sapphire, alumina, beryllia, ferrite/garnet, RT/duroid, FR-4, quartz, silicon, GaAs, InP, and so on;
2. *Conductor materials:* copper, gold, silver, aluminum, and so on;
3. *Dielectric films:* SiO, SiO_2, Si_3N_4, Ta_2O_5, and so on;
4. *Resistive films:* NiCr, Ta, Ti, TaN, WN, cermet, GaAs, and so on.

13.1.1.1 Substrate Materials

The substrate selected for MICs must have the following general characteristics [5–7]:

1. The cost of the substrate must be justifiable for the application.
2. The choice of thickness and permittivity determines the achievable impedance range as well as the usable frequency range.
3. The loss tangent should be low, for negligible dielectric loss.
4. The substrate surface finish should be good (an ~0.05- to 0.1-μm finish), with relative freedom from voids, to minimize conductor loss and maintain good metal–film adhesion.

5. There should be good mechanical strength and thermal conductivity.
6. Minimal deformation should occur during processing of the circuit.
7. A matching CTE with solid-state devices or packaging materials is important if they are attached to such substrates to avoid susceptibility to large temperature variations for improved reliability.

The dielectric constant of the substrate should be high while meeting the other criteria to keep the circuit size small. A variety of substrate materials and their properties are listed in Table 13.1. The data provided here for materials are of a general nature and must be used with care. For accurate data, refer to the manufacturer's data sheets.

Use of a high dielectric constant substrate $\epsilon_r \cong 10$ is highly desirable. However, the substrate thickness is limited by the presence of higher order modes. High-impedance lines on thin substrates require very narrow conductors, which become lossy and the definition of these narrow conductors can be difficult. The temperature dependence of the dielectric constant of substrates (such as rutile) can lead to problems in certain applications, where temperature variations are large.

For low frequencies, up to about 4 to 6 GHz for circuits and up to and beyond 20 GHz for array antennas, plastic substrates ($\epsilon_r \cong 2$–4) are often used. Alumina (Al_2O_3) is one of the most suitable substrate materials for use up to 20 GHz. The grade of the Al_2O_3 used depends on the fabrication technology employed: thin or thick film. Alumina having less than 85% purity has high dielectric loss and poor reproducibility and is normally not used for high-performance circuits. Commonly used alumina for microwave applications has greater than 99% purity. The dielectric constant of alumina may be too high for millimeter-wave circuits because high-impedance lines are difficult to fabricate with required tolerances and are lossy. Quartz with a dielectric constant of 4 is more suitable and widely used for high-frequency (>20-GHz) microwave and millimeter-wave integrated circuits.

Beryllia and aluminum nitride (AlN) have excellent thermal conductivity and are suitable for power applications in which heat dissipation from active devices mounted on the substrate is large and a low thermal resistance is required. GaAs is one of the most suitable substrates for MMICs, because most of the active devices, such as low-noise MESFETs, power MESFETs, and Schottky diodes, are fabricated on GaAs substrates, and the material has semi-insulating properties.

13.1.1.2 Conductor Materials

Conductor materials used for MICs should have high conductivity, a low-temperature coefficient of resistance, low RF resistance, good adhesion to the substrate, good etchability and solderability, and be easy to deposit or electroplate

Table 13.1
Properties of Substrates for MICs

Material	Surface Roughness (μm)	Loss Tangent (tan δ) at 10 GHz (10^{-4})	Relative Dielectric Constant (ϵ_r)	Thermal Conductivity (W/cm-°C)	Dielectric Strength (kV/cm)	MIC Applications
Alumina 99.5%	2–8	1–2	10	0.37	4×10^3	Microstrip, suspended substrate, lumped element
96%	20	6	9	0.28	4×10^3	
85%	50	15	8	0.2	4×10^3	
Sapphire	1	1	9.3–11.7	0.4	4×10^3	Microstrip, lumped element
AlN	1–2	5	8.8	2.3	—	Compound substrate, package
Glass	1	20	5	0.01	—	Lumped element
Beryllia (BeO)	2–50	1	6.6	2.5	—	Compound substrate, package
Rutile	10–100	4	100	0.02	—	Microstrip
Ferrite/garnet	10	2	13–16	0.03	4×10^3	Microstrip, coplanar
GaAs (high resistivity)	1	6	12.9	0.46	350	High-frequency, microstrip, MMIC
Si (high resistivity)	1	10–100	11.7	1.45	300	MMICs
Quartz	1	1	3.8	0.01	10×10^3	Microstrip, high frequency
Polyolefin	1	1	2.3	0.001	~300	
InP	—	—	14	0.68	—	MMICs

[5, 7]. The resistance is determined by the RF surface resistivity and skin depth, and thus the skin depth determines the thickness required. The conductor thickness should be at least three to four times the skin depth, to include 98% of the maximum possible current density within the conductor.

Table 13.2 shows the properties of some widely used conductor materials for MICs. These materials have good conductivity and can be deposited by a number of methods. Some conductors have good electrical conductivity but poor substrate adhesion, whereas others have poor electrical conductivity and good substrate adhesion. To obtain good adhesion with high-conductivity materials, a very thin layer (100–500Å) of a poor conductor is deposited between the substrate and the good conductor. Some examples of typical conductor combinations to obtain good adhesion and good conductivity are Cr/Au, Pd/Au,

Table 13.2
Properties of Conductors for MICs

Material	Surface Resistivity (Ω/square $\times 10^{-7}\sqrt{f}$	Skin Depth δ at 2 GHz (μm)	Coefficient of Thermal Expansion (α_t/°C $\times 10^6$)	Adherence to Dielectrics	Deposition Technique
Ag	2.5	1.4	21	Poor	Evaporation
Cu	2.6	1.5	18	Poor	Evaporation plating
Au	3.0	1.7	15	Poor	Evaporation plating
Al	3.3	1.9	26	Poor	Evaporation
Cr	4.7	2.7	9.0	Good	Evaporation
Ta	7.2	4.0	6.6	Good	Electron-beam sputtering
Ti	—	—	—	Good	Evaporation sputtering
Mo	4.7	2.7	6	Fair	Electron-beam sputtering evaporation
W	4.7	2.6	4.6	Fair	Sputtering, vapor phase, electron-beam, evaporation
Pt	—	3.6	9	—	Sputtering, electron beam
Pd	—	3.6	11	—	Evaporation, sputtering, electroplating

and Ta/Au for hybrid MICs, and Cr/Au and Ti/Au for MMICs. The selection of the conductors is determined by compatibility with other materials required in the circuit and the process required. A typical adhesion layer may have a surface resistivity ranging from 500 to 1,000 Ω/square, but does not contribute to any loss because of its extremely small thickness.

13.1.1.3 Dielectric Materials

Dielectric films in MICs are used as insulators for capacitors, protective layers for active devices, and insulating layers for passive circuits. The desirable properties of these dielectric materials are reproducibility, high-breakdown field, low-loss tangent, and the ability to undergo processing without developing pinholes [7]. Table 13.3 shows some of the properties of commonly used dielectric films in MICs. SiO is not very stable and can be used in noncritical applications, such as bypass and dc blocking capacitors. A quality factor Q of more than 100 can be obtained for capacitors using SiO_2, Si_3N_4, and Ta_2O_5 materials. These materials can be deposited by sputtering or plasma-enhanced *chemical vapor deposition* (CVD). For high-power applications, a breakdown voltage in excess of 200V is required. Such capacitors can be obtained with fairly thick dielectric films (~1 μm) that have a low probability of pinholes.

13.1.1.4 Resistive Films

Resistive films in MICs are required for fabricating resistors for terminations and attenuators and for bias networks. The properties required for a resistive material are: good stability, a low TCR, and sheet resistance in the range of 10 to 2,000 Ω/square [7, 8]. Table 13.4 lists some of the thin-film resistive materials used in MICs. Evaporated nichrome and tantalum nitride are the most commonly used materials.

Table 13.3
Properties of Dielectric Films for MICs

Material	Method of Deposition	Relative Dielectric Constant (ϵ_r)	Dielectric Strength (V/cm)	Microwave Q
SiO	Evaporation	6–8	4×10^5	30
SiO	Deposition	4	10^7	100–1,000
Si_3N_4	Vapor-phase sputtering	7.6	10^7	
Al_2O_3	Anodization evaporation	7–10	4×10^6	
Ta_2O_5	Anodization evaporation	22–25	6×10^6	100

Table 13.4
Properties of Resistive Films for MMICs

Material	Method of Deposition	Resistivity (Ω/square)	TCR (%/°C)	Stability
Cr	Evaporation	10–1,000	–0.100 to +0.10	Poor
NiCr	Evaporation	40–400	+0.001 to +0.10	Good
Ta	Sputtering	5–100	–0.010 to +0.01	Excellent
Cr-SiO	Evaporation or cement	Up to 600	–0.005 to –0.02	Fair
Ti	Evaporation	5–2,000	–0.100 to +0.10	Fair
TaN	Sputtering	50–300	–0.01 to –0.02	Excellent

13.1.2 Mask Layouts

Any MIC design starts with a schematic diagram for the circuit. After the circuit is finalized, an approximate layout is drawn. The next step is to obtain an accurate mask layout for producing a single mask layer for hybrid MICs or a set of masks for miniature MICs and MMICs. Finally, hybrid MIC substrates are etched using these masks for the required pattern, and for miniature and monolithic MICs, various photolithographic steps are carried out using a set of masks.

For MICs the layout is carefully prepared keeping in mind the chip or packaged devices (active and passive), crosstalk considerations, microstrip and layout discontinuities, and tuning capability. Several techniques have been used to produce accurate layouts for MICs. In addition to manually prepared printed circuit taping and rubylith methods [9, 10], digitally controlled methods are being used. Both microwave CAD interactive and stand-alone IC layout tools are used to translate the circuit descriptions into mask layouts (single layer for hybrid MICs or multilayer for LTCC/MMICs). The output is in the form of a coordinate printout, pen plot of the circuit, and the complete circuit that can be given to a mask manufacturer on a magnetic tape.

13.1.3 Mask Fabrication

Optical masks are usually used for both hybrid MICs and MMICs. However, in MMICs, new lithography techniques (considered very important for good process yield and fast turnaround) are headed in the direction of beam writing, including electron beam, focused ion beam, and laser beam. However, except for a small percentage of direct writing on the wafers (only critical geometries), optical masks are widely used. These masks are usually generated using optical techniques or electron-beam lithography.

Masks consist of sheets of glass or quartz (also called blanks) with the desired pattern defined on them in thin-film materials such as photoemulsion (silver halide based), chromium, or iron oxide. Emulsion mask coatings are still the most widely used for hybrid MICs and for noncritical working plates. Silver-halide-based emulsions have numerous advantages such as low cost, high photosensitivity, good image resolution and contrast, and reversal processing. Their major disadvantages are scratch sensitivity and higher image defect density. Polished chrome is the most popular hard-surface coating for glass blanks and has been proven successful for high-resolution work when used with positive optical photoresists. The main difficulty with chromium is its high reflectivity, which is solved by using an antireflection layer of chromium oxide. Iron oxide is another hard-surface coating material that has very low reflectivity and is used commonly to make *see-through* masks. Iron oxide is transparent at longer wavelengths, allowing the operator to "see through" the entire mask when aligning it to the pattern on the wafer. Shorter wavelength light, at which the photoresist is sensitive and the iron oxide mask is opaque, is then used to make the exposure.

Many different processes are available for transferring digital pattern data onto mask plates [11]. The magnetic tape on which the pattern data are stored is loaded into the console, and a light-field emulsion reticle, typically at 10×, is obtained through computer control of the exposure shapes and placement. This reticle is then contact printed to yield a dark-field emulsion reticle. The next step is to make a 10× reticle on a hard-surface blank and step-and-repeat it into 1× emulsion master masks for the complete die. Finally, these emulsion masters are contact printed to make hard-surface working plates.

13.2 Printed Circuit Boards

PCBs [12, 13] or *printed wiring boards* (PWBs) are used extensively for electronic packaging and RF front-end circuit boards. In these applications, the primary function of PCBs is to provide mechanical support and multilevel electrical interconnections for packaged solid-state devices, resistors, capacitors, and inductors. For RF/microwave applications, there is a need for high-performance, low-cost PCB materials that can provide low-loss finer lines (≅5 mil wide) and narrower spacings (≅5 mil) for high-density circuits and also provide limited impedance-matching capability. Also, high-speed data processing by means of digital circuits requires higher performance, low dielectric constant PCB materials. All of these materials have low-loss copper conductors capable of carrying high current densities. The PCB can be single sided, double sided, or consist of multilayer substrates. Multilayer PCBs have two or more layers of dielectric and metallization layers, with the latter being interconnected by plated-through via holes. Substrates may be rigid or flexible.

Substrate manufacturers have tried to combine the characteristics of various basic materials to obtain desired electrical and mechanical properties. The resulting material is called a *composite.* By adding fiberglass, quartz, or ceramic in suitable proportions to organic or synthetic materials, the mechanical properties are modified and the dielectric constant value is adjusted. A very wide variety of products are now available with a dielectric constant range of 2.1 to 10 and tan δ values from 0.0004 to 0.01. Table 13.5 shows important electrical and thermal parameters of several PCB materials currently in use. The FR-4 (fire retardant) is an epoxy-based glass substrate that is widely used and has the lowest cost, whereas *polytetrafluoroethylene* (PTFE) gives the highest performance and can be operated above 300°C. FR-4, BT/epoxy, and polyimide, called *thermoset materials,* are hard and elastic. These materials become soft above their glass transition temperature (T_g). The glass transition temperatures of FR-4, BT/epoxy, and polyimide are about 150°, 210°, and 250°C, respectively. Materials such as PTFE/glass, known as thermoplastics, become soft and melt if heated. The melting temperature (T_m) of PTFE/glass is about 325°C.

The CTE as given for several materials in Table 13.5 is a measure of the dimensional stability with temperature. The thermal conductivity of these materials is quite poor, and their typical value is about 0.2 W/m-°C. Glass-reinforced epoxy laminates offer the lowest cost, but PTFE-based laminates have the lowest dielectric constant and loss. PTFE substrates also provide better protection from moisture and offer ultrahigh adhesion strengths. The high-loss tangent of FR-4 and relatively variable ϵ_r limits its usage to applications below 3 GHz. The values of parameters of composite materials vary slightly from manufacturer to manufacturer.

Table 13.5
Electrical Properties and Thermal Expansion Characteristics of a Wide Range of Dielectric Materials

Material	Dielectric Constant	Dissipation Loss	CTE *x/y* ppm/°C	CTE *z* ppm/°C
FR4/glass	4.5	0.03	16–20	50–70
Driclad/glass	4.1	0.01	16–18	55–65
BT/epoxy/glass	4.0	0.01	17	55–65
Epoxy/PPO/glass	3.9	0.01	12–18	150–170
Cyanate ester/glass	3.5	0.01	16–20	50–60
Polyimide/glass	4.5	0.02	12–16	65–75
Ceramic fill thermoset	3.3	0.0025	15	50
EPTFE w/thermoset	2.8	0.004	50–70	50–70
Silica-filled PTFE	2.9	0.003	16	24–30
PTFE/glass	2.4	0.001	12–20	140–280
PTFE	2.1	0.0004	70–90	70–90

13.2.1 PCB Fabrication

Salient steps in the fabrication of PCBs are shown in Figure 13.1. In a basic multilayer PCB fabrication process, first a copper foil is laminated to the dielectric sheets and the required interconnect/wiring patterns are etched on all substrates by using a photolithographic technique. The substrates are then stacked and laminated under heat and pressure to make a monolithic board. Next, via holes are drilled in the board and catalyzed to make interlayer metallic connections, and the whole board is plated with electroless copper. This increases the thickness of the surface conductor pattern and provides the copper layer in the via holes. The board is then tinned for soldering or nickel or gold plated for gold wire bonding. Finally, the board is cut into required small sizes.

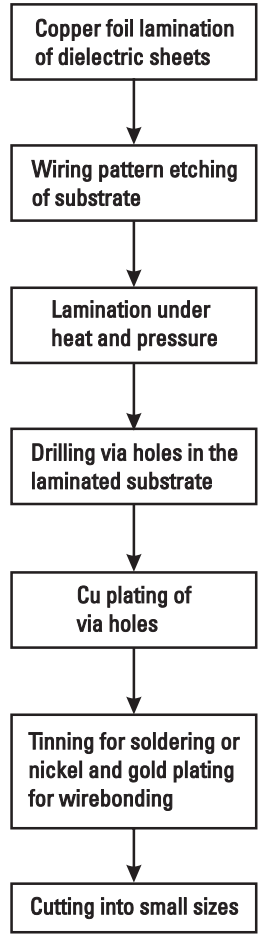


Figure 13.1 Flow diagram for the multilayer PCB process.

The RF prototyping PCB is generally made from multilayer FR-4. The top dielectric layer is 10 mil thick. The top metal layer is made from 1 oz Cu (1.4 mil thick). The ground plane is made from 2 oz Cu (2.8 mil). The 10-mil thickness between the RF layer and the ground layer sets the width of a 50Ω microstrip line to 17.5 mils. The total board thickness is set to 62 mil to make it compatible with standard RF connectors. The PCB (62 mil thick) is very rigid and capable of withstanding bench top tuning.

13.2.2 PCB Inductors

Multilayer PCB technology is quite suitable for realizing the high inductances suitable for applications up to 1 to 2 GHz. These inductors (50–200 nH) can carry currents up to 3 to 5A and can have Q values in the range of 100 for applications up to 100 to 200 MHz.

13.3 Microwave Printed Circuits

Microwave printed circuit (MPC) technology is widely used for microwave passive circuits and printed antennas. Substrate choice and evaluation are essential parts of the design procedure. Many substrate properties may be involved in these considerations: dielectric constant and loss tangent and their variation with temperature and frequency, homogeneity, isotropicity, CTE and temperature range, dimensional stability with processing, temperature, humidity and aging, and thickness uniformity of the substrate are all important. Similarly, other physical properties, such as resistance to chemicals, tensile and structural strengths, flexibility, machinability, impact resistance, strain relief, formability, bondability, and substrate characteristics when clad, are important in fabrication.

The principal microstrip substrates currently used are listed in Table 13.6. Most types are available from several manufacturers. The large range of PTFE, hydrocarbon, and polyester composite substrates available permits considerable flexibility in the choice of a substrate for particular applications. There is no one ideal substrate and the choice depends on the application. For instance, conformal MPCs require flexible substrates, whereas low-frequency applications require high dielectric constants to keep the size small. In terms of high-power operation, moisture absorption, processibility, and cost, substrates such as hydrocarbon and PTFE ceramic, PTFE glass, polyester glass and hydrocarbon, and polyester glass, respectively, are more suitable.

A wide range of substrate materials is available, clad with copper, aluminum, or gold. Most of these substrates use 0.5- to 2-oz electrodeposited or rolled copper. Laminates are usually available in 1/32-, 1/16-, or 1/8-inch thicknesses and, more recently, in 10-, 25-, 50-, 75-, and 100-mil thicknesses

Table 13.6
Dielectric Properties of MPC Substrate Materials at Room Temperature

Material	Trade Name	Supplier	ϵ_r	tan δ	TC of ϵ_r	k (W/m-K)	Density (g/cm^3)	CTE x/y	CTE z	T_g (°C)
Hydrocarbon glass	RO4003	Rogers	3.38	0.0025	+40	0.64	1.8	13	46	280
Hydrocarbon glass	RO4350	Rogers	3.48	0.0040	+50	0.62	1.9	15	50	280
PTFE ceramic	RO3003	Rogers	3.0	0.0013	13	0.50	2.1	17	24	325
PTEE ceramic	RO3006	Rogers	6.15	0.0025	–169	0.61	2.6	17	24	325
PTFE ceramic	RO3010	Rogers	10.2	0.0035	–295	0.66	3.0	17	24	325
PTFE glass fiber	5880	Rogers	2.2	0.0009	–125	0.2	2.2	40	237	—
PTFE glass	TLC-32	Taconic	3.2	0.0030	–125	—	—	10	70	325
PTFE glass	AR320	Arlon	3.2	0.0030	–125	—	—	10	71	325
Thermoset ceramic glass	25N	Arlon	3.25	0.0024	0	—	—	17	70	100
Polyester glass	GML1000	Glasteel	3.05	0.0040	—	—	—	40	60	140

Note: Units of TC and CTE are ppm/°C.

or thicknesses in increments of 5 mil. The cladding material is usually designated in terms of weight per square yard, such as 14g (1/2 oz), 28g (1 oz), 57g (2 oz), and so on. Typical cladding thicknesses for these ounce designations are given in Table 13.7. Low cladding thicknesses simplify fabrication of the MPCs to required tolerances, whereas thicker claddings ease soldering. For high-power applications, a thick cladding is desirable. These substrates are easily machined, and through-holes are made by punching or drilling.

During the past decade, the explosive growth in wireless RF and microwave applications has generated a significant market for lightweight, compact, and low-cost passive components such as couplers, filters, and baluns. These components must be manufactured without tuning and so forth. It is well known that the wavelength of a signal is inversely proportional to the square root of the dielectric constant of the medium in which it propagates. Hence, increasing the dielectric constant of the medium by a factor of 100 will reduce the circuit dimensions by a factor of 10. This simple concept is being exploited extensively as distributed circuit technology is being adopted at S-band and below for cellular telephony, GPS receivers, and mobile SATCOM.

A number of very high dielectric constant ceramic substrates with ϵ_r = 20 to 95, very low dielectric loss (Q factor = 5,000 to 20,000), and high temperature stability (3 ppm/°C) are currently available. They are composed of solid solutions of various titanates and are relatively inexpensive. A list of such materials with their properties is given in Table 13.8.

13.3.1 MPC Fabrication

MPCs are fabricated like conventional PCBs using a photoetching process. Figure 13.2 shows a flow diagram for MPC fabrication. The first step is to generate the artwork from the design. The enlarged artwork is then photo reduced using a highly precise camera to produce a high-resolution negative (also known as a mask) that is used for exposing the photoresist, which is spin coated on the substrate. The laminate/substrate is properly cleaned in accordance with the manufacturer's recommended procedure to ensure proper adhesion to the photoresist, which is applied to both sides of the substrate. The mask is placed on the substrate and held using a vacuum frame or other technique to

Table 13.7
Standard Copper Foil Weights and Foil Thickness (t)

Foil weight	g	14	28	57	142
	oz	0.5	1	2	4
Foil thickness	mm	0.01778	0.03556	0.07112	0.14224
	in	0.0007	0.0014	0.0028	0.0056

Table 13.8
Dielectric Properties of High-K Ceramic Materials at Room Temperature [14]

Ceramic	Dielectric Constant (1 GHz)	Dielectric Loss (1 GHz) ($\times 10^{-4}$)	Thermal Coefficient of ϵ_r (ppm/°C)	Thermal Coefficient of Expansion (ppm/°C)
TiO_2	86	2.0	–800	7–9 (rutile)
$SrTiO_3$	232	1.0	–3,000	9.4
$CaTiO_3$	165	2.4	–1,300	14
$BaTiO_3$	800	3.0	Almost flat, nonlinear	17
$BaNdTiO_3$	92	1.0	–20 (<25°C), 20 (>25°C)	9.0

ensure the fine-line resolution required. With exposure to the proper wavelength light, a polymerization of the exposed photoresist occurs, making it insoluble in the developer solution. The backside of the substrate is exposed completely without a mask, since the copper foil is retained to act as a ground plane. The substrate is developed to remove the soluble photoresist material. Visual inspection is used to ensure proper development.

When these steps have been completed, the substrate is ready for etching. This is a critical step and requires considerable care so that proper etch rates are achieved. After etching, the excess photoresist is removed using a stripping solution. Visual and optical inspections should be carried out to ensure quality and conformance with dimensional tolerances. The substrate is rinsed in water and dried.

If desired, a thermal bonding can be applied by placing a bonding film between the laminates to be bonded. Dowel pins can be used for alignment and the assembly is then heated under pressure until the melting point temperature of the bonding film is reached. The assembly is allowed to cool under pressure below the melting point of the bonding film and then removed for inspection.

The preceding procedure outlines the general steps necessary in producing a microstrip printed circuit. The substances used for the various processes, for example, cleaning and etching, or the tools used for machining and so on depend on the substrate chosen. Most manufacturers provide informative brochures on the appropriate choice of chemicals, cleaners, etchants, and other processing techniques for their substrates.

13.3.2 MPC Applications

MPC technology is exclusively applied to a wide variety of microwave passive components including manifolds for power distribution, filters, couplers, baluns,

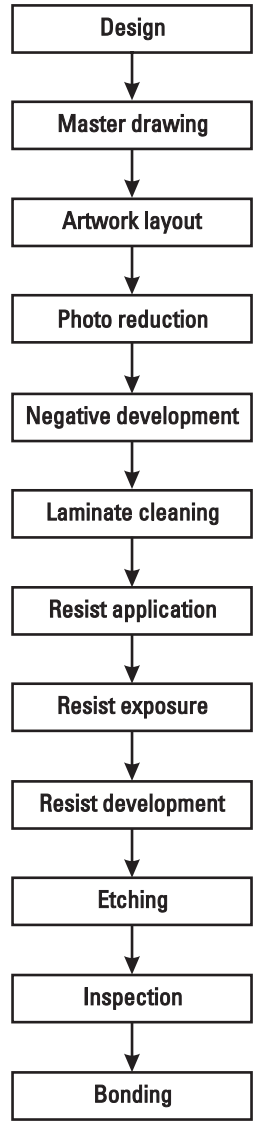


Figure 13.2 Flow diagram for MPCs.

and printed antennas. Both stripline and microstrip lines are used. Among MPC components, directional couplers and filters are the most popular. At RF frequencies, these components are realized using lumped inductors and capacitors. The inductors are printed on the MPC substrate and the discrete chip capacitors are wire bonded or soldered to inductor pads. Figure 13.3 shows a lowpass filter configuration.

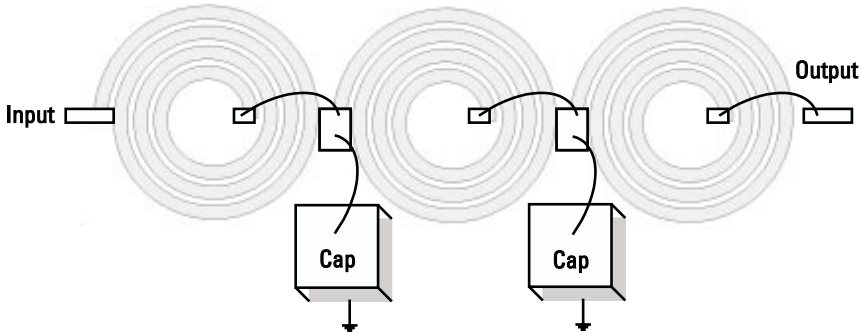


Figure 13.3 Lumped-element lowpass filter configuration.

13.4 Hybrid Integrated Circuits

Hybrid MICs have been used almost exclusively in the frequency range of 1 to 20 GHz for wireless, space, and military applications because they meet the requirements for shock, temperature conditions, and severe vibration. This section is intended to provide a brief introduction to several hybrid technologies such as thin film, thick film, and cofired ceramic. The most commonly used ceramic for MICs is alumina (Al_2O_3). A number of other ceramic materials are available, with ϵ_r ranging between 10 and 150. High dielectric constant materials are useful for circuit size reduction at RF and low microwave frequencies. Hybrid integrated technologies are used exclusively to manufacture discrete lumped inductors, capacitors, and resistors as well as lumped-element-based passive components. The lumped elements are realized by using multilevel sputtering of different materials.

13.4.1 Thin-Film MICs

Thin-film fabrication technology used for MICs is continuously developing to meet the requirements of increasing frequency of operation, higher yield, and reduced costs. This can be achieved by a thin-film manufacturing process that is carefully controlled and repeatable in a clean room environment. The first step in the fabrication process is the deposition of a first layer (seed layer) of metal film on the substrate. The selection of the film is made based on the criteria of good adhesion to the substrate and is one of the important factors in selection of a conductor material for the first layer of metal film. Some precautions specific to MIC conductors should be mentioned with regard to the deposition techniques. At RF frequencies the electromagnetic fields are confined to several skin depths of the conductors. To achieve low loss, the layer of high-resistivity materials such as the chromium used for adhesion must be

extremely thin. The main conductor must have a low bulk dc resistivity for low-loss propagation. Improper processing techniques can result in high RF loss for a low sheet resistance material made of thin chromium and a thicker gold structure. In particular, as a result of the very high substrate temperatures (>300°C) sometimes encountered during sputtering, this thin sputtered chromium layer will diffuse into an overlaying gold film. This results in a high RF loss, even though the sheet resistance may be low with a thick gold layer. Therefore, techniques such as sputtering must be used with care when creating MIC materials. Metal films are deposited on substrates by three methods: vacuum evaporation, electron-beam evaporation, and sputtering.

A typical metal combination for alumina substrate is Cr/Cu/Au or NiCr/Ni/Au. A very thin seed layer of suitable metal is deposited on the substrate by one of the preceding techniques and then the bulk conductor metal is deposited by electroplating techniques. The seed layers of metal provide mechanical and electrical foundation layers on which to electroplate a good-quality bulk conductor metal. The circuit definition can be accomplished by a plate-through technique or by an etchback technique. The techniques that are used to define patterns in metal layers can influence the deposition choice. Figure 13.4 illustrates the two fabrication techniques.

The plate-through technique begins with a substrate coated with a thin layer of evaporated metal. This is followed by an application of a thick photoresist,

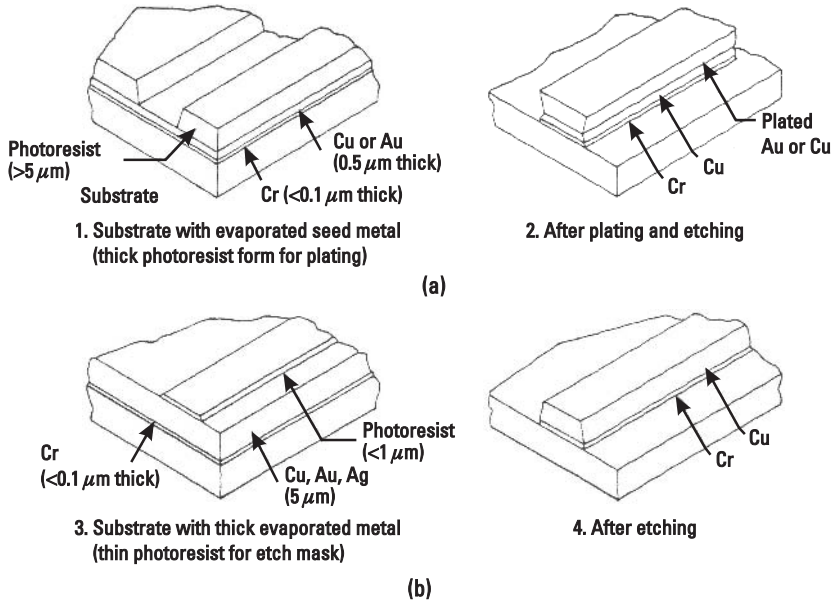


Figure 13.4 Techniques for defining conductor pattern in hybrid MICs: (a) fabrication by plating and etching and (b) fabrication by etching thin plated metal.

as shown in Figure 13.4(a). The thickness of this photoresist is similar to the thickness of the final metal film required. After defining a pattern in the photoresist, the second metal layer is plated up to the desired thickness with precise definition and only in the areas where metal is required. The photoresist layer is then washed away and the thick seed-metal is etched with very little undercut from the undesired areas. This technique is also suitable for fabricating lines that are 25 to 50 μm wide or for use when the separation between them is 25 to 50 μm.

The second technique is the etchback technique. This technique, as illustrated in Figure 13.4(b), utilizes a thick metal layer obtained either completely by evaporation or by a combination of a thin evaporated layer and a thicker plated layer. A thin photoresist layer is used as a mask to define the circuit pattern. The undesired areas of metal are then removed by etching. This technique results in undercutting the metal film by about twice the line conductor thickness. The plate-through technique not only permits better definition for thick conductors, but also saves on cost in that only the required material is deposited.

Traditionally, single-layer discrete capacitors are manufactured by firing ceramic substrates that typically have a 5-mil thickness [15]. Then both sides are metallized using a thin- or thick-film process. Finally, the substrate is sawed into chip capacitors. Thin-film resistors are realized by depositing nichrome or tantalum nitride films on alumina substrates similar to the process described for conductor films. A laser trimming technique is used to achieve ±1% tolerances in the resistor values. Termination or connecting pads are of metallized chromium-gold. For high-power resistors, substrates used are BeO and AlN. Finally, the substrate is sawed into chip resistors.

In the early 1980s, a thin-film technology variant was introduced called a *miniature hybrid* [16]. Miniature hybrid MIC technology is based on thin-film technology in which the multilevel passive circuits including lumped resistors and capacitors are batch fabricated on the substrate and solid-state devices are externally attached to these circuits. The advantages of this circuit technology are small size, lightweight, excellent heat dissipation, and broadband performance.

13.4.2 Thick-Film Technology

Thick-film MICs are manufactured using various inks pressed through patterned silk screens. Thick-film MICs are inexpensive and are generally limited to the lower end of the microwave spectrum. In conventional thick-film technology, the multilayer interconnects are formed by successive screen printing of conductors, dielectric layers, and resistor patterns on a base substrate. The materials are in the form of inks or pastes. After screen printing, each layer is dried at about 150°C for 15 minutes and fired at about 850°C for 30 to 60 minutes. Figure 13.5 shows the first-layer screen printing process using a paste through a mesh.

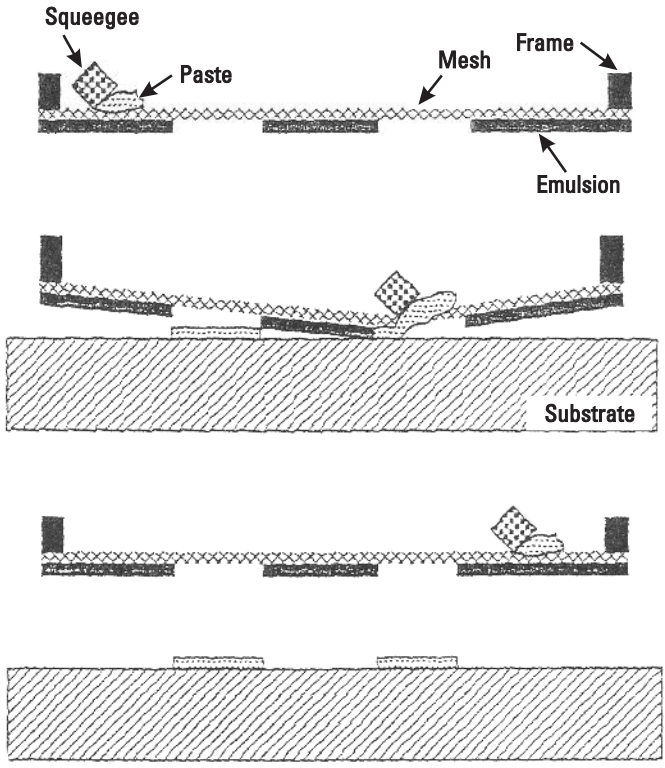


Figure 13.5 Screen printing process for material deposition onto a substrate.

The mesh is designed according to the pattern to be made. The printing, drying, and firing steps are repeated to fabricate the multilayer circuitry in a fully automated way to produce high-volume, cost-effective components.

The commonly used base substrate materials are alumina (Al_2O_3), beryllia (BeO), and aluminum nitride (AlN). The dielectric pastes are typically glass-ceramic compositions having low dielectric constant and loss tangent, high-breakdown voltage, and a CTE matched to the substrate material. The conductors may be gold, copper, silver, palladium-silver/gold, and platinum-silver/gold. Properties of various conductor materials are given in Table 13.2. The commonly used resistor material is ruthenium doped glass (RuO_2).

Recently this technology has been improved by using a photoimageable thick-film process that is capable of producing 1-mil lines and gaps and 3-mil vias [17]. In this process, both Cu and Au conductors up to 10 layers can be used. Earlier, thick-film technology was used to interconnect discrete components; however, improved technology is also capable of printing conductor patterns for low-loss passive circuits at RF and low microwave frequencies.

13.4.3 Cofired Ceramic and Glass-Ceramic Technology

Around the time of the introduction of hybrid miniature MICs, the thick-film variant known as LTCC was also introduced [18]. The LTCC manufacturing process is similar to the thick-film process except that it does not use a base substrate. Dielectric layers are in the form of unfired ceramic tapes (also called green tapes) instead of paste. This technology also enables the printing of reliable capacitors and resistors. The process as shown in Figure 13.6 consists of blanking,

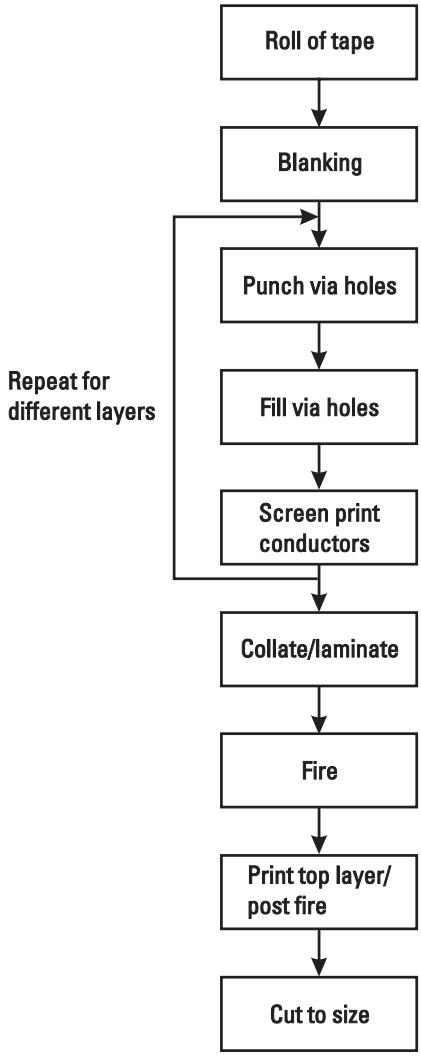


Figure 13.6 Basic steps for the cofired ceramic and cofired glass-ceramic process.

punching vias, conductor screen printing, collating, laminating, and firing. The vias are punched in the green tape and filled with conducting paste. At the same time, conductor patterns are screen printed.

This process is carried over for each dielectric layer and finally the composite structure is fired to obtain a monolithic substrate. The firing temperature for glass-ceramic substrates is 850°C to 900°C and this technology is known as low-temperature cofired ceramic technology. Low-temperature firing allows one to use high-conductivity metals such as Ag, Cu, and gold. The dielectric tapes use a glass-ceramic composite optimized for a better CTE match with the base metal and the semiconductor chips. As many as 50 layers can be combined in a single LTCC substrate measuring 6 × 6 inches. When ceramic tapes are used they are fired at 1,500°C to 1,600°C and the technology is known as *high-temperature cofired ceramic* (HTCC) technology. Commonly used conductors in this case are tungsten (W) and molybdenum (Mo). The dielectric properties of cofired glass-ceramic are compared with cofired alumina ceramic, alumina, BeO, and AlN in Table 13.9.

LTCC technology, due to its multilayer process, offers several advantages over conventional thin-film, thick-film, and HTCC technologies. These advantages include a higher level of integration of components, for example, capacitors, resistors, inductors, inductor transformers, transmission lines, and bias lines; and greater design flexibility by enabling the realization of different types of transmission-line media such as microstrip, stripline, coplanar waveguide, and rectangular coax. Passive components, matching networks, bias lines, and shielding of RF lines can be combined in LTCC technology using several available ceramic and metal layers. Finally, solid-state, low-power devices are attached on the top surface to realize active or passive circuits. High-power devices can be integrated with LTCC by attaching the devices directly to the next level assembly chassis through via holes fabricated in the LTCC MIC.

Table 13.9
Typical Electrical and Thermal Properties of Ceramic Materials

Property	Al_2O_3	HTCC	LTCC	BeO	AlN
Relative dielectric constant at 1 MHz	9.8	9.5	5.0	6.4	8.8
Loss tangent at 1 MHz	0.0002	0.0004	0.0002	0.0003	<0.001
Coefficient of thermal expansion, 10^{-6}/°C	6.5	7.1	3.0	7.2	4.4
Thermal conductivity, W/m-°C	37	25	2	250	230
Dielectric strength, kV/m	25	23	1.5	26	14
Density, g/cm^3	3.8	3.9	2.6	2.8	3.3

The conductors for inductors, transformers, capacitors, interconnects, and other passive components are screen-printed using conductive pastes of gold or silver or copper. Their sheet resistances, measured in milliohms per square, are in the range of 4–10, 2–8, and 3–4, respectively. A paste of glass frit and conductive powder is used to screen print thick-film resistors. The ratio of glass frit content to conductive powder is adjusted to vary the sheet resistance from about 5 Ω/square to 10 MΩ/square. The surface resistors are trimmed to achieve ±1% tolerances in the resistor values, while for buried resistors the tolerance is generally ±25%. The materials for MIM capacitors are available in both paste and tape forms. The dielectric constant value varies from 5 to 200. The capacitance range and dissipation factor for low dielectric constant materials (ϵ_r = 5–10) are 1 to 200 pF and <0.3%, while for high-K materials (ϵ_r = 100–200) these values are 10 to 3,000 and <2%, respectively. The breakdown voltage and capacitance tolerance are 500V and ±10% for low-K materials, and 200V and ±20%, respectively, for high-K materials [19].

Figure 13.7 shows a three-dimensional view of a LTCC module with embedded passive components and bias lines. Wire bonding of a solid-state device and surface mounting of a bypass capacitor are also shown.

MIC technology is very diverse in its application of materials and processes and can be used to implement a broad array of functions. Table 13.10 lists some of these materials and processes.

13.5 GaAs MICs

Whereas most MMICs currently in production operate in the 0.5- to 30-GHz microwave range, an increasing number of applications are covering the millimeter-wave spectrum from 30 to 300 GHz. Monolithic technology is particularly beneficial to millimeter-wave applications through the elimination of parasitic

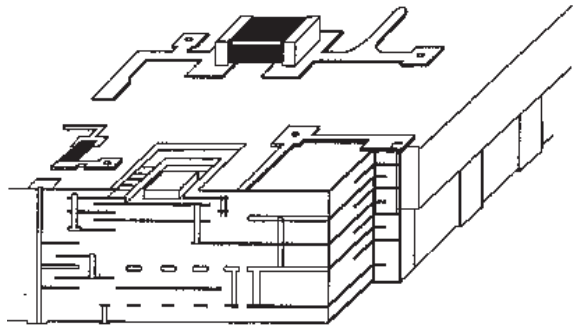


Figure 13.7 3-D view of the LTCC module.

Table 13.10
Summary of Typical Materials and Processes Used to Fabricate MICs

Materials/ Processes	MPC	Thin Film	Thick Film	LTCC	HTCC
Base substrates	PTFE glass fiber, PTFE ceramic, hydrocarbon ceramic, polyester glass	Al_2O_3, AlN, BeO, quartz, glass/ ceramic	Al_2O_3, AlN, BeO	N/A	N/A
Conductors	Cu	Au, Al, Cu	Au, PdAu, PtAu, Ag, PdAg, PtAg, PtPdAg, Cu	Au, Ag, PdAgCu	W, Mo
Dielectrics	N/A	SiO_2, polyimide, BCB	Glass-ceramics, recrystallizing glasses	Glass-ceramic tape	Ceramic (Al_2O_3) tape
Resistors	N/A	NiCr, TaN	RuO_2 doped glass	RuO_2 doped glass	N/A
Processes	Photolithography, etch, collate sheets, bonding	Sequentially vacuum deposit, spin coat, and/or plate conductors, dielectrics, and resistors; photolithography; etch	Sequentially print, dry, and fire conductor, dielectric, and resistor pastes	Punch vias, print and dry conductors on tape, collate layers, laminate, cofire	Punch vias, print and dry conductors on tape, collate layers, laminate, cofire

effects of bond wires, which connect discrete components in conventional hybrid MICs. In MMIC-based millimeter-wave subsystems the cost can be lowered by a factor of 10 or more compared to hybrid solutions.

Advantages of MMICs include low cost, small size, low weight, circuit design flexibility, broadband performance, elimination of circuit tweaking, high-volume manufacturing capability, package simplification, improved reproducibility, radiation hardness, improved reliability, and multifunction performance on a single chip. Indeed, the concept of implementing a "subsystem on a chip" became a reality through monolithic microwave technology.

Typically MMICs use microstrip and MIM capacitors for matching networks, whereas at low microwave frequencies, lumped inductors and MIM capacitors are commonly used. Via holes, metal-filled holes from the bottom of the substrate (ground plane) to the top surface of MMICs, provide low-loss and low-inductance ground connections. Figure 13.8 shows a three-dimensional view of an MMIC.

MMICs can be fabricated in any of many different ways [20–28]. MMICs using MESFETs and *high electron mobility transistors* (HEMTs) are most commonly fabricated with a recessed gate process, but the *self-aligned gate* (SAG) process is gaining popularity because of its ability to efficiently fabricate devices optimized for different functions, such as microwave small signal, microwave power, and digital logic, on the same wafer at the same time. The SAG process has demonstrated superior performance uniformity in a manufacturing environment.

13.5.1 MMIC Fabrication

To give the reader an understanding of the relative complexity of GaAs MMIC manufacturing, a process flowchart for the SAG process [27] is given in Figure 13.9. The process for recessed gate MMICs has many similarities. The process includes the fabrication of active devices, resistors, capacitors, inductors, distrib-

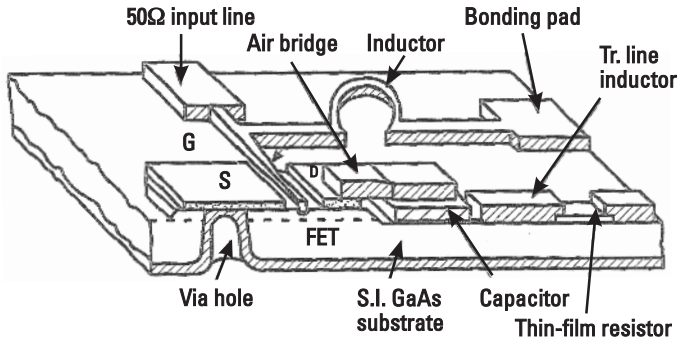


Figure 13.8 Three-dimensional view of a MMIC.

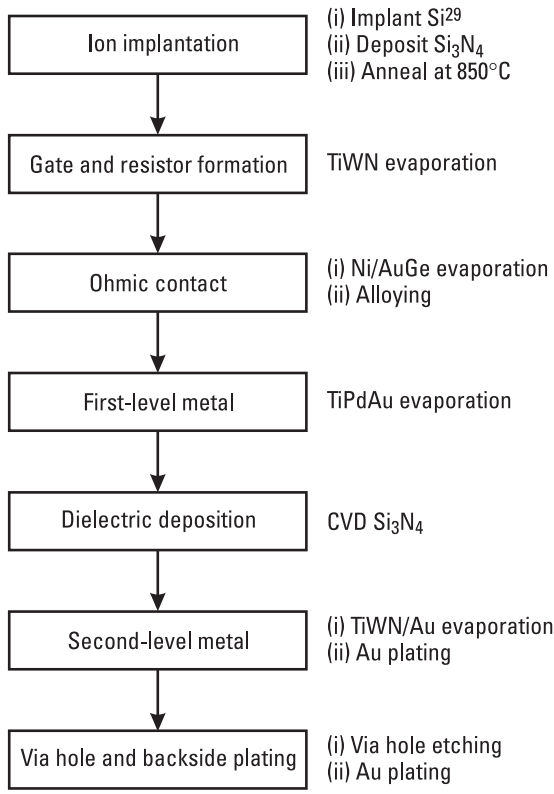


Figure 13.9 MMIC process flowchart for the multifunction SAG process.

uted matching networks, air bridges, and via holes for ground connections through a substrate. The basic process steps are similar in any MMIC technology.

Note that GaAs MMIC processing is less complex than silicon processing for devices operating at the low end of the microwave spectrum. Because silicon has inherently lower frequency capability and poorer isolation properties for integration purposes, more exotic processing is required to compete in the frequency region of overlap with GaAs applicability (~1–2 GHz). For example, a silicon BiCMOS process for such IC applications may require two or three times as many mask layers, adding significantly to the cost.

The MMIC process starts with the formation of an active layer on a qualified semi-insulating GaAs substrate. Two methods are used to form an *n*-type active layer: ion implantation and epitaxy. Next a gate is formed using a refractory metal such as TiWN or WSi. The quality and placement of the gate metal is critical to device performance in both low-noise and power applications. The choice of the gate metal is generally based on good adhesion to

GaAs, electrical conductivity, and thermal stability. Lumped-element resistors are realized using a TiWN layer having sheet resistance of 10 to 11 Ω/square as well as an active layer having sheet resistance of 120 to 150 Ω/square.

The device ohmic contacts are made next. The purpose of an ohmic contact on a semiconductor material is to provide a good contact between the interconnect metal and the active channel at the semiconductor surface. The most common approach in industry is to fabricate ohmic contacts on GaAs by alloying gold and germanium (88% Au and 12% Ge by weight, with a melting point of 360°C). The sheet resistance of a AuGe layer is about 1 Ω/square, which can also be used to realize small resistance values.

Next, a thick TiPdAu metal is overlayed on the gate by evaporation and liftoff. The metal reduces the gate resistance and also serves as a first-level metallization for MMIC fabrication, for example, as a capacitor bottom plate or the interconnect metal under airbridges or crossovers. Dielectric films are used in GaAs MMICs for the passivation of active areas of devices and resistors, for MIM capacitors, and for crossover isolation. Silicon nitride (Si_3N_4) is commonly used as a dielectric material that is easily deposited either by plasma-assisted chemical vapor deposition or sputtering. The thickness of the dielectric film determines the capacitance per unit area of the MMIC capacitor. Typical values for the film thickness, capacitance, and breakdown voltage are 0.2 μm, 300 pF/mm^2, and 60V, respectively.

Interconnection of components, airbridges, and the top plate of MIM capacitors is formed with a second layer of metal. Backside processing, consisting of thinning by grinding or lapping, via-hole etching, and ground contact metallization and plating, is an important and cost-sensitive part of the processing. In a production environment, a significant investment has been made in the wafer by the time the frontside processing is completed and the backside processing is started.

After the frontside process, the wafer is thinned by a lapping technique from ~600 μm to the required thickness, typically 100 to 125 μm for small-signal MMICs and 75 μm for power MMICs (to maximize heat conduction). High-performance MMICs require low-inductance ground connections to the FET source and other passive components, and good thermal dissipation paths from the FET to its ground. In via-hole technology, holes are etched through the GaAs substrate under each FET source connection, as well as under other pads where ground connections are needed. Then the backside and the via-hole sidewalls are metallized. This provides a good connection from the frontside devices and components to the backside ground plane. This also eliminates the need for separate wire bonds to ground each FET and other RF ground connections. The first check for a good circuit is automatic testing on wafer with microwave probes. After identifying RF good ICs, the wafer is diced into chips.

13.5.2 MMIC Example

Figure 13.10 shows the photograph of an MMIC 12-W X-band high-power amplifier. The chip uses three stages designed to operate with V_{DD} = 10V at a quiescent operating point of 25% of I_{dss}. The output stage employs a 20-mm gate periphery of MSAG MESFETs [29]. Typical measured output power and PAE were more than 12W and 35%, respectively, in the 8.5- to 10.5-GHz frequency range.

13.6 CMOS Fabrication

For RF wireless applications, several Si-based device technologies including bipolar, CMOS, BiCMOS, and SiGe HBT are being pursued to obtain an optimum solution. In the Si-based processes, Si wafers are larger and cheaper than GaAs wafers but the fabrication involves a relatively larger number of process steps. Salient features of a commonly used n-type or n-well CMOS fabrication process [30–32] are discussed next.

CMOS IC fabrication starts with thin circular (6- to 12-inch) silicon wafers also known as substrates. The wafers are doped with phosphorus (donor

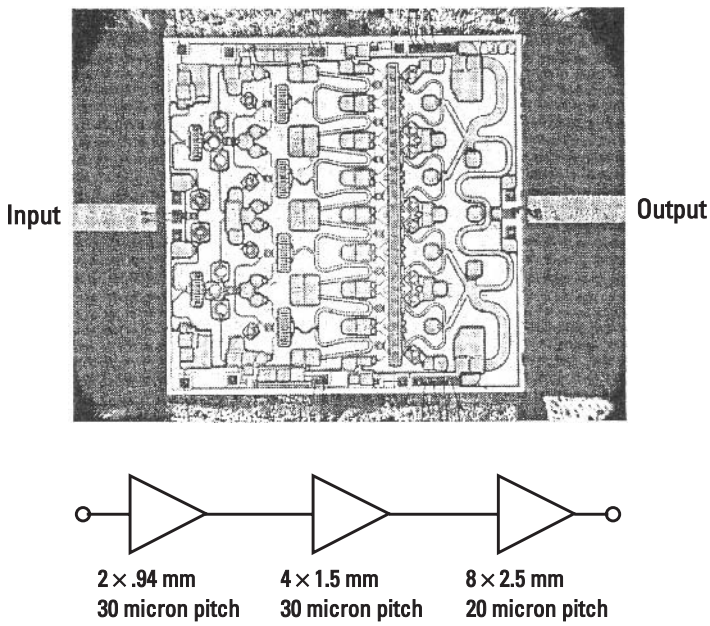


Figure 13.10 Layout and schematic for a 12-W high-power amplifier. Chip is 4.6 × 4.6 mm.

atoms) or boron (acceptor atoms) for an n-type or p-type wafer, respectively. For n-channel MOSFETs or NMOS, a p-type wafer is used. Basic steps for an n-well CMOS fabrication are shown in Figure 13.11. The process starts with the epitaxial growth of a p-type layer on a wafer/substrate. This layer provides a controlled thickness (1–20 μm) of high-purity silicon. The next step is n-well formulation using an ion implantation. Next, a layer of SiO_2 is grown and covered with Si_3N_4 to define active device areas followed by a p^+ field implant (known as a channel-stop implant) outside active device areas to isolate the active devices. After the channel-stop implant, a thick layer of *field oxide* (FOX) is grown in areas where the Si_3N_4 layer is absent, and next the Si_3N_4 and SiO_2 layers are removed. Following these steps, a thin layer of gate oxide ($\cong$ 80–200Å) is grown in active device areas.

Next, a layer of polysilicon is deposited and transistor gates, resistor connections, capacitor electrodes, and interconnections are defined. Oxide areas at the

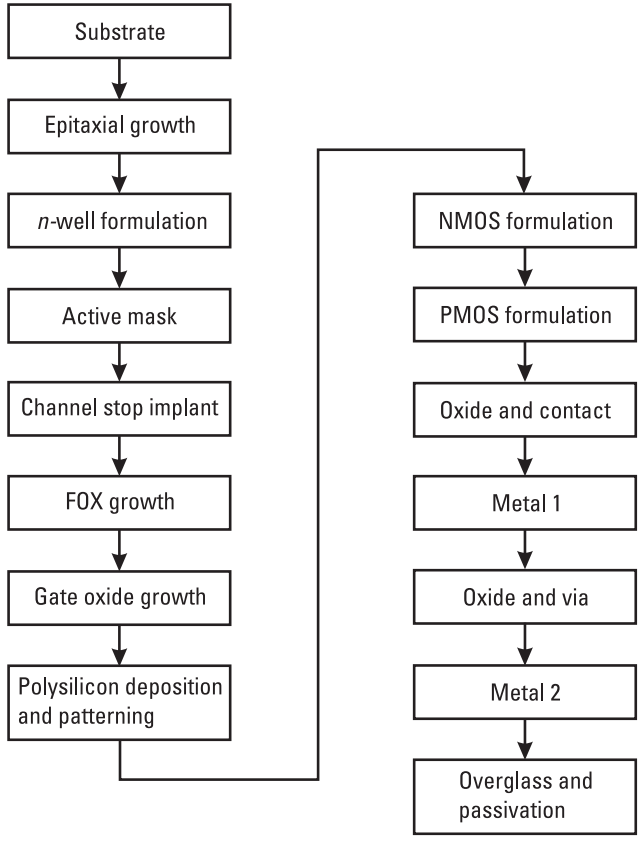


Figure 13.11 Basic steps for an n-well CMOS process.

drain and source locations of the n-type channel device are removed and donor atoms are introduced by diffusion or ion implantation to make n^+ regions for connections. Similarly acceptor atoms are introduced for p-type channel devices. This is followed by depositions of thick layers of oxide and metal 1 and metal 2. Connections between polysilicon and various metals are made through etched vias. At the end of the process, the wafers are passivated by another SiO_2 layer, leaving opened bonding pads areas for wire connections. Table 13.11 summarizes typical parameters of CMOS materials.

Lumped-element passive components such as resistors, capacitors, and inductors are realized in many different ways. Resistors include well, diffused, polysilicon, and thin-film resistors. Capacitors are comprised of poly-poly, metal-poly, metal-silicon, and silicon-silicon. Inductors include metal 1-metal 2 and many other metal layers.

The well and diffused resistors are formed by connecting a well region and n-channel or p-channel regions through source and drain connections. The well region's sheet resistivity is on the order of 10 kΩ/square, whereas diffused resistors have resistivity in the range of 100 to 200 Ω/square. Polysilicon gate layers are also used as resistors. The sheet resistivity of polysilicon layers used in CMOS fabrication is on the order of 20 to 80 Ω/square. Thin film resistors use nichrome and tantalum and are deposited on a SiO_2 layer. Depending on their thickness and composition, the range of sheet resistivity is 100 to 1,000 Ω/square.

A SiO_2 layer sandwiched between two polysilicon electrodes comprises poly-poly capacitors. The tolerance on the value of the capacitor is 10% to 20%. In the case of a poly-metal capacitor, one can adjust the thickness of SiO_2 between the polysilicon and metal 1 electrodes. Properties of such capacitors are similar to poly-poly capacitors. Figure 13.12 shows a cross-sectional view of a typical CMOS circuit.

For RF applications, inductors are also becoming part of the CMOS standard process. In this case the inductors are realized by using many available metal layers to improve the quality factor.

Table 13.11
Typical Parameters of CMOS Materials

Layer	Material	Thickness (μm)	Resistivity (Ω/square)
Poly 1	Polycrystalline	0.040	21
Poly 2	Polycrystalline	0.046	25
Metal 1	Al	0.6	0.06
Metal 2	Al	1.15	0.03

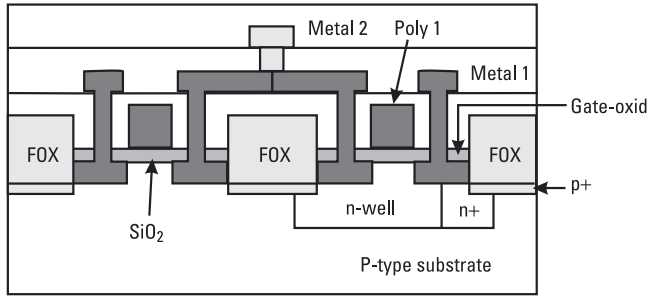


Figure 13.12 Cross-section of a finished CMOS device.

13.7 Micromachining Fabrication

Micromachining is commonly used to enhance the quality factor of inductors and transformers and is more popular with Si than GaAs substrates. Micromachining techniques can be employed using a frontside or backside etch process [33–35]. In the frontside process, first a thin layer of Si_3N_4 is deposited on a Si substrate. Then inductor conductors are patterned using standard photolithography, gold evaporation, and electroplating techniques. Next, a thick layer of Si_3N_4 is deposited, and an opening is defined on the frontside on the inductor pattern. Finally, openings in Si_3N_4 are dry etched and Si under the inductor pattern is anisotropically wet etched using KOH, leaving the inductor pattern on the suspended Si_3N_4 membrane. Figure 13.13 shows a cross-sectional view of a suspended inductor.

In the backside etch process, first a three-layer structure of $SiO_2/Si_3N_4/SiO_2$ is deposited on a silicon substrate to realize a flat and rigid membrane. Then inductor conductors are formed on this multilayer structure using standard photolithography, gold evaporation, and electroplating techniques. Finally, an opening is defined on the backside of the Si wafer underneath the inductor pattern, and the silicon is wet etched using KOH solution until the transparent dielectric membrane appears. The backside micromachining process in GaAs is compatible with the via-hole technique used in MMICs.

In general, frontside etching is preferred over backside etching for these reasons: It requires a shorter etch time, no backside alignment is required, it is independent of wafer thickness, and it allows for a higher package density.

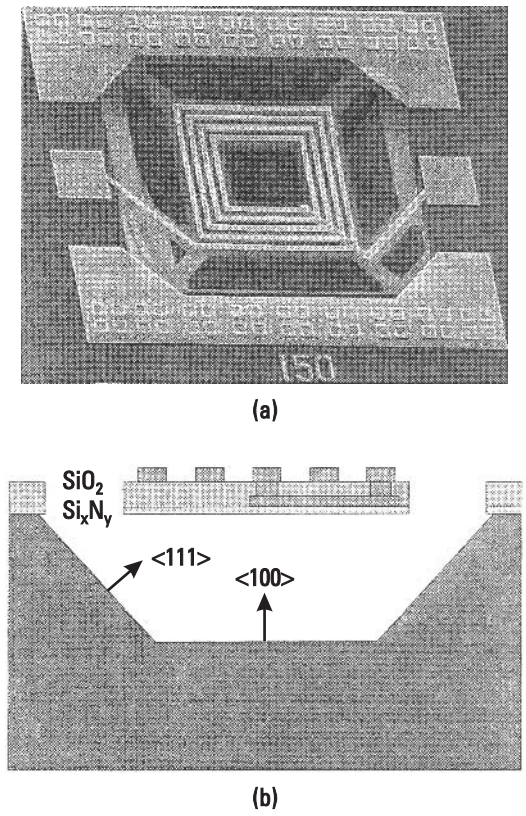


Figure 13.13 (a) Top and (b) cross-sectional views of a micromachined inductor.

References

[1] Tummala, R. R., and E. J. Rayaszewski, (Eds.), *Microelectronic Packaging Handbook,* New York: Van Nostrand Reinhold, 1989.

[2] Manzione, L. T., *Plastic Packing of Microelectronic Devices,* New York: Van Nostrand Reinhold, 1990.

[3] Sergent, J. E., and C. A. Harper, (Eds.), *Hybrid Microelectronic Handbook,* 2nd ed., New York: McGraw-Hill, 1995.

[4] Garrou, P. E., and I. Turlik, *Multichip Module Technology Handbook,* New York: McGraw-Hill, 1998.

[5] Kesiter, F. Z., "An Evaluation of Materials and Processes for Integrated Microwave Circuits," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-16, July 1978, pp. 469–475.

[6] Caulton, M., and H. Sobol, "Microwave Integrated Circuit Technology—A Survey," *IEEE J. Solid-State Circuits,* Vol. SC-5, December 1970, pp. 292–303.

[7] Sobol, H., "Applications of Integrated Circuit Technology to Microwave Frequencies," *Proc. IEEE,* Vol. 59, August 1971, pp. 1200–1211.

[8] Sobol, H., "Technology and Design of Hybrid Integrated Circuits," *Solid State Technol.,* Vol. 13, February 1970, pp. 49–57.

[9] Laverghetta, T. S., *Microwave Materials and Fabrication Techniques,* Dedham, MA: Artech House, 1984.

[10] Jones, R. D., *Hybrid Circuit Design and Manufacture,* New York: Dekker, 1982.

[11] Elliott, D. J., *Integrated Circuit Mask Technology,* New York: McGraw-Hill, 1985.

[12] Farquhar, D. S., A. M. Seman, and M. D. Paliks, "Manufacturing Experience with High Performance Mixed Dielectric Circuit Board," *IEEE Trans. Advanced Packaging,* Vol. 22, May 1999, pp. 153–159.

[13] Aguayo, A., "PTFE and Low Cost, High Performance Materials for High Speed and High Frequency Applications," *Proc. 6th Annual Wireless Symp.,* 1998, pp. 243–267.

[14] Walpita, L. M., et al., "Temperature-Compensated Thermoplastic High Dielectric-Constant Microwave Laminates," *IEEE Trans. Microwave Theory Tech.,* Vol. 47, August 1999, pp. 1577–1583.

[15] Devoe, L., and A. Devoe, "Technology and Innovation in Single Layer Capacitors," *Microwave J.,* Vol. 37, February 2002, pp. 144–152.

[16] Sechi, F., et al., "Miniature Beryllia Circuits—A New Technology for Microwave Power Circuits," *RCA Review,* Vol. 43, 1982, p. 363.

[17] Barnwell, P., and J. Wood, "A Novel Thick Film on Ceramic MCM Technology Offering MCM-D Performance," *6th Int. Conf. Multichip Modules,* Denver, CO, April 1997.

[18] Brown, R. L., P. W. Polinski, and A. S. Shaikh, "Manufacturing of Microwave Modules Using Low-Temperature Cofired Ceramics," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1994, pp. 1727–1730.

[19] Mohammed, A. A., "LTCC for High-Power RF Applications," *Advanced Packaging,* October 1999, pp. 46–50.

[20] Williams, R. E., *Gallium Arsenide Processing Techniques,* Dedham, MA: Artech House, 1984.

[21] Pucel, R. A., (Ed.), *Monolithic Microwave Integrated Circuits (A Reprint Volume),* Piscataway, NJ: IEEE Press, 1985.

[22] Ferry, D. K., (Ed.), *Gallium Arsenide Technology,* Indianapolis, IN: Howard Sams, 1985.

[23] Einspruch, N. G., and W R. Wisseman, *GaAs Microelectronics,* San Diego, CA: Academic Press, 1985.

[24] Mun, J., (Ed.), *GaAs Integrated Circuits: Design and Technology,* New York: Macmillan, 1988.

[25] Bahl, I. J., and P. Bhartia, *Microwave Solid State Circuit Design,* New York: John Wiley, 1988.

[26] Goyal, R., (Ed.), *Monolithic Microwave Integrated Circuits: Technology and Design,* Norwood, MA: Artech House, 1989.

[27] Fisher, D., and I. Bahl, *Gallium Arsenide IC Applications Handbook,* San Diego, CA: Academic Press, 1995.

[28] Bahl, I. J., "Monolithic Microwave Integrated Circuits," *Wiley Encyclopedia of Electrical and Electronics,* Vol. 13, New York: John Wiley, 1999, pp. 490–513.

[29] Griffin, E. L., "Application of Loadline Simulation to Microwave High Power Amplifiers," *IEEE Microwave Magazine,* Vol. I, June 2000, pp. 58–66.

[30] Baker, R. J., H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation,* Piscataway, NJ: IEEE Press, 1997.

[31] Kang, B., S. Lee, and J. Park, *CMOS Layout Design,* Sunnyvale, CA: MyCAD.

[32] Gray, P. R., and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits,* 3rd ed., New York: John Wiley, 1993.

[33] Chi, C.-Y., and G. M. Rebeiz, "Planar Microwave and Millimeter-Wave Lumped Elements and Coupled-Line Filters Using Micro-Machining Techniques," *IEEE Trans. Microwave Theory Tech.,* Vol. 43, April 1995, pp. 730–738.

[34] Sun, Y., et al., "Micromachined RF Passive Components and Their Applications in MMICs," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 9, July 1999, pp. 310–325.

[35] Ribas, R. P., et al., "Micromachined Microwave Planar Spiral Inductors and Transformers," *IEEE Trans. Microwave Theory Tech.,* Vol. 48, August 2000, pp. 1326–1335.

14

Microstrip Overview

14.1 Design Equations

Microstrip line is the most commonly used transmission medium in RF and microwave circuits, due to its quasi-TEM nature and excellent layout flexibility. When the size of the microstrip section is reduced to dimensions much smaller than the wavelength, it can be used as a lumped element. Thus, the basic design of many lumped elements is based on a microstrip structure. A cross-sectional view of a microstrip line with physical parameters is shown in Figure 14.1. The important parameters for designing these transmission lines are the characteristic impedance (Z_0), effective dielectric constant (ϵ_{re}), attenuation constant (α), discontinuity reactances, frequency dispersion, surface wave excitation, and radiation. Several methods to determine these parameters are summarized in [1–12]. A complete set of design equations for microstrips is presented in this chapter, including closed-form expressions for the characteristic impedance and effective dielectric constant, and their variation with metal strip thickness, enclosure size, and dispersion. Expressions for microstrip loss and quality factor Q are also described.

14.1.1 Characteristic Impedance and Effective Dielectric Constant

Closed-form expressions for Z_0 and ϵ_{re} when conductor thickness $t = 0$ are given here [1]:

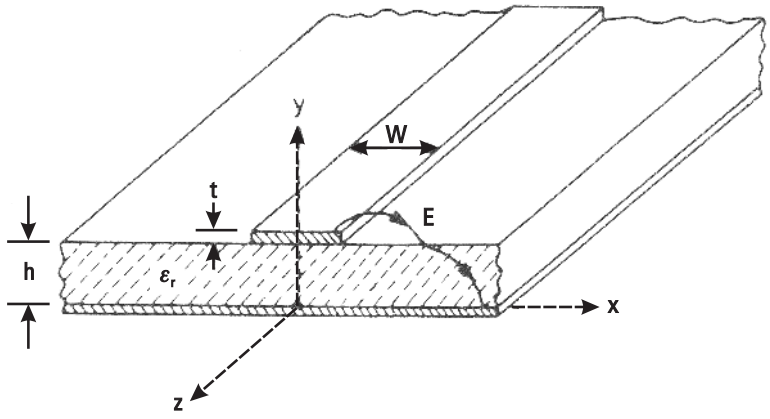


Figure 14.1 Microstrip configuration.

$$Z_0 = \begin{cases} \dfrac{\eta}{2\pi\sqrt{\epsilon_{re}}} \ln\left(\dfrac{8h}{W} + 0.25\dfrac{W}{h}\right) & \text{for } (W/h \le 1) \\ \dfrac{\eta}{\sqrt{\epsilon_{re}}}\left\{\dfrac{W}{h} + 1.393 + 0.667 \ln\left(\dfrac{W}{h} + 1.444\right)\right\}^{-1} & \text{for } (W/h \ge 1) \end{cases} \quad \begin{matrix} (14.1a) \\ (14.1b) \end{matrix}$$

where $\eta = 120\pi$ ohm and

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} F(W/h) \tag{14.2}$$

$$F(W/h) = \begin{cases} (1 + 12h/W)^{-1/2} + 0.041(1 - W/h)^2 & \text{for } (W/h \le 1) \\ (1 + 12h/W)^{-1/2} & \text{for } (W/h \ge 1) \end{cases} \tag{14.3}$$

The maximum relative error in ϵ_{re} and Z_0 is less than 1%. The expressions for W/h in terms of Z_0 and ϵ_{re} are as follows:

For $Z_0\sqrt{\epsilon_{re}} > 89.91$,

$$W/h = \frac{8\exp(A)}{\exp(2A) - 2} \tag{14.4a}$$

For $Z_0\sqrt{\epsilon_{re}} \le 89.91$,

$$W/h = \frac{2}{\pi}\left\{B - 1 - \ln(2B-1) + \frac{\epsilon_r - 1}{2\epsilon_r}\left[\ln(B-1) + 0.39 - \frac{0.61}{\epsilon_r}\right]\right\} \tag{14.4b}$$

where

$$A = \frac{Z_0}{60}\left\{\frac{\epsilon_r + 1}{2}\right\}^{1/2} + \frac{\epsilon_r - 1}{\epsilon_r + 1}\left\{0.23 + \frac{0.11}{\epsilon_r}\right\} \tag{14.5a}$$

$$B = \frac{60\pi^2}{Z_0\sqrt{\epsilon_r}} \tag{14.5b}$$

These expressions also provide an accuracy of better than 1%. Values of the characteristic impedance and effective dielectric constant as a function of the W/h ratio are shown in Figure 14.2. Here $Z_0 = Z_0^a/\sqrt{\epsilon_{re}}$.

14.1.2 Effect of Strip Thickness

Simple and accurate formulas for Z_0 and ϵ_{re} with finite strip thickness are as follows:

$$Z_0 = \begin{cases} \dfrac{\eta}{2\pi\sqrt{\epsilon_{re}}}\ln\left\{\dfrac{8h}{W_e} + 0.25\dfrac{W_e}{h}\right\} & \text{for } (W/h \le 1) \\ \dfrac{\eta}{\sqrt{\epsilon_{re}}}\left\{\dfrac{W_e}{h} + 1.393 + 0.667\ln\left(\dfrac{W_e}{h} + 1.444\right)\right\}^{-1} & \text{for } (W/h \ge 1) \end{cases} \tag{14.6a}$$
(14.6b)

where

$$\frac{W_e}{h} = \begin{cases} \dfrac{W}{h} + \dfrac{1.25}{\pi}\dfrac{t}{h}\left(1 + \ln\dfrac{4\pi W}{t}\right) & \text{for } (W/h \le \tfrac{1}{2}\pi) \quad (14.7a) \\ \dfrac{W}{h} + \dfrac{1.25}{\pi}\dfrac{t}{h}\left(1 + \ln\dfrac{2h}{t}\right) & \text{for } (W/h \ge \tfrac{1}{2}\pi) \quad (14.7b) \end{cases}$$

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}F(W/h) - C \tag{14.7c}$$

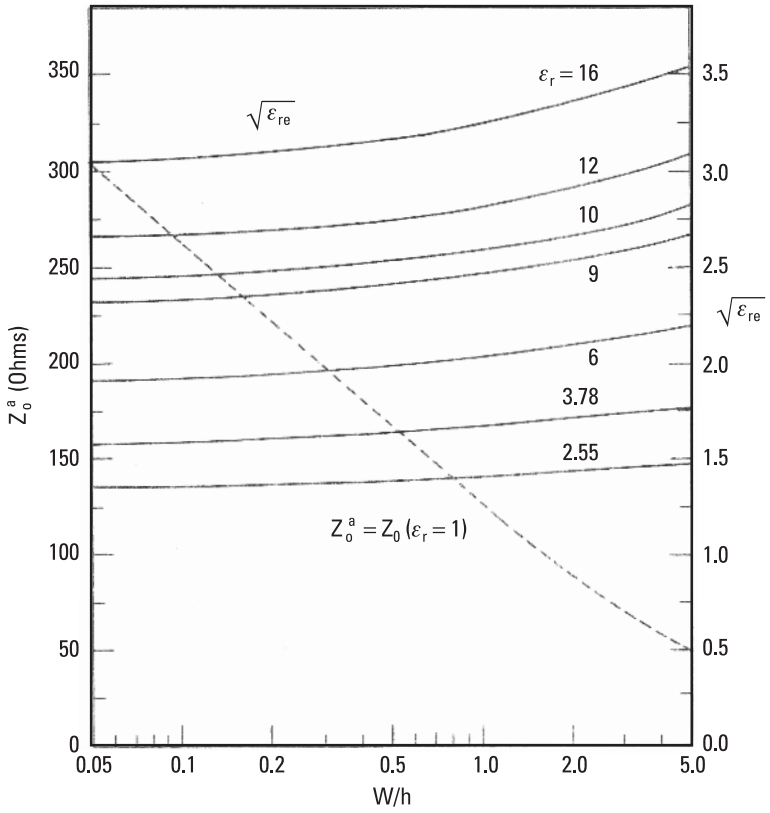


Figure 14.2 Characteristic impedance and effective dielectric constant of microstrip lines calculated using Wheeler's method.

in which

$$C = \frac{\epsilon_r - 1}{4.6} \frac{t/h}{\sqrt{W/h}} \tag{14.8}$$

Note that the effect of thickness on Z_0 and ϵ_{re} is insignificant for small values of t/h. However, the effect of strip thickness is significant on conductor loss in the microstrip line. This is described later in Section 14.2.2.

14.2 Design Considerations

In this section, important design parameters of microstrip lines are discussed, including dispersion, attenuation constant, enclosure effect, frequency range of operation, and power-handling capability.

14.2.1 Effect of Dispersion

The effect of frequency f on the characteristics of Z_0 and ϵ_{re} is known as dispersion. The accurate expressions of Hammerstad and Jensen [10] for $Z_0(f)$, and Kobayashi [12] for $\epsilon_{re}(f)$ are given here:

$$Z_0(f) = Z_0 \frac{\epsilon_{re}(f) - 1}{\epsilon_{re} - 1} \sqrt{\frac{\epsilon_{re}}{\epsilon_{re}(f)}} \tag{14.9}$$

$$\epsilon_{re}(f) = \epsilon_r - \frac{\epsilon_r - \epsilon_{re}}{1 + (f/f_{50})^m} \tag{14.10}$$

where

$$f_{50} = \frac{f_{k,TM_0}}{0.75 + \{0.75 - (0.332/\epsilon_r^{1.73})\} W/h} \tag{14.11a}$$

$$f_{k,TM_0} = \frac{c \tan^{-1}\left(\epsilon_r \sqrt{\dfrac{\epsilon_{re} - 1}{\epsilon_r - \epsilon_{re}}}\right)}{2\pi h \sqrt{\epsilon_r - \epsilon_{re}}} \tag{14.11b}$$

$$m = m_o m_c$$

$$m_o = 1 + \frac{1}{1 + \sqrt{W/h}} + 0.32 \left(\frac{1}{1 + \sqrt{W/h}}\right)^3$$

$$m_c = \begin{cases} 1 + \dfrac{1.4}{1 + W/h}\left\{0.15 - 0.235 \exp\left(\dfrac{-0.45f}{f_{50}}\right)\right\} & \text{for } W/h \le 0.7 \\ 1 & \text{for } W/h > 0.7 \end{cases} \tag{14.12}$$

with Z_0, ϵ_{re} as the quasistatic values obtained earlier and c the velocity of light. If $h/\lambda << 1$, the effect of dispersion is negligible.

14.2.2 Microstrip Losses

Attenuation in a microstrip structure is caused by two loss components: conductor loss and dielectric loss. Closed-form expressions for the conductor (α_c) and dielectric (α_d) attenuation constants expressed in decibels per unit length are as follows:

$$\alpha_c = \begin{cases} 1.38A\dfrac{R_s}{hZ_0}\dfrac{32-(W_e/h)^2}{32+(W_e/h)^2} & (W/h \le 1) \\ 6.1\times 10^{-5}A\dfrac{R_s Z_0 \epsilon_{re}(f)}{h}\left[W_e/h + \dfrac{0.667W_e/h}{W_e/h+1.444}\right] & (W/h \ge 1) \end{cases} \tag{14.13}$$

and

$$\alpha_d = \begin{cases} 4.34\eta\sigma\dfrac{\epsilon_{re}(f)-1}{\sqrt{\epsilon_{re}(f)}(\epsilon_r-1)} & \text{or} \\ 27.3\dfrac{\epsilon_r}{\epsilon_r-1}\dfrac{\epsilon_{re}(f)-1}{\sqrt{\epsilon_{re}(f)}}\dfrac{\tan\delta}{\lambda_0} \end{cases} \tag{14.14}$$

where λ_0 is the free-space wavelength. Other variables are defined here:

$$A = 1 + \frac{h}{W_e}\left\{1 + \frac{1.25}{\pi}\ln\frac{2B}{t}\right\}$$

$$R_s = \sqrt{\pi f \mu_0 \rho_c}; \quad \rho_c = \text{resistivity of the strip conductor}$$

$$\sigma = \omega\epsilon_0\epsilon_r \tan\delta = \text{conductivity of the dielectric substrate}$$

and

$$B = \begin{cases} h & \text{for } \left(W/h \ge \dfrac{1}{2\pi}\right) \\ 2\pi W & \text{for } \left(W/h \le \dfrac{1}{w\pi}\right) \end{cases}$$

The dielectric loss is normally very small compared with the conductor loss for dielectric substrates such as alumina, AlN, and BeO. The dielectric loss in silicon substrates (used for MMICs), however, is usually of the same order or even larger than the conductor loss. This is because of the lower resistivity available in silicon wafers. However, higher resistivity can be obtained in GaAs semiconductors; therefore, the dielectric loss is lower for this material. Values of conductor and dielectric losses per unit length for 50-Ω microstrip lines on various substrates (insulator as well as semiconductor) are plotted in Figure 14.3 as a function of frequency.

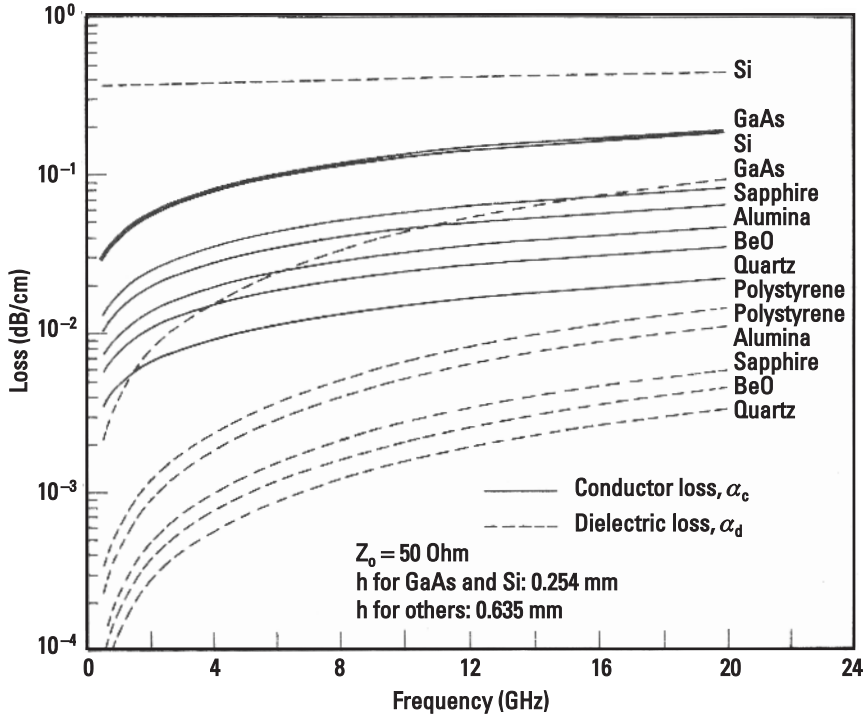


Figure 14.3 Conductor and dielectric losses as a function of frequency for microstrip lines on various substrates.

At a given frequency the total loss can be obtained by adding the two values, that is,

$$\alpha_T = \alpha_c + \alpha_d \tag{14.15}$$

Tables 14.1–14.6 summarize microstrip characteristics for several line widths and substrate materials. The data were calculated at 10 GHz. The substrate thickness for ϵ_r = 2.2, 4.3, 6.7, and 9.9 was 15 mil, whereas for ϵ_r = 11.7 and 12.9 it was 4 mil. The values for metallization thickness t and tan δ were 5 μm and 0.0005, respectively.

14.2.3 Quality Factor *Q*

The quality factor, Q, of a microstrip resonator can be related to the total loss in the line by

$$Q_T = \frac{\beta}{2\alpha_T} = \frac{\pi\epsilon_{re}}{\alpha_T \lambda_0} \tag{14.16}$$

Table 14.1
Microstrip Data Summary for $h = 381\ \mu$m, $t = 5\ \mu$m, tan $\delta = 0.0005$, $f = 10$ GHz, and $\epsilon_r = 2.2$

W (μm)	W/h	Z_0	ϵ_{re}	α (dB/cm)	Line Capacitance (pF/100 μm)	Line Inductance (nH/100 μm)
50	0.13	183.9	1.66	0.122	0.002	0.079
75	0.20	166.7	1.68	0.099	0.003	0.072
100	0.26	154.2	1.69	0.086	0.003	0.067
125	0.33	144.3	1.70	0.077	0.003	0.063
150	0.39	136.2	1.71	0.070	0.003	0.059
200	0.52	123.3	1.73	0.062	0.004	0.054
250	0.66	113.4	1.74	0.056	0.004	0.050
300	0.79	105.3	1.75	0.052	0.004	0.046
400	1.05	92.6	1.78	0.047	0.005	0.041
500	1.31	83.0	1.80	0.045	0.005	0.037
750	1.97	66.6	1.84	0.041	0.007	0.030
1,000	2.62	55.9	1.87	0.039	0.008	0.025
1,500	3.94	42.6	1.92	0.037	0.011	0.020
2,000	5.25	34.5	1.96	0.036	0.014	0.016
3,000	7.87	25.2	2.00	0.035	0.019	0.012
4,000	10.50	19.8	2.04	0.035	0.024	0.009

where Q_T is the total Q of the resonator (quarter wavelength), α_T is the total loss in the resonator, and λ_0 is the free-space wavelength. When losses in a resonant line that is open circuited and a quarter-wavelength long are considered, another loss factor, α_r, due to radiation at the open end discontinuities must also be taken into account. The corresponding radiation Q-factor is given by:

$$Q_r = \frac{Z_0}{480\pi(h/\lambda_0)^2 R} \tag{14.17}$$

where

$$R = \frac{\epsilon_{re}(f) + 1}{\epsilon_{re}(f)} - \frac{[\epsilon_{re}(f) - 1]^2}{2[\epsilon_{re}(f)]^{3/2}} \ln\left\{\frac{\sqrt{\epsilon_{re}(f)} + 1}{\sqrt{\epsilon_{re}(f)} - 1}\right\} \tag{14.18}$$

The total Q of the resonator can be expressed by

$$\frac{1}{Q_T} = \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_r} \tag{14.19}$$

Table 14.2
Microstrip Data Summary for $h = 381\ \mu$m, $t = 5\ \mu$m, tan $\delta = 0.0005$, $f = 10$ GHz, and $\epsilon_r = 4.3$

W (μm)	W/h	Z_0	ϵ_{re}	α (dB/cm)	Line Capacitance (pF/100 μm)	Line Inductance (nH/100 μm)
25	0.07	164.6	2.75	0.214	0.003	0.091
50	0.13	142.2	2.82	0.159	0.004	0.080
75	0.20	128.5	2.86	0.130	0.004	0.072
100	0.26	118.6	2.89	0.112	0.005	0.067
125	0.33	110.9	2.92	0.100	0.005	0.063
150	0.39	104.5	2.95	0.092	0.005	0.060
200	0.52	94.4	2.99	0.081	0.006	0.054
250	0.66	86.6	3.03	0.074	0.007	0.050
300	0.79	80.3	3.07	0.069	0.007	0.047
400	1.05	70.4	3.13	0.064	0.008	0.042
500	1.31	63.0	3.19	0.061	0.009	0.038
750	1.97	50.2	3.31	0.057	0.012	0.030
1,000	2.62	42.0	3.41	0.054	0.015	0.026
1,500	3.94	31.8	3.55	0.052	0.020	0.020
2,000	5.25	25.7	3.65	0.051	0.025	0.016

Here, Q_c, Q_d, and Q_r are the quality factors corresponding to conductor, dielectric, and radiation losses, respectively. Finally, the circuit quality factor, Q_0, is defined as

$$\frac{1}{Q_0} = \frac{1}{Q_c} + \frac{1}{Q_d} = \frac{\lambda_0(\alpha_c + \alpha_d)}{\pi\sqrt{\epsilon_{re}(f)}} \tag{14.20}$$

The variation of Q_0, Q_r, and Q_T for a quarter-wave resonator on GaAs, alumina, and quartz substrates is shown in Figure 14.4. A quarter-wave 50-Ω resonator on a 25-mil-thick alumina substrate has a Q_0 of about 240 at 2.0 GHz and 550 at 10.0 GHz, whereas Q_T is 230 at 2.0 GHz and nearly 160 at 10.0 GHz. This is due to the fact that the radiation losses are higher than the conductor and dielectric losses at higher frequencies. On the other hand, a quarter-wave 50-Ω resonator on a 10-mil-thick GaAs substrate has a Q_0 of about 82 at 2.0 GHz and 160 at 10.0 GHz, whereas Q_T is 82 at 2.0 GHz and nearly 145 at 10.0 GHz. This is explained by smaller radiation losses for thin substrates.

The variation of Q_T, with substrate thickness, for quarter-wave resonators on RT/duroid, quartz, and alumina is shown in Figure 14.5 for $f = 30$, 50, and 100 GHz.

Table 14.3
Microstrip Data Summary for $h = 381\ \mu$m, $t = 5\ \mu$m, tan $\delta = 0.0005$, $f = 10$ GHz, and $\epsilon_r = 6.7$

W (μm)	W/h	Z_0	ϵ_{re}	α (dB/cm)	Line Capacitance (pF/100 μm)	Line Inductance (nH/100 μm)
10	0.03	159.4	3.87	0.377	0.004	0.105
25	0.07	136.8	4.02	0.258	0.005	0.091
50	0.13	118.0	4.14	0.192	0.006	0.080
75	0.20	106.5	4.21	0.157	0.006	0.073
100	0.26	98.2	4.27	0.136	0.007	0.068
125	0.33	91.7	4.33	0.122	0.008	0.064
150	0.39	86.4	4.37	0.112	0.008	0.060
200	0.52	78.0	4.45	0.099	0.009	0.055
250	0.66	71.5	4.52	0.091	0.010	0.051
300	0.79	66.2	4.58	0.085	0.011	0.047
400	1.05	58.0	4.70	0.079	0.012	0.042
500	1.31	51.8	4.81	0.076	0.014	0.038
750	1.97	41.3	5.02	0.071	0.018	0.031
1,000	2.62	34.4	5.19	0.068	0.022	0.026
1,500	3.94	26.0	5.45	0.065	0.030	0.020
2,000	5.25	21.0	5.63	0.064	0.038	0.017

For a given frequency, there is an optimum substrate thickness at which the Q is maximum. This optimum value of h decreases with increasing frequency and decreasing dielectric constant value, mainly because of radiation.

14.2.4 Enclosure Effect

Most microstrip circuit applications require a metallic enclosure for hermetic sealing, mechanical strength, electromagnetic shielding, mounting connectors, and ease of handling. Figure 14.6 shows the enclosed microstrip configuration. Both the top cover and sidewalls tend to lower impedance and effective dielectric constant. This is because the fringing electric field lines are prematurely terminated on the enclosure walls. This increases the electric flux in the air. Closed-form equations for a microstrip with top cover (without side walls) are obtained as follows [6, 11]:

$$Z_0^a = Z_{0\infty}^a - \Delta Z_0^a \tag{14.21}$$

where $Z_{0\infty}^a$ is the characteristic impedance with infinite shield height and superscript a designates air as dielectric. The decrease in impedance ΔZ_0^a is given by

Table 14.4
Microstrip Data Summary for $h = 381\ \mu$m, $t = 5\ \mu$m, tan $\delta = 0.0005$, $f = 10$ GHz, and $\epsilon_r = 9.9$

W (μm)	W/h	Z_0	ϵ_{re}	α (dB/cm)	Line Capacitance (pF/100 μm)	Line Inductance (nH/100 μm)
10	0.03	134.6	5.50	0.447	0.006	0.105
25	0.07	115.3	5.73	0.307	0.007	0.092
50	0.13	99.3	5.92	0.229	0.008	0.080
75	0.20	89.5	6.04	0.187	0.009	0.073
100	0.26	82.5	6.14	0.162	0.010	0.068
125	0.33	77.1	6.22	0.146	0.011	0.064
150	0.39	72.6	6.29	0.134	0.012	0.061
200	0.52	65.5	6.42	0.118	0.013	0.055
250	0.66	60.0	6.53	0.108	0.014	0.051
300	0.79	55.6	6.63	0.101	0.015	0.048
400	1.05	48.7	6.83	0.096	0.018	0.042
500	1.31	43.5	7.00	0.093	0.020	0.038
750	1.97	34.6	7.35	0.087	0.026	0.031
1,000	2.62	28.8	7.62	0.084	0.032	0.027
1,500	3.94	21.7	8.03	0.080	0.043	0.021
2,000	5.25	17.5	8.32	0.079	0.055	0.017

$$\Delta Z_0^a = \begin{cases} P & \text{for } W/h \le 1 \\ P \cdot Q & \text{for } W/h \ge 1 \end{cases} \tag{14.22}$$

where

$$P = 270\left[1 - \tanh\left(0.28 + 1.2\sqrt{\frac{h'}{h}}\right)\right\} \tag{14.23a}$$

$$Q = 1 - \tanh^{-1}\left(\frac{0.48\sqrt{\dfrac{W}{h} - 1}}{\left(1 + \dfrac{h'}{h}\right)^2}\right) \tag{14.23b}$$

and h' is the height of the top cover above the strip conductor. In this expression, the distance between the ground plane and the top cover is $h + h'$. The effective dielectric constant is calculated from the concept of the filling factor q as follows:

Table 14.5
Microstrip Data Summary for $h = 100\ \mu$m, $t = 5\ \mu$m, tan $\delta = 0.0005$, $f = 10$ GHz, and $\epsilon_r = 11.7$

W (μm)	W/h	Z_0	ϵ_{re}	α (dB/cm)	Line Capacitance (pF/100 μm)	Line Inductance (nH/100 μm)
10	0.10	91.8	6.30	0.685	0.009	0.077
20	0.20	78.6	6.60	0.517	0.011	0.067
30	0.30	70.3	6.80	0.447	0.012	0.061
40	0.40	64.2	6.95	0.403	0.014	0.056
50	0.50	59.4	7.08	0.373	0.015	0.053
75	0.75	50.7	7.35	0.327	0.018	0.046
100	1.00	44.5	7.57	0.301	0.021	0.041
125	1.25	39.9	7.76	0.287	0.023	0.037
150	1.50	36.2	7.93	0.280	0.026	0.034
200	2.00	30.6	8.22	0.269	0.031	0.029
250	2.50	26.6	8.46	0.263	0.036	0.026
300	3.00	23.5	8.66	0.258	0.042	0.023
400	4.00	19.2	8.99	0.253	0.052	0.019
500	5.00	16.2	9.25	0.250	0.062	0.016

Table 14.6
Microstrip Data Summary for $h = 100\ \mu$m, $t = 5\ \mu$m, tan $\delta = 0.0005$, $f = 10$ GHz, and $\epsilon_r = 12.9$

W (μm)	W/h	Z_0	ϵ_{re}	α (dB/cm)	Line Capacitance (pF/100 μm)	Line Inductance (nH/100 μm)
10	0.10	87.8	6.89	0.716	0.010	0.077
20	0.20	75.1	7.23	0.541	0.012	0.067
30	0.30	67.2	7.45	0.468	0.014	0.061
40	0.40	61.4	7.62	0.422	0.015	0.056
50	0.50	56.8	7.76	0.390	0.016	0.053
75	0.75	48.4	8.06	0.342	0.020	0.046
100	1.00	42.5	8.31	0.315	0.023	0.041
125	1.25	38.1	8.52	0.301	0.026	0.037
150	1.50	34.5	8.71	0.293	0.028	0.034
200	2.00	29.2	9.03	0.282	0.034	0.029
250	2.50	25.4	9.30	0.276	0.040	0.026
300	3.00	22.5	9.52	0.271	0.046	0.023
400	4.00	18.3	9.89	0.265	0.057	0.019
500	5.00	15.5	10.18	0.262	0.069	0.016

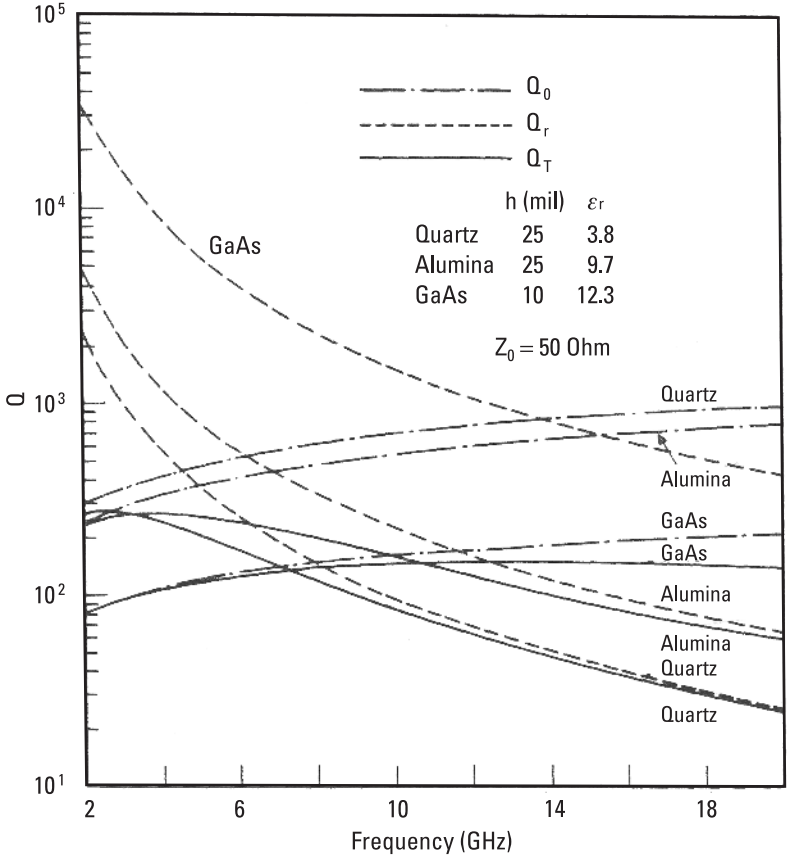


Figure 14.4 Variation of Q-factors with frequency for quarter-wave microstrip resonators on quartz, alumina, and GaAs substrates.

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + q\frac{\epsilon_r - 1}{2} \tag{14.24a}$$

$$q = (q_\infty - q_T)q_c \tag{14.24b}$$

where

$$q_\infty - q_T = F(W/h) \tag{14.25a}$$

$$q_T = \frac{2}{\pi}\frac{\ln 2}{\sqrt{\frac{W}{h}}}\frac{t}{h} \tag{14.25b}$$

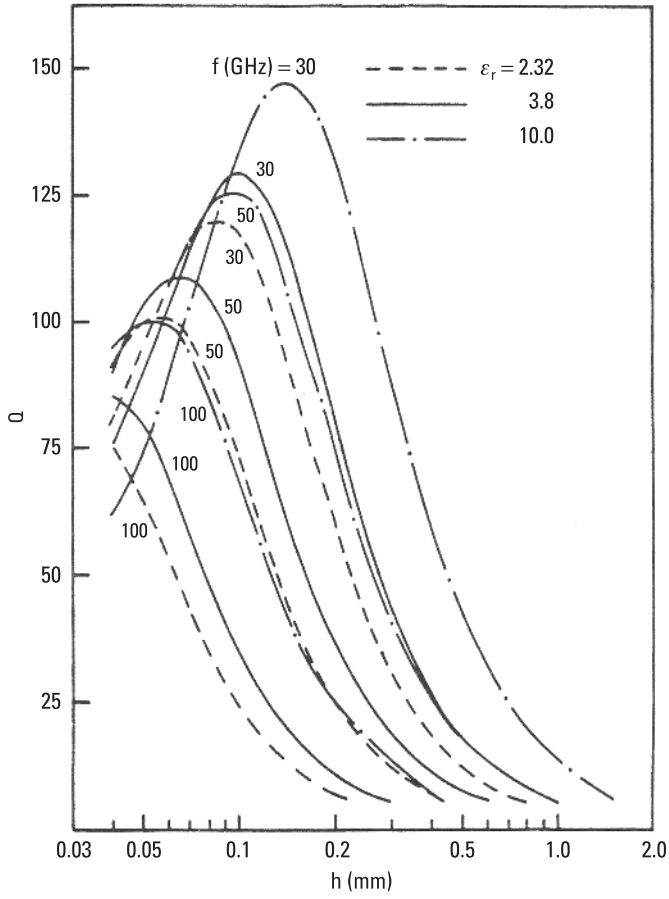


Figure 14.5 Total Q for a quarter-wave resonator on RT/Duroid ($\epsilon_r = 2.32$), quartz ($\epsilon_r = 3.8$), and alumina ($\epsilon_r = 10.0$) versus substrate thickness.

$$q_c = \tanh\left(1.043 + 0.121\frac{h'}{h} - 1.164\frac{h}{h'}\right) \tag{14.25c}$$

Here $F(W/h)$ is given by (14.3). Using the preceding equations, the characteristic impedance of the shielded microstrip can be calculated from $Z_0 = Z_0^a/\sqrt{\epsilon_{re}}$.

For the range of parameters, $1 \le \epsilon_r \le 30$, $0.05 \le W/h \le 20$, $t/h \le 0.1$, and $1 < h'/h < \infty$, the maximum error in Z_0 and ϵ_{re} is found to be less than $\pm 1\%$. When $h'/h \ge 5$, the effect of the top cover on the microstrip characteristics becomes negligible.

The effect of sidewalls on the characteristics of microstrip must also be included. It is found that the sidewall effect is negligible when $S/h \ge 5$, where

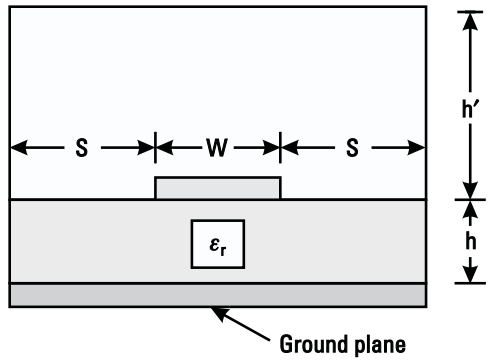


Figure 14.6 Enclosed microstrip configuration.

S is the separation between the microstrip conductor edge and the sidewall of the enclosure.

14.2.5 Frequency Range of Operation

The maximum frequency of operation of a microstrip is limited due to several factors such as excitation of spurious modes, higher losses, pronounced discontinuity effects, low Q due to radiation from discontinuities, effect of dispersion on pulse distortion, tight fabrication tolerances, handling fragility, and, of course, technological processes. The frequency at which significant coupling occurs between the quasi-TEM mode and the lowest order surface wave spurious mode is given here [1, 3]:

$$f_T = \frac{150}{\pi h}\sqrt{\frac{2}{\epsilon_r - 1}}\tan^{-1}(\epsilon_r) \tag{14.26}$$

where f_T is in gigahertz and h is in millimeters. Thus the maximum thickness of the quartz substrate ($\epsilon_r \cong 3.8$) for microstrip circuits designed at 100 GHz is less than 0.3 mm.

The excitation of higher order modes in a microstrip can be avoided by operating below the cutoff frequency of the first higher order mode, which is given approximately by

$$f_c \cong \frac{300}{\sqrt{\epsilon_r}(2W + 0.8h)} \tag{14.27}$$

where f_c is in gigahertz, and W and h are in millimeters. This limitation is mostly applied to low impedance lines that have wide microstrip conductors.

14.2.6 Power-Handling Capability

The power-handling capacity of a microstrip, like that of any other dielectric filled transmission line, is limited by heating as a result of ohmic and dielectric losses and by dielectric breakdown. An increase in temperature due to conductor and dielectric losses limits the average power of the microstrip line, whereas the breakdown between the strip conductor and ground plane limits the peak power.

14.2.6.1 Average Power

Microstrip lines are well suited for medium power (about 100 to 200W) applications and have been extensively used in power MMIC amplifiers. *Average power-handling capability* (APHC) of microstrip lines has been discussed in [1, 13–15]. Recent advancements in multilayer microstrip line technologies have made it possible to realize compact MMICs [16], compact modules [17], low-loss microstrip lines [18], and high-Q inductors [19]. In multilayered components, along with substrate materials, low dielectric constant materials such as polyimide or BCB are used as a multilayer dielectric. The thermal resistance of polyimide or BCB is about 200 times the thermal resistance of GaAs or alumina. To ensure reliable operation of multilayered components such as inductors, capacitors, crossovers, and inductor transformers for high-power applications, thermal models are needed for these structures. Bahl [20] discussed the average power-handling capability of multilayer microstrip lines used in MICs and MMICs.

The APHC of a multilayer microstrip is determined by the temperature rise of the strip conductor and the supporting dielectric layers and the substrate. The parameters that play major roles in the calculation of average power capability are (1) transmission-line losses, (2) the thermal conductivity of dielectric layers and the substrate material, (3) the surface area of the strip conductor; (4) the maximum allowed operating temperature of the microstrip structure, and (5) ambient temperature; that is, the temperature of the medium surrounding the microstrip. Therefore, dielectric layers and substrates with low-loss tangents and large thermal conductivities will increase the average power-handling capability of microstrip lines.

Typically a procedure for APHC calculation consists of the calculation of conductor and dielectric losses, heat flow due to power dissipation, and the temperature rise. The temperature rise of the strip conductor can be calculated from the heat flow field in the microstrip cross section. An analogy between the heat flow field and the electric field is provided in Table 14.7. The heat generated by the conductor loss and the dielectric loss is discussed separately in the following sections. It has been assumed that there are no nonuniformities in the line and that the line is perfectly matched at two ends.

14.2.6.2 Density of Heat Flow Due to Conductor Loss

A loss of electromagnetic power in the strip conductor generates heat in the strip. Because of the good heat conductivity of the strip metal, heat generation

Table 14.7
Analogy Between Heat Flow and Electric Field

Heat Flow Field	Electric Field
1. Temperature, T (°C)	Potential, V (V)
2. Temperature gradient, T_g (°C/m)	Electric field, E (V/m)
3. Heat flow rate, Q (W)	Flux, ϕ (coulomb)
4. Density of heat flow, q (W/m^2)	Flux density, D (coulomb/m^2)
5. Thermal conductivity, K (W/m-°C)	Permittivity, ϵ (coulomb/m/V)
6. Density of heat generated, ρ_h (W/m^3)	Charge density, ρ (coulomb/m^3)
7. $q = -K\nabla T$	$D = -\epsilon\nabla V$
8. $\nabla \cdot q = \rho_h$	$\nabla \cdot D = \rho$

is uniform along the width of the conductor. Because the ground plane of the microstrip configuration is held at ambient temperature (i.e., acts as a heat sink), this heat flows from the strip conductor to the ground plane through the polyimide layer/layers and the GaAs/alumina substrate. The heat flow can be calculated by considering the analogous electric field distribution. The heat flow field in the microstrip structure corresponds to the electrostatic field (without any dispersion) of the microstrip. The electric field lines (and the thermal field lines in the case of heat flow) spread as they approach the ground plane.

As a first-order approximation, the heat flow from the microstrip conductor can be considered to follow the rule of 45° thermal spread angle [21] as shown in Figure 14.7 for a two-layered microstrip configuration. This means that the heat generated in the microstrip conductor (assuming there are no other heat sources and heat flow is mainly by conduction) flows down through the dielectric materials through areas larger than the strip conductor as it approaches the ground plane, where the ground plane acts as a heat sink. However, to account accurately for the increase in area normal to heat flow lines, the parallel plate

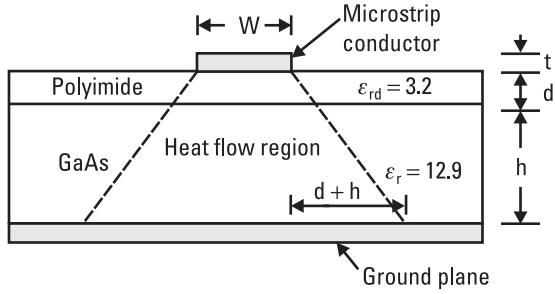


Figure 14.7 Schematic of microstrip line heat flow based on 45° thermal spread angle rule.

waveguide model of a microstrip has been used [1, 13]. In the parallel plate waveguide model of Figure 14.8(c), the capacitance per unit length is the same as for the multilayer microstrip, Figure 14.8(a), therefore we should have same electric flux ϕ per unit length of the line. Thus, for a given heat generated, the heat flow rate will be the same in the two-layer structure of Figure 14.8(a) and

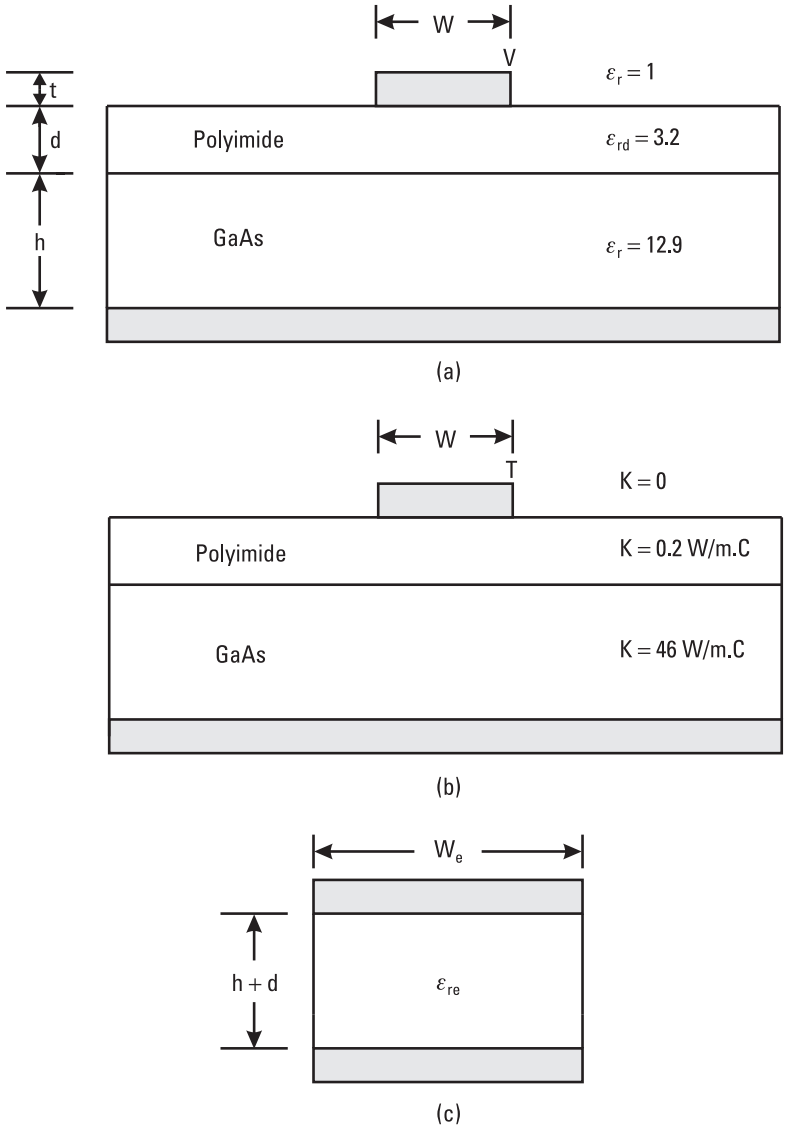


Figure 14.8 (a) Electrical and (b) thermal representation of the two-layer microstrip, and (c) the equivalent parallel-plate model.

in the equivalent parallel plate model of Figure 14.8(c). The equivalent width of the strip (W_e) in the parallel plate thermal model is calculated from the electrical analog and is given by

$$Z_0 = Z_0^a/\sqrt{\epsilon_{re}} = \frac{120\pi(d+h)}{W_e} \tag{14.28a}$$

or

$$W_e = \frac{120\pi(h+d)}{Z_0^a} \tag{14.28b}$$

where $(h + d)$ is the thickness of the dielectric between the plates, ϵ_{re} is the effective dielectric constant of the multilayer medium, and Z_0^a is the microstrip impedance with air as the dielectric.

By considering a 1-m-long line and 1-W incident power at the input of the line, the power available at the end of the line is given by

$$P = e^{-2\alpha_c} \tag{14.29}$$

The power absorbed (ΔP) in the line, due to conductor loss in the strip when 1W of power is incident, is given by

$$\Delta P_c = 1 - e^{-2\alpha_c} \qquad \text{(W/m)}$$

or

$$\Delta P_c = 0.2303\alpha_c \qquad \text{(W/m)} \tag{14.30}$$

where α_c (in decibels per meter), the attenuation coefficient due to loss in the strip conductor, is assumed small. The average density of heat flow q_c due to the conductor loss can be written

$$q_c = \frac{0.2303\alpha_c}{W_e} \qquad \text{(W/m}^2\text{)} \tag{14.31}$$

14.2.6.3 Density of Heat Flow Due to Dielectric Loss

In addition to the conductor loss, heat is generated by dielectric loss in the dielectric layers and the supporting substrate. The density of the heat generated is proportional to the square of the electric field. However, we can consider a parallel plate model wherein the electric field is uniform and the density of the

heat generated can also be considered uniform. This assumption ignores the increased dielectric loss in regions of high electric field near the strip edges. However, because in most applications the dielectric loss is a small fraction of the total loss (except for semiconductor substrates like Si or at millimeter-wave frequencies), the above assumption should hold. The effective width for this parallel plate waveguide model depends on the spread of electric field lines and is a function of frequency. Here, as a first-order approximation, no dispersion is included, and the effective width given in (14.28) can also be used here.

The heat flow in the y-direction caused by a sheet of heat sources due to dielectric loss can be evaluated by considering the configuration in Figure 14.9. Here the parallel plate waveguide model is used to calculate the volume for total heat generated; however, in such calculations, the top conductor is replaced by an air–dielectric interface. The heat conducted away by air is negligible, and the air–dielectric boundary can be considered as an insulating wall (corresponding to a magnetic wall in the electric analog). Therefore, the configuration is modified by removing the insulating wall and incorporating an image source of heat and an image of the ground plane as shown in Figure 14.9. The space between the two ground planes is filled by a dielectric media. Now the heat flow at a point A is obtained by applying the divergence theorem (for heat flow field) to the volume shown by the dotted lines, that is,

$$\iiint (\nabla \cdot q_d)\, dv = \oiint_s q_d \cdot ds = \iiint \rho_h\, dv \tag{14.32}$$

where s is the enclosed area, and q_d and ρ_h are the density of heat flow due to dielectric loss and heat generated by the dielectric loss, respectively. The total q_d at $y = y_1$ is contributed by the heat sources lying between $y = y_1$ and

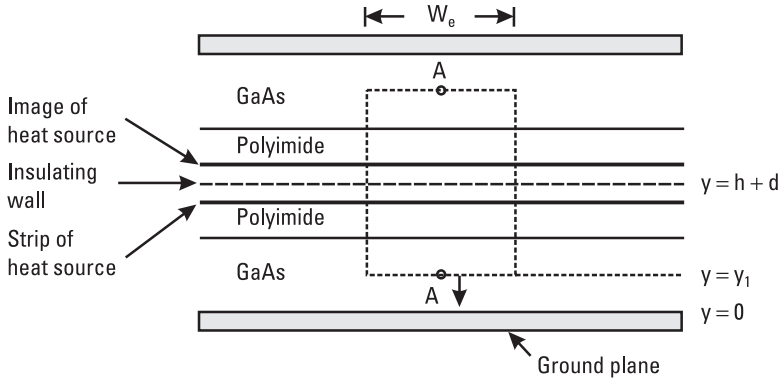


Figure 14.9 Line geometry for calculating the density of heat flow due to dielectric loss in a multilayer microstrip.

$y = h' = h + d$ (and their images). Note that sources located at $y < y_1$ (and their images) do not contribute to the heat flow at $y = y_1$. Thus,

$$q_d(y) = -(h' - y)\rho_h \tag{14.33}$$

The negative sign implies that the heat flow is in the $-y$-direction (for $y < h'$). If ΔP_d and α_d (in decibels per meter) are power absorbed and the attenuation coefficient due to dielectric loss, respectively, the density of heat generated, ρ_h, can be written

$$\rho_h = \frac{\Delta P_d}{W_e h'} = \frac{0.2303\alpha_d}{W_e h'} \tag{14.34}$$

This assumes that the heat is being generated uniformly in the parallel plate waveguide model.

From (14.33) and (14.34)

$$q_d(y) = -\frac{0.2303\alpha_d}{W_e}(1 - y/h') \tag{14.35}$$

14.2.6.4 Temperature Rise

The total density of the heat flow due to conductor and dielectric losses can be expressed in terms of a temperature gradient as

$$q = q_c + q_d(y) = -K\frac{\partial T}{\partial y} \tag{14.36}$$

where K is the thermal conductivity of the dielectric media. Therefore, the temperature at $y = h'$ (i.e., at the strip conductor) is given by

$$\begin{aligned} T &= 0.2303 \int_0^{h'} \left\{ \frac{\alpha_c}{W_e K} + \frac{\alpha_d}{W_e K}(1 - y/h') \right\} dy + T_{\text{amb}} \\ &= 0.2303 \left[\int_0^{h} \frac{\alpha_c}{W_e K_g}\, dy + \int_h^{h+d} \frac{\alpha_c}{W_e K_p}\, dy + \int_0^{h} \frac{\alpha_d}{W_e K_g}\left(1 - \frac{y}{h+d}\right) dy \right. \\ &\qquad \left. + \int_h^{h+d} \frac{\alpha_d}{W_e K_p}\left(1 - \frac{y}{h+d}\right) dy \right] + T_{\text{amb}} \end{aligned} \tag{14.37}$$

where T_{amb} is the ambient temperature. The corresponding rise in temperature is

$$\Delta T = T - T_{amb} \tag{14.38}$$

$$= 0.2303\left[\alpha_c\left(\frac{h}{W_e K_g} + \frac{d}{W_e K_p}\right) + \alpha_d\left(\frac{h(h+2d)}{2W_e K_g(h+d)} + \frac{d^2}{W_e K_p(h+d)}\right)\right]$$

where K_g and K_p are the thermal conductivities of the GaAs substrate and polyimide layer, respectively. This relation is used for calculating the average power-handling capability of the microstrip line. Following the procedure discussed earlier for the two-layered microstrip line, this analysis can be extended to multilayered microstrip lines.

14.2.6.5 Average Power-Handling Capability

The maximum average power, P_{avg}, for a given line can be calculated from

$$P_{avg} = (T_{max} - T_{amb})/\Delta T \tag{14.39}$$

where ΔT denotes rise in temperature per watt and T_{max} is the maximum operating temperature. The maximum operating temperature of microstrip circuits is limited due to (1) change of substrate properties with temperature, (2) change of physical dimensions with temperature, and (3) connectors. One can assume the maximum operating temperature of a microstrip circuit to be the one at which its electrical and physical characteristics remain unchanged.

The conductor loss consists of two parts: the strip conductor loss and the ground plane conductor loss. Conductor loss in the ground plane does not contribute to APHC limitation. However, because the ground plane loss is very small compared to the strip loss [1], formulas for the total loss could be used to calculate APHC. The properties of various substrate and conductor materials [22] are given in Tables 14.8 and Table 14.9, respectively.

For T_{max} = 150°C, T_{amb} = 25°C, and Z_0 = 50Ω, values of APHC for various substrates at 10 GHz are calculated and given in Table 14.10. Among the dielectrics considered, APHC is the lowest for Duroid (0.144 kW) and it is at a maximum for BeO (52.774 kW). For commonly used alumina (or sapphire) substrates, a 50Ω microstrip can carry about 4.63 kW of CW power at 10 GHz.

Table 14.11 shows the APHC of several multilayer 50-Ω microstrip lines on 75-μm-thick GaAs at several frequencies; note that the APHC decreases with increasing frequency. Lines having characteristic impedances higher than 50Ω will have lower APHC values as given in Table 14.5 due to higher loss and narrower line widths.

Table 14.8
Properties of Various Dielectric Materials at 10 GHz and 25°C

Material	Dielectric Constant, ϵ_r	Loss Tangent tan δ ($\times 10^{-4}$)	Thermal Conductivity K (W/m-°C)
Alumina (Al_2O_3)	9.8	2	37.0
Sapphire	11.7	1	46.0
Quartz	3.8	1	1.0
Si ($\rho = 10^3$ Ω-cm)	11.7	>50	145.0
GaAs ($\rho = 10^8$ Ω-cm)	12.9	5	46.0
InP	14.0	5	68.0
AlN	8.8	5*	230.0
BeO	6.7*	40	260.0
SiC	40.0	>50	270.0
Polyimide	3.0	10	0.2
Teflon	2.1	5	0.1
Duroid	2.2	9	0.26
Air	1.0	0	0.024

*At 1 MHz.

Table 14.9
Properties of Various Conductor Materials [22]

Metal	Melting Point (°C)	Electrical Resistivity (10^{-6} (Ω-cm)	Thermal Expansion Coefficient (10^{-6}/°C)	Thermal Conductivity (W/m-°C)
Copper	1,093	1.7	17.0	393
Silver	960	1.6	19.7	418
Gold	1,063	2.4	14.2	297
Tungsten	3,415	5.5	4.5	200
Molybdenum	2,625	5.2	5.0	146
Platinum	1,774	10.6	9.0	71
Palladium	1,552	10.8	11.0	70
Nickel	1,455	6.8	13.3	92
Chromium	1,900	20.0	6.3	66
Kovar	1,450	50.0	5.3	17
Aluminum	660	4.3	23.0	240
Au–20% Sn	280	16.0	15.9	57
Pb–5% Sn	310	19.0	29.0	63
Cu–W(20% Cu)	1,083	2.5	7.0	248
Cu–Mo(20% Cu)	1,083	2.4	7.2	197

Table 14.10
Comparison of APHC of 50Ω Microstrip Lines on Various Substrates at 10 GHz*

Substrate	ϵ_r	tan δ	h (μm)	W (μm)	ΔT (°C/W)	Maximum Average Power (kW)
Duroid	2.2	0.0009	250	760	0.8682	0.144
Si	11.7	0.1540	100	75	0.126	0.992
GaAs	12.9	0.0010	75	50	0.0865	1.445
Al_2O_3	9.8	0.0002	250	235	0.027	4.630
BeO	6.4	0.0003	250	352	0.00237	52.774

Gold conductors are 4.5 μm thick, $d = 0$, and $T_{amb} = 25°C$.

Table 14.11
Comparison of APHC of 50Ω Multilayer Microstrip Lines on 75-μm-Thick GaAs*

Polyimide Thickness d (μm)	Maximum Average Power (W) 5 GHz	10 GHz	20 GHz	40 GHz
0	2,049	1,445	1,020	720
1	260	181	129	91
3	107	76	53	38
7	71	51	36	25
10	63	44	31	22

*Gold conductors are 4.5 μm thick except in 3-μm polyimide case, where $t = 9$ μm and $\epsilon_{rd} = 3.2$.

Figures 14.10, 14.11, and 14.12 show the variation of APHC as a function of line width at 5, 10, 20, and 40 GHz for polyimide thicknesses of $d = 3$, 7, and 10 μm, respectively. As frequency increases from 5 to 40 GHz, the APHC values decrease by a factor of about 3 due to higher losses; also, as expected, APHC increases monotonically with line width and decreases with polyimide thickness.

14.2.6.6 Practical Considerations

The calculations presented above hold good for matched lines. If a transmission line is not matched to its characteristic impedance, the power distribution becomes nonuniform along the line due to standing waves that cause nonuniform heat dissipation. For example, when sections of transmission lines are used in passive components and matching networks, the APHC of each section will depend on the standing waves on that line section. The APHC of a long line

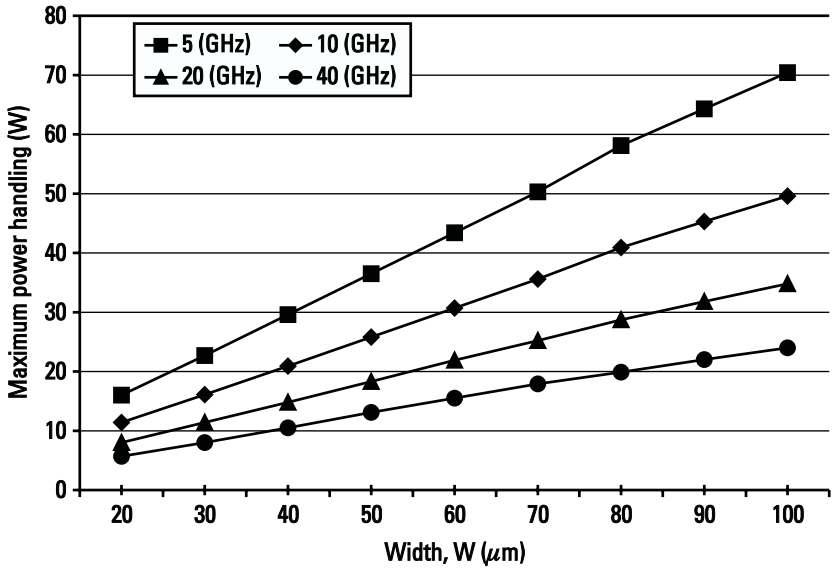


Figure 14.10 Variation of maximum power-handling capability of multilayer microstrip lines when the polyimide thickness is 3 μm.

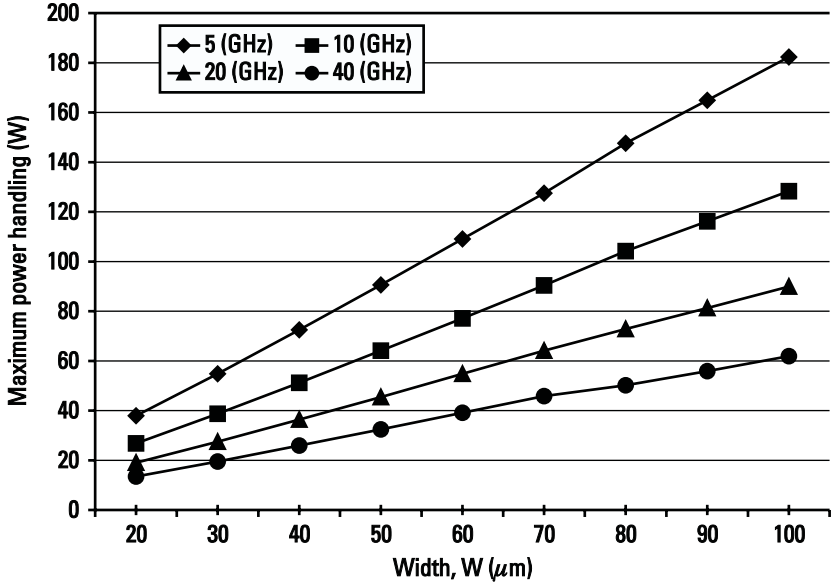


Figure 14.11 Variation of maximum power-handling capability of multilayer microstrip lines when the polyimide thickness is 7 μm.

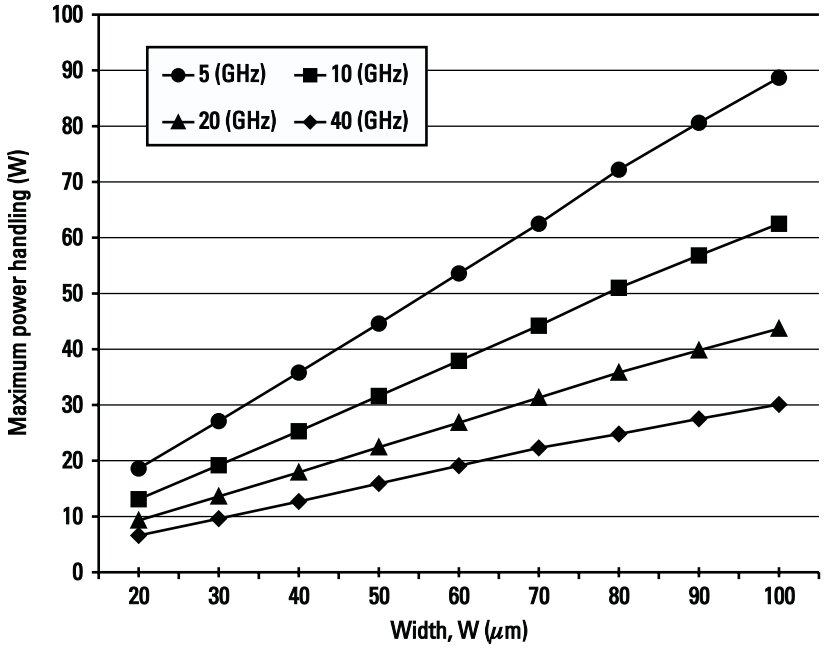


Figure 14.12 Variation of maximum power-handling capability of multilayer microstrip lines when the polyimide thickness is 10 μm.

is determined at the input point of the line where the RF/microwave signal enters and the signal is strongest.

Consider a microstrip line of length L and attenuation constant α as shown in Figure 14.13. If S_i is the VSWR at the input and S_o is the VSWR at the output, they are related by the following relation [23]:

$$S_i = \frac{S_o + 1 + (S_o - 1)\,e^{-2\alpha L}}{S_o + 1 - (S_o - 1)\,e^{-2\alpha L}} \tag{14.40}$$

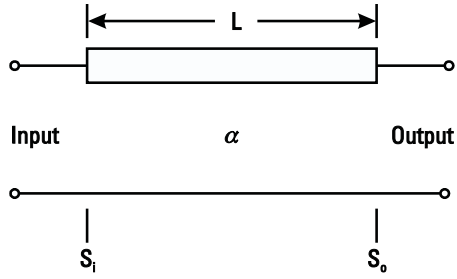


Figure 14.13 A microstrip line section representation.

For $\alpha L << 1$,

$$S_i = \frac{S_o(1 + \alpha L)}{1 + S_o \alpha L} \tag{14.41}$$

The factor $(1 + \alpha L)/(1 + S_o \alpha L)$ is always less than unity, therefore, S_i is less than S_o and thus in the worst case $S_i \cong S_o$. The attenuation constant for the unmatched line, α_m, is given by [23]

$$\alpha_m = \alpha[2(S_i^2 + 1)/(S_i + 1)^2] \tag{14.42a}$$

Thus, for the worst-case condition, when the output end of the line is short circuited or open circuited ($S_o \cong \infty$), α_m becomes

$$\alpha_m = 2\alpha \tag{14.42b}$$

Therefore, in a worst-case condition, the calculations presented in the previous section can be derated by a factor 2. Table 14.12 shows derating coefficient γ calculated using (14.42) and increased ambient temperature. This means that when the line is not matched to its characteristic impedance and the ambient temperature is greater than 25°C, the calculated APHC values should be reduced by γ factor.

If the case temperature is about 60°C and the circuits have short-circuited lines, the derating factor for such lines is about 2.78. This means that at 10

Table 14.12
APHC Derating Coefficient γ Calculated as a Function of VSWR at Various Ambient Temperatures

VSWR	T_{amb} = 25°C	T_{amb} = 60°C	T_{amb} = 80°C
1	1.00	1.39	1.79
2	1.11	1.54	1.98
3	1.25	1.74	2.23
4	1.36	1.89	2.43
5	1.44	2.00	2.57
6	1.51	2.10	2.70
7	1.56	2.17	2.79
8	1.61	2.24	2.88
9	1.64	2.28	2.93
10	1.67	2.32	2.98
20	1.82	2.53	3.25
∞	2.00	2.78	3.57

GHz, the maximum average power-handling values of a 30-μm-wide multilayer microstrip lines are 312, 13.9, 6.9, and 5.8W for polyimide thicknesses of 0, 3, 7, and 10 μm, respectively.

14.2.6.7 Peak Power-Handling Capability

The calculation of peak power-handling capability of microstrip lines is more complicated. The peak voltage that can be applied without causing dielectric breakdown determines the *peak power-handling capability* (PPHC) of the microstrip. If Z_0 is the characteristic impedance of the microstrip and V_0 is the maximum voltage the line can withstand, the maximum peak power is given by

$$P_p = \frac{V_0^2}{2Z_0} \tag{14.43}$$

Thick substrates can support higher voltages (for the same breakdown field). Therefore, low impedance lines and lines on thick substrates have higher PPHC.

The sharp edges of a strip conductor serve as field concentrators. The electric field tends to a large value at the sharp edges of the conductor if it is a flat strip and decreases as the edge of the conductor is rounded off more and more. Therefore, thick and rounded strip conductors will increase breakdown voltage.

The dielectric strengths of the substrate material as well as of the air play important roles. The breakdown strength of dry air is approximately 30 kV/cm. Thus the maximum (tangential) electric field near the strip edge should be less than 30 kV/cm. To avoid air breakdown near the strip edge, the edge of the strip conductor can be painted with a dielectric paint that has the same dielectric constant as that of the substrate and is lossless or by using an overlay of silicon rubber as discussed in Section 7.2.5. An additional factor, which may reduce PPHC, is the effect of internal mismatches.

14.3 Coupled Microstrip Lines

Inductors and transformers can be analyzed using coupled microstrip line theory. The theory of such structures has been treated in a recently published book [22]. Coupled microstrip structures are characterized by characteristic impedances (or admittances) and phase velocities (or effective dielectric constants) for the two modes known as even and odd. Design equations given later for coupled lines relate mode impedances and effective dielectric constants to the coupled line geometry, that is, strip width, spacing S between the strips, dielectric thickness

h, and dielectric constant ϵ_r. One can write design equations for these characteristics directly in terms of static capacitances for the coupled line geometry. Even- and odd-mode capacitances for the symmetric two-conductor coupled lines shown in Figure 14.14 are obtained first.

14.3.1 Even-Mode Capacitance

As shown in Figure 14.14(a), the even-mode capacitance C_e can be divided into three capacitances:

$$C_e = C_p + C_f + C_f' \tag{14.44}$$

where C_p denotes the parallel plate capacitance between the strip and the ground plane, and C_f is the fringe capacitance at the outer edge of the strip. It is the

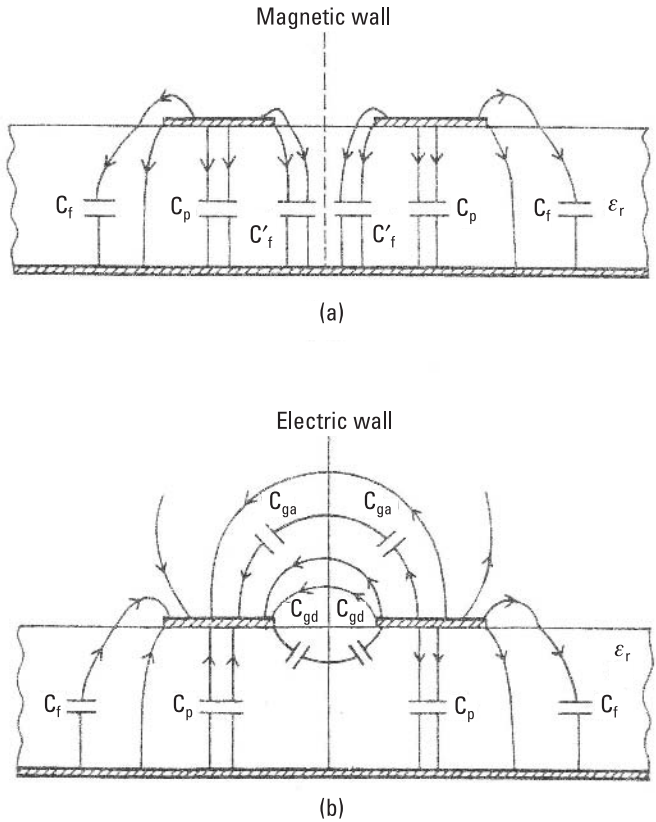


Figure 14.14 Analysis of coupled microstrip lines in terms of capacitances: (a) even-mode capacitance and (b) odd-mode capacitance.

fringe capacitance of a single microstrip line and can be evaluated from the capacitance of the microstrip line and the value of C_p. The term C_f' accounts for the modification of fringe capacitance C_f of a single line due to the presence of another line. Expressions for C_p, C_f, and C_f' are given here [1, 24]:

$$C = \epsilon_0 \epsilon_r W/h \tag{14.45a}$$

$$2C_f = \sqrt{\epsilon_{re}}/(cZ_0) - \epsilon_0 \epsilon_r W/h \tag{14.45b}$$

and

$$C_f' = \frac{C_f}{1 + A(h/S)\ \tanh(10S/h)} \left(\frac{\epsilon_r}{\epsilon_{re}}\right)^{1/4} \tag{14.45c}$$

where

$$A = \exp[-0.1\ \exp(2.33 - 1.5W/h)] \tag{14.45d}$$

The capacitances obtained by using the preceding design equations were compared with those obtained from [25]. The values are found to be accurate to within 3% over the following range of parameters:

$$0.1 \le W/h \le 10 \qquad 0.1 \le S/h \le 5 \qquad 1 \le \epsilon_r \le 18$$

14.3.2 Odd-Mode Capacitance

Odd-mode capacitance C_o can be decomposed into four constituents: C_f, C_p, C_{gd}, and C_{ga} as shown in Figure 14.14(b); that is,

$$C_o = C_f + C_p + C_{gd} + C_{ga} \tag{14.46}$$

Expressions for C_f and C_p are the same as those given earlier in the case of C_e. Capacitance C_{ga} describes the gap capacitance in air. Its value can be obtained from the capacitance of a slotline of width W with air as dielectric as given below:

$$C_{ga} = \epsilon_0 \frac{K(k')}{K(k)}, \quad k = \frac{S}{S + 2W}, \quad \text{and} \quad k' = \sqrt{1 - k^2} \tag{14.47a}$$

where $K(k)$ and $K(k')$ denote the elliptic function and its complement. Use of simplified expressions for $K(k')/K(k)$ yields the following value for C_{ga}:

$$C_{ga} = \begin{cases} \dfrac{\epsilon_0}{\pi} \ln\left\{2\dfrac{1+\sqrt{k'}}{1-\sqrt{k'}}\right\} & \text{for } 0 \le k^2 \le 0.5 \\ \pi\epsilon_0 / \ln\left\{2\dfrac{1+\sqrt{k}}{1-\sqrt{k}}\right\} & \text{for } 0.5 \le k^2 \le 1 \end{cases} \tag{14.47b}$$

The last term C_{gd} represents the capacitance value due to the electric flux in the dielectric region and its value is evaluated as follows:

$$C_{gd} = \frac{\epsilon_0 \epsilon_r}{\pi} \ln \coth\left(\frac{\pi S}{4h}\right) + 0.65 C_f \left\{\frac{0.02}{S/h}\sqrt{\epsilon_r} + \left(1 - \frac{1}{\epsilon_r^2}\right)\right\} \tag{14.48}$$

The first term in (14.48) is obtained from coupled stripline geometry. The second term represents its modification for coupled microstrip.

14.3.3 Characteristic Impedances

Characteristic impedances Z_{0e} and Z_{0o} can be obtained by using the following relationships:

$$Z_{0e} = \left[c\sqrt{C_e^a C_e}\right]^{-1} \tag{14.49a}$$

$$Z_{0o} = \left[c\sqrt{C_o^a C_o}\right]^{-1} \tag{14.49b}$$

where C_e^a and C_o^a are even- and odd-mode capacitances for the coupled microstrip configuration with air as the dielectric.

The values of impedances obtained by using the preceding design equations have an error of less than 3% for the parameters lying in the range $\epsilon_r \le 18$, $0.1 \le W/h \le 2$, and $0.05 \le S/h \le 2$.

14.3.4 Effective Dielectric Constants

Effective dielectric constants ϵ_{ree} and ϵ_{reo} for even and odd modes, respectively, can be obtained from C_e and C_o by these relations:

$$\epsilon_{ree} = C_e / C_e^a \tag{14.50a}$$

$$\epsilon_{reo} = C_o / C_o^a \tag{14.50b}$$

More accurate values of capacitances can be obtained from the closed-form expressions reported by Kirschning and Jansen [25].

14.4 Microstrip Discontinuities

Various types of discontinuities that occur in the conductor of planar transmission lines, such as microstrips, are shown in Figure 14.15. Examples of circuits

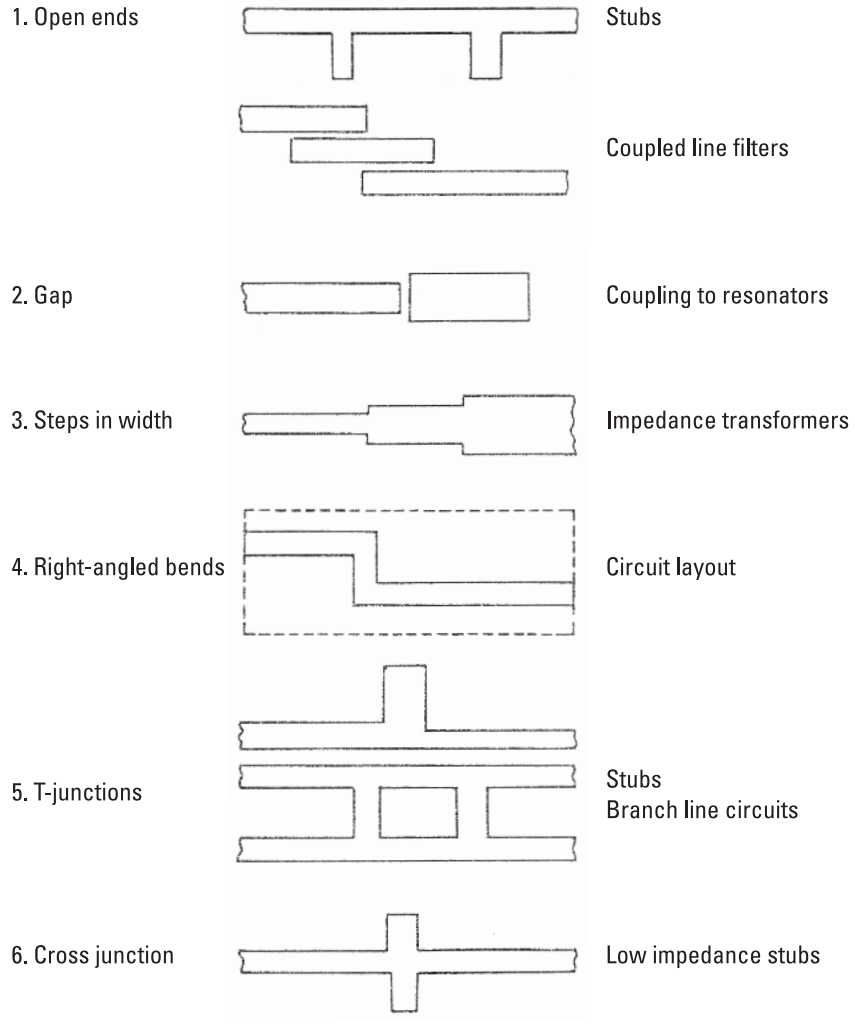


Figure 14.15 Typical planar strip transmission-line discontinuities.

and circuit elements, wherein these discontinuities are frequently encountered, are also shown in this figure.

A complete understanding of the design of MICs requires characterization of the discontinuities present in these circuits. Approximate closed-form expressions for various discontinuity elements are given in [1].

14.5 Compensated Microstrip Discontinuities

In MIC designs, microstrip discontinuities should either be taken into account or microstrip structures with compensated discontinuities should be used. In general, compensated discontinuities improve circuit performance and the bandwidth. Usually chamfered bends or rounded corners are used in MICs and MMICs. The chamfered discontinuity technique is also known as *discontinuity compensation* in which the discontinuity reactances are minimized by removing appropriate portions of the microstrip conductor near the discontinuity location. In this section, we describe briefly the step-in-width, right-angled bend, and T-junction compensated microstrip discontinuities.

14.5.1 Step-in-Width

Compensation of a step discontinuity has been reported [1, 26–31] using appropriate tapers. In this case the effect of discontinuity reactances is reduced by chamfering the large width. The taper length depends on the step ratio, dielectric constant value, and the substrate thickness h. For $h/\lambda \leq 0.01$ and a step ratio of less than 3, the step discontinuity reactance is negligible and generally no compensation technique is needed. Figure 14.16 shows three types of tapers. The taper shown in Figure 14.16(a) has been studied using a planar waveguide model, which was described in Section 14.2.6. For a gradual taper, shown in Figure 14.16(b), closed-form expressions for the contour of a taper compensating step discontinuity in microstrip lines is given by Raicu [29]. For

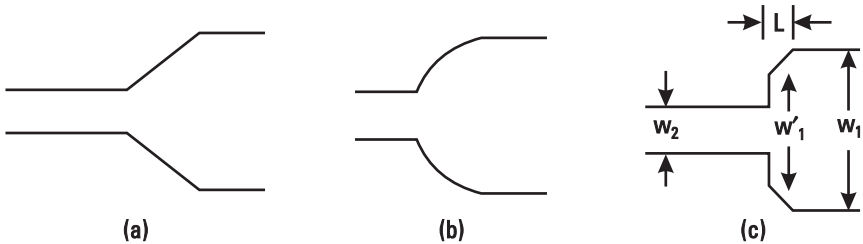


Figure 14.16 Three different kinds of compensated step-in-width discontinuity configurations: (a) linear taper, (b) curved taper, and (c) partial linear taper.

a partial taper, shown in Figure 14.16(c), discontinuity compensation on the 75- to 125-μm-thick GaAs substrate using a commercial full-wave analysis CAD tool was performed. For a step width ratio ranging from 3 to 13, the step discontinuity reactance is negligible when $L = W_1/8$ and $W_1' = 0.33W_1$.

14.5.2 Chamfered Bend

Data on the optimum amount of chamfering in a microstrip bend have been given in [30] as follows:

$$M = 52 + 65 \exp(-1.35W/h) \tag{14.51}$$

for $W/h \geq 0.25$ and $\epsilon_r \leq 25$, where M is the percentage chamfer given by $(X/d) \times 100\%$ with X and d shown in Figure 14.17. For a chamfered bend, the reflection coefficient $S_{11} \sim 0$, when the transmission line is terminated by an impedance equal to its characteristic impedance, but the discontinuity reactances cause a reduction Δb in length compared to that measured along the centerlines of the microstrip lines. A closed-form expression for this reduction in length can be written [31]

$$\Delta b/D = 0.16\{2 - (f/f_p)^2\} \tag{14.52}$$

where D and f_p are given by

$$D = 120\pi h/\left(\sqrt{\epsilon_{re}} Z_0\right)$$

$$f_p = 0.4Z_0/h$$

where f_p and h are in gigahertz and millimeters, respectively.

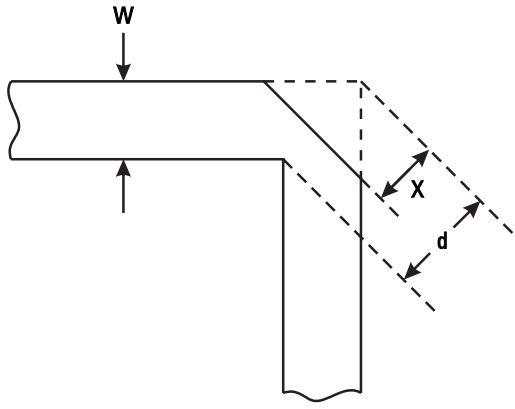


Figure 14.17 Geometry of a chamfered bend.

Several other types of chamfering, as shown in Figure 14.18, have been studied and optimum chamfer dimensions are also given. Figure 14.19 compares calculated S_{11} for uncompensated right-angled bend discontinuity with compensated topologies. We note that the configuration shown in Figure 14.18(c) provides the best compensation for this example.

14.5.3 T-Junction

T-junction discontinuity compensation is much more difficult than the step-in-width and right-angled bend discontinuity compensation techniques described in previous subsections. Figure 14.20(a) shows T-junction compensation configura-

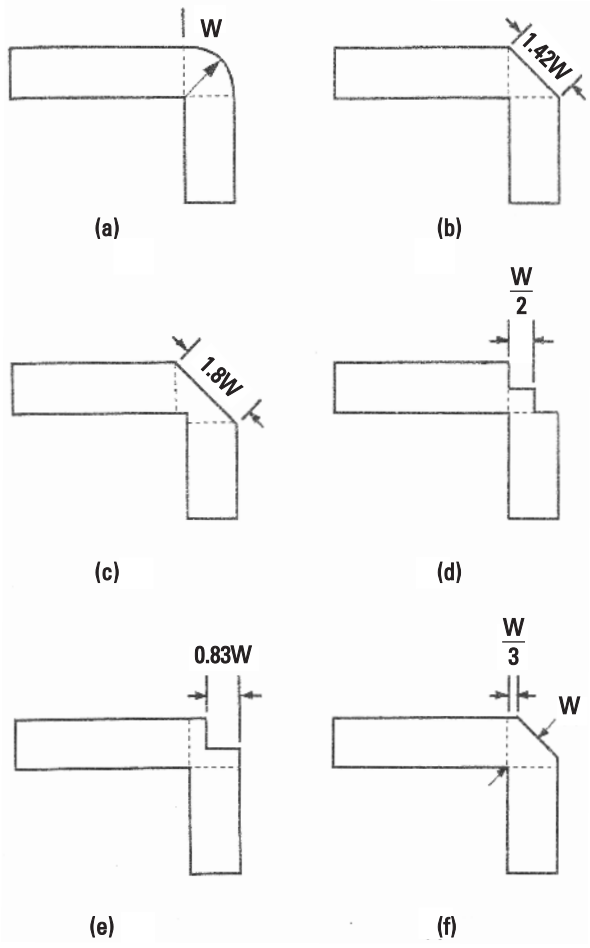


Figure 14.18 (a–f) Six different configurations for compensated right-angled bends.

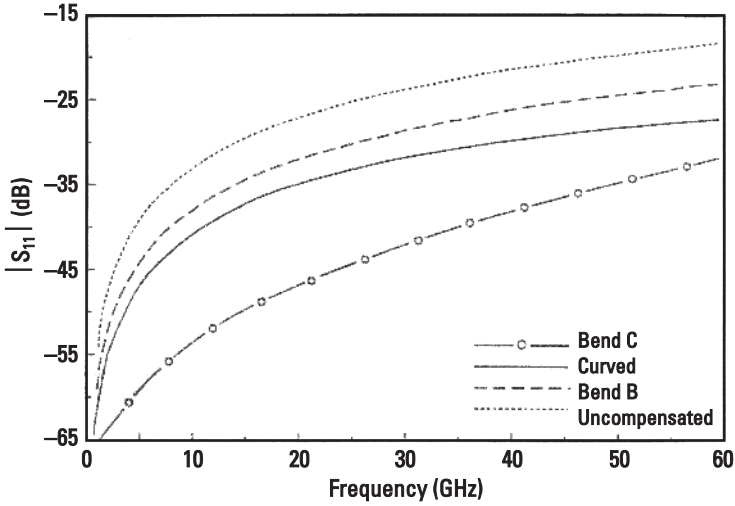


Figure 14.19 Magnitude of the reflection coefficient as a function of frequency for several compensated and uncompensated right-angled bends: $W = 73\ \mu$m, $h = 100\ \mu$m, $\epsilon_r = 12.9$, and the curved line has a mean radius = 220.

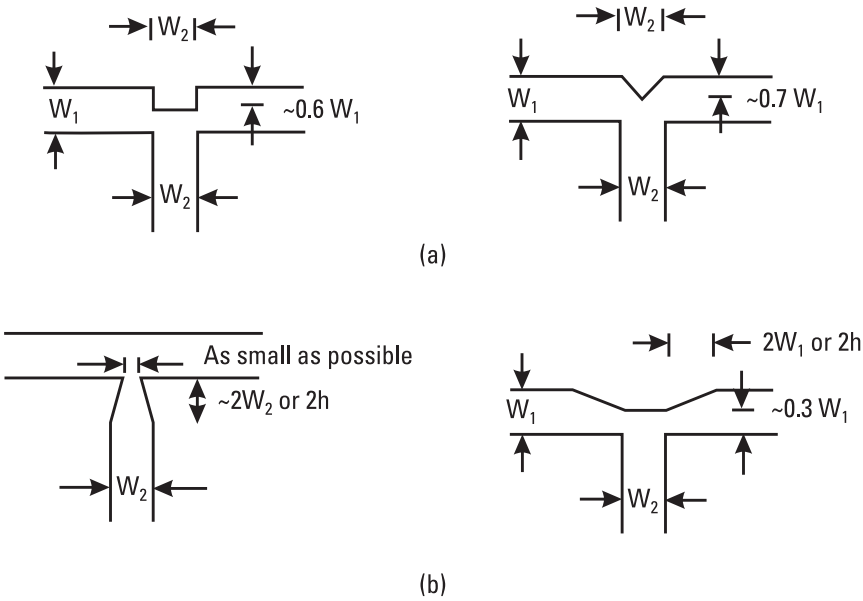


Figure 14.20 (a) T-junction discontinuity compensation configurations and (b) minimized T-junction discontinuity effect configuration.

tions using rectangular and triangular notches and their approximate dimensions for $h/\lambda << 1$. However, accurate compensation depends on line widths, dielectric constant, and the substrate thickness. Figure 14.20(b) illustrates T-junction discontinuity minimization configurations in which the line widths are tapered to minimize the junction effect. In this case the taper length is about twice the line width or substrate thickness whichever is larger, and the tapered length becomes a part of the design parameter.

References

[1] Gupta, K. C., et al., *Microstrip Lines and Slotlines,* 2nd ed., Norwood, MA: Artech House, 1996.

[2] Wheeler, H. A., "Transmission Line Properties of Parallel Strips Separated by a Dielectric Sheet," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-13, March 1965, pp. 172–185; see also Wheeler, H. A., "Transmission Line Properties of a Strip on a Dielectric Sheet on a Plane," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-25, August 1977, pp. 631–647.

[3] Vendelin, G. D., "Limitations on Stripline Q," *Microwave J.,* Vol. 13, May 1970, pp. 63–69.

[4] Hammerstad, E. O., "Equations for Microstrip Circuit Design," *Proc. European Microwave Conf.,* 1975, pp. 268–272.

[5] Bahl, I. J., and D. K. Trivedi, "A Designer's Guide to Microstrip Line," *Microwaves,* Vol. 16, May 1977, pp. 174–182.

[6] Bahl, I. J., "Easy and Exact Methods for Shielded Microstrip Design," *Microwaves,* Vol. 17, December 1978, pp. 61–62.

[7] Bahl, I. J., and K. C. Gupta, "Average Power Handling Capability of Microstrip Lines," *IEEE J. Microwaves, Optics and Acoustics,* Vol. 3, January 1979, pp. 1–4.

[8] Garg R., "Microstrip Design Guides," *Int. J. Electronics,* Vol. 46, 1979, pp. 187–192.

[9] Denlinger, E. J., "Losses in Microstrip Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-28, June 1980, pp. 513–522.

[10] Hammerstad, E., and O. Jensen, "Accurate Models for Microstrip Computer-Aided Design," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1980, pp. 407–409.

[11] March, S. L., "Empirical Formulas for the Impedance and Effective Dielectric Constant of Covered Microstrip for Use in the Computer-Aided Design of Microwave Integrated Circuits," *Proc. European Microwave Conf.,* Kent, England: Microwave Exhibitors & Publishers Ltd., 1981, pp. 671–676.

[12] Kobayashi, M., "A Dispersion Formula Satisfying Recent Requirements in Microstrip CAD," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-36, August 1988, pp. 1246–1250.

[13] Bahl, I. J., and K. C. Gupta, "Average Power-Handling Capability of Microstrip Lines," *IEEE J. Microwaves, Optics and Acoustics,* Vol. 3, January 1979, pp. 1–4.

[14] Sturdivant, R., and T. Theisen, "Heat Dissipating Transmission Lines," *Applied Microwave and Wireless,* Vol. 7, Spring 1995, pp. 57–63.

[15] Parnes, M., "The Correlation Between Thermal Resistance and Characteristic Impedance of Microwave Transmission Lines," *Microwave J.,* Vol. 43, March 2000, pp. 82–94.

[16] Toyoda, I., T. Tokumitsu, and M. Aikawa, "Highly Integrated Three-Dimensional MMIC Single-Chip Receiver and Transmitter," *IEEE Trans. Microwave Theory Tech.,* Vol. 44, December 1996, pp. 2340–2346.

[17] Nakatsugawa, M., et al., "Line-Loss and Size Reduction Techniques for Millimeter-Wave RF Front-End Boards by Using a Polyimide/Alumina-Ceramic Multilayer Configuration," *IEEE Trans. Microwave Theory Tech.,* Vol. 45, December 1997, pp. 2308–2315.

[18] Bahl, I. J., et al., "Low Loss Multilayer Microstrip Line for Monolithic Microwave Integrated Circuits Applications," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 8, November 1998, pp. 441–454.

[19] Bahl, I. J., "High Current Capacity Multilayer Inductors for RF and Microwave Circuits," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 10, March 2000, pp. 139–146.

[20] Bahl, I. J., "Average Power Handling Capability of Multilayer Microstrip Lines," *Int. J. RF and Microwave Computer-Aided Engineering,* Vol. 11, November 2001, pp. 385–395.

[21] Masana, F. N., "A Closed Form Solution of Junction of Substrate Thermal Resistance in Semiconductor Chips," *IEEE Trans. Components, Packaging, and Manufacturing Tech. Part A,* Vol. 19, December 1996, pp. 539–545.

[22] Mongia, R., I. Bahl, and P. Bhartia, *RF and Microwave Coupled-Line Circuits,* Norwood, MA: Artech House, 1999, pp. 499–500.

[23] Fuks, R., "Compute Power Rating for Unmatched Lines," *Microwaves and RF,* Vol. 37, October 1998, pp. 100–112.

[24] Garg, R., and I. J. Bahl, "Characteristics of Coupled Microstrip Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-27, 1979, pp. 700–705; see also Corrections, *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-28, 1980, p. 272.

[25] Kirschning, M., and R. H. Jansen, "Accurate Wide-Range Design Equations for Parallel Coupled Microstrip Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-32, 1984, pp. 83–90; see also Corrections, *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-33, 1985, p. 288.

[26] Malherbe, J. A. G., "The Compensation of Step Discontinuities in TEM-Mode Transmission Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-26, November 1978, pp. 883–885.

[27] Chadha, R., and K. C. Gupta, "Compensation of Discontinuities in Planar Transmission Lines," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-30, December 1982, pp. 2151–2156.

[28] Hoefer, W. J. R., "A Contour Formula for Compensated Microstrip Steps and Open Ends," *IEEE MTT-S Int. Microwave Symp. Dig.,* Boston, MA, 1983, pp. 524–526.

[29] Raicu, D., "Universal Taper for Compensation of Step Discontinuities in Microstrip Lines," *IEEE Microwave Guided Lett.,* Vol. 1, September 1991, pp. 249–251.

[30] Douville, R. J. P., and D. J. James, "Experimental Study of Symmetric Microstrip Bends and Their Compensation," *IEEE Trans. Microwave Theory Tech.,* Vol. MTT-26, 1978, pp. 175–182.

[31] Hammerstad, E., "Computer-Aided Design of Microstrip Couplers with Accurate Discontinuity Models," *IEEE MTT-S Int. Microwave Symp. Dig.,* 1981, pp. 54–56.

Appendix

Physical Constants

Permittivity of vacuum, $\epsilon_0 = 8.854 \times 10^{-12} \cong (1/36\pi) \times 10^{-9}$ F/m
Permeability of vacuum, $\mu_0 = 4\pi \times 10^{-7}$ H/m
Impedance of free space, $\eta_0 = 376.7 \cong 120\pi\Omega$
Velocity of light, $c = 2.998 \times 10^{8}$ m/sec
Charge of electron, $e = 1.602 \times 10^{-19}$ C
Mass of electron, $m = 9.107 \times 10^{-31}$ kg
Boltzmann's constant, $k = 1.380 \times 10^{-23}$ J/K
Planck's constant, $h = 6.547 \times 10^{-34}$ J-sec

About the Author

Inder Bahl received a Ph.D. in electrical engineering from the Indian Institute of Technology (ITT), Kanpur, India, in 1975. From 1969 to 1981, Dr. Bahl held positions at IIT Kanpur, the Ottawa University, and the Defense Research Establishment, Ottawa, Canada. He joined the ITT Gallium Arsenide Technology Center in 1981 and worked on microwave and millimeter wave GaAs ICs. At M/A-COM (formerly ITT GTC), in his present capacity as a Distinguished Fellow of Technology, his interests are in the area of device modeling, high efficiency high-power amplifiers, high-power limiter/LNAs, three-dimensional MMICs, and the development of MMIC products for commercial and military applications.

Dr. Bahl is the author or coauthor of more than 140 research papers. He has authored, coauthored, or edited eleven books: *Microstrip Lines and Slotlines* (Artech House, 1979); *Microstrip Antennas* (Artech House, 1980); *Millimeter Wave Engineering and Applications* (John Wiley, 1984); *Microwave Solid State Circuit Design* (John Wiley, 1988); *Microwave and Milllimeter-Wave Heterostructure Transistors and Their Applications* (Artech House, 1989), *Gallium Arsenide IC Applications Handbook* (Academic Press, 1995); *Microstrip Lines and Slotlines, Second Edition* (Artech House, 1996); *RF and Microwave Coupled-Line Circuits* (Artech House, 1999); *Microstrip Antenna Design Handbook* (Artech House, 2001), *RF and Microwave Circuit and Component Design for Wireless Systems* (John Wiley, 2002); and *Microwave Solid State Circuit Design, Second Edition* (John Wiley, 2003). He has also contributed chapters to *Handbook of Microwave and Optical Components* (John Wiley, 1990); *Handbook of Electrical Engineering* (CRC Press, 1997); and *Wiley Encyclopedia of Electrical and Electronics*

Engineering, Vol. 13 (John Wiley, 1999). He holds 15 patents in the areas of microstrip antennas and microwave circuits.

Dr. Bahl is an IEEE fellow and a member of the Electromagnetic Academy. He is also an associate editor of the *International Journal of RF and Microwave Computer-Aided Engineering.*

Index