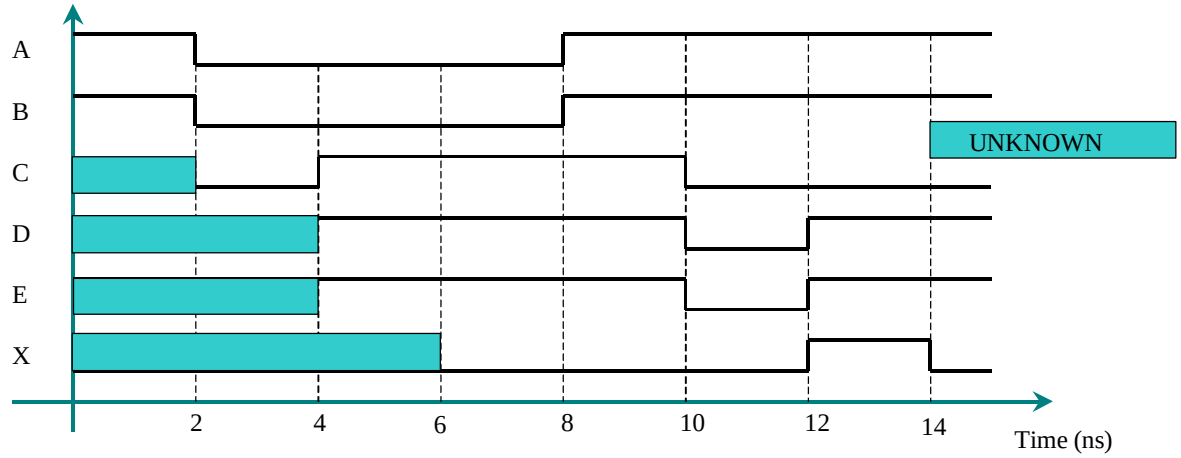
DOC Course 112: Hardware: Tutorial 4 Solution

1.

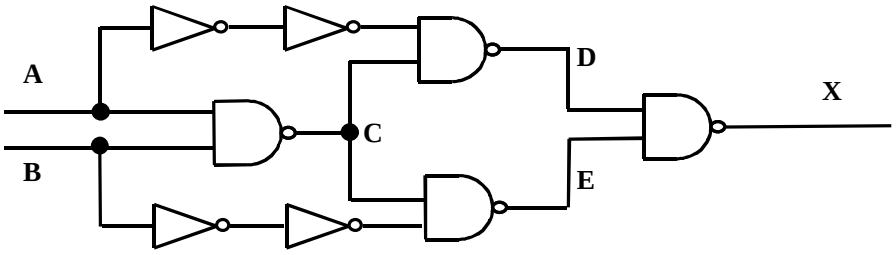
A	B	C	D	E	X
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

It is the exclusive or circuit.

2.



3.



If the invertor delay was exactly 1ns then this would be Ok, but no two invertors are identical, so there will still be a spike though much shorter than before.

4.

The key observation to make is that the gate capacitances will add when we connect gates in parallel (fan-out). So, if the input capacitance for a gate is C, then in the first circuit the invertor has to supply a total capacitance of 8*C. Taking the equation from lecture 5, for the change of a gates input voltage with time we have:

$$V = 5(1- \exp(-t/RC))$$

So, if in practice we can take V=1 for the point where the gate has definitely switched then we can calculate the time taken to switch as:

$$5\exp(-t/RC) = 4 \qquad \exp(t/RC) = 5/4 \qquad t = R\ C \log(5/4)$$

so, the time taken to switch when there are eight capacitors to charge will be $t= 8RC\log(5/4)$. Now consider the second circuit. At each stage a single invertor drives just two invertors (or two nand gates at the last stage) so the time delay associated with each stage is $2RC \log(5/4)$, and so the total delay for the second circuit is: $6RC\text{Log}(5/4)$. Making the assumption that Cnand=Cint (which is reasonable) the second circuit is faster.