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HTS JOSEPHSON JUNCTION DEVELOPMENT

Josephson junctions are the fundamental building blocks for a variety of superconducting electronics applications, including high-speed, low-power digital logic, and sensitive magnetic field and high-frequency electromagnetic detectors. A Josephson junction consists of a "weak" connection between two superconductors which exhibits the Josephson effects (described below). While low-temperature superconductor (*LTS*) Josephson junction technology is well-developed, high-temperature superconductor (*HTS*) Josephson junctions are still relatively immature. Nonetheless, extensive HTS junction fabrication efforts are in progress due to the possibility of applying Josephson effects at temperatures compatible with reliable, low-cost refrigerators. In this article we discuss the more common approaches to HTS junction fabrication and optimization, with a focus on potential digital circuit applications.

Introduction to Josephson Junctions

According to the Bardeen–Cooper–Schreiffer (*BCS*) theory of superconductivity, the electrons in a superconductor are weakly bound into Cooper pairs and can be described mathematically by a complex wave function with spatially dependent amplitude and phase. The fact that all of these electrons occupy a macroscopic quantum state leads to several profound properties of superconductivity, such as zero resistance, quantization of the magnetic flux threading a hole in a superconductor, and the Josephson effects.

If two pieces of superconductor, each characterized by their own wave function, are brought very close together, but separated by a thin insulating layer, then the two wave functions can overlap. It was predicted by Brian Josephson (1) that this overlap would lead to novel phenomena associated with the dissipationless tunneling of Cooper pairs through the insulating barrier. The first of these, the direct current (*dc*) Josephson effect, is that a dc current can flow through this "Josephson junction" without the appearance of a voltage drop across the junction, and furthermore that the magnitude of this "supercurrent" is a function of the phase difference between the two electrodes. The maximum value of the supercurrent is called the critical current, I_c. Josephson's second prediction was that if a dc voltage were applied across the junction, then the phase difference would evolve at a rate proportional to the voltage, leading to a time-oscillating Cooper pair current. This is the alternating current (*ac*) Josephson effect.

Most of the above discussion can also be applied in cases where two superconducting electrodes are separated not by an insulator, but by other nonsuperconducting or weakly superconducting regions. These include normal metals, semiconductors, or even extremely narrow superconducting constrictions. This broader class of Josephson devices is generally known as "weak links," and essentially all HTS Josephson devices being developed fall under this heading. In particular, the use of a normal metal, or of a superconductor above its transition temperature, is the focus of much of the development work, and thus of the discussion in this article.

2 HTS JOSEPHSON JUNCTION DEVELOPMENT

HTS versus LTS Materials

Fabrication of HTS Josephson junctions is complicated by the materials properties of the high-temperature superconductors. Low-temperature superconductor junctions are typically produced using polycrystalline metallic Nb as the superconductor. In contrast, the new HTS materials are multicomponent ceramic oxides with four or more elements, such as yttrium–barium–copper–oxide ($YBa_2Cu_3O_{7-x}$ or YBCO). The oxide superconductors have perovskite-based crystal structures with two to three copper–oxygen planes in a layered structure within a unit cell. As a consequence, these materials are anisotropic, with higher critical current densities and longer superconducting coherence lengths parallel to the CuO_2 planes. The superconductive coherence length is the characteristic length over which the Cooper pair density decays, as for example in approaching an interface between a superconductor and a normal metal. It also corresponds to the average physical separation of the two electrons which make up a Cooper pair. For a clean material (mean free path much longer than coherence length) it is given by the approximate expression $\xi \approx 0.18\hbar v_F/k_B T_c$, where v_F is the Fermi velocity and T_c is the superconducting transition temperature (1). In contrast to most LTS materials, the coherence lengths in the oxide superconductors are on the scale of atomic dimensions ($\approx$30 Å parallel to the copper oxide planes, and $\approx$4 Å perpendicular to the planes). Since damaged layers thicker than the coherence length result in degraded superconducting properties, surface cleaning and film growth at device interfaces are especially critical in the HTS materials.

Also unlike in most low temperature superconductors, grain boundaries in the HTS oxide superconductors lead to reduced critical current densities, and in fact can behave like Josephson junctions (see the section entitled "HTS Josephson Junction Types"). Because of the anisotropy and grain boundary problems associated with the high-temperature superconductors, epitaxial (single crystal) HTS films grown at high temperatures (650°C to 800°C) are required for many applications. High-temperature growth and the need to maintain high epitaxial quality in each layer of multilayer structures make HTS junction and circuit fabrication considerably more complex than the corresponding LTS processes.

Selection of YBCO for HTS Junctions

Nearly all Josephson junction development in HTS materials has been based on YBCO or nearly identical compounds with another rare-earth element in place of yttrium. The superconducting critical temperature, T_c, for this family of compounds is approximately 90 K. The main advantage of using YBCO compared with other HTS material families is the low volatility of all cation elements which permits films to be grown in a single step from a source—for example, a laser ablation target or sputtering target—fabricated with a stoichiometric ratio of yttrium, barium, and copper.

In contrast, films of the HTS families with the highest critical temperatures, Tl–Ba–Ca–Cu–O (*TBCCO*) and Hg–Ba–Ca–Cu–O (*HgBCCO*), are typically prepared in a two-step process in which a Tl- or Hg-deficient as-deposited film is annealed to the point of partial melting in a container sealed to obtain a high pressure of Tl or Hg vapor. Although grain boundary junctions can be formed by using this technique with bicrystal substrates or substrates with patterned steps, it is not extendible to multilayers. In the case of the Bi–Sr–Ca–Cu–O (*BSCCO*) or Ba–K–Bi–O (*BKBO*) families, films can be produced in a single step, but the volatility of K and Bi has limited film reproducibility and has discouraged junction development efforts. The TBCCO, HgBCCO, and BSCCO materials are also more highly anisotropic than YBCO, which introduces additional complications in 3-D structures.

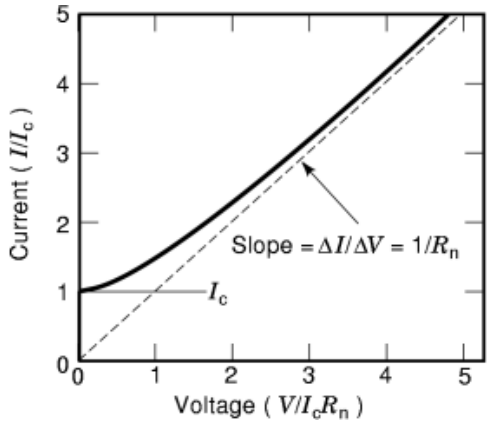

Fig. 1. Current–voltage characteristic of a Josephson weak link in the zero-capacitance limit, without thermal noise, showing definitions of the critical current, I_c, and normal resistance, R_n. The dashed line is the high-current asymptote of the I–V curve.

Basic HTS Josephson Junction Characterization

The current–voltage characteristic for an ideal Josephson junction described by the Resistively-Shunted-Junction (*RSJ*) model is shown in Fig. 1. The RSJ model adequately describes the behavior of many HTS junctions, as explained in more detail in the section entitled "Josephson Effects." The primary junction parameters of interest are the critical current, I_c, the normal state resistance, R_n, and the product of these two factors, I_cR_n. The critical current is the maximum current that can flow through the junction without a voltage drop, while the normal state resistance is given by the inverse of the slope of the I–V characteristics at a few times I_c, as shown in Fig. 1. R_n is due to dissipation in the device, for example, by current flow through the normal metal in a superconductor/normal metal/superconductor weak link. I_c and R_n are often expressed in terms of area-normalized quantities: the critical current density, $J_c = I_c/A$, and the resistance–area product, R_nA. Characterization for an HTS Josephson junction typically includes (a) measurement of the current–voltage (I–V) characteristics as a function of temperature and (b) measurement of I_c modulation in a magnetic field. In some cases, the I–V characteristics are also studied under microwave irradiation as a measure of the ac Josephson effect. In a well-behaved HTS junction the I–V shape will show the concave-up curvature consistent with the resistively shunted junction model. The temperature dependence of I_c and R_n gives information on the nature of coupling across the Josephson junction (e.g., proximity-effect coupling or tunneling), while the dependence of I_c on magnetic field provides a gauge of the uniformity of Cooper pair transport across the weak link. More comprehensive Josephson junction studies can also include determination of the J_c dependence on tunnel barrier or interlayer thickness, as well as measurement of J_c uniformity across multiple junctions on a chip (important for circuit applications).

Survey of Junction Configurations

Josephson effects in HTS materials were first observed at naturally occurring grain boundaries in films and in weak links between two HTS samples created by either breaking a sample in vacuum and coupling across the vacuum gap or bringing two pieces in contact and coupling through a surface layer that was degraded by reaction in air. Most of the configurations used since that time to fabricate junctions with controllable and reproducible properties are shown in Fig. 2. All configurations require epitaxial films to prevent naturally

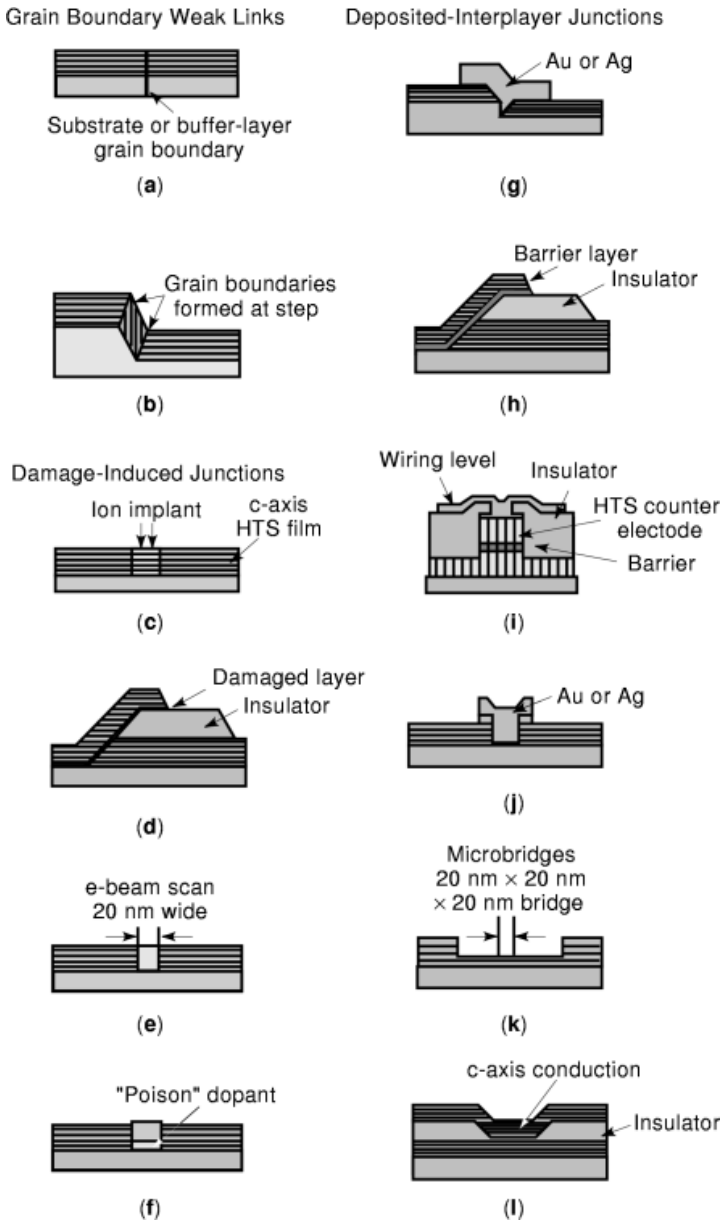

Fig. 2. The wide range of fabrication methods for HTS Josephson junctions can be loosely grouped into four classes: grain boundary junctions, damage-induced junctions, deposited-interlayer junctions, and microbridges. The deposited-interlayer approaches are thought to be the most promising for applications requiring more than a few junctions.

occurring and randomly placed grain-boundary junctions from interfering with the engineered junctions. The fill pattern for HTS film layers in Fig. 2 indicates the orientation of Cu–O planes.

The junction configurations shown in Fig. 2 are grouped in the four categories of grain-boundary weak links, damage junctions, deposited interlayer junctions, and microbridges. The chronology of development was

that single-HTS-film configurations that did not require special substrate treatments were explored first—for example, the junctions in Figs. 2(c), 2(f), and 2(j). These were followed by more complex processes where substrates were fabricated to promote the formation of a junction during HTS film growth as in Figs. 2(a), 2(b), and 2(g). Since the configurations in Figs. 2(d), 2(h), and 2(i) are direct analogues of LTS junctions, they were identified as candidate structures soon after discovery of HTS, but development did not begin until multilayer growth and patterning techniques were developed.

Application Requirements

The key electrical parameters of an individual junction, which determine its suitability for a given application, are principally its I_c and R_N and secondarily such parameters as capacitance C and inductance L. For applications which require many junctions, such as digital circuits, the uniformity of these parameters is of critical importance, while for sensor applications, such as superconducting quantum interference devices (*SQUID*s), low intrinsic noise is a key characteristic.

For digital circuits a number of constraints dictate the range of parameters required. First, the product of I_c and a typical gate inductance L_g should be not much more than a flux quantum, $\approx 2.07 \times 10^{-15}$ Wb ($\approx$2.07 pH-mA). Since it is difficult to fabricate gates with inductance less than about 4 pH in HTS (see the section entitled "Circuit Integration"), I_c can be no more than about 0.5 mA. At the same time, I_c should be large enough that the Josephson energy, $I_c/2e$, is much larger (say by a factor of 100 to 1000) than the thermal energy, k_BT, otherwise there will be too many thermally induced, erroneous switching events. For operation at 40 K this dictates that I_c be greater than 0.04 mA to 0.4 mA. At the same time, the product of I_c and R_n establishes the maximum reliable operating frequency of the circuit, $2eI_cR_n/h$. For Josephson devices to be competitive, this frequency must be at least tens of gigahertz. This means that I_cR_n must be greater than approximately 0.3 mV, and R_n must be of order 1 Ω to 10 Ω. While different arguments are applied for sensor applications of SQUIDs, such as magnetometry, the resulting requirements for I_c and R_n are quite similar.

Josephson Effects

The dc and ac Josephson effects introduced in the section entitled "Introduction to Josephson Junctions" can be stated mathematically as follows:

$$\theta = \theta_2 - \theta_1 \tag{1a}$$

$$I = I_c \sin(\theta) \tag{1b}$$

$$V = \frac{h}{2e}\frac{d\theta}{dt} \tag{1c}$$

where θ_1 and θ_2 are the phases of the wavefunction in the two electrodes. In the presence of a magnetic field, with vector potential A, Eq. (1a) is generalized as follows:

$$\theta = \theta_2 - \theta_1 + \frac{2e}{\hbar}\int_1^2 \vec{A}\cdot\overrightarrow{dl} \tag{1d}$$

where θ_1 and θ_2 refer to two specific points on opposite electrodes, and the integral is taken along a straight line between those two points (1). While the phase difference across the junction cannot be directly measured, Josephson's predictions have several measurable consequences. For example, as a result of the periodic depen-

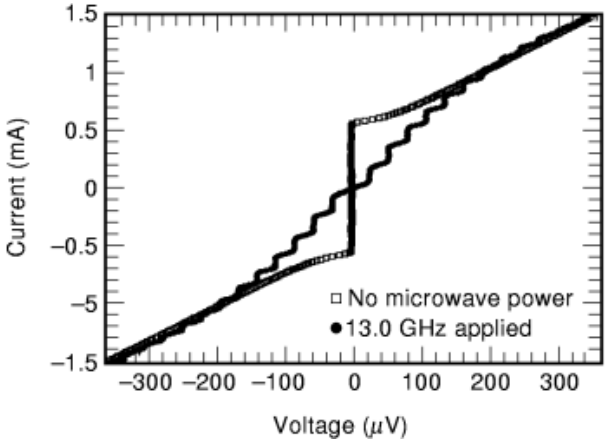

Fig. 3. Current–voltage characteristics of a YBCO/Co–YBCO/YBCO edge SNS junction, showing Shapiro steps in response to 13 GHz radiation. Such steps are a manifestation of the ac Josephson effect.

dence of supercurrent on phase difference, and the field-dependence of the phase difference given by Eq. (1d), the critical current of a spatially extended junction displays a dependence on the magnetic field described by the Fraunhofer pattern characteristic of single-slit diffraction in optics: $I_c \propto |\sin(\Phi/\Phi_0)/\Phi|$, where Φ is the magnetic flux through the junction and $\Phi_0 = h/2e$ is the superconducting flux quantum. The ac Josephson effect is responsible for Shapiro steps, which are constant voltage steps in the I–V characteristics of the junction in the presence of microwave radiation. Such steps occur when the average voltage across the junction has values such that the oscillation frequency of the supercurrent is a multiple of the frequency of the applied radiation. This effect is the basis for the definition of the standard volt, which uses a precisely known frequency to generate a fixed voltage across a series array of many junctions. Figure 3 shows an example of Shapiro steps induced in a YBCO/Cobalt-YBCO/YBCO edge superconductor/normal metal/superconductor (*SNS*) junction (see the section entitled "Edge-Geometry Weak Links") by 13 GHz radiation.

Real Josephson junctions can be modeled by the so-called resistively and capacitively shunted junction (*RCSJ*, or, for small capacitance, just RSJ) model, which takes the ideal Josephson element described by Eq. (2) and shunts it with a resistor and a capacitor. The resistor models the path by which quasiparticles cross the junction. For HTS junctions we can use the RSJ model with a linear resistor and zero capacitance for comparison with the data. In this case the RSJ model, without thermal noise, predicts a hyperbolic shape for the I–V characteristic:

$$\begin{aligned} V &= 0 \quad \text{for } I < I_c \\ V &= R_n\sqrt{I^2 - I_c^2} \qquad \text{for } I > I_c \end{aligned} \tag{2}$$

where V is the time average of the instantaneous voltage, $V(t)$, which oscillates at the Josephson frequency with amplitude I_cR_n. The dc behavior is illustrated in Fig. 1. In the presence of thermal noise the sharp voltage onset at I_c is smeared out.

Hts Josephson Junction Types

As described in the section entitled "Survey of Junction Configurations," there are a wide variety of HTS Josephson junctions. In fact, it has proven relatively easy to fabricate HTS devices which exhibit Josephson effects, with the technology ranging in sophistication from naturally occurring grain boundary weak links to all-epitaxial structures incorporating superconductors, insulators, and deposited interlayers. However, it has proven difficult to meet the requirements of some of the more demanding applications. For example, single flux quantum (*SFQ*) digital circuits require junctions with high resistance, high I_cR_n products, and $1-\sigma$ I_c spreads less than 10%. No junction technology to date has consistently met these constraints. At present the most widely used HTS junctions are grain boundary weak links and SNS edge junctions with doped YBCO interlayers. The grain boundary devices have excellent characteristics but relatively poor I_c spreads, while the SNS edge junctions are more difficult to produce but appear to be the most viable candidate for fabrication of complex circuits.

Grain Boundary Junctions.

Naturally Occurring Grain Boundary Junctions. Within a few months of the discovery of YBCO, Josephson effects were measured in bulk ceramic samples. An example of these measurements can be found in Robbes et al. (2), where a polycrystalline ceramic pellet was bonded to a glass slide, polished to a thickness of 0.25 mm, and constrictions were engraved to pattern a dc SQUID. Shapiro steps and modulation of the critical current by a magnetic field were observed.

Although randomly oriented grain boundary junctions in polycrystalline material are too poorly controlled to be practical for electronics, they are the most important obstacle in fabrication of HTS conductors for carrying large currents for large-scale, high-power applications. Many of the possible mechanisms for weak link formation at grain boundaries, such as impurities or second phase formation, have been eliminated by careful synthesis. However, the grain boundary continues to be the subject of research on topics such as the relationship between local strain fields and oxygen deficiency (3).

Bicrystal Grain Boundary Junctions. Dimos et al. (4) were the first to fabricate grain boundaries in HTS materials with controlled angles of misalignment. They cut and polished bulk $SrTiO_3$ single crystals with symmetric [100] tilt boundaries. The two crystals were sintered together with parallel [001] axes. The bicrystal was then cut and polished to obtain [001] surfaces for growth of epitaxial *c*-axis-oriented YBCO films. At least on a macroscopic scale, the misorientation angle in the basal plane of YBCO matched the misorientation angle in the $SrTiO_3$ bicrystal.

The bicrystal experiments elegantly quantified the need for biaxial alignment in YBCO high-current conductors by demonstrating the rapid decrease in J_c with increasing grain misalignment. They also provided a route for synthesis of grain boundary junctions, so-called bicrystal junctions, with controlled misalignment between grains and controlled placement of junctions along a single line. Strontium titanate bicrystals with 24° and 37° tilt rotations—angles where particularly well-defined, clean interfaces can be formed—are commercially available.

Bicrystal junctions are still in use for low-junction-count applications, usually where an integrated HTS groundplane is not required. Specifically, most commercially available dc SQUIDs are fabricated in this way. Bicrystal junctions are the simplest and least expensive way for a university laboratory to pattern a few junctions for research. However, in addition to the obvious disadvantage imposed by placement of junctions along a single line, junction uniformity has not matched the level obtained by other junction configurations. Several different explanations for the lack of uniformity are based on the observation that the junction interface meanders along the substrate bicrystal boundary on a microscopic scale as YBCO grains overgrow the boundary from each side.

Biepitaxial Grain Boundary Junctions. Biepitaxial junctions are a variant of bicrystal junctions in which the bicrystal template for junction formation is provided not by a bulk bicrystal substrate but by the tendency of particular buffer layers to grow with different epitaxial orientations depending on the presence

or absence of an intermediate "seed" layer. The first implementation was by Char et al. (5), who observed that $SrTiO_3(001)$ grew on *R*-plane sapphire, $Al_2O_3(1\underline{1}02)$, when there was no seed layer with in-plane parallel directions, $SrTiO_3[110]//Al_2O_3[11\underline{2}0]$. However, when there was an MgO(001) seed layer present, the in-plane orientation was $SrTiO_3[100]//MgO[100]//Al_2O_3[11\underline{2}0]$. So, by patterning the MgO layer with conventional lithography, 45° grain boundaries in the $SrTiO_3(001)$ buffer layer could be placed in arbitrary positions.

Other combinations of substrates, seed layers, and buffer layers were later found to work. All of them had in common with the original concept that the materials were oxides with dissimilar crystal structures and large lattice mismatches so that $\sqrt{2}$ times one lattice constant provided as close a match with a 45° in-plane rotation as could be achieved by cube-on-cube growth. While the virtue of this technique compared to bicrystal junctions is the ability to arbitrarily place grain boundary junctions on a mask, its disadvantage is that 45° is larger than the angle normally selected for bicrystal junctions. At this large angle, I_cR_n products at 77 K were on the order of just 10 μV to 20 μV and critical currents per unit junction width approximately 3 $\mu A/\mu m$. Although some multilayer SQUIDs have been based on biepitaxial junctions, there has been little work on their integration with an HTS groundplane for digital circuits.

Step-Edge Grain Boundary Junctions. When a *c*-axis YBCO film is grown over a sharp step in a cubic (or nearly cubic) substrate or deposited insulator, the YBCO grows such that the *c*-axis is perpendicular to the *local* principal crystalline axes of the substrate material (6), forming a pair of grain boundaries (at the top and bottom of the step), which behave electrically as one or two Josephson junctions. Figure 2(b) shows the simplest example, where each grain boundary (*GB*) is of the symmetric, (103)(103) type. Figure 4 shows a transmission electron micrograph of a cross section of such a boundary, formed at the top of a step in a single-crystal $LaAlO_3$ substrate. In practice the lower GB often consists of a mixture of orientations, including (010)(001).

Such devices show *I–V* characteristics with rather ideal RSJ shape, and they also show the signatures of true Josephson behavior, including critical current modulation with field (though often nonideal), Shapiro steps, and the emission of Josephson radiation. Values of J_c are fortuitously close to those required for digital and SQUID applications in the 65 K to 77 K range, with I_cR_n values of up to several hundred microvolts at 77 K (7). Electrical characteristics, and stability with thermal cycling, are improved by paying close attention to forming a sharp, clean step—for example, by the use of ion milling with a very hard mask, such as amorphous carbon. While there have been reports of sets of such junctions with J_c spreads as narrow as 5% ($1-\sigma$), typical spread values are 30% or above, making the long-term viability of this junction technique for complex circuits doubtful. For SQUIDs this is not an issue; and the simplicity of fabrication, along with the low measured noise of such junctions, makes them attractive. Their incorporation into multilayers is relatively straightforward.

The nature of the Josephson junction in this geometry is controversial. For example, GBs similar to those observed in step edge junctions have been deliberately fabricated in planar YBCO films, by the use of seed layers to control film orientation (see the section entitled "Biepitaxial Grain Boundary Junctions"), and have been found to *not* exhibit weak link behavior. Also, while some of the most definitive work on these junctions has attributed the weak link to a (010)(001) GB at the bottom of the step (6), recent measurements which probe the GBs individually (by use of a narrow YBCO lead, formed by shadowing, along the step face) suggest that it is the symmetric GB at the *top* which is the weakest.

Damage-Induced HTS Josephson Junctions.

Ion-Damaged Weak Links. Weak links based on ion damage can be classed into two categories: (i) single-layer devices in which a focused ion beam (*FIB*) creates a weak link [Fig. 2(c)]; and (ii) multilayer structures where ion surface damage of a base electrode produces a Josephson junction after deposition of a counterelectrode [Fig. 2(d)]. FIB junctions have been produced by a number of groups including Zani et al. (8), who used a 300 keV Si ion beam. The main attraction of the FIB approach is its relative simplicity, since only a single HTS film is required. However, because the typical FIB spot size is much greater than HTS coherence lengths, weak link behavior in these devices is presumably due to local variations in damage which lead to a parallel array of filamentary connections across the damaged region. Consequently, FIB-defined weak

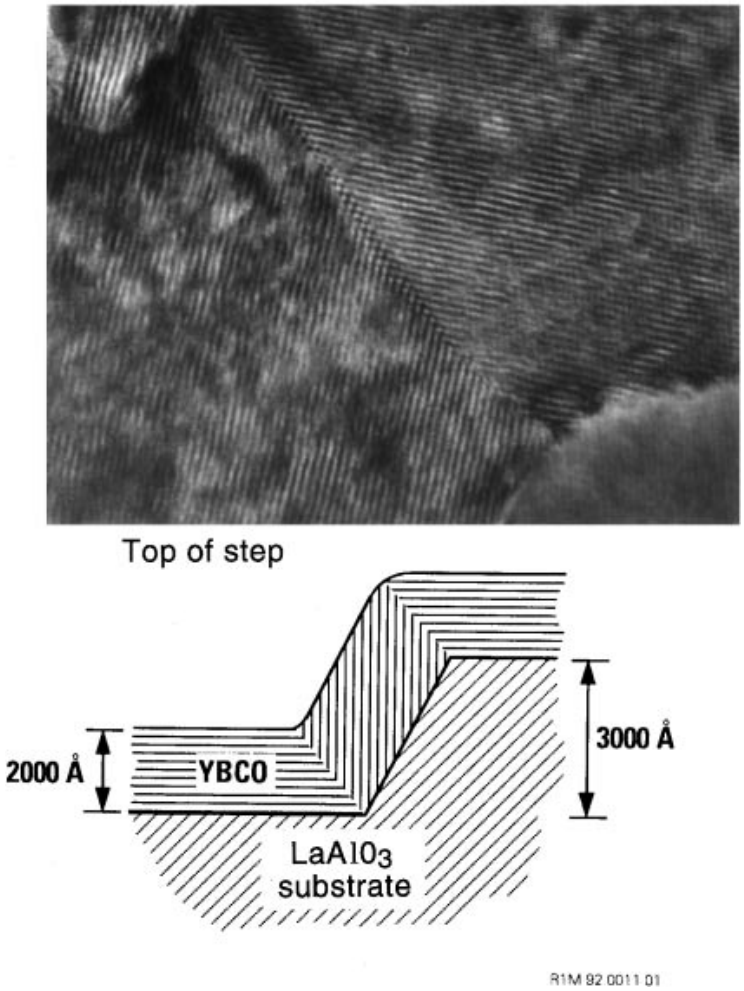

Fig. 4. TEM cross–section of the upper, symmetric grain boundary in a step-edge grain boundary junction formed at a step in a $LaAlO_3$ substrate. (Courtesy of Claire Pettiette-Hall of TRW.)

links often show nonideal *I–V* characteristics, as well as excess SQUID inductance. While this technology has produced high-resistance junctions and working SQUIDs up to 60 K, it has been largely superseded by other junction processes.

The second type of HTS Josephson junctions based on ion damage rely on ion bombardment at relatively low energies to create surface damage on a base electrode, which is then overlayed by an epitaxial counter-electrode. Work in this area has included room-temperature oxygen–argon and oxygen–fluorine-based plasma treatments (9), as well as low-energy Ar and Xe ion mill processing (10). The surface ion damage approach avoids the complication of a deposited interlayer and has produced high-quality Josephson junctions with

I_cR_n products up to 250 μV at 77 K. However, the weak links working at 77 K also typically have current densities and resistances which are not well-suited to digital and SQUID applications ($J_c > 10^5$ A/cm^2 and $R_nA < 2 \times 10^{-9}$ Ω-cm^2). More recently it has been found that radio-frequency (*RF*) plasma exposure at 400° to 500°C can produce higher resistance weak links with J_c $1-\sigma$ spreads as small as 8% at 4.2 K (11).

Electron-Beam-Damaged Weak Links. Electron-beam-damaged junctions are fabricated by writing a line across a narrow, 2 μm to 10 μm wide bridge with an electron beam in a transmission electron microscope with 120 keV or 350 keV beam energies (12). The electrons are thought to disorder oxygen ions located in the chains of copper and oxygen which are present in YBCO. The higher damage energy, 350 keV, results in a weak link that is stable at room temperature, whereas disorder caused by 120 keV electrons starts to heal even at room temperature. In either case, the evidence for oxygen disorder is mainly found in (a) the annealing behavior of these junctions which tends to a recovery of the initial, undamaged bridge properties over time with temperatures <400°C and (b) energy barriers of 1.1 eV which are characteristic of the chain oxygen sites.

Targeted junction properties can be achieved by adjusting the total damage dose and the junction length. Critical current modulation in a magnetic field indicates that the damage is uniform compared to the scale of the junction width. The most sophisticated digital circuit demonstrations that have been performed without integrated HTS groundplanes have used this type of junction. A possible long-term limitation of any sequential process of writing to form junctions using either electron or focused ion beams is that writing time can become significant as circuit complexity and junction counts increase. The special equipment required, the lack of junction stability, and the fact that groundplane integration has not yet been demonstrated are other probable reasons why this technique has been used in university laboratories but has not been adopted by industrial labs.

"Poisoned" Weak Links. An alternative technique for weakening a small area is to dope an HTS film with a small patch of a material that degrades the superconducting properties. In the example of Simon et al. (13), a 10 nm thick, several-micron-wide Al stripe was patterned on a substrate before deposition of a 200 nm thick YBCO film. A weak link formed where a bridge patterned in the YBCO film crossed the Al stripe. The Al dopant depressed the critical current of the YBCO by two orders of magnitude.

This technique has the benefit of a simple fabrication process but has not been used in recent years. It is included here for completeness and to illustrate two of the factors that influence junction reproducibility: control of bridge length and control of interface thickness. Since the ideal length of a coupling region between YBCO banks is no greater than tens of nanometers, it is preferable that the length is determined by a reproducible scale such as a film thickness or step height rather than the width of a patterned line. The deposited interlayer junction configurations described below are designed to use these better-controlled length scales and to maintain a thinner interface layer between undamaged YBCO banks and a more weakly superconducting region than one can achieve by an interdiffusion process.

Deposited-Interlayer Josephson Junctions.

Step-Edge SNS Junctions. Like the step-edge grain boundary (*SEGB*) junction, the step-edge SNS junction is formed at a step, either in the substrate or a deposited insulator, but in this case the deposition is performed directionally, from behind the step, so that the YBCO is discontinuous. This discontinuity is bridged by an in situ deposited noble metal such as Ag (14,15), making the nominally SNS structure illustrated in Fig. 2(g). A cross-sectional scanning electron micrograph of an actual device is shown in Fig. 5, which clearly shows the YBCO to be discontinuous across the step. In practice the resistance of such a device is dominated not by the normal metal itself, but by the interfaces with the YBCO. By using a directional ion mill from behind the step, it is possible to remove most of the normal metal, leaving only that which is shadowed by the step. In this case, R_n can be as much as 10 Ω, and I_cR_n as high as several millivolts, at 4.2 K. Useful SQUIDs operating at 77 K, with either "flip-chip" or integrated pick-up coils, are routinely fabricated, with modulation voltage of several microvolts. Statistics for large numbers of junctions are not available to evaluate the critical current spreads. The directionality of the fabrication process means that this junction type does not scale well for complex circuit fabrication.

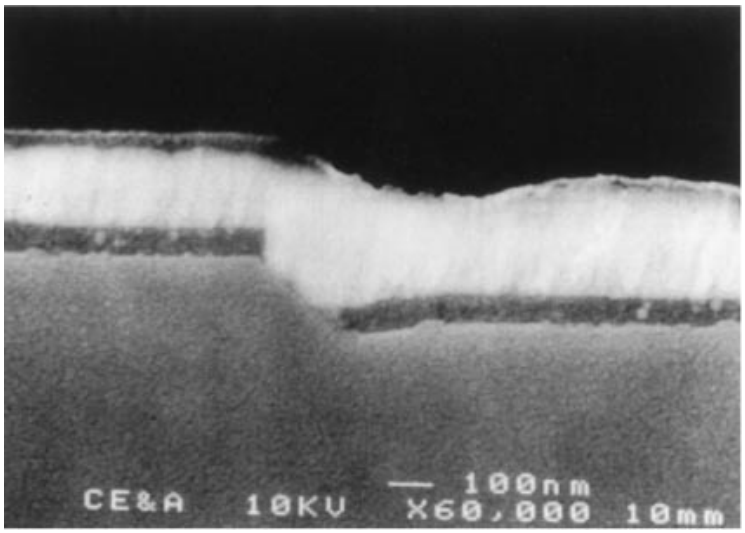

Fig. 5. Cross-sectional electron micrograph of a step-edge SNS junction of the type shown in Fig. 2(g), clearly showing the discontinuity of the YBCO film (dark) over the step, bridged by the Au–Ag alloy (light). (Courtesy of Mark DiIorio of Magnesensors Inc.)

Edge-Geometry Weak Links. The HTS edge-geometry weak link is also known as an edge junction or ramp junction and is shown in Fig. 2(h). This structure typically consists of a *c*-axis-oriented HTS base electrode film overlaid by a thick insulator (not necessarily epitaxial) with an edge produced in the bilayer by ion milling or more rarely by wet etching. An epitaxial normal metal interlayer is deposited on the exposed edge followed by growth and patterning of the HTS counterelectrode. The SNS edge junction configuration is the most widely used HTS junction approach, because this geometry offers a number of advantages, including the fact that the critical superconductor/normal metal (*SN*) interfaces are located on the longer-coherence-length surfaces of the superconducting electrodes. The edge structure also enables the fabrication of very-small-area devices using conventional photolithography because one of the device dimensions is determined by the thickness of the base electrode film. Not surprisingly, however, successful fabrication of uniform sets of high-quality SNS edge junctions requires great care in base electrode edge formation. Shallow edges ($<40^\circ$) are needed to avoid grain boundary formation in the counterelectrod, and the edge properties must be independent of edge orientation for ease of circuit layout. The most common approach to edge formation uses argon ion milling with rotating substrates and a tapered photoresist mask. Base electrode edge cleaning before growth of the normal metal and counterelectrode is also important and is usually done by low-energy ion milling or by etching in a dilute ($<1\%$) solution of bromine in alcohol.

As with trilayer junctions (discussed below), the edge junction approach utilizes an all-epitaxial stack of base electrode, normal metal interlayer, and counterelectrode which places tight constraints on potential interlayers. Suitable interlayers must be lattice-matched to the HTS electrodes, grow without pinholes, and be chemically compatible with the superconductors at the elevated temperatures necessary for epitaxial growth. These requirements point to the use of materials with similar structures and compositions to YBCO such as $PrBa_2Cu_3O_7$ (PBCO) or $YBaCu_{3-x}Co_xO_7$ (Co-doped YBCO) (16), the two most commonly used interlayers. Note that the interlayers are often referred to as "normal metals," but, in fact range from semiconductors (PBCO) to superconductors operating above their transition temperature (Co-doped YBCO).

I–V characteristics for a set of Co-doped YBCO edge junctions produced at Northrop Grumman are shown in Fig. 6 (17). The normal metal layer is 50 Å of $YBaCu_{2.8}Co_{0.2}O_7$. For this chip the average junction parameters,

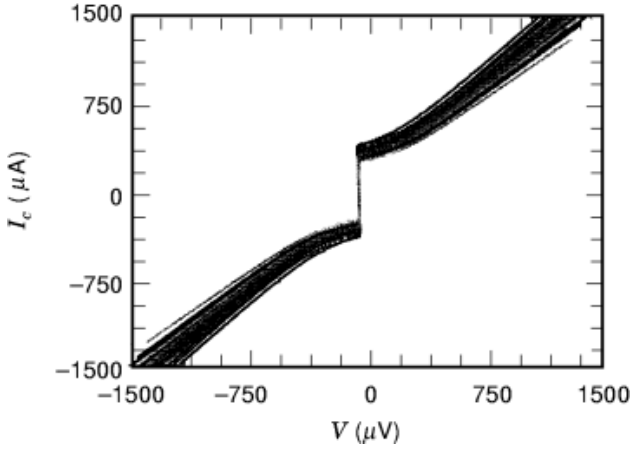

Fig. 6. I–V characteristics at 65 K for a chip with junction parameters suitable for SFQ logic. There are nineteen 4 μm wide junctions with 50 Å Co-doped YBCO interlayers and an average resistance of 0.97 Ω ($1-\sigma = 6\%$). The average I_c is 327 μA ($1-\sigma = 13\%$) and the average I_cR_n product is 315 μV ($1-\sigma = 9\%$).

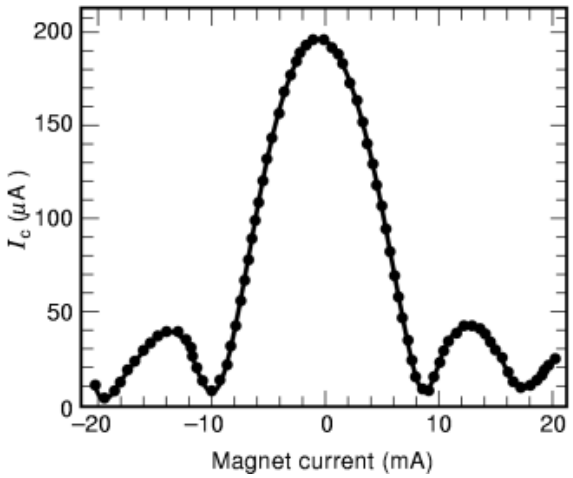

Fig. 7. Critical current modulation at 55 K for a 4 μm wide SNS junction with La-YBCO base electrode, with the magnetic field normal to the substrate. The normal metal layer is 50 Å of Co-doped YBCO, and the junction resistance is 1.1 Ω.

at 65 K, are $J_c = 4.1 \times 10^4$ A/cm^2 with $1-\sigma = 13\%$, $I_cR_n = 315$ μV with $1-\sigma = 9\%$, and $R_nA = 7.7 \times 10^{-9}$ Ω-cm^2 with $1-\sigma = 6\%$ ($R_n = 0.97$ Ω), values which are suitable for small-scale SFQ circuit applications. Note that this resistance value is surprisingly high for SNS junctions, as will be discussed in more detail in the section entitled "Advanced Issues." As shown in Fig. 7, the critical current modulation in edge-geometry weak links can approach the ideally expected $|(\sin x)/x|$ behavior, indicating fairly uniform pair current transport through the normal metal layer (17). Good results have also been obtained for junctions utilizing PBCO and Ga-doped PBCO interlayers. For example, Verhoeven et al. (18) have produced Ga-doped PBCO edge junctions with I_cR_n products up to 8 mV at 4.2 K. The data suggest that transport in these devices takes place by resonant tunneling.

Trilayer-Geometry Weak Links. Trilayer-geometry Josephson junctions [Fig. 2(i)] consist of a layered sandwich structure of HTS, interlayer, and HTS epitaxial films, as well as associated wiring and insulator layers. This approach most closely resembles the highly successful LTS Nb–Al tunnel junction process and consequently has attracted considerable attention. However, the trilayer process does require additional epitaxial insulator and HTS layers for wiring. Another potential disadvantage of this approach is the relatively large area of the devices, which can lead to unacceptably low values of R_n in many SNS processes, as well as a greater sensitivity to defects such as pinholes. Some of the earliest work in HTS deposited-interlayer weak links utilized *c*-axis oriented YBCO electrodes with a PBCO interlayer (19). Researchers at Varian have used a molecular beam epitaxy approach to engineer *c*-axis trilayers on a layer-by-layer basis (20). Most recent studies of trilayer junctions have focused on *a*-axis-oriented or (103)-oriented trilayers due to the longer superconducting coherence length parallel to the *a*–*b* planes, which in principle should lead to larger I_cR_n products. While it is not clear how an *a*-axis trilayer epitaxial wiring scheme will deal with the inherently lower J_c for wiring runs along the *c*-axis direction, some promising results have been obtained with this approach. Sato et al. (21) have produced (103)-oriented trilayer junctions with 350 Å PrBaCuO interlayers that exhibit RSJ *I*–*V* characteristics at 50 K with $J_c = 440$ A/cm^2, $1-\sigma = 38\%$; $R_nA = 1.2 \times 10^{-7}$ Ω-cm^2, $1-\sigma = 21\%$ (1.3 Ω for a 3×3 μm^2 junction), as well as sensible magnetic field modulation.

Planar or In-Line Junctions. These junctions, illustrated in Fig. 2(j), consist of a narrow gap (<1 μm) in a YBCO film, bridged by a normal conducting film either situated below the YBCO or deposited on top after the gap is etched by, typically, a focused ion beam. The normal layer is usually Au or Ag (above the YBCO) or PBCO (above or below). While the normal metal coherence length of Au is long enough that gaps of order 1 μm should support a critical current, the estimated values of ξ_N for PBCO and similar materials are so short that even devices as short as 0.1 μm should not exhibit a critical current. The fact that they do has been used as evidence to suggest the existence of a "long-range proximity effect" in these materials, although the existence of this is controversial. For example, it is possible that the critical current is partly due to YBCO not fully removed from the gap.

There is little data on the reproducibility of these devices, but it is generally believed that they have little potential for applications requiring many junctions. In addition, their characteristics are relatively nonideal, often exhibiting large excess current for example.

Microbridges. If a superconducting bridge is made with a width comparable to the coherence length, ξ, it behaves as a Josephson junction. Since ξ is only a few angstroms in YBCO, this is not a practical way to make a Josephson device. However, if a bridge is wider than ξ, but still less than the penetration depth λ, it can behave in many ways as a Josephson junction, for example, exhibiting constant voltage steps in response to applied microwaves, in this case as a result of magnetic field vortices moving across the bridge in synchronization with the microwave field. As such they may be useful for SQUID applications, but not for SFQ circuits.

These devices have been fabricated both in the *a*–*b* direction [Fig. 2(k)], using focused ion beam etching for example, and in the vertical direction in a *c*-axis film [Fig. 2(l)]. The latter case is interesting in that the corresponding penetration depth is long enough ($\sim$1 μm at 77 K) that conventional photolithography suffices. The *c*-axis microbridges have demonstrated encouraging I_c uniformity [13% for a few devices (22)], although critical currents are typically somewhat high, and resistances low, compared to typical application requirements, suggesting that more aggressive lithography may still be required. Low-inductance multilayer SQUIDs have been demonstrated, and the fabrication process is quite compatible with the needs of a multilayer process.

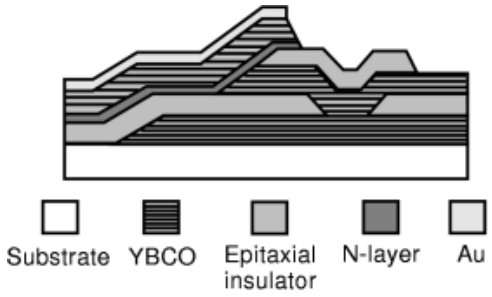

Fig. 8. Schematic cross section of a multilayer process incorporating edge SNS junctions over an HTS groundplane. The horizontal shading of the YBCO layers indicates the direction of the copper–oxide planes. All layers are expitaxial except for the Au, used for contacts.

Circuit Integration

Multilayer Circuit Requirements. Multilayer structures are required for many important applications of HTS junctions including digital circuits, SQUIDs with integrated pickup coils, voltage standards, and phase shifters, among others. Junction-specific requirements on I_c and R_n for some of these applications have already been discussed in the section entitled "Overview." It is desirable that these junction properties be independent of location in a multilevel structure—for example, on or off of groundplanes. This is a nontrivial constraint because junction performance is often intimately related to details of film microstructure which can be affected by growth over the underlying layers in a multifilm stack. Multilayer circuits also require good electrical isolation ($>10^4$ Ω-cm) between superconducting layers, using insulators with low dielectric constants and low losses, if high-frequency applications are the objective. High-critical-current-density vias and crossovers ($>10^5$ A/cm^2) are essential for most HTS circuit applications. Digital circuits also call for the integration of superconducting groundplanes to produce the low-inductance SQUIDs and interconnects needed for SFQ logic. More complex circuits can require additional epitaxial insulators and wiring levels as well as integrated resistors.

Fabrication Issues. A cross-sectional schematic view of the multilayer structure used to integrate edge SNS junctions on an HTS groundplane is shown in Fig. 8. A minimum of four mask levels and six epitaxial oxide film layers are needed for this process. Additional epitaxial film layers are often used such as buffer layers between the substrate and groundplane, or passivation layers above the groundplane, but these additional layers do not alter the basic processing steps.

The substrate selected for the most complex multilayer structures is single-crystal, perovskite-structure $NdGaO_3$ which is representative of the other candidate substrates. The (110) and (001) faces of $NdGaO_3$ are virtually identical in providing a square two-dimensional lattice with approximately a 1% lattice mismatch for growth of *c*-axis-oriented epitaxial YBCO films.

The most important requirements for YBCO groundplane films are magnetic penetration depths, λ(T), close to intrinsic values and smooth surfaces. These properties can be achieved, in principle, by films grown by a number of different techniques. In practice, pulsed laser deposition, sputtering, and co-evaporation are the three techniques most commonly used for multilayer film growth. The effect of the penetration depth on circuit inductance is discussed in the next section. The smoothest films, those with approximately 1 nm root-mean-square (*rms*) roughness, have less than 10^3/cm^2 of the outgrowths that are commonly found in YBCO films. Most of the outgrowths are second-phase copper oxide particles that are 0.5 mm to 1.0 mm in diameter and grow higher than the film surface by a distance comparable to the film thickness.

As long as a copper oxide outgrowth does not form in a location where a junction is patterned, it does not have a deleterious effect on YBCO film properties. For applications of YBCO films requiring a single layer,

such as bandpass radio frequency (RF) filters, no effort is made to minimize them. In fact, their presence is a sign that excess copper available at the growing film surface has been consumed, leaving behind a matrix of stoichiometric YBCO which has optimized properties. However, outgrowth density must be minimized by a slightly copper-deficient film composition for multilayer circuits to maintain electrical isolation between layers by the epitaxial insulators.

The epitaxial insulator that grows with the best edge coverage and smoothest surfaces is $SrTiO_3$. Its high dielectric constant, on the order of $\varepsilon = 500$, is not a problem for low-frequency applications such as SQUID magnetometers. However, there is no consensus materials choice at present for high-speed digital circuits where a dielectric with $\varepsilon = 10$ to 30 is a practical maximum. Examples of relatively low-ε materials used as epitaxial insulators are Sr_2AlNbO_6 and Sr_2AlTaO_6.

Since the integration level is very low at this stage of the development of HTS circuits, demands on lithography are minimal, and this is usually performed with contact lithography and standard resists. However, to avoid formation of step-edge grain-boundary junctions where interconnects cross steps in underlying films, an etch process is required that results in sidewalls that are sloped just 5° to 30° from the plane of the substrate—similar to the angles used for edge SNS junction fabrication. Tapered edges are obtained by ion milling with Ar or Ar/O_2 mixtures with the ion beam at an angle with respect to the substrate and the substrate rotating about its normal.

Because the surface of YBCO reacts with air and photoresist to form an amorphous layer of carbonates and hydroxides 2 nm to 10 nm thick, the surface must be cleaned after lithography and before a subsequent epitaxial film layer can be grown. In the case of edge SNS junctions shown in Fig. 8, the most important exposed surface is the edge cut in the base electrode which will serve as the template for growth of an N-layer and YBCO counterelectrode. Some combination of oxygen plasma ashing, blanket removal of the reacted layer by ion milling, and wet chemical etching, typically with bromine–alcohol mixtures, is performed to prepare surfaces for the next film deposition.

Figure 8 shows that a Au contact layer is typically used to complete this multilayer structure. The contact layer is normally deposited in situ—that is, after the YBCO counterelectrode layer has been deposited and cooled to room temperature in oxygen, but before it has been exposed to air. In situ Au deposition lowers contact resistance and improves adhesion. Other room-temperature film layers may be required for resistors and for electrical isolation of the resistor layers, but they do not require the same care that must be taken for film layers grown at high temperature.

Groundplanes. As discussed in the section entitled "Application Requirements," digital circuits require low inductances, of order a few picohenries, to ensure that the LI_c product is about a flux quantum. The standard way to keep inductances low is to incorporate a superconducting ground plane above or below the active devices, which tends to confine the magnetic field in the relatively small volume between the two (or more) superconductor layers. Calculation of inductance is also simplified for this geometry since the problem is essentially reduced to counting squares and using the expression for the inductance per square of such a microstrip line:

$$L_{sq} = \mu_0 d\kappa \left(1 + \frac{\lambda_1}{d}\coth\left(\frac{b_1}{\lambda_1}\right) + \frac{\lambda_2}{d}\coth\left(\frac{b_2}{\lambda_2}\right)\right) \qquad (3)$$

where d is the insulator thickness, b_1 and b_2 the superconductor thicknesses, and κ is a factor that determines the field strength at the center of the finite width microstrip. The long penetration depth of YBCO, compared to Nb for example, means that the inductance per square is much higher. For example at 65 K we have $\lambda_1 = \lambda_2 = \lambda \approx 0.23$ nm, so for $d = b_1 = b_2 = 0.2$ nm and $\kappa \approx 1$, we have $L_{sq} \approx 0.84$ pH. Contrast this with the case for Nb at 4.2 K, where $\lambda \approx 0.04$ nm and $L_{sq} \approx 0.35$ pH. Thus the circuit-driven constraints of low inductance are particularly

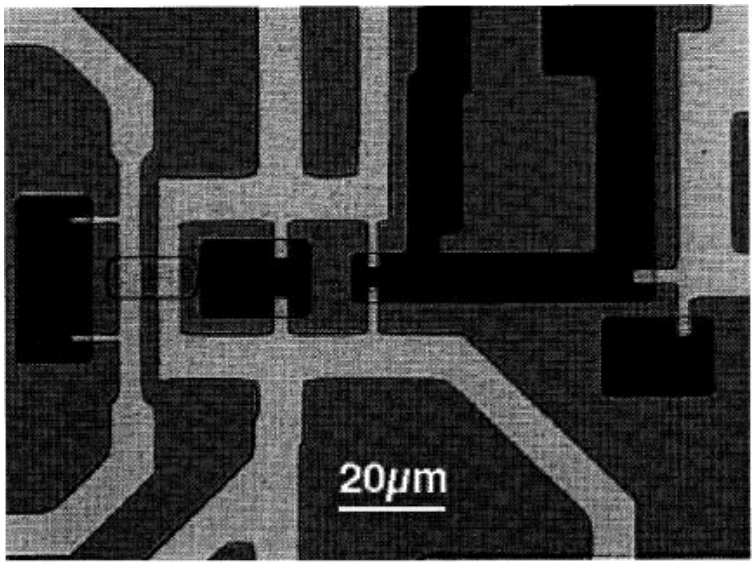

Fig. 9. An example of a simple multilayer HTS circuit, a 1-bit analog-to-digital converter, fabricated with edge SNS junctions over an HTS groundplane. The lightest areas are the gold-coated counterelectrode, while the darkest are the base electrode. The process used to produce the circuit is extendible to much more complex circuits, provided that junction critical current uniformity can be improved sufficiently.

difficult to meet for HTS materials. Given the need for high I_c for thermal stability, the requirement that LI_c be about a flux quantum is particularly difficult to achieve, suggesting the need for novel gate layouts in HTS.

The integration of a YBCO groundplane has been demonstrated for several HTS junction types, including step-edge SNS, step-edge grain boundary, and edge SNS junctions. Measured inductances are consistent with other measurements of the penetration depth.

Example Circuits. The key factor in determining the yield of working HTS circuits is the degree of control over junction critical currents—especially the on-chip spread. The more complex the circuit, the tighter the I_c spread must be, although the numerical relationship between I_c spread and circuit yield depends on the circuit margins. While LTS SFQ circuits often exhibit wide margins, of order 30% or more, extrapolating such values to HTS operation at 40 K to 65 K is controversial. If these margins do hold out, possibly in cases where bit-error rate is not a driving concern, then spreads of 15% should allow, based purely on statistical arguments, yields of 50% for circuits with up to about twenty junctions (24). In fact a number of such circuits have been demonstrated at up to about 65 K, at least at low speed, bearing out some optimism.

Demonstrated HTS gates or circuits include digital devices such as logic gates (OR, AND, etc.), set-reset flip-flops, toggle flip-flops, sampling circuits, and shift registers, as well as analog devices such as SQUID amplifiers. For digital devices, in which all of the junctions need to "work" for correct operation, the highest junction count is about 30. Figure 9 shows an example of a 10-junction circuit—the first stage of a low-power analog-to-digital converter, fabricated with edge SNS junctions over a ground plane.

So far there has been very little work to quantify the experimental margins of such HTS circuits. Should the more pessimistic estimates of HTS SFQ margins be borne out, then it may be necessary to rely on voltage-state logic, where increased power dissipation will erase one of the major advantages of superconductivity, or on multi-flux-quantum schemes, several of which have been proposed.

Manufacturability of HTS circuits will also require that chip-to-chip parameter spreads be well controlled. For a single circuit it may be feasible to tune the operating temperature to, for example, adjust the average

critical current to the desired value, but this is clearly not practical for a system consisting of several separately manufactured superconducting circuits. Adjustment of overall circuit biases is a more practical solution to poorly targeted critical current values but will significantly increase costs due to the need for increased circuit testing and qualification. Thus ultimately it will be necessary to control chip-to-chip parameter reproducibility to the level of a few percent at most, which will be a significant challenge for these complex materials.

There is no single answer to the question of what is the best application for HTS Josephson junctions. However, a consensus of those working in the field believes that applications that utilize the analog precision of Josephson devices constitute the most promising niche where Josephson devices can surpass semiconductor circuits. Thus there is an emphasis on high precision analog-to-digital and digital-to-analog converters in such applications as radar, communications, and precision instrumentation. For example, an A-to-D converter with 20 bits of accuracy on a 10 MHz signal bandwidth would leapfrog semiconductor A-to-D converters, based on their historical rate of progress, by about 10 years. A potential application of such a converter is in radar, where it is desired to pick out a small target (airplane, missile) from a large "clutter" signal (rain, mountainous terrain, waves). Such a circuit should contain, depending on the details of the architecture, anywhere from several hundred to several thousand Josephson junctions. Assuming circuit margins of 30% (which may be optimistic), the required junction critical current spread for 50% yield, based on the calculations of Ref. 23, would be approximately 10% to 8%. Should the margins be reduced to, for example, 15% due to thermal noise issues, then the required spread would be more like 5% to 4%.

The issue of operating temperature is also of crucial importance, and is influenced by the potential circuit performance, as limited by thermal noise, and the availability, reliability, size, weight, and cooling power of the cryocooler. For example, a typical Stirling-cycle cooler with 0.3 Watts of heat-lift at 4.2 K would have an input requirement of some 1500 W, and would weigh about 250 pounds. This power and weight probably rules out the application of LTS circuits in most airborne platforms. On the other hand a Stirling cooler with 4 W of heat lift at 77 K would only require about 100 W of input power, and should weigh only about 10 pounds, making airborne deployment much easier. Operating at 40 K, should thermal noise require it, might reduce the available heat lift to 0.4 W, which should still be sufficient circuits of several thousand junctions.

Advanced Issues

Proximity Effect. When a superconductor and normal metal are brought into contact, Cooper pairs from the superconductor can diffuse into the normal metal. Due to phonon-induced pair breaking, the pair amplitude (also known as the superconducting order parameter or wavefunction) in the normal metal decays exponentially over a decay length defined as the normal metal coherence length, ξ_n. In the clean limit where l_n, the mean free path in N, is much greater than ξ_n, the coherence length is given by

$$\xi_{ac} = \frac{\hbar v_n}{2\pi kT} \tag{4}$$

while in the dirty limit with $l_n \ll \xi_n$, the coherence length is

$$\xi_{nd} = \sqrt{\frac{\hbar D_n}{2\pi kT}} \tag{5}$$

where the diffusion constant, D_n equals $v_n l_n/d$ and d is the dimensionality. Theories describing the details of the superconductor–normal-metal "proximity-effect" interaction have been developed for a variety of cases including back-to-back SN contacts—that is, the SNS weak link (24,25). In the SNS Josephson junction,

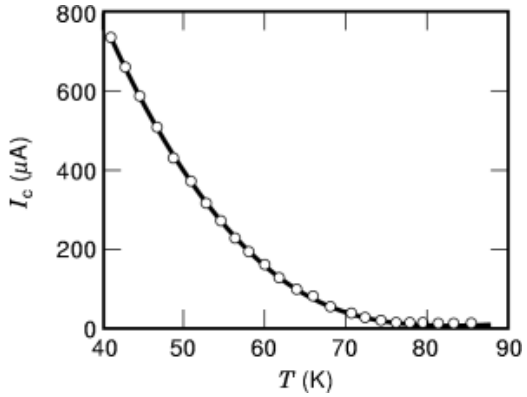

Fig. 10. Critical current versus temperature for a YBCO/Co–YBCO/YBCO edge SNS junction. The solid line is a fit to the proximity effect theory of DeGennes. Despite the fact that the junction is nonideal, in that it exhibits a large interface resistance, it still appears to exhibit behavior consistent with the proximity effect.

pairs from each superconducting electrode "leak" into the normal metal interlayer and the overlap of the exponentially decaying pair amplitudes determines the strength of interaction between the superconductors. Consequently, the magnitude of the Josephson critical current scales as $\exp[-L/\xi_n(T)]$, where L is the normal metal bridge length. More specifically, in the dirty limit for long SNS bridges ($L \gg \xi_n$) relatively close to T_c ($T > 0.3T_c$), it is found that

$$I_c(T;L) \cong \frac{\pi}{2eR_n}\frac{|\Delta_i|^2}{kT_c}\frac{L}{\xi_{nd}(T)}e^{-L/\xi_{nd}(T)} \qquad (6)$$

where Δ_i is the superconducting gap at the superconductor–normal-metal interface. This equation indicates that the critical current of an SNS weak link should also vary exponentially with temperature, because of the $(T)^{-1/2}$ temperature dependence of the dirty-limit normal-metal coherence length. The exponential length and temperature dependence of the critical current are the distinguishing signatures of true proximity effect devices. Indeed, there are a number of examples of HTS SNS devices which are largely consistent with proximity effect theory, most notably the junctions using Co- or Ca-doped YBCO as the normal metal layer. An example of exponential critical current dependence on temperature for a Co-doped YBCO SNS edge junction is shown in Fig. 10, along with a proximity theory fit to the data (26). However, it is often found that HTS devices with a nominal SNS configuration do not show an exponential critical current dependence on temperature. In fact, such devices commonly exhibit a quasilinear temperature dependence, which may indicate that pinhole conduction through the normal metal is dominating the electrical characteristics (25).

Control of Resistance in SNS Devices. The normal state resistance of an SNS weak link is given by the sum of the normal metal resistance plus the resistance of each of the two SN interfaces. In the "ideal" SNS device the interface resistances are zero and the total device resistance is just $R_n = \rho_n L/A$, where ρ_n is the normal metal resistivity, L is the normal metal thickness, and A is the cross-sectional area. For typical values of these parameters in an SNS edge junction with a $YBa_2Cu_{2.8}Co_{0.2}O_7$ normal metal layer at 65 K ($\rho_n = 250$ $\mu\Omega$-cm, $L = 100$ Å, and $A = 4 \times 0.2$ μm^2) we find $R_n = 0.03$ Ω. In practice, such low values of resistance are often undesirable. For example, for SFQ digital applications at 65 K junctions are biased at a fixed current of order 500 μA so that the available I_cR_n product with $R_n = 0.03$ Ω is only 15 μV, far less than the required value of approximately 300 μV. Increasing SNS device resistances to a practical level requires adding interface resistance without degrading the inherent I_cR_n product. In principle, this can be done in at least two ways: (1)

by incorporating an inhomogeneous interface resistance to reduce the effective device area or (2) by producing a thin insulator at one SN interface to form an SINS structure. In practice, different groups have seen widely varying values of SNS resistance, ranging from the ideal but impractical case of very low R_nA (16) to the more technologically interesting case of high-R_nA devices (27).

For SNS weak links using Co-YBCO as the normal metal, it has been found that the interface resistance is sensitive to a variety of factors including the base electrode material and the normal metal and counterelectrode deposition conditions (17). For example, SNS devices using $YBa_2Cu_3O_7$ base electrodes grown by pulsed laser deposition (*PLD*) exhibit more than an order of magnitude lower resistance than devices with La-doped YBCO base electrodes ($YBa_{1.95}La_{0.05}Cu_3O_7$), or $GdBa_2Cu_3O_7$ or $NdBa_2Cu_3O_7$ base electrodes. Varying the normal metal and counterelectrode growth parameters can also have a dramatic effect on device resistance: High-pressure PLD growth in an $Ar–O_2$ atmosphere results in R_nA products over a factor of 10 smaller than for devices produced using the more conventional PLD deposition conditions in a pure oxygen background. While the detailed nature of the interface resistance is not understood at this point, the base electrode material dependence suggests that cation disorder (e.g., Y and Ba exchange) is affecting device resistance. The fact that the growth conditions of the normal metal also have a strong effect on SNS resistance indicates that defects "frozen in" in the early stages of normal metal growth may also play an important role in determining interface resistances. Because SNS interface resistances are strongly affected by a number of material and fabrication parameters, it is possible to control SNS device resistances over two to three orders of magnitude, with R_nA products ranging from 0.03 Ω-μm^2 to more than 10 Ω-μm^2. Importantly, even in the relatively high R_nA limit required for SFQ applications (0.5 Ω-μm^2 to 2 Ω-μm^2), Co-doped YBCO SNS devices incorporating significant interface resistance still behave like true proximity effect devices (see, for example, Fig. 10) with parameter uniformity suitable for small-scale SFQ circuits.

Limits on Reproducibility. Speculation on the origins of parameter spreads have led to many experiments in fabrication of edge SNS junctions. Surprisingly, the fabrication parameters which result in junction resistances greater than $R_n = \rho_n L/A$ do not appear to systematically contribute to larger spreads in critical currents or other junction parameters. Similarly, the uniformity of current flow through a junction which can be inferred from $I_c(B)$ indicates that junctions with significant interface resistance maintain uniform current distributions.

Poor control over many fabrication parameters will certainly result in junction spreads worse than the state of the art. A good example is the roughness of YBCO base electrodes which gets transferred into the edge by patterning with Ar ion milling. While improvements from 10 nm to 2 nm rms surface roughness provide a measurable benefit for junction reproducibility, further improvements in smoothness have had a negligible effect. A second example is that junctions facing in all four in-plane directions sometimes exhibit a distribution of critical currents that is direction-dependent. However, when all processing steps are made isotropic, state-of-the-art junction uniformity can be achieved as easily in a set of junctions facing in four directions as in a set facing just one way.

These results have led us to examine defects that are intrinsic to YBCO. The role of oxygen disorder in YBCO has been investigated in several types of edge junction experiments. Decreasing the number of oxygen vacancies by plasma oxidation or annealing in ozone simply scales I_c for all treated junctions by a constant factor as large as five. Experiments in which orthorhombic YBCO electrodes were replaced by doped YBCO compounds which were tetragonal have been inconclusive in determining the possible role that twinning in YBCO might have on parameter spreads. Junctions were fabricated to face in ⟨110⟩ in-plane directions instead of the standard ⟨100⟩ directions to minimize the effects attributable to twinning, but no improvement in junction uniformity was observed.

Finally, the fact that similar best-case critical current spreads are observed for different junction fabrication processes using the same base electrode materials suggests that microstructural defects in the base electrode or base electrode edge are limiting I_c spreads. Further improvements in materials quality and edge formation techniques are expected to lead to improved junction spreads.

Conclusions

Josephson junctions based on YBCO are the fundamental building blocks for a variety of superconducting electronics applications operating at temperatures >50 K. The properties of individual junctions fabricated in a variety of configurations are sufficiently close to ideal Josephson behavior to meet application requirements. However, integration of junctions into multilayer circuits and demands on reproducibility of junction parameters when higher junction counts are needed have narrowed development efforts to a few promising configurations. Most of the current HTS circuit fabrication effort in industrial laboratories is based on edge SNS junctions which have been used for the most sophisticated and extendible digital circuit demonstrations. Further incremental improvements in the uniformity of these junctions to $1-\sigma I_c$ spreads less than 10% will permit medium-scale integrated circuit fabrication. A parallel effort, mainly by university researchers, is exploring higher-risk alternative junction configurations intended to circumvent some of the limitations to junction uniformity that may exist for edge junctions.

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