CIRCUIT ANALYSIS COMPUTING OF SEMICONDUCTOR PACKAGES AND SYSTEMS

The electronic package has four major functions: (1) supply of electrical power necessary for operation of electronic circuits, (2) distribution of electrical signals carrying information, (3) removal of heat generated during operation of circuits, and (4) mechanical support of circuits and protection from environment. Electrical package design is concerned primarily with the first two functions. The typical goal of electrical design is to obtain a package that supports required speed of system operation and maintains electrical noises at or below tolerances. Package design is also influenced by cost and reliability considerations. However, this article deals with a package electrical performance, which is related to the first two listed package functions.

Design is based on package mathematical modeling, which describes relations between a performance of designed object and design variables. Mathematical modeling of electronic packaging is quite involved, and resulting models are complicated. Consequently, analytical approaches to package design are so limited that computer support is required. Simulation that involves computer implementation of package models and numerical imitation of package performance is commonly used as a design support.

ELECTRICAL PACKAGE MODELING

Electrical package modeling (i.e., description of relations between electrical performance and design variables) is based on a number of simplifying assumptions that depend on the type of signals considered and packaged device/system application. Therefore, packages can be classified into specific categories on the basis of application and modeling features. Thus modeling the following package categories will be discussed: radio-frequency (RF) packages (i.e., packages housing RF circuits), digital packages housing digital circuits, and mixed-signal packages containing circuits that perform operations on both analog and digital signals.

RF Package Modeling

Modeling of RF packages is closely related to modeling of packaged devices and circuits, and in most cases it is very complicated. Modeling of parasitic couplings between the components is a particularly troublesome problem. Typical models are developed in frequency domain because the relevant circuits and packages usually operate in narrow frequency bands. These models are based on linear approximation (linearization), which is valid for small signal operations. Specialized software tools must be used to support modeling. Such tools are being intensively developed because of growing demand for a variety of RF circuits needed in wireless communication. These tools are continually updated and modified in cooperation with the user community. In light of the rapid changes of simulation tools, they are not described here in detail.

Some circuits such as RF power amplifiers operate with large signals such that the linear approximation cannot be used, and novel methods like harmonic balance are used in modeling instead (1). Both modeling methods and supporting software are under vigorous development.

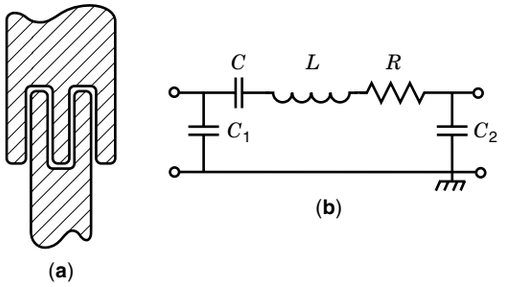

Figure 1. Interdigitated capacitor and its equivalent circuit showing that the structure has inductive and capacitive effects and resistive losses: (a) layout, (b) equivalent circuit.

To illustrate the complexity of modeling RF circuits and packages and to point to some of the most important features of modeling, a few examples of models for passive components are presented. A layout of an interdigitated capacitor and its equivalent circuit is shown in Fig. 1. The capacitor has losses represented by the resistor R and inductive effects (capability to store magnetic energy) represented by the inductor L. The values of parameters of the equivalent circuit, C, L, R, C_1, and C_2 cannot be determined accurately from the layout. In addition, these parameters depend on the frequency with which the device operates. In fact, the capacitive effects are dominating at frequencies significantly different from the self-resonant frequency of the circuit. That is at such frequencies the device operates approximately as a capacitor, and at other frequencies its function is not clearly that of capacitor.

An example of layouts of spiral inductors and the equivalent circuit illustrate the same point. The spiral inductor (Fig. 2) has inductive effects represented by the lumped inductor L, losses R, and capacitive effects represented by the lumped capacitors C_1, C_2, and C_3. Again, the function of the device cannot be described as an inductor, but it is a mixture of losses and capacitive and inductive effects, and the role of those effects varies with the frequency of operation.

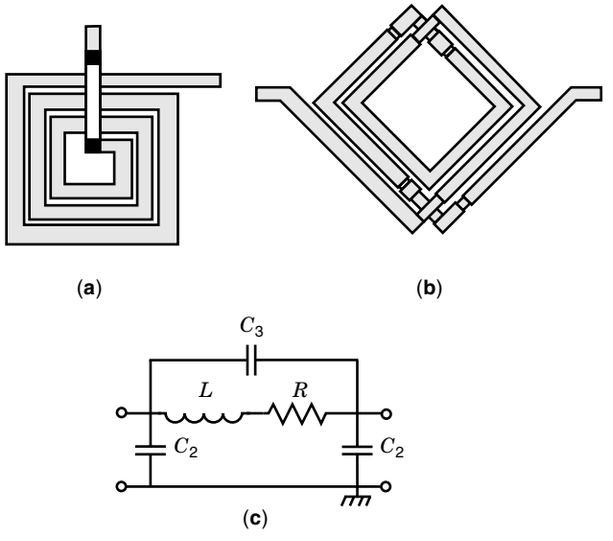

Figure 2. Spiral inductors of two types with equivalent circuits illustrating that inductor has many parasitic components (C_1, C_2, C_3, R): (a) layout of concentric inductor, (b) layout of nonconcentric inductor, (c) equivalent circuit.

The parameters of equivalent circuit are often determined by characterization (i.e., measurement of actual devices and matching the equivalent circuit behavior to that of the device). It should be added here that the equivalent circuits are not unique, and one could select another equivalent circuit for the same device that may give similar approximation in a given frequency range.

Nonuniqueness of equivalent circuit and difficulties in determining its parameters are so serious that another approach, also based on characterization, was developed to represent components of RF circuits. This approach consists of constructing special tables, termed look-up tables, depicting the input-output relations determined by characterization of devices. The look-up table techniques avoid the problems associated with determination of equivalent circuits and ambiguities related to nonuniqueness but require characterization of a number of parts of various dimensions (various layouts). Because manufacturing and characterization are both expensive, there is a problem with determining the minimum number of parts to construct a look-up table model for a given modeling accuracy. This minimum number of parts is a function of required accuracy and interpolation routines used in computing input-output relations. Use of higher-order interpolation routines reduces this number but increases output processing time. Look-up table techniques with cubic spline interpolation provide a good solution to this trade-off in applications to passive elements and active devices (2) of RF circuits.

Digital Package Modeling

Digital circuits are widely used and produced in a great variety and large volume. Consequently, digital packages are very common, and because of substantial development resources available with large volume production, they are very advanced. Analogous modeling and design methods are also advanced. Two basic electrical systems—(1) signal distribution and (2) power/ground distribution—performing the two major package functions and the associated electrical performance and signal integrity issues will be discussed.

Signal Distribution System. Basic components of the signal distribution in a digital system are internal logic, input-output drivers/receivers, and interconnections. Modeling of internal logic components and input/output driver/receiver circuits is the subject of microelectronics, and thus it will not be discussed here. Propagation of an electrical signal requires the use of two conductors. One is called the signal line, which is dedicated to a transmission of specific signal, whereas the other, which is called a return, reference, or ground conductor, is usually shared by many signals. Modern digital signals have a significant energy spectrum up to the range of a few gigahertz. The interconnections carrying these signals must be treated as a high-frequency transmission system. It can be shown that in most practical cases propagation of signals in digital systems can be adequately described by electromagnetic field equations under the assumption of quasi-traverse electromagnetic (TEM) wave propagation. Degradation of signals occurs as they propagate through package interconnections. There are reflections resulting from discontinuities of

the structure or terminations, which when improperly designed can increase the transition time or in the worst case cause a false switching in some parts of the system. The interconnection resistance causes attenuation and dispersion (giving an undesirable change in the waveform), which increases the transition time. The result of attenuation is such that in a very long interconnection the signal may not reach the switching threshold. A magnetic field associated with current changes induces voltage on the line and its neighbors (effects of self and mutual inductance). Voltage induced on neighboring lines called cross-talk may build up and also cause false switching. Evaluation of those effects is necessary in the design and can be accomplished by modeling interconnections and system simulation.

Circuit Attributes in Signal Transmission. Circuit attributes important in modeling signal distribution are logic swing V_{LS}, rise time t_r, static noise tolerance (NT) [noise margin (NM) or noise immunity (NI = NT/V_{LS})], and dynamic noise tolerance/immunity. The immunity is a dimensionless noise tolerance (or margin) referenced to the logic swing. The immunity is a convenient measure of noise because it may be used to compare noise properties of various technologies (having different logic swings). The logic swing is the difference between the potentials of signals in high and low logic state. The rise time is the time needed for the signal to pass through the central 80% of the logic swing in transition from the low to the high logic state. Falling time is analogously defined for the falling signal and is usually assumed to be equal to the rise time. Static noise tolerance is determined from the transfer curve of the receiving gate as the smaller difference between the input voltage corresponding to the switching threshold and the logic high value NT_H or low value NT_L of input signal (Fig. 3). Noise margin is defined as the smaller difference between logic high value NM_H or low values NM_L of input voltages and input voltages corresponding to "unity gain" points on the transfer curve (points where the slope of the tangent is 45°, see Fig. 3). The dynamic noise tolerance/immunity (Fig. 4) of an input gate is determined by characterization of existing gate or its extensive simulation with the use of a circuit simulation program such as SPICE, originated at the University of California at Berkeley and now widely used and available from many companies. The dynamic noise sensitivity takes into account the inertia of the receiving gate and allows for larger amplitude perturbations if the perturbations are of shorter duration. To use the dynamic noise sensitivity curve in the design, it is necessary to estimate the amplitude and the duration of the representative perturbation acting at the receiver's input. Such an estimate can be obtained from the cross-talk, reflection, and switching perturbation studies.

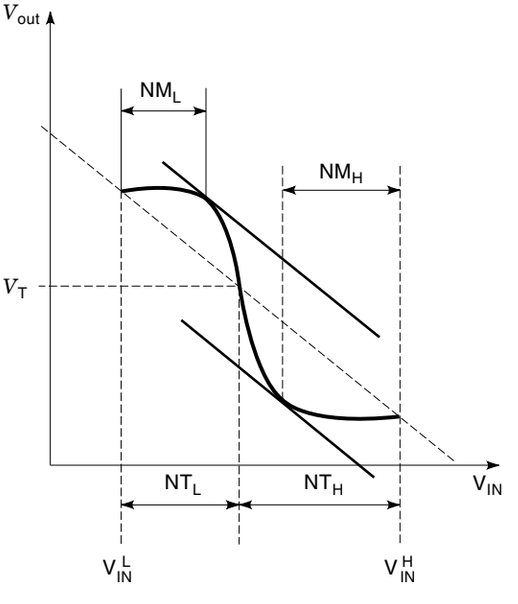

Figure 3. Transfer curve of an inverter is used to define noise tolerances, NT, noise margins, NM, and switching threshold, V_T.

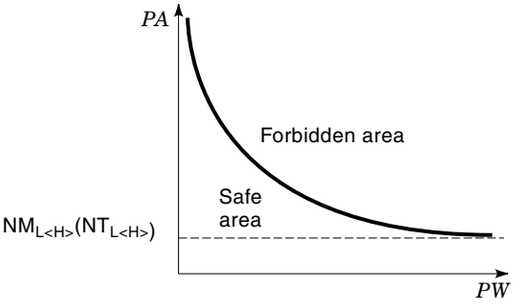

Figure 4. Typical dynamic noise tolerance curve illustrating the point that a receiver has smaller tolerance for longer perturbations.

Power/Ground Distribution System. Power/ground distribution systems bring electrical energy from external sources (power supplies) to an individual circuit, which is necessary for the operation of packaged circuits. Conductors in this system are designed to carry larger currents than the conductors in the signal distribution system. There is a hierarchy of conductors distinguished by their technology and current levels such as (1) chip level—thin film (10 mÅ to 1 Å), (2) package/chip carrier level—thin or thick film (1 Å to 10 Å), (3) printed wire board level—printed wires (10 Å to 100 Å), (4) large system level—bus bars (kÅ). A typical dc problem: for given current (I), voltage level (E), voltage drop tolerance (η in %), and conductor length (D), determine the conductor geometry-cross section (Å) and material (with resistivity ρ) such that the voltage drop satisfies the inequality $\rho(D/A)I \leq (E\eta/100)$. Usually the voltage drop tolerance is 1% to 2% at each level of interconnection. Typically, the conductor material is imposed by other considerations and designer decisions are restricted to the selection of the conductor cross section.

Switching Perturbations. Transitions between logic levels are associated with current transitions in digital circuits. These transient currents flow on power/ground conductors and cause transitional voltage drops because of parasitic inductive parameters of conductors. These voltage drops are often termed switching noise or alternatively $\Delta - I$ noise and are very undesirable because they may cause false switching. The perturbations are magnified by simultaneous switching of many gates as the effects of current changes in individual gates may cumulate. For this reason switching perturbations are also called simultaneous switching noise. Switching perturbations may manifest themselves on power or ground lines. In reference to effects on ground lines these perturba-

tions are called ground bounce. More details concerning these effects are given in the section on the mechanism of switching perturbations. Analysis of switching noise and estimation of its levels and effects is in general not easy because the power and ground conductors have very complex shapes (wires, pins, perforated plates, etc.), which makes electrical modeling quite difficult. There are several publications proposing analysis of switching effects with the use of effective inductance of ground and power connections. This type of analysis is restricted to some special structures with long interconnections that can be adequately represented by the effective inductance. However, many practical structures involve ground and power plates that cannot be meaningfully represented by an effective inductance, and specialized, sophisticated numerical software has to be used in design. The advantage of effective inductance is that it is very simple and could be used for pedagogical purposes, as is done below, to explain the mechanism of switching perturbations.

Mechanism of Switching Perturbations. The mechanism of switching perturbations is explained using an example of signal transmission between two CMOS chips (Fig. 5), showing the line drivers on chip A and the receivers on chip B with their respective power (V_{DD}) and ground connections (V_{SS}). Here, for the sake of simplicity, we utilize the effective inductance of power connections, L_{DD}, and the effective inductance of ground connections, L_G. We shall assume that a group of drivers switches (i.e., changes their logical state as a result of an input signal), while the input signal to one (or more) of the drivers remains constant. Such a driver with constant input signal will be called quiescent. We shall discuss the effect of switching in the signal line involving this driver. We will consider two simplified cases: (1) the switching drivers are at logic "1," with their output voltages close to V_{DD}, and they receive an input signal to switch to logic "0" while the quiescent driver is at logic "0" with its output voltage close to the ground level; (2) the switching drivers are at logic "0," with their output voltages close to V_{SS}, and they receive an input signal to switch to logic "1" while the quiescent driver is at logic "1" with its output voltage close to V_{DD}. In case (1), the drivers originally maintained the interconnecting lines charged to the level of their output voltage (V_{DD}) and, as a result of changing input signals, they discharge the line charges to the ground through their ground connections, to bring the line potentials to the level of V_{SS}. The discharging currents cause a voltage drop on ground connections due to their parasitic inductive effects. Considering a simplified model with effective inductance, L_{G1}, this voltage drop is proportional to the rate of change of discharging current, $L_{G1}(di_D/dt)$, where i_D is the total line discharging current. In a typical CMOS design with first-reflection switching the discharging occurs in two steps and the rate of change in discharging current of one switching driver is $1/2\ V_{DD}/1.2t_rZ_o$. In derivation of this formula it is assumed that V_{DD} represents the potential difference between power and ground lines which in CMOS circuits is the same as the logic swing V_{LS}. The total effect may be approximated by multiplication of this quantity by the number of simultaneously switching drivers. The described voltage drop will raise the potential on the ground conductors on the chip A with respect to V_{SS} and consequently the output of quiescent driver will rise. This phenomenon is often called ground bounce. The corresponding receiver on the chip B will not be able to detect that this rise is caused by the switching perturbation and not by the input signal, which may lead to false switching if the perturbation exceeds the level of receiver noise tolerance. In the case of (b) the signal lines connected to switching drivers are originally discharged and in the transition they are charged to V_{DD} (this involves two steps due to the first reflection switching in CMOS). The transitional currents, i_C, are drawn via power lines and they cause the voltage drop $L_{DD1}(di_C/dt)$ on the power connections. Consequently, the voltage on the power connections in the chip A drops by this amount from V_{DD} and the output voltage of the quiescent driver follows this drop, which is interpreted by the corresponding receiver on the chip B as a change in the signal. Again, if the perturbation is large it may lead to false switching. The rate of change in the charging current for CMOS circuits implementing first-reflection switching can be estimated by the formula given above. It should be emphasized here that the most difficult element in evaluation of switching perturbations is the estimation of inductive effects of power or ground connections represented in this discussion by the effective inductances (L_{DD1}, L_{G1}). Typical bipolar drivers and receivers in ECL technology are designed for the first reflection switching where the drivers output impedance is significantly smaller than the line characteristic impedance and the receivers input impedance is matched to the line. In this case the rate of driver current change can be estimated as $V_{LS}/1.2t_rZ_o$. The simple discussion presented here shows that level of switching perturbations is proportional to the effective inductance of power/ground connections and number of simultaneously switching drivers and inversely proportional to the rise time and characteristic impedance of signal lines. This indicates some of the techniques that are used to reduce the switching effects such as: (1) reduction of inductive parasitics of connections by design of wide, closely spaced ground and power conductors and allocation of several package I/O connections

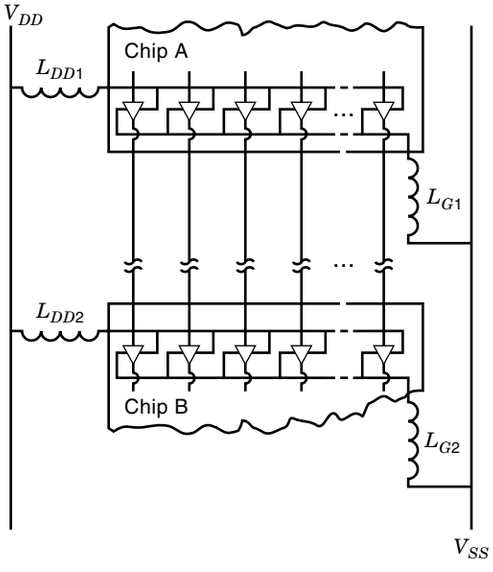

Figure 5. Schematics of signal connections between drivers on the chip A and the receivers on the chip B showing power and ground connections with parasitics represented by equivalent inductors (L_{DD1}, L_{DD2}, L_{G1}, L_{G2}) used to illustrate the mechanism of switching perturbations.

("pins") to ground and power, (2) reduced logic swing (this technique agrees with the general trend toward circuits operating at lower voltages), (3) tradeoffs like increased characteristic impedance (usually lowers the speed by increasing the total signal delay) or decreased rise time (again, it lowers the speed). A common technique for reduction of switching effects is the use of by-pass capacitors which provide the charge (current) needed for the transitions, thus reducing the currents flowing from power supply, and are replenished with charge during quiescent periods. The by-pass capacitors should be placed as close as possible to the circuits undergoing transitions. However, due to space restrictions, which limit the capacitor sizes we have small on-chip capacitors, in proximity to the circuits, larger capacitors built into packages, and large, discrete capacitors on printed wire boards.

Interconnection Technology, Models, and Model Parameters. The interconnections are formed by chip-substrate connections (bonding), package carrier lines, package-printed wire board connections, printed wire board (PWB) lines, vias, connectors, and system cables. Chip-substrate interconnections are made using one of the three following techniques: wire bonding (WB), tape-automated bonding (TAB), or controlled collapse chip connection (C4) also called flip-chip (FC) technology. Chip package-PWB connections are made using pins for plated through hole (PTH) mounting or J-leads, gullwings, solder balls in the surface mounting technology (SMT). Chip-substrate bonding structures and PWB connectors are usually modeled using lumped equivalent circuits composed of resistors R, inductors L, and capacitors C. Chip lines are usually modeled as lumped equivalent networks composed of resistors R or resistors and capacitors C. Some on-chip connections are modeled as distributed R, C lines. New, larger, and high-speed integrated circuits with submicron devices will require modeling of distributed interconnection effects. Chip carrier lines, PWB lines, and cables are modeled as distributed lossless or lossy transmission lines. Line junctions, bends, and vias are modeled using lumped equivalent R, L, and C circuits.

Interconnections are three-dimensional structures that are represented by models simplified to a one-dimension (transmission line models) or to lumped equivalent circuits. Parameters of the models are determined using the principle of equivalency of energy stored (or power dissipated) in the model and in the actual interconnecting structure. The concepts will be illustrated first using the example of two conductors (signal and reference conductors).

The equivalency of power dissipated at direct current (dc) conditions in the model and in the homogeneous metal (resistivity ρ) strip (width w, thickness t) yields the following formula for the distributed resistance in the units (ohms per centimeter):

$$r = \frac{\rho}{wt}$$

Definition and calculation of alternating current (ac) resistance (resistance at ac steady state) is more complicated. The time-average power dissipated in the actual conductor in the steady ac state is

$$P_c = \frac{1}{2}\int_S j^* \left(\frac{j}{\rho}\right) dS$$

where S is the conductor cross section, j is the current density, and j^* is the conjugate current density. The calculation of power involves solution of quasi-static field equations. The power dissipated in the model is

$$P_M = \frac{1}{2} I^2 r_{ac}$$

where I is the magnitude of the total current flowing through the conductor and r_{ac} is the equivalent ac resistance.

The power equivalency ($P_M = P_c$) yields the ac resistance

$$r_{ac} = \frac{\int_S j^* \left(\frac{j}{\rho}\right) dS}{I^2}$$

which accounts for the skin effect well known in electromagnetism.

Approximate Evaluation of the Skin Effect. A simple one-dimensional analysis of infinite half-open homogeneous metal layer of resistivity ρ shows that the electric field decays exponentially in the direction z perpendicular to the metal surface (4)

$$E_x = E_o e^{z/\delta}$$

where the quantity $\delta = \sqrt{\rho/(2\pi\mu f)}$ is called the skin depth, μ is the metal permeability, and f is the field frequency (3). The skin effect can be interpreted by replacing the metal layer by a sheet of thickness δ, where the sheet resistance $R_s = \rho/\delta = \sqrt{2\pi\mu\rho f}$ is proportional to the square root of the frequency. Specific quantities for copper, aluminum, and silver are, respectively, $R_{Cu} = 2.61 \cdot 10^{-7}\sqrt{f}$, $R_{Al} = 3.26 \cdot 10^{-7}\sqrt{f}$, and $R_{Ag} = 2.52 \cdot 10^{-7}\sqrt{f}$ all in the units of ohms per square. Using the same concept of sheet conductance, the resistance r_{ac} per unit of length of uniform conductor of width w and thickness t can be approximated as follows:

$$r_{ac} = \frac{\rho}{S_{eq}} \approx \frac{\rho}{2(w+t)\delta} = \frac{1}{\sqrt{2}}\frac{1}{w+t}\sqrt{\pi\mu\rho f}$$

where S_{eq} is the equivalent area of conductor (of thickness δ) available for current conducting. The total resistance [including the direct current (dc) part] of such a square conductor can be expressed as

$$r = r_{dc} + r_{ac} = \frac{\rho}{wt} + \frac{1}{\sqrt{2}}\frac{1}{w+t}\sqrt{\pi\mu\rho f} = \frac{\rho}{wt} + \frac{1}{2}\frac{1}{w+t}\sqrt{\mu\rho\omega}$$

This formula may be used to evaluate the effect of resistive losses on signal transmission. This approximation is better for low and high frequencies. It is not very good for medium frequency range (megahertz) frequencies.

The equivalency of magnetic energy stored in the structure and in the model yields the inductance (per unit of length) of the conductor. The time average magnetic energy stored in the conductor is

$$u_c = \frac{1}{4}\mathrm{Re}\left\{\int_S j^* \cdot A\, dS\right\}$$

where A is the magnetic vector potential calculated via solution of steady state field equations determined by a current

source forcing the sinusoidal current through the conductor. The symbol Re{·} designates the real part of the complex quantity in the brackets. The time average magnetic energy stored in the model is

$$u_{\mathrm{M}} = \frac{1}{4}\ell I^2$$

where I is the amplitude of current source and ℓ is the model inductance per unit of length. The magnetic energy equivalency yields

$$\ell = \frac{4u_{\mathrm{c}}}{I^2} = \frac{\mathrm{Re}\left\{\int_S j^* \cdot A\, dS\right\}}{I^2}$$

Analogously, the capacitance per unit of length can be determined on the basis of electrostatic energy equivalency. The electrostatic energy is proportional to the product of voltage (potential difference between the signal and reference conductors) and charge stored in the structure. With dc potentials, the voltage is constant; therefore, the equivalency condition can be expressed in terms of charges, which simplifies the computation. The charge Q_{c} stored in the conductor is computed via solutions of electrostatic field equation, and the charge stored in the model is $Q_{\mathrm{m}} = cV$, where c is the capacitance of the structure per unit of length and V is the potential difference between the signal and the reference conductors. The equivalency principle yields

$$c = \frac{Q_{\mathrm{c}}}{V}$$

Multiconductor Interconnections. Modeling of interconnections formed by m parallel and perfect conductors emerged in homogeneous dielectric layers with the dielectric constant ϵ_{r} will be presented in this section. Then effects of material imperfections such as resistivity of conductors and dielectric losses in insulators will be discussed. A cross section of a representative interconnection structure is shown in Fig. 6. The interconnection capacitance matrix C is defined using the Maxwell electrostatic formula depicting the relations between the charges on the conductors q_i and the conductor potentials V_j with respect to the reference:

$$q_i = c_{i1}V_1 + c_{i2}V_2 + \cdots + c_{im}V_m$$
$$i = 1, 2, \ldots, m$$

Solution of electrostatic field equations defined by the applied potentials yields the charges, and then the capacitance c_{ij} values are computed using the Maxwell formula. The resulting values are usually arranged in the form of capacitance matrix $C = \|c_{i,j}\|_{i,j=1}^{m}$, which is symmetric and diagonally dominant. The elements of the matrix do not determine capacitances in the sense used in the circuit theory; for example, the off-diagonal elements are negative. To emphasize this difference, they are sometimes called Maxwell capacitances. The structure inductances are computed using the fact that the product of inductance and capacitance matrices for the same conductor structure formed in vacuum satisfies the relation $LC^0 = (1/\nu^2)\mathsf{E}$, where C^0 is the capacitance matrix computed under the assumptions that all dielectric constants are unity (this corresponds to the replacement of dielectrics by vacuum), ν is the velocity of light in vacuum, and E is the unity matrix. Thus the inductance matrix is computed using the formula

$$L = \frac{1}{v^2}(C^0)^{-1}$$

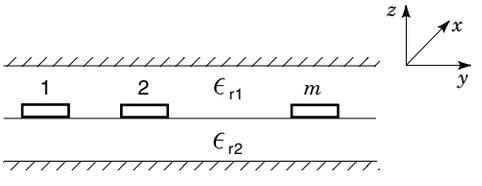

Figure 6. Cross section of prototypical interconnecting structure showing the conductors formed on a dielectric layer (ϵ_{r2}) and coated by another dielectric layer (ϵ_{r2}), all sandwiched between two conductive planes.

Imperfect Dielectrics. Two types of imperfect dielectric substrates are used in packaging: (1) substrates with polarization losses that are usually observed in organic materials such as, for example, very common printed wire board material composed of glass fiber cloth with epoxy resin filler (an example of this category is FR-4, which is Electronic Industries Association's designation for fire-retardant epoxy resin/glass laminate), (2) substrates with ohmic losses that are encountered in multichip modules using high resistivity silicon ($\approx$ 300 kΩcm) as a substrate. These two types of losses result in material behavior depending on frequency of transmitted signals. Lossy dielectric is characterized by a complex dielectric coefficient:

$$\epsilon_{\mathrm{r}} = \epsilon_{\mathrm{r}}' - j\epsilon'' \quad ; \quad j = \sqrt{-1}$$

or by loss tangent

$$\tan\delta = \frac{\epsilon_{\mathrm{r}}''}{\epsilon_{\mathrm{r}}'}$$

and the magnitude $\sqrt{(\epsilon_{\mathrm{r}}')^2 + (\epsilon_{\mathrm{r}}'')^2}$ or real part of the dielectric coefficient ϵ_{r}'. These quantities should be specified as functions of frequency. The polarization losses are negligible at low frequencies. The resistive losses show at low and moderate frequencies, and their effect drops with frequency as indicated by the approximate [valid for moderate frequencies $>$ 20 MHz and such that $\sigma/(2\omega\epsilon_{\mathrm{r}}\epsilon_0) \leq 1$] loss tangent formula (polarization losses are included) $\tan(\delta) = (\epsilon_{\mathrm{r}}''/\epsilon_{\mathrm{r}}') + \sigma/(\omega\epsilon_{\mathrm{r}}\epsilon_0)$, where σ represents the conductivity of substrate layer. For example, at the frequency of 800 MHz, the loss tangent due to the ohmic losses $(\sigma/\omega\epsilon_{\mathrm{r}}'\epsilon_0)$ in high resistivity silicon substrate $(300\ k\Omega cm)$ is of the same order as the loss tangent due to polarization losses $(\epsilon_{\mathrm{r}}''/\epsilon_{\mathrm{r}}' = 10^{-3})$. At the frequency of 8 GHz, the ohmic loss tangent in the same material drops one order of magnitude below the polarization loss tangent.

Effect of Dielectric Losses on Modeling. Considering admittance $Y = j\omega C$ related to structure capacitive effects with capacitance $C = \epsilon_{\mathrm{r}}C_0$, we obtain

$$Y = \omega\epsilon_{\mathrm{r}}''C_0 + j\omega\epsilon_{\mathrm{r}}'C_0$$

which indicates clearly that dielectric losses are modeled by the conductance to the ground $g(\omega) = \omega\epsilon_{\mathrm{r}}''C_0$ and capacitance $C_{\mathrm{L}}(\omega) = \epsilon_{\mathrm{r}}'C_0$.

Imperfect Conductors. Resistivity of conductor material influences the inductance and resistance matrices of the structure model. Computation of those matrices involves solution of steady-state electromagnetic fields imposed by the sinusoidal current sources $I_k(t) = I_k \cos(\omega t + \phi_k)$ appropriately connected to the conducting traces. The inductances are defined by the principle of equivalency of magnetic energy stored in the model and the actual structure yielding

$$\ell_{ii} = \frac{4u_{ii}}{I_i^2}$$

where u_{ii} is the magnetic energy stored in the system when the ith conductor is driven and all others are left open and

$$\ell_{ij} = \frac{2u_{ij} - u_{ii} - u_{jj}}{I_i I_j}$$

where u_{ij} is the magnetic energy stored in the structure when ith and jth conductors are driven by the current source of amplitudes I_i and I_j, respectively, and the remaining ones are open. The resistances are defined using equivalency of power dissipated in the model and in the structure, which results in

$$r_{ii} = \rho_i \frac{\int_{S_i} |J_i|^2 dS}{\frac{1}{2} I_i^2} \qquad r_{ij} = \rho_j \frac{\int_{S_j} |J_j|^2 dS}{\frac{1}{2} I_i^2}$$

where J_i and J_j are the current densities in the ith and jth conductors, conductor ith is assumed to be driven, and remaining conductors are open.

There are many commercial and public domain programs available for computing capacitance and inductance maxtrices for models of interconnections constructed with perfect materials, as well as more involved software packages for computing, capacitance, conductance, inductance, and resistance matrices of imperfect interconnection models.

SIMULATION OF SIGNAL TRANSMISSION

Simulation of signal transmission on interconnections may involve lumped models in the form of networks composed of resistors R, inductors L, and capacitors C; distributed models of perfect interconnections in the form of lossless transmission lines; and distributed models of imperfect interconnections in the form of lossy transmission lines. The computational efforts in simulation of signal transmission in lumped models are insignificant, but they are very significant in the case of lossy transmission line models. Therefore, in practical applications it is important to select the simplest model that would adequately depict most critical phenomena in signal transmission. The selection is based both on physical length of interconnections and speed of transmitted signals, which may be specified by the signal rise time or maximum frequency in the spectrum of signals to be transmitted. Actually a digital signal characterized by its rise time can be represented by a spectrum of signals determined using the Fourier transformation of periodic clock signal where the clock period is approximately 10 times the rise time (this is a "rule of thumb" used by some designers). The clock signal is assumed to be approximated by a train of trapezoidal pulses with identical rise and fall times, t_r, interval of time at high level, 3.8 t_r, and the separation between the pulses equal to 3.8 t_r. The periods 3.8 t_r between the transitions are needed for signals to settle. This setting time is needed because of imperfections in transmission (ringing on the lines) and clock skew. The highest frequency of signal (3-rd harmonic) that would have to be transmitted can then be determined as follows:

$$f_{\max} = \frac{0.3}{t_r}$$

Using this approximation, the modeling criteria based on the ratio of rise time t_r and the line time delay t_D, also called the time-of-flight (TOF), are constructed. This last term (TOF), which is used to emphasize that delay, is the time that is necessary for a signal to travel through the entire line length. In the lossless line defined by the parasitic parameters ℓ and c (representing the line inductance and capacitance per unit of length), the time delay is given by the formula $t_D = D\sqrt{\ell c}$, where D represents the line length. The modeling criteria are put in the following form:

$\frac{t_r}{t_D} \geq 100$
: the interconnection can be modeled as an ideal wire,

$4 < \frac{t_r}{t_D} < 100$
: the interconnection can be modeled as a lumped circuit, composed of resistor R, and capacitor C,

$\frac{t_r}{t_D} \leq 4$
: the interconnection should be modeled as a transmission line.

These criteria are established analyzing responses of simplified models to a runup excitation (rising linearly from zero to constant value with given rise time), comparing them with the exact transmission line solution, and accepting the model when its amplitude error does not exceed 12.5%.

Simulation of Signal Transmission on Perfect Interconnection

Perfect interconnection composed of one signal and one reference conductor, both with negligible resistance separated by an ideal dielectric, is modeled as a lossless transmission line described in the time-domain by the equations

$$\frac{\partial u}{\partial x} = -\ell \frac{\partial i}{\partial t}, \quad u = u(x,t)$$
$$\frac{\partial i}{\partial x} = -c \frac{\partial u}{\partial t}, \quad i = i(x,t)$$

where the symbols ℓ and c represent inductance and capacitance per unit of length of interconnecting structure, u is the potential of signal conductor with respect to the reference conductor, and i is the line current (i.e., the current in the signal conductor).

Mathematical analysis of these equations reveals the following important quantities: (1) unit time delay $\tau = \sqrt{\ell c}$, (2) time delay $t_D = \text{TOF} = D\tau = D\sqrt{\ell c}$ with D representing the line length, (3) characteristic impedance $Z_0 = \sqrt{\ell/c}$. A solu-

tion of transmission line equations was investigated by French scientist J. d'Alembert who determined that it may be decomposed into forward (positive x-direction) traveling wave, $u_+(x,t) = u_+(t - \tau x)$, and reverse (negative x-direction) traveling wave, $u_-(x,t) = u_-(t + \tau x)$, such that the total solution for the line voltage $u(x,,t)$ and the line current $i(x,t)$ may be expressed as follows:

$$u(x,t) = u_+(x,t) + u_-(x,t)$$
$$i(x,t) = \frac{u_+(x,t)}{Z_0} - \frac{u_-(x,t)}{Z_0}$$

An important effect in signal transmission is reflection at the line terminations and in general in points of discontinuity where the line impedance changes. An interaction of transmission line with terminating circuits is described by the voltage reflection coefficients ρ_D at the driver's output terminals and analogous reflection coefficient ρ_R at the receiver's input. These coefficients are defined using the driver output impedance Z_D, the receiver's input impedance Z_R, and the line characteristic impedance as follows:

$$\rho_D = \frac{r_D - Z_0}{r_D + Z_0}, \quad \rho_R = \frac{r_R - Z_0}{r_R + Z_0}; \quad -1 \le \rho_{D\langle R\rangle} \le 1$$

Effect of Material Imperfections

Interconnections constructed using conductors with resistance and dielectric materials with losses are modeled as lossy transmission lines with models determined in the frequency domain

$$\frac{dV}{dx} = -(r + j\omega\ell)I; \quad V = V(x,\omega), \quad V = F\{u(x,t)\}$$
$$\frac{dI}{dx} = -(g + j\omega c)V; \quad I = I(x,\omega), \quad I = F\{i(x,t)\}$$

The symbol $F\{\cdot\}$ represents the Fourier transform of the time-domain functions of line voltage and current, respectively. The definitions of model parameters [ℓ line inductance, $r = r(\omega)$ conductor resistance, c line capacitance, and $g = \omega\epsilon_r'' C_0$ dielectric conductance, all expressed per unit of length] are given in the section dealing with modeling.

For uniform lines (r, l are constant vs. x), the model can be written in the form of wave equation

$$\frac{d^2V}{dx^2} = \underbrace{(r + j\omega\ell)(g + j\omega c)V}_{\gamma^2}$$

where $\gamma = \sqrt{(r + j\omega\ell)(g + j\omega c)}$ is the propagation coefficient. The propagation coefficient can be expanded into real and imaginary parts

$$\gamma = \alpha + j\beta$$

The real part α is the attenuation coefficient and the imaginary part β is the quantity characterizing frequency.

A general solution of wave equation in frequency domain is of the form

$$V = V_+ e^{-\gamma x} + V_- e^{\gamma x}$$

where V_+, V_- are phasors of forward and backward propagating voltage waves, respectively.

The characteristic impedance (derived using the general equation) is

$$Z_c = \sqrt{\frac{r + j\omega\ell}{g + j\omega c}}$$

From the solution in the frequency domain, we can obtain the time domain solution using

$$V(t) = \mathrm{Re}\{Ve^{j\omega t}\}$$

After some simple transformations we get

$$V(t) = V_+ e^{-\alpha x} \cos\left[\omega\left(t - \frac{\beta}{\omega}x\right)\right] + V_- e^{\alpha x} \cos\left[\omega\left(t + \frac{\beta}{\omega}x\right)\right]$$

It should be noted that the ratio β/ω has the dimension of time per unit of length and corresponds to the unit time delay τ, which is defined for the lossless transmission line. Qualitative discussion of solution in this general form is quite difficult. There are two simplifiations that can be used: (1) low loss approximation, which assumes $r \ll \omega\ell$ and $g \ll \omega c$, and (2) low loss conductor on a perfect dielectric, which assumes $r \ll \omega\ell$ and $g \equiv 0$. In order to describe the role of conductor losses in signal transmission, we shall use the second approximation as well as the complex algebra relations given in Reference 4 in order to obtain the attenuation coefficient

$$\alpha \cong \frac{r}{2Z_0}$$

the "unit time delay"

$$\tilde{\tau} = \frac{\beta}{\omega} \cong \tau\left[1 + \frac{1}{2}\left(\frac{r}{2\omega\ell}\right)^2\right]$$

and the characteristic impedance

$$Z_c \cong Z_0\left[1 + \frac{1}{2}\left(\frac{r}{2\omega\ell}\right)^2 - j\frac{r}{2\omega\ell}\right]$$

where $Z_0 = \sqrt{\ell/c}$ is the characteristic impedance and $\tau = \sqrt{\ell c}$ is the unit time delay of lossless line.

It should be noted that with the increasing frequency ω, we have a decrease in unit time delay $\tilde{\tau}$ (or equivalently increase in the velocity v of the traveling wave). Consequently, the conductor resistance is responsible for (1) attenuation (amplitude of signal decreases with x) and (2) dispersion (velocity of signal component increases with its frequency).

Transient in a Transmission Over a Low-Loss Line Constructed on a Perfect Dielectric. The mathematical model of the line is

$$\frac{dV}{dx} = -(r + j\omega\ell)I$$
$$\frac{dI}{dx} = -j\omega cV; \quad \gamma = \sqrt{(r + j\omega\ell)j\omega c}$$

It is convenient to use the notation $r + j\omega\ell = z$, where the resistance r has dc and ac components.

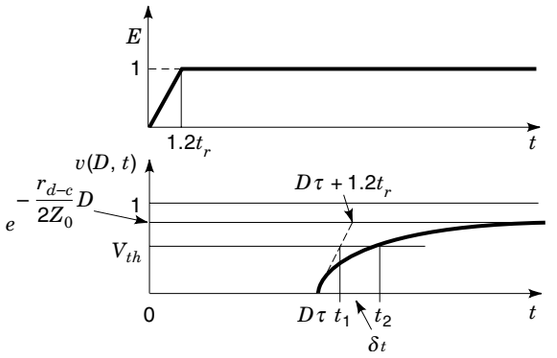

Figure 7. Response of a lossy transmission line (b) to the ramping excitation (a) illustrating transport delay ($D\tau$), attenuation ($\alpha = \exp(-(r_{DC}/2Z_0)D)$), dispersion, and the contribution of skin effect to the signal delay (δt).

Using the notation $\eta = \sqrt{\mu\rho/2}\ [1/(w + t)]$ and algebraic identity $1/\sqrt{2} = \sqrt{j} - j(1/\sqrt{2})$, we can write

$$r = r_{\mathrm{dc}} + \eta\sqrt{j\omega} - j\eta\sqrt{\frac{\omega}{2}}$$

and

$$z = r_{\mathrm{dc}} + \eta\sqrt{j\omega} + j\left(\omega\ell - \eta\sqrt{\frac{\omega}{2}}\right)$$

where $r_{\mathrm{dc}} = \rho/A$ and A is the conductor cross-sectional area.

With a low-loss assumption ($r \ll \omega\ell$), we have

$$r_{\mathrm{ac}} \ll \omega\ell \Rightarrow \eta\sqrt{\frac{\omega}{2}} \ll \omega\ell$$

which results in

$$z = r_{\mathrm{dc}} + \eta\sqrt{j\omega} + j\omega\ell$$

and the propagation coefficient

$$\gamma = \sqrt{zj\omega c} = \sqrt{j\omega c r_{\mathrm{dc}} + j\omega c\eta\sqrt{j\omega} + (j\omega)^2\ell c}$$

The propagation coefficient can be approximated (4) as follows:

$$\gamma \cong j\omega\tau + \frac{r_{\mathrm{dc}}}{2Z_0} + \sqrt{j\omega}\frac{\eta}{2Z_0}$$

where $Z_0 = \sqrt{\ell/c}$.

For the transient analysis we assume that $j\omega = s$, where s is the differential operator and obtain

$$\gamma(s) = s\tau + \sqrt{s}\frac{\eta}{2Z_0} + \frac{r_{\mathrm{dc}}}{2Z_0}$$

Assuming the unit ramp excitation (Fig. 7), with the slope 1/1.2 tr, at the near-end ($x = 0$) of the perfectly matched or infinitely long line described by the wave equation in the operator (s) domain

$$\frac{d^2V(x,s)}{dx^2} = \gamma^2(s)V(x,s)$$

we obtain (via the solution in the operator domain at $x = D$ and inverse operator transformation) the time-domain solution at $x = D$ in the form

$$v(D,t) = e^{-r_{\mathrm{dc}}/2Z_0}[p(t - \tau D)u(t - \tau D) - p(t - \tau D - t_{\mathrm{r}})u(t - \tau D - t_{\mathrm{r}})]$$

where $u(\xi)$ is the unit step function, which is zero for negative argument and one for the nonnegative values of the argument.

The function $p(\cdot)$ is defined as follows:

$$p(\xi) = \frac{\xi}{t_{\mathrm{r}}}\left[\left(1 + \frac{b^2}{2\xi}\right)\mathrm{erfc}\left(\frac{b}{2\sqrt{\xi}}\right) - \frac{b}{\sqrt{\pi\xi}}e^{-b^2/4\xi}\right];$$

$$b = \frac{\eta}{2Z_{\mathrm{o}}}D$$

$$\mathrm{erfc}(\chi) = \frac{2}{\sqrt{\pi}}\int_{\chi}^{\infty} e^{-y^2}dy$$

where $\mathrm{erfc}(\cdot)$ is a complementary error function. Plot of the solution at $x = D$ (Fig. 7) shows the effect of attenuation due to the dc resistance and dispersion due to the skin effect. In further discussion of attenuation and skin effect it will be convenient to introduce the notation $e^{(-r_{DC}/2Z_0)D} = \alpha$ and $p(t - \tau D)u(t - \tau D) - p(t - \tau D - t_r)u(t - \tau D - t_r) = F(t)$. The maximum tolerable dc resistance may be determined from the condition that in steady state the amplitude of far-end signal, α, must exceed the switching threshold, ν_{th}, which yields $Dr_{DC} < -2Z_0 \ln(\nu_{th})$. Note that in general ν_{th} represents a multiplier (fraction) of logic swing. A contribution of skin effect to the delay, δt, can be computed as $\delta t = t_2 - t_1$, where t_2 is the time when the far-end signal (with attenuation and dispersion) reaches the threshold and t_1 is the time when the far-end signal without dispersion, but with attenuation reaches the threshold. The time t_1 is defined by the relation $\alpha(t_1 - D\tau)/(1.2t_r) = \nu_{th}$, and the time t_2 can be computed from the relation $\alpha F(t_2) = \nu_{th}$.

Distortion-Free Interconnections. It is worth mentioning another special type of interconnections in which the model parameters satisfy the relation $r/\ell = g/c$ such that the propagation coefficient can be written in the form $\gamma = \kappa\sqrt{\ell c} + j\omega\sqrt{\ell c}$, where κ is the constant defined by the model parameter ratio $\kappa = r/\ell = g/c$. In this case, the attenuation coefficient and line delay are independent of frequency, and the signal propagation is distortionless. This type of interconnection is designed for telecommunication applications but is not common in electronic packaging.

Numerical Calculation of Model Parameters

The model parameters are obtained using equivalency principles of energy stored in a structure and its model. The energy stored in a structure is usually obtained via numerical solution of electromagnetic field equations. A large body of commercial and public domain software is available for such calculations. Some of the better-known software packages are HFSS (5), Mafia (6), and Maxwell (7) and can be used for solution of two- and three-dimensional static and frequency-dependent problems. Interconnections are piecewise, uniform, straight transmission lines connected to discontinuities like vias, wire bonds, junctions, bends, and connectors. Exploiting

the uniform cross section of lines, one can calculate the model parameters, solving two-dimensional problems. The capacitance c is calculated using the solution of an electrostatic field problem. In cases when frequency dependence of inductance can be neglected, the Maxwell relation $LC = \mu\epsilon I$ (where I is the unity matrix) can be utilized for calculation of L. This relation is valid when conductor and dielectric are perfect. To calculate L, R, G in case of imperfect materials, one has to solve the quasi-static field problem because the currents must be taken into account. When frequency dependencies must be considered, then the L, R, G matrices are computed via field solutions in the frequency domain. Discontinuities are modeled using equivalent circuits. The structure of an equivalent circuit must be assumed in advance, and its parameters are determined through fitting to the results obtained from a three-dimensional solver used for frequency-domain or time-domain solutions (8). Vias are usually modeled using parallel capacitors, and bond wires are modeled using series inductors. The procedure involving field solvers is time-consuming, and again engineers are forced to use simplifications in determining the parameter values. There are some rules of thumb in use such as the one stating that bond wire has inductance of order 1 (nH/mm). Another option for solving three-dimensional problems is characterization of discontinuities and fitting the model parameters to the measurements. The structure model is assumed, and nonuniqueness of the problem must be considered in model selection. The measurements can be made in the frequency domain with the use of a network analyzer or in the time domain using time-domain reflectometry equipment.

Interconnections On Silicon Substrates

Interconnections on silicon substrates have different characteristics than those formed on typical packaging dielectric materials that have negligible low-frequency conductance. Silicon substrates exhibit finite conductivity at low frequencies, including the dc regime. The importance of modeling such substrates is increasing because silicon is used as a substrate in some multichip packages (Multi Chip Modules with Deposited Structures, known as MCM-D type) and because on-chip interconnections in contemporary, large, and fast chips must be modeled as transmission lines. Typically the metal lines are formed on the layer of silicon dioxide ($t_{ox} \approx 0.2$ μm) grown on the layer of silicon ($t_{Si} \approx 1000$ μm), which is supported by a metal plane (Al). The final conductivity of silicon σ_{Si} ($\sigma_{Si} = \rho_{Si}^{-1}$, where ρ_{Si} is the silicon resistivity) adds special properties to the interconnection such that three modes (9) of signal transmission are possible: (1) quasi-TEM mode, (2) skin effect mode, and (3) slow mode. The quasi-TEM mode is characterized by a small loss tangent, $\tan(\delta) = (\omega\rho_{Si}\epsilon_0\epsilon_{Si})^{-1} \ll 1$. The symbol ϵ_0 represents the permittivity of vacuum, and ϵ_{Si} is the relative dielectric constant of silicon. If the product of the frequency and the resistivity of silicon substrate is large enough such that $\omega\rho_{Si} \gg 1/(\epsilon_0\epsilon_{Si})$, we can assume a double layer with the effective dielectric constant equal to that of silicon. The velocity of signal propagation is then $\nu = c_0/\sqrt{\epsilon_{Si}}$ where c_0 is the velocity of light in vacuum. The skin effect mode that occurs in low resistivity silicon (10^{-2} Ω cm or less) is characterized by a small depth of penetration into silicon $\delta = \sqrt{(2\rho_{Si})/(\omega\mu_0)} \ll t_{Si}$, where μ_0 is the permeability of vacuum. In this case, the line behaves highly dispersively with the velocity of propagation $\nu_{Se} = c_0/\sqrt{\epsilon_{ox}[1 + \delta/(2t_{ox})]}$, where ϵ_{ox} is the relative dielectric constant of silicon dioxide. The slow wave mode occurs when the silicon resistivity is moderate such that the substrate is neither an ideal ground nor an insulator and the frequency of signal is in the low MHz range (no more than 100 MHz). In this case, the electric field concentrates in the silicon dioxide layer, but the magnetic field penetrates the entire layer of silicon. The propagation velocity is given by the formula $\nu_{sm} = c_0/\sqrt{\epsilon_{ox}(1 + t_{Si}/t_{ox})}$, which indicates that the velocity of propagation is reduced significantly (typically $c_0/30 \Rightarrow c_0/40$), hence the name of the mode.

Multiconductor Lines

An example of a mathematical model for an interconnection system composed of two signal conductors (and a reference conductor) constructed of perfect materials consists of two sets of equations: (1) the equations for the line voltages u_1 and u_2

$$\frac{\partial}{\partial x}\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = -\underbrace{\begin{bmatrix} \ell_{11} & \ell_{12} \\ \ell_{21} & \ell_{22} \end{bmatrix}}_{L} \frac{\partial}{\partial t}\begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

and (2) the equations for the line currents i_1, i_2

$$\frac{\partial}{\partial x}\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = -\underbrace{\begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix}}_{C} \frac{\partial}{\partial t}\begin{bmatrix} u_1 \\ u_2 \end{bmatrix}$$

In general, the matrix equation of perfect interconnection composed of m conductors (plus a reference conductor) is

$$\frac{\partial u}{\partial x} = -L\frac{\partial i}{\partial t}$$
$$\frac{\partial i}{\partial x} = -C\frac{\partial u}{\partial t}$$

where L and C are inductance and capacitance matrices, respectively, and u and i represent vectors of line voltages and line currents, respectively. In the form of the wave equation, the interconnection model is

$$\frac{\partial^2 u}{\partial x^2} = LC\frac{\partial^2 u}{\partial t^2}$$

The interconnections modeled by the equations of this type are called lossless transmission lines. The equations are called telegrapher's equations.

Model Properties. The solution of d'Alembert is of the form

$$u = P\underbrace{\begin{bmatrix} g_1(t - \tau_1 x) \\ g_2(t - \tau_2 x) \\ \vdots \\ g_m(t - \tau_m x) \end{bmatrix}}_{u_+} + P\underbrace{\begin{bmatrix} h_1(t + \tau_1 x) \\ h_2(t + \tau_2 x) \\ \vdots \\ h_m(t + \tau_m x) \end{bmatrix}}_{u_-}$$

where the symbol P represents the eigenvector matrix of the matrix LC, and the functions $g_i(t - \tau_i x)$, $h_i(t - \tau_i x)$ where $i = 1, 2, \ldots, m$ are determined by the initial and boundary con-

ditions (excitations). The values $\tau_1, \tau_2, \ldots, \tau_m$ represent unit time delays of corresponding modes. These values are square roots of eigenvalues of the matrix LC, which in general are determined by an involved numerical process especially in the cases of multiple eigenvalues. It is convenient for further discussion to arrange the unit time delays in the form of diagonal matrix T. Analogous to the single-line case, the voltage solution may contain components traveling in the positive direction of the x axis, which are represented by the vector u_+, and components traveling in opposite direction designated by the vector u_-, such that the total line voltage is the superposition of both components (i.e., $u = u_+ + u_-$).

Characteristic Admittance Matrix. The characteristic admittance matrix of a system of coupled transmission lines is defined as an admittance matrix of a perfectly matching terminating network. A brief discussion of techniques for computing the characteristic admittance matrix is included in this section. The model equations can be used to derive the current voltage relation in the form

$$i = L^{-1}PTP^{-1}(u_+ - u_-)$$

which shows that the characteristic admittance matrix relating the voltage waves to the currents waves ($i_+ = Y_0 u_+$, $i_- = -Y_0 u_-$, with $i = i_+ + i_-$) is

$$Y_D = L^{-1}PTP^{-1}$$

It should be noted that the matrix T contains the square roots of eigenvalues of the matrix LC. The diagonalization of LC yields

$$P^{-1}LCP = T^2$$

which shows that

$$PTP^{-1} = (LC)^{1/2}$$

The last relation can be easily verified by a simple multiplication. Finally the characteristic admittance matrix can be computed as follows

$$Y_D = L^{-1}(LC)^{1/2}$$

This formula is quite useful because it shows that the admittance matrix can be computed using directly the square root of matrix LC (10) without performing a complete eigenanalysis, which may be quite involved especially in the case of multiple eigenvalues.

The Matrix of Reflection Coefficients. Analogous to the case of the single line, the terminations may cause reflections. Impedance discontinuities will cause reflections. In practical cases, each line is terminated by a load that is isolated from other loads. Assuming for simplicity the resistive terminations (Fig. 8), it is possible to write the relation between the termination voltages and currents in matrix form

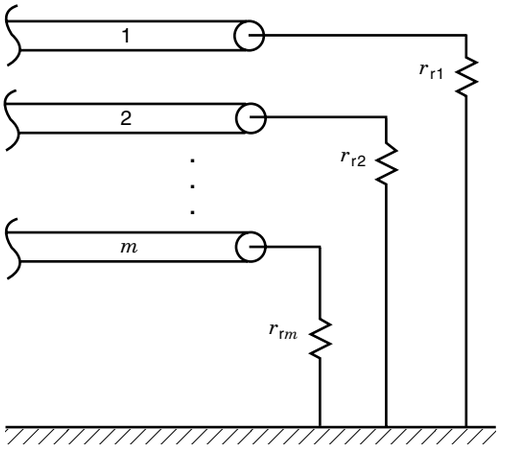

Figure 8. Idealized (resistive) terminations of transmission lines at the far end; schematics used for calculation of reflections and diagonally matched loads.

$$I = Y_L V$$

where Y_L is the admittance matrix of terminations. Using the transmission line equations, it is possible to derive (e.g., at $x = D$) the relation between the incident voltage u_+ and the reflected voltage u_- in the form

$$u_- = (Y_0 + Y_R)^{-1}(Y_0 - Y_R)u_+$$

where Y_R is the admittance matrix of receivers. This relation defines the reflection coefficient matrix at the receiver's end

$$\rho_R = (Y_0 + Y_R)^{-1}(Y_0 - Y_R)$$

Analogous derivation of the reflection coefficient matrix at the drivers' end yields

$$\rho_D = (Y_0 + Y_D)^{-1}(Y_0 - Y_D)$$

where Y_D is the admittance matrix of drivers.

Terminating Loads. In signal transmission, the reflections must be controlled because they generate noise that may cause faults. In the case of a single line, we can control the reflection coefficient by the load impedance. However, in the case of multiconductor lines, we do not have a complete control over the reflections because in practical applications we can control m load values (m is the number of lines) only, but there are $m(m + 1)/2$ different reflection coefficients considering that the matrices $P_{R(D)}$ are symmetric. In the case of bipolar technology, the drivers are designed to achieve minimum output impedance (impedance much smaller than the representative impedance of the lines), and thus the driver end is not properly terminated. Consequently, the receivers' input impedance must be carefully designed to minimize the reflections. The receivers' input impedances can be selected in such a way that the main diagonal elements of the reflection coefficient matrix are zero. For fastest operation, the receivers

should absorb incoming signals at the level of logic swing which yields first incident switching. In the case of CMOS technology, the receivers' input impedance is very high, and thus the receivers' end is practically open, which results in perfect reflections. This phenomenon is incorporated into design of signal transmission, which aims at first reflection switching. In this technology, the drivers' impedance must be selected so that it is close to the representative impedance of lines in order to avoid multiple reflections and resulting problems such as overshoot (and oscillatory behavior of signal in case of low driver impedance) or increased delay (and stepwise increase of signal in case of drivers with too high impedance). In designing for signal integrity in bipolar technology, it is therefore necessary to obtain impedance of receivers close to the lines' impedance and in the CMOS technology the impedance of drivers should be close to the lines' impedance.

Diagonally Matched Loads. The diagonal match consists of such a selection of terminating impedance that the main diagonal in the matrix of reflection coefficients contains elements of zero value

$$\rho_{\mathrm{R(D)}} = \begin{bmatrix} 0 & & \\ & \ddots & \\ & & 0 \end{bmatrix}$$

An efficient iterative algorithm for computation of impedances in the case of diagonal matching is available (11). The experience indicates that the terminations connected to the external conductors should have higher impedance than those connected to the internal conductors. This result is useful for designing bipolar receivers (for the first incident switching) and CMOS drivers (for the first reflection switching).

Near-End Cross-Talk. The near-end cross-talk is discussed using the schematics shown in Fig. 9. The circuit equations are

$$u = E - Y_{\mathrm{D}}^{-1} i$$

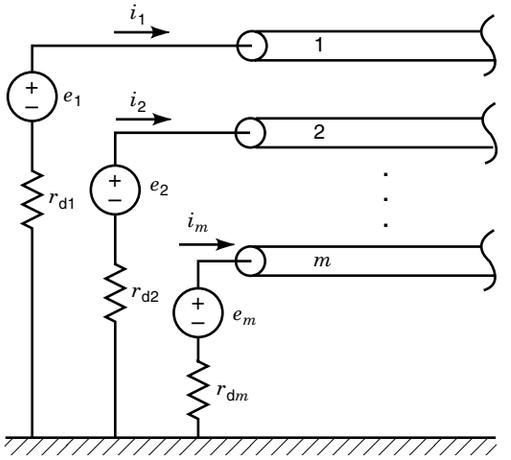

Figure 9. The configuration of ideal drivers and transmission lines (the drivers are represented by their output impedances ($\mathbf{Z}_{\mathrm{di}}$) and voltage sources ($\boldsymbol{e}_{\mathrm{i}}$).

where E is the vector of voltages representing the drivers equivalent sources and Y_{D} is the diagonal matrix of drivers admittances.

The transmission line equations at the near-end ($x = 0$) yield

$$u_+ = (Y_0 + Y_{\mathrm{D}})^{-1} Y_{\mathrm{D}} E + (Y_0 + Y_{\mathrm{D}})^{-1} (Y_0 - Y_{\mathrm{D}}) u_-$$

If the drivers provide the only excitation of lines, then the solution for $0 \le t \le 2t_{\mathrm{D}_{\min}}$, that is, for the time before the arrival of the far-end reflections is

$$u_+ = (Y_0 + Y_{\mathrm{D}})^{-1} Y_{\mathrm{D}} E$$

because during this time $u_- \equiv 0$. The solution so obtained can be used to estimate the near-end cross-talk (neglecting reflection from the far-end). The maximum near-end cross-talk is expected to occur when the center line is quiescent (the so-called listening or victim line) and the surrounding lines are excited in an identical manner. In this case, the vector E has the zero entry corresponding to the position of quiescent line (assume ith line), and the cross-talk is given by the ith component of the vector u_+. The computation of near-end cross-talk for time exceeding $2t_{\mathrm{D}_{\min}}$ and computation of far-end cross-talk is based on the equation of transmission line equivalent circuit because multiple reflections have to be taken into account. This computation is so involved that use of a specialized computer program is necessary.

Far-End Cross-Talk. Far-end cross-talk can be computed assuming resistive terminations. The result (quoted here without derivation) for limited time $t_{\mathrm{D}_{\max}} + t_{\mathrm{r}} < t < 3t_{\mathrm{D}_{\min}}$ (multiple reflections are not included) is given by

$$V_{\mathrm{FE}} = 2(Y_0 + Y_{\mathrm{R}})^{-1} Y_0 (Y_0 + Y_{\mathrm{D}})^{-1} Y_{\mathrm{D}} E$$

Again, as in the case of near-end cross-talk, it is expected that the maximum of far-end cross-talk occurs in the center line under identical excitations of remaining lines.

An Approximate Analysis of Cross-Talk

We shall consider approximate cross-talk relations based on the theory of week coupling (12). For simplicity of formulation, only two identical lines will be considered, and matching at both ends will be assumed. The line 1 will be active, and line 2, passive (listening). The terminating admittance matrices are

$$Y_{\mathrm{D}} = \begin{bmatrix} \dfrac{1}{r_{\mathrm{d1}}} & \\ & \dfrac{1}{r_{\mathrm{d2}}} \end{bmatrix}, \quad Y_{\mathrm{R}} = \begin{bmatrix} \dfrac{1}{r_{\mathrm{r1}}} & \\ & \dfrac{1}{r_{\mathrm{r2}}} \end{bmatrix}$$

The inductance and capacitance matrices under the assumption of line symmetry are

$$L = \begin{bmatrix} \ell_{11} & \ell_{12} \\ \ell_{12} & \ell_{11} \end{bmatrix}, \quad C = \begin{bmatrix} c_{11} & c_{12} \\ c_{12} & c_{11} \end{bmatrix}$$

The weak coupling can be expressed as follows:

$$|c_{12}| \ll c_{11}, \quad \ell_{12} \ll \ell_{11}$$

The specified simplifying assumptions concerning the excitation and matching terminations result in the following relations:

$$E = \begin{bmatrix} e \\ 0 \end{bmatrix}, \quad r_{d1} = r_{d2} = r_{r1} = r_{r2} = Z_0, \quad Z_0 = \sqrt{\frac{\ell_{11}}{c_{11}}}$$

The analysis of the line equations yields the following formula:

$$u_{bo}(t) = \frac{1}{4}\left(\frac{|c_{12}|}{c_{11}} + \frac{\ell_{12}}{\ell_{11}}\right)\frac{e(t) - e(t - 2t_D)}{2}; \quad t_D = D\sqrt{\ell_{11}c_{11}}$$

for the near-end cross-talk (the voltage on line 2 at $x = 0$). The following quantities may be identified in this formula: (1) capacitive coupling coefficient: $k_c = |c_{12}|/c_{11}$, (2) inductive coupling coefficient: $k_\ell = |\ell_{12}|/\ell_{11}$, b) backward coupling coefficient: $K_{one} = \frac{1}{4}(k_c + k_\ell)$. Analogous analysis of the far-end cross-talk ($x = D$) gives the formula

$$u_{fD}(t) = \frac{1}{4}\left(\frac{|c_{12}|}{c_{11}} - \frac{\ell_{12}}{\ell_{11}}\right)D\sqrt{\ell_{11}c_{11}}\frac{d}{dt}[e(t - t_D)]u(t - t_D)$$

where $u(t - t_D)$ is the unit step function with the shifted argument.

An alternative formula using the forward coupling coefficient $K_{fe} = \frac{1}{2}(Z_0|c_{12}| - \ell_{12}/Z_0)$ has the form

$$u_{fD}(t) = \frac{1}{2}K_{fe}D\frac{d}{dt}[e(t - t_D)]u(t - t_D)$$

It should be noted that the far-end cross-talk (also called forward cross-talk) can be positive, negative, or zero, depending on the ratio of the capacitive and inductive coupling coefficients. These coefficients are equal (forward cross-talk is then zero) in the case of conductors placed in a homogeneous dielectric of infinite extend or forming a layer enclosed between two reference planes. The last case is an approximate model of interconnections in multilayer printed wire boards that contain repeated basic structure composed of uniform dielectric layer and conductors enclosed between two reference conductor planes.

Multiconductor Lossy Lines

The mathematical model of lossy multiconductor interconnection is defined in the frequency domain and has the following form:

$$\frac{dV}{dx} = -(R + j\omega L)I; \quad V = V(x, \omega) = \mathcal{F}\{u(x, t)\}$$
$$\frac{dI}{dx} = -(G + j\omega C)V; \quad I = I(x, \omega) = \mathcal{F}\{i(x, t)\}$$

where the symbol $\mathcal{F}(\cdot)$ designates the Fourier transform of the time-domain function, and R, L, G, and C are matrices of resistance, inductance, conductance, and capacitance, respectively. The elements of these matrices are frequency-dependent. These elements are computed using the principles described in the first section of this article dealing with the interconnection electrical modeling. Analysis of signal transmission over lossy lines is so involved that it must be supported by simulation with a use of specialized computer programs. Numerical complications in the simulation arise from the fact that the lines model is defined in the frequency domain whereas the terminations are determined by nonlinear transistor circuits modeled in the time domain. Many programs are offered for simulation of transient behavior of transmission lines with nonlinear circuit terminations. However, each program has its limitations; error analysis and control are usually inadequate, and search for better solution methods and more efficient programs continues.

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CIRCUIT, ANALYSIS IN THE FREQUENCY DOMAIN. See FREQUENCY-DOMAIN CIRCUIT ANALYSIS.

CIRCUIT ANALYSIS IN TIME DOMAIN. See TIME-DOMAIN NETWORK ANALYSIS.

CIRCUIT ANALYSIS, SYMBOLIC. See SYMBOLIC CIRCUIT ANALYSIS.

CIRCUIT BOARDS. See PRINTED WIRING BOARD TECHNOLOGY.