CAD FOR MANUFACTURABILITY OF INTEGRATED CIRCUITS

Computer-aided design (CAD) for manufacturability provides computer support for the design of electronic products and processes for ease of manufacturing throughout their development life cycles. Viewed broadly, CAD for manufacturability supports the optimization of electronic products and processes for profitability. From this perspective, it expands conventional CAD to include manufacturing cost as a primary design criterion. In so doing, it enables this cost to be balanced with other costs and with revenue to optimize the overall profitability of a product or process. Viewed narrowly, CAD for manufacturability focuses on manufacturing variation and its impact on products and processes. From this more common perspective, CAD for manufacturability introduces manufacturing variation into the design process, enabling the effects of this variation to be reduced or balanced with other design factors, such as performance. Although narrower, this second perspective is consistent with the first. Indeed, manufacturing variation incurs a cost in revenue lost due to units scrapped in production or sold at discounted prices due to inferior performance. Thus, variation acts as a surrogate for manufacturing cost. The other design factors determine the market value of the product and, hence, act as surrogates for revenue. Thus, balancing variability and performance in effect optimizes profitability via surrogates.

This article explores the concepts of CAD for manufacturability, reviews the CAD models and methodologies most commonly used to support design for manufacturability (DFM) in practice, and discusses open questions and issues for research. The sections entitled “Concepts of CAD for Manufacturability” and “The Role of CAD for Manufacturability in the Development Life Cycle” treat CAD for manufacturability and DFM from the broad perspective. The section entitled “Concepts of CAD for Manufacturability” defines the relevant concepts, and the section entitled “The Role of CAD for Manufacturability in the Development Life Cycle” considers how CAD can support DFM in different phases of the development lifecycle. Examples from the electronics industry illustrate the applications of CAD for manufacturability. The section entitled “Models and Methods for CAD for Manufacturability” treats CAD for manufacturability from the narrow perspective, reviewing models and methodologies used to introduce manufacturing variation into the design process. The article concludes in the section entitled “Research Directions in CAD for Manufacturability” with a discussion of open questions and issues for research.

CONCEPTS OF CAD FOR MANUFACTURABILITY

Product and Process Development Life Cycle

Figure 1 shows a typical product or process development life cycle as consisting of four phases: definition, implementation, ramp, and volume manufacturing. The life cycle starts with an initial specification of the product or process and a (usually) unspecified number of problems or issues that must be resolved. Progress toward volume manufacturing occurs in cycles of learning and decision-making in which these problems are explored through experimentation and prototyping and suitable solutions are selected. The rate of learning in these cycles determines the time required to reach volume manufacturing. As Fig. 1 shows, most of the life-cycle costs are determined in the definition phase. Indeed, the first 20% of development has been estimated to determine 70% to 80% of the ultimate manufacturing cost of a product (1,2). In contrast, most of the actual expenditure occurs in the transfer and volume manufacturing phases, during which equipment, materials, and labor costs escalate rapidly.

Manufacturability and Yield

Manufacturability, a primary attribute of the quality of an electronic product or process, determines the ease with which the product or process can be manufactured. Thus, a manufacturable product can be ramped rapidly in manufacturing with little or no rework and can be produced correctly and inexpensively at desired levels of output. Similarly, a manufacturable process can be rapidly ramped to high levels of output and can cost effectively produce “good” product with relatively little loss to misprocessing, defects, and variation. (“Good” product is defined to be correctly functioning units meeting product specifications.) Since it determines the ease with which a product or process can be manufactured, manufacturability also determines the costs in time, effort, and money required to ramp it to volume production and to sustain production at volume levels. This includes (1) the *direct costs* of the equipment, materials, and labor required to fabricate, assemble, and test the product and (2) the *indirect costs* associated with the loss of material in manufacturing due to equipment failures, mistakes, defects, parametric variations, and other “process disturbances.” [A *process disturbance* is de-

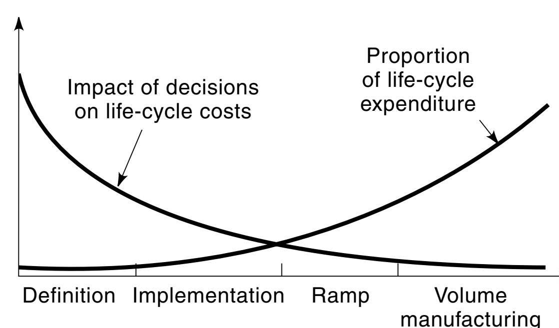

Figure 1. Phases of the product and process development life cycle. This figure shows the four main phases of the process and product development life cycle and illustrates that early decisions have the most impact on life-cycle costs, while most of the costs are incurred late in the life cycle.

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fined as any random phenomenon that manifests itself in a modification of the physical characteristics of a manufactured product (3). Thus, disturbances cause differences among units of a product fabricated using the same process and specifications.]

In CAD for manufacturability, consideration of cost has conventionally been limited to indirect manufacturing costs and to only two types of process disturbance contributing to these costs—defects and parametric variations. *Defects* are isolated events leading to failures or degradation of product performance. They include (1) local disturbances, such as particles leading to shorts or narrow lines, that cause localized failures or degradations of electrical functionality, and (2) global disturbances, such as misalignments, that cause massive failures or degradation in electrical functionality. *Parametric variations* are random fluctuations in process conditions and material properties leading to variations in the local or global characteristics of a product. For example, variations or fluctuations in oven temperatures, the chemical properties of materials, and the optical properties of equipment all contribute to variations in the performance of electronic circuits.

Both types of disturbance can manifest as either functional or performance faults (4,5). *Functional faults* occur when a product fails to function correctly. Defects leading to short circuits and parametric variations causing failures due to timing mismatches between signals are both examples of functional faults. *Performance faults* occur when a product functions correctly, but some measure of performance, such as propagation delay or power consumption, lies outside of a specified range. Both types of fault reduce the *yield* of a process, which is defined as the ratio of the number of units which meet all product specifications after successfully completing all manufacturing steps to the total number of units started in the manufacturing line (4). Two types of yield are conventionally defined, based upon the two types of fault: *functional yield,* incorporating functional failures, and *parametric yield,* incorporating parametric faults.

Design for Manufacturability

DFM is an "integrated approach to designing products and processes for cost-effective, high-quality downstream operation" (1). It incorporates cost as an essential criterion in the design of electronic products and processes and, in so doing, enables cost to be considered early in product and process development, enabling them to be optimized for profitability over their life spans.

The profitability of an electronic product is determined by the cost required to manufacture it, loaded by (1) the costs incurred in developing the product and the manufacturing process and (2) the price the product can attract in the market place. Conventionally, product and process development methodologies partitioned the responsibility for the various components of profitability among separate engineering disciplines. Thus, product engineering groups have conventionally had primary responsibility for those factors determining product price, including the features, performance, and quality of a product and the time at which it appeared on the market. Similarly, process development and manufacturing engineering groups have conventionally had primary responsibility for those factors determining the cost of producing revenue-generating units.

While enabling individual engineering groups to develop a high level of expertise in their respective disciplines, such partitioning of responsibility discourages a business-oriented approach to product and process development, leading to decisions that, while optimal from the narrow view of an engineering group, might not be optimal from the standpoint of the business. For example, product designers might choose a physical design strategy that leads to better performance and, hence, higher unit prices for the product. However, such a strategy might increase the vulnerability of the product to defects and thereby increase manufacturing cost, leading to reduced overall profitability. Similarly, partitioning responsibility can lead to missed opportunities for improving business profitability. For example, integrating self-test capabilities into printed circuit boards will increase design time and fabrication cost, but can reduce test cost and failures in the field, potentially leading to overall cost reductions and profit improvement.

DFM addresses this problem by endorsing an interdisciplinary approach to the development of electronic products and processes. Thus, with DFM, product engineers can consider the impact of their decisions on cost as well as profitability. Similarly, manufacturing engineers can consider the impact of their decisions on market value as well as cost. In effect, DFM encourages the codevelopment of product and process. However, circumstances often dictate the degree to which this can occur. For example, a dedicated manufacturing line might be developed to produce a high-volume microprocessor. In this case, the product and process could be jointly developed to maximize profitability. On the other hand, an ASIC process might be developed to manufacture a broad range of products. In this case, product design decisions would have little or no influence over the process and the process would, at best, be optimized for the planned range of products.

CAD for Manufacturability

DFM comes with its own cost. By introducing another dimension into product and process design, it expands the size of the design space that must be explored, complicating the design process and making it more difficult to achieve optimal results. Thus, in most application areas, DFM requires computer support. CAD can provide this support in three ways. First, manufacturability criteria can be integrated into existing CAD tools, through design rules, guidelines, and simulation conditions formulated to ensure manufacturability (6–9) or through the incorporation of manufacturability-related models, constraints, and objectives in simulation and optimization tools (10–13). Second, tools or frameworks built upon existing simulation and analysis tools can guide engineers through the exploration of design options and assist them in arriving at optimal results (14–17). Third, standalone CAD tools and environments can provide comprehensive support for DFM by enabling cost and revenue to be quantified and optimized (18–21).

Since manufacturability is determined by decisions made throughout the development life cycle, optimization of profitability requires computer support for DFM in all development phases. During definition, DFM introduces manufacturing

cost as an additional criterion to be weighed in selecting implementation strategies and in defining design methodologies. Computer tools support DFM in this phase by enabling the impact of different options on cost and profitability to be quantified through simulation and modeling. During implementation, DFM introduces manufacturing cost as an additional criterion to be balanced in the specification and optimization of the detailed design. Computer tools support DFM in this phase by assisting designers in exploring high-dimensional design spaces for solutions that best satisfy the design goals. Design rules, guidelines, and simulation conditions incorporated in design tools help steer designers toward acceptable solutions. Automatic analysis and optimization tools help designers arrive at superior solutions. In manufacturing, computer tools used for DFM have also found application in helping to diagnose manufacturing problems and in supporting continuous improvement activities (22).

Incorporating manufacturability into the design process requires the representation of manufacturability either directly or by surrogates. Unfortunately, as is true of most quality attributes, manufacturability cannot be directly measured. However, appropriate surrogates do exist and are widely applied. Where practical to estimate, manufacturing cost is the preferred surrogate since it is directly determined by manufacturability and must be estimated to optimize profitability. Since relatively few decisions are made during the definition phase and the decisions made during that phase often have significant impacts on downstream costs, the detailed analysis required to estimate cost can usually be afforded and is highly desirable. However, during implementation, the cost impact of decisions can be difficult or inconvenient to estimate. In these cases, surrogates reflecting the impact of decisions on overall cost and profitability can be used. Yield has been a commonly recommended surrogate for manufacturing cost and must usually be estimated if this cost is to be estimated. However, yield can itself be difficult to estimate in complex designs, especially at low levels in the design hierarchy. In these cases, designers can employ measures of the vulnerability of a design to parametric variations and defects that can be calculated from local information. For example, sensitivity and robustness analyses (5,23,24) can be performed.

THE ROLE OF CAD FOR MANUFACTURABILITY IN THE DEVELOPMENT LIFE CYCLE

CAD for Manufacturability in Product and Process Definition

The importance of the definition phase in determining the overall life cycle costs of a product or process reflects the broad impact of decisions made during this phase. Typical of these decisions are the definition of a manufacturing strategy; the selection of a design style, including electrical and physical design strategies; the definition of product or process development methodologies, including computer tools and usage methodologies; and the definition of high-level architecture, including the major architectural features. Since most of these decisions are discrete and have far-reaching impacts on the product or process, they are typically supported by extensive prototyping and experimentation. Computer tools complement these activities by enabling options to be simulated so that inferior options can be eliminated and choices narrowed before expensive prototyping and experimentation activities are undertaken (25,26). By incorporating manufacturability-related models into the simulation domain, CAD for manufacturability expands the capabilities of conventional simulators, enabling the impact of different options on development and manufacturing cost to be quantified. This enables options to be ranked based on their impact on business profitability.

As an example, Strojwas et al. (27) have considered the use of CAD to compare low-power CMOS technology and implementation options on the basis of their manufacturability. Three technologies were considered for manufacturing lower-power circuits: a scaled-down twin-tub CMOS technology, a triple-well bulk CMOS technology, and a silicon-on-insulator technology. CAD tools were used to project power consumption and circuit performance for each option and to simulate the impact of variability on both of these attributes. CAD tools were also used to optimize device parameters, such as threshold voltage for each option. This enabled the technology options to be compared based on manufacturing cost, power, and performance and the transistors to be optimized for the same criteria.

As another example, Lopez-Serrano and Strojwas (6) demonstrated the use of CAD tools to develop layout design rules balancing the impacts of reduced design rules in a very large scale integration (VLSI) manufacturing process on performance, density, and yield. The authors applied process and device simulators to estimate parametric yield and critical area analysis to estimate functional yield. Analyses were performed on a 2500-transistor 8-bit multiplier and extrapolated to a 500,000-transistor product by multiplying the area by 200. An integrated computer tool suite was applied to perform the Monte Carlo simulations and extrapolations required for the analysis.

More broadly, Levitt et al. (28) describe the selection of manufacturability, "debuggability," and testability features of the UltraSparc microprocessor. At the outset of the project, the product design team set high-level goals balancing cost and revenue considerations. Functional yield goals, expressed as targets for defects per million, and testability goals, ensuring economical testing at all levels of assembly, addressed manufacturing cost. Debuggability goals focusing on enhanced visibility into the product to support product debugging and failure analysis, and yield enhancement addressed cost during the ramp to volume manufacturing and the time to market acceptance. These high-level goals had to be achieved while minimizing the design time impact and performance penalties of the added features, addressing time to market acceptance and sales price. A cost–benefit analysis was performed to guide the selection of features addressing each goal and to facilitate the development of design methodologies.

In another application domain, Sandborn (2) describes CAD tool requirements for balancing cost and performance in the early phases of the design of printed circuit boards. He describes important early life-cycle decisions, such as physical partitioning and the selection of packaging technologies, which must be supported by CAD tools. He describes five classes of tools required to provide this support: life cycle analysis tools, process flow analysis tools addressing cost, manufacturability analysis tools, other performance optimization tools, and disassembly and recyclability process analysis tools.

CAD for Manufacturability in Product and Process Implementation

During implementation, designers create a complete manufacturable product or process design following the directions set during the definition phase. For electronic products, the designers translate high-level architectural specifications into a detailed design, capable of being manufactured, using design tools and methodologies specified during the definition phase. For processes, the designers specify the detailed process recipes, equipment settings, control limits, and manufacturing procedures required to produce a feasible product. In both cases, designers first produce an initial implementation specifying the detailed design and then optimize the design to meet high-level targets for criteria such as performance, reliability, and cost.

Most of the implementation of electronic products is performed on computers. The large number of detailed design decisions and the complexity of the design prohibit the use of prototyping as the primary design paradigm. Architectural specifications are translated into detailed electrical and physical representations using CAD tools and systems. Through automation, CAD tools perform most of the routine design work, allowing designers to focus on those aspects of the design to which they can add the most value. Because of complexity, especially during initial implementation, tools must rely on simplified representations of cost and performance factors. Thus, during the initial phases of implementation, cost and performance factors are introduced into CAD tools as design rules and analysis conditions (such as temperature and supply voltage) chosen to help ensure that the results are close to product targets and specifications. Manufacturability can be introduced at this stage by considering this criterion during the formulation of the rules and guidelines. If properly chosen, the rules and analysis conditions should be sufficient for most of the design. However, in general, some portions of the design will appear to violate the design targets after the initial implementation. In these cases, more accurate analysis might reveal that the violations are not real (8); otherwise, further optimization of the design is required. During optimization, design elements such as transistor sizes and wire routes are adjusted to bring the design into full compliance with the design targets. Optimization tools can be built “on top” of existing simulation tools, leading to tools such as circuit yield optimizers (29), or can be delivered as stand-alone tools, such as the tools that optimize physical designs for performance and manufacturability (12).

Despite considerable progress in the development of process simulation and design tools, the development of manufacturing processes still relies heavily on extensive physical experimentation. However, increasingly complex processes with large numbers of controlling parameters are leading to increasing use of process CAD tools to complement physical experiments. Indeed, when properly calibrated, process CAD tools can rapidly narrow the number of options that must be considered, focusing much of the physical experimentation on verifying the results of computer experiments (25). Manufacturability is considered in systems built “on top” of process simulation tools, creating process yield simulators (15–17), or as stand-alone parametric yield simulation and optimization tools (20,21). These tools complement physical experimentation by allowing the impact of variation to be quantified prior to the existence of large amounts of data (22).

As an example of the application of CAD for manufacturability in the implementation phase, Mozumder and Chatterjee (30) describe its application to the design of DRAM cells for manufacturability. A primary design goal in their example was the achievement of a manufacturable design for a DRAM cell. Employing yield and performance optimization tools, they selected process settings to minimize the probability of cell failure. Similarly, many authors (5–7) describe tools that optimize interconnect routing in integrated circuits and printed circuit boards to reduce their vulnerability to defects.

CAD for Manufacturability in Ramp and Volume Production

During the ramp to volume production and during volume production, process and product engineers identify and remove sources of product loss in manufacturing, primarily through experimentation in the manufacturing line. Time becomes especially critical during these phases since manufacturing facilities incur enormous expenses and the rate of progress through the ramp phase determines the time at which the product or process will start generating revenue. Although the design should be essentially “frozen” during these phases, the same computer tools used to support DFM can be used to help diagnose loss, identify opportunities for improvements, and control the manufacturing line. Several authors (22,31,32) demonstrate this application.

MODELS AND METHODS FOR CAD FOR MANUFACTURABILITY

Disturbances occur in every manufacturing process, causing every manufactured part to deviate in some way from its intended characteristics. In most processes, the indirect costs caused by these disturbances are important or dominant contributors to manufacturing cost. Consequently, identifying and reducing disturbances and their impacts is a primary focus of process development activities and can be a significant focus of product development activities as well, especially during the ramp to volume production. So, process disturbances can be important contributors to both development and manufacturing cost. For this reason, most models and tools supporting DFM incorporate some representation of process disturbances and their impacts. Indeed, many of these models and tools effectively treat process disturbances as the only component of cost. These disturbances are usually represented and treated statistically, leading to the use of the expression “statistical design.”

Statistical Circuit Design

The models and methods of CAD for manufacturability and statistical design are illustrated in this section by examples taken from integrated circuit design. The design of a complex integrated circuit product requires the design of many smaller electronic circuits. The design of these circuits is typical of many electronic design problems. The design starts with a specification of the functionality of the circuit, the constraints the circuit must meet, and the design objectives. The constraints and objectives are usually stated in terms of physical and electrical characteristics of the circuit, such as its

area, power consumption, and performance. The design process consists of an iterative exploration of design options. At each iteration, alternative implementations of the circuit are generated and compared based on their compliance with the constraints and their relative success in achieving the design objectives. Simulators, such as SPICE (33), are used to simulate each of these options, producing data, typically waveforms, from which the constraints and objective values are calculated.

The manufacturing process is represented in this design process by models of circuit elements characterized using measured data and incorporated into the circuit simulator. An example of such a model is the BSIM3 model (34) describing the electrical characteristics of metal–oxide–semiconductor (MOS) transistors. The parameters of this model are characterized using electrical data measured on a set of transistors. Therefore, the fitted parameters of the model reflect the processing conditions under which the transistors were manufactured, and they can be varied to introduce process variations into the simulator. Conventionally digital CMOS circuit simulations are performed under worst-case conditions, with process and operating conditions adjusted in worst-case directions. For example, slow conditions are formulated by elevating temperatures, lowering voltages, and adjusting model parameters to reduce the switching speed and drive strength of the transistors. With properly selected simulation conditions, such worst-case design methodologies can ensure that circuits are robust to parametric variations in the process. However, different circuits and different measures of circuit performance can exhibit significantly different sensitivities to process and operating conditions. This complicates the selection of simulation conditions, leading to a significant risk of over- or underestimating the impact of process variations. Overestimating the impact of process variations introduces unnecessary margin, which increases development cost by increasing design time and increases manufacturing cost by increasing circuit size. Similarly, underestimating the impact of process variations increases manufacturing cost by decreasing parametric yield.

These considerations have led to the use of statistical formulations that can capture the effect of parametric process variations more completely than worst-case formulations. In these statistical design techniques, parametric variations are represented by statistical models of circuit input parameters, usually the parameters of device models. Circuit simulators are used to propagate input parameter variations through to variations in circuit responses. Techniques such as Monte Carlo simulation, response surface modeling, and design centering can be used to estimate yield, worst-case performance, variability, sensitivity to process variations, indirect costs, and other metrics related to circuit profitability.

Although individual circuits can be designed using these methods, the complexity of integrated circuit products prevents the simulation of an entire product at the circuit level. This has led to the development of hierarchical design methodologies in which relatively small portions of the complete product are simulated using circuit simulators. Circuit simulation has two primary roles in these methodologies: to characterize models used in higher levels of design and to provide accurate analysis of critical circuits. Parametric variations can be introduced in both of these circumstances. Thus, statistical circuit simulation can be used to characterize statistical delay models (10,11), select simulation conditions, and provide accurate statistical analysis of critical circuits (8).

Therefore, statistical circuit simulation is the primary tool used in the statistical design of integrated circuits. Similar tools are used for statistical design in other disciplines. These tools require three components:

1. Statistical models of process disturbances
2. Models or simulators capable of simulating the impacts of process disturbances on product or process responses
3. Analysis and optimization tools and methodologies

Modeling Process Disturbances

Computer analysis of the impact of process disturbances on process or product responses requires the representation of the disturbances in a form that can be simulated. Most commonly, process disturbances are represented by statistical models. Defects are usually modeled by discrete probability distributions representing the probability of occurrence of defects and continuous distributions representing the size of the defects (6,21). Parametric variations are usually modeled by continuous distributions, often assumed to be normal, representing variations in simulator or model input parameters over time and space (35,36). Which input parameters are represented by these models depends on the application, and possibilities include the following:

- *Process parameters,* such as diffusion times and oven temperatures in semiconductor manufacturing
- *Physical parameters,* such as the dimensions (lengths, widths, and thickness) of representative structures
- *Model parameters,* such as the parameters of the models used in the simulation of process steps and circuits
- *Electrical parameters,* such as the resistance and capacitance of wires of the saturation current of transistors

These models can include both systematic and random components and can describe variation at different scales. For example, in semiconductor manufacturing, a statistical model can describe the variation in interlayer dielectric thickness or metal line width within a die and from die to die (37). The models can be characterized from data measured in the manufacturing line, from electrical test data measured at the end of manufacturing (38), from product test data, and from data measured on special test structures (39).

The computational costs of many statistical simulation techniques depend on the number of effects represented by the statistical models. This has led to the development of many techniques for reducing the complexity of statistical models. These include analysis of variance, linear principal components analysis, nonlinear principal components, and factor analysis (40).

Modeling Responses

Statistical design tools usually rely on general-purpose simulators to analyze the impact of parametric process variations; however, simpler models have also been used in statistical design tools such as FABRICS (20). Simulators typically provide the most complete and accurate representation of physical phenomena. Based on detailed mathematical models, of-

ten expressed as ordinary or partial differential equations derived from basic physical principles, they can be used to extrapolate well beyond the characterization conditions. For this reason, simulators have been used extensively in many electrical engineering applications. Examples include the semiconductor process simulator SUPREM (41), the device electrical simulator PISCES (42), and the circuit simulator SPICE (33). In contrast to parametric variations, special-purpose tools, such as VLASIC (21), are generally used to analyze the impact of defects.

Because simulators typically require the solution or integration of differential equations, they usually require significant computational resources. This acts as a barrier to their use in statistical design applications that often require large numbers of model evaluations. This has led to the development of indirect statistical analysis and optimization methods that perform most of their operations on computationally efficient surrogates for the simulators. These surrogates, referred to as empirical models, macromodels, or response surface models, are constructed from data generated by simulating designed experiments. Classical methods for the design and analysis of experiments have been used extensively in this application. Thus, many authors have simulated factorial and axial designs to produce data that they modeled using polynomial regression (see, for example, Refs. 15 and 16). Other authors have developed experimental designs and empirical modeling techniques that take advantage of the lack of random error in the computer environment. This has led to an explosion in experimental design and modeling techniques. Examples of experimental designs applied in statistical design include Latin hypercubes (23), orthogonal arrays, and low-discrepancy sequences. Examples of modeling techniques include generalizations of the geostatistical technique of kriging (43), additive regression splines (44), and neural networks.

The most appropriate form of a model depends on the application. Even with advanced modeling techniques, responses can be difficult to represent accurately over the entire domain of interest. Especially in high-dimensional spaces, a large number of simulations can be required to adequately resolve complex responses. In these cases, the number of simulations required to construct an accurate empirical model can exceed the number required when the methods operate directly on the simulators. However, in some applications, notably when empirical models are fit in the course of automatic optimization, accuracy is not required over the entire domain, and the use of these models can result in substantial cost savings.

Estimation and Optimization Methods

Optimization of profitability requires cost and revenue to be estimated, either directly or via surrogates, for each design option considered. Alternative design options can then be compared and design parameters adjusted in order to provide the best results. Computer tools can support this process by providing the estimates to support manual optimization and by automating the optimization process. Where it is feasible, automatic optimization can significantly reduce design time and can produce superior results due to its more thorough exploration of the design options. Similar methods are used to estimate responses and response distributions in both manual and automated optimization. However, automated optimization often uses simplified approximations to reduce computational effort.

A variety of problem formulations have been employed in both manual and automatic optimization. Examples include (3,29,45,46):

- Minimizing variability subject to fixed performance specifications
- Maximizing performance subject to fixed yield specifications
- Maximizing quality
- Maximizing performance under worst-case conditions
- Minimizing defect-related yield loss subject to fixed performance specifications

Defects and parametric process variations are rarely treated together in a single tool or methodology because of the differences in the analysis methodologies used and because the two types of disturbance tend to be most important in different parts of design.

Methods treating parametric variations have been broadly grouped into two categories: input and output space methods. Input spaces are defined by the input parameters varied in a particular design task. Input parameters include design parameters, such as wire lengths and transistor sizes, and model parameters represented by statistical models. Output spaces are defined by the design responses of interest, such as propagation delay and power consumption. As discussed in the previous section, inputs are mapped to outputs by simulators, empirical models, or other response functions. Design specifications typically appear as upper and lower bounds in output spaces, defining rectilinear regions of acceptable output values, as illustrated in Fig. 2. In general, the corresponding regions of acceptable input values will have complex, nonlinear boundaries.

Input space methods use response functions to construct approximations to regions of acceptability in the input space. Yield, failure probability, and other metrics can then be calcu-

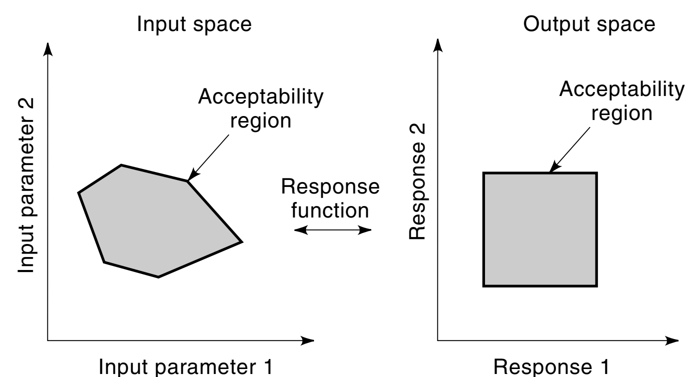

Figure 2. Input and output spaces. This figure shows the relationship between input and output spaces. The region of acceptability is the set of acceptable values of the parameters in each space. It typically has a rectangular shape in the output space, reflecting the use of upper and lower bounds to define acceptable values of the responses. The corresponding region in the input space is complex and irregular due to the nonlinearity of the mapping between the input and output spaces.

lated without further evaluation of the response function. Although the construction of the approximations can be very expensive, once constructed the remainder of the analysis can be performed very cheaply. In addition, the distributions of input parameters can be changed without having to update the approximation, enabling a rapid evaluation of the impact of distribution changes on yield. Input space methods include (29,46) radial exploration, simplicial approximation, design centering, centers of gravity, minimum distances, and boundary integral methods, many of which are used in automatic optimization tools.

Output space methods use response functions to estimate or optimize different metrics of manufacturability (16,17,29). These include the sensitivities of responses to parametric variations, worst-case performance, quality metrics, and parametric yield. Each metric is estimated by propagating samples of input parameters described by statistical models (see section entitled “Statistical Circuit Design”) and also described by response variations using simulators, empirical models, or other response functions (see section entitled “Modeling Process Disturbances”). The sampling scheme depends on the application. “Crude” Monte Carlo sampling has been used extensively to estimate response distributions, from which other metrics can be derived. A variety of variance reduction techniques can be applied to reduce the number of functional evaluations required in Monte Carlo analysis. Many of these are described by Rubenstein (47) and include importance sampling, control variates, stratified sampling, acceptance sampling, and Latin hypercube sampling. Latin hypercube sampling, orthogonal arrays, stratification, and face-centered designs have been used to estimate the sensitivities of responses to input variations.

Output space methods are also used for treating defect-related process disturbances. They typically operate on physical designs, estimating or optimizing the impact of defects on electrical functionality and performance. Examples of these tools include adjusting wire distribution, wire length, and via distribution to improve functional yield (3,13,14).

RESEARCH DIRECTIONS IN CAD FOR MANUFACTURABILITY

Despite the potential benefits of CAD for manufacturability in lower costs and greater profitability, it has seen only modest use in practice, with its wider use impeded by both technical and organizational barriers. Overcoming the organizational barriers will require movement away from entrenched development processes and narrowly focused engineering groups to a more business-oriented, codevelopment model. Other barriers can potentially be reduced through advances in tools and methodologies. Several of these are discussed in this section.

First, introducing cost as a design criterion increases the complexity of the design problem—in many cases, overburdening an already complex design process. Due to this cost and an apparent lack of manufacturing problems arising from conventional design methodologies, most organizations have not seen a compelling need to employ statistical design tools. The additional complexities introduced by statistical methods can be mitigated somewhat by the measures already discussed. Specifically, development methodologies can be structured so that computationally burdensome statistical simulations are applied during the definition phase, when they are most affordable, to choose design rules and simulation conditions balancing manufacturability and performance. When incorporated into design tools employed during implementation, these rules and conditions will ensure that most of the design will satisfy manufacturability constraints by construction. Those small portions of the design for which the manufacturing constraints or performance goals cannot be met using these simplified rules and conditions can be analyzed using more accurate and expensive tools. If this methodology is supported by well-integrated, easy-to-use design frameworks, the barrier to DFM posed by complexity can be lowered significantly. However, several technical hurdles remain to be crossed before such a methodology can be deployed. First, to work properly, the methodology must ensure consistency at each stage of analysis. As described in Ref. 8, guidelines and simulation conditions must be chosen so that they are more conservative than the more accurate analysis tools. Techniques for formulating conditions satisfying this requirement are needed. Second, worst-case simulation conditions carry a significant risk of under- or overdesign, especially when design margins are very narrow. Computationally efficient alternatives to worst-case simulation conditions or less risky selection techniques are needed. Finally, considerations of manufacturability need to be integrated more completely in design methodologies. Several authors (48,50) have pioneered hierarchical statistical design methodologies in the semiconductor industry. Further work is required in this area.

A second barrier to the use of CAD for manufacturability has been the deficiencies of the simulators and models on which many statistical design methods are based. This is illustrated by the technology CAD tools used to simulate semiconductor manufacturing processes. The physics and chemistry of many fabrication steps are poorly understood and, where physical models do exist, they usually contain parameters that are often unknown due to a lack of experimental data (25,26). These problems are compounded in statistical design, which requires not only nominal parameter settings but also representations of their variations. Indeed, since simulators are deterministic, all major sources of disturbances must be represented in order to capture the impact of process disturbances in CAD tools. Deficiencies in these models risk serious underdesign. Since it is rarely possible to fully characterize all process disturbances, methods are needed to compensate for this deficiency. In particular, means are needed for systematically combining simulation and data so that all of the variation is captured in CAD tools.

A third barrier to the use of CAD for manufacturability is design uncertainty arising from model inefficiencies, approximations, incomplete specifications, and parallel development. Model inefficiencies (3) are inherent inaccuracies and approximations in numerical procedures. Design approximations are made to reduce simulation time, simplify the representation, or compensate for missing information. For example, the impact of the wires and transistors surrounding a circuit under design might be approximated by simplified models in order to reduce simulation effort. Similarly, wiring capacitance and resistance must be estimated when simulating electrical performance before the completion of physical design. The parallel development of products and processes introduces a significant element of uncertainty in the inability to predict the ultimate characteristics of the process while the product is

being designed. Errors in assumed characteristics can lead to significant manufacturing problems. When combined, all of these sources of uncertainty can overwhelm the inherent fluctuations of manufacturing processes. Tools and methodologies are needed to cope with this uncertainty. Styblinski et al. (49) have made an initial attempt at managing capturing this uncertainty through the use of fuzzy models. Alternatively, sensitivity analysis can be used to gauge the impact of this uncertainty on the design. However, these are incomplete solutions. Tools and methodologies must support the management and control of design uncertainty over the entire development process.

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