SCHOTTKY OXIDE RAMP DIODES

High-speed devices are now used in all fields dealing with power electronics. Power switches designed to operate below a blocking voltage of 100 V are needed in power supplies, automotive electronics, and peripheral drives. Silicon rectifier diodes and MOS transistors have become common in these applications (1–3).

Rectifier diodes need to exhibit low forward voltage, high current capability, and high breakdown voltage. They must withstand reverse current transient pulses and have a short reverse recovery time, low switching noise, and a high operating temperature.

These requirements are not easily obtained. The Schottky is often the best choice. Unfortunately the breakdown voltage of Schottky diodes is dependent upon edge termination for the planar technology. Field peaking and crowding along the periphery of the Schottky diode (i.e., the edge effect) causes a premature and uncontrolled corner breakdown and high current density at the periphery.

Over the past 25 years, many different edge terminations have been proposed to improve the voltage handling capability without degrading the forward and switching behavior (2–11). A substantial reduction of the electric field at the contact edge is achieved by ramp etching of the oxide at the contact window under small angles (4,7,9,10).

In this article, a new Schottky diode with its edge optimized by an oxide ramp is investigated. The influence of the oxide ramp angle on the breakdown properties was simulated. A major concern is shown to be the possibility of a premature edge breakdown. A design with ramp angle smaller than 2° is proposed, enabling volume breakdown with reduced leakage

J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*. Copyright © 1999 John Wiley & Sons, Inc.

current. Further improvement in operation is obtained by using two epitaxial layers, which insures a higher reverse pulse current handling capability of the Schottky diode with single epitaxial layer. An optimized technology of Schottky oxide ramp diode which uses only low-temperature steps, conserving the quality of the metal–semiconductor interface, enabling high manufacturing yields is implemented. The small ramp angles are achieved by using two oxide layers, having distinct etching rate, surrounding the Schottky contact. Simple and accurate analytical models of the current and capacitance characteristics are presented. In comparison with other terminations, the ramp oxide termination offers simple design and processing close to ideal electrical characteristics for Schottky diodes.

SIMULATION

The ORS diode was simulated using the MEDICI program (12). A cross section of the simulated diode is presented in Fig. 1. There may be a single epitaxial layer (SE-ORS diode) or a double epitaxial layer (DE-ORS diode). The SE-ORS has a 5 μm thick single epitaxial layer (1.5×10^{15} cm^{-3} doped), and the DE-ORS has a 1.7 μm layer (1.5×10^{15} cm^{-3}) and a second epitaxial layer growth on the 3.3 μm, 8×10^{15} cm^{-3} first epitaxial layer (7).

Figure 2 shows the electric field distribution along the interface ($x = 0$, Fig. 1) of 2°, 5°, 10°, and 20° oxide ramp angles for the DE-ORS structure and SE-SOR structure, respectively. In the contact window center the electric field has a center value (E_s); at the contact edge, the electric field monotonously increases to a maximum field (E_{max}). The electric field has an another maximum at end of ramp (E_R). Under the oxide layer the electric field is smaller than the Schottky field. When the ramp angle increases, E_{max} increases too (Fig. 2). For the 2° ramp the electric field peak is less than 10% higher than the center field [Fig. 2(a)]. Therefore at small ramp angles, the edge effects are practically eliminated. Hence a uniform current density is proved in Fig. 3(a) and a volume breakdown results for the DE-ORS diode.

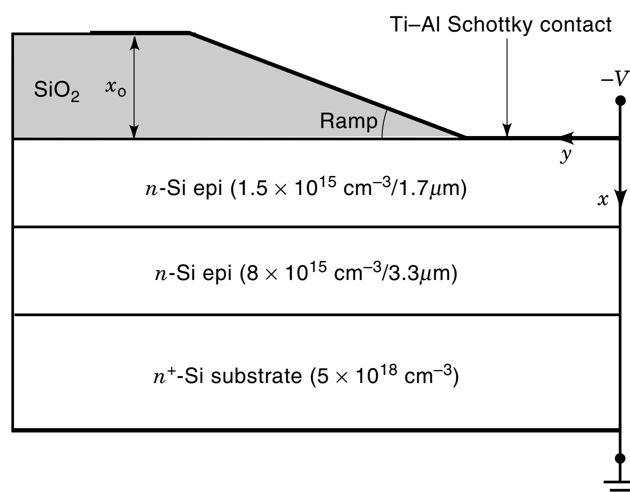


Figure 1. Schottky structure with oxide ramp termination used in MEDICI simulation. Structure has two epitaxial layers, increased on high doped n^+ substrate.

For ramp angles of 20° the difference between maximum electric field is twice higher than the center field [Fig. 2(d)]. In this case a high current density at the edge [Fig. 3(b)] and the corner low breakdown voltage is obtained.

The DE layer effect is evident in Figs. 2(c) and 2(e). The distinction between the DE and SE structure is due to the difference between the center contact field and the edge maximum field. The E_{max}/E_s report at the DE structure (1.33) is smaller than at the SE structure (1.45). Consequently, the use of the DE layer in conjunction with the ramp oxide technique preserves a reduced variation of the electric field along the Schottky contact frontier. The high electric field area of the DE structure under high reverse voltages extends virtually over the entire active Schottky contact area as shown in Fig. 4(a). As opposed to the SE structure and the other Schottky structure types, the high electric field region is confined to a narrow crown or even a circular contour along the Schottky contact edge [Fig. 4(b)]. Figure 5 shows the change of the current vector distribution for DE-ORS and SE-ORS, respectively. This modification could be explained in terms of the good performances of the DE-ORS to the transient reverse current pulses (10).

DEVICE FABRICATION

The experimental implementation of the ramp oxide profile can be achieved using multiple SiO_2 films with different etching rates. The etching rate of one undoped SiO_2 layer is lower than a phosphorus-doped SiO_2 layer. For example, there is a 26.3 etching rate report for a 8% phosphorus-doped SiO_2 layer in comparison with the undoped SiO_2 in the p-etch solution (13). With a proper choice of phosphorus contain in the doped SiO_2 layer, a 5° oxide ramp or smaller can be realized.

SE-ORS and DE-ORS were manufactured starting with the same (72 mm diameter ⟨111⟩ n-type arsenic-doped 0.003 $\Omega \cdot$ cm^{-1}) silicon substrate. The epitaxial layer for SE had the donor concentration of $N_d = 2 \times 10^{15}$ cm^{-3} and thickness 5 μm. The top epitaxial layer of DE diode wafers have same concentration as SE diodes and the buffer layer of larger concentration ($N_D = 8 \times 10^{15}$ cm^{-3}). The thickness of these layers were $x_{e1} = 1.7$ μm and $x_{e2} = 3.3$ μm, respectively. A 1,000 A undoped SiO_2 layer and subsequently 10,000 A phosphorus-doped oxide were deposited. The oxide deposition was performed by CVD at atmospheric pressure only at low temperature (400°C). Therefore the quality of the epi layers surface was not disturbed.

Several metallization systems were investigated for Schottky contact (10), the selection of one or another system depending on constraints imposed by the maximum working temperature demanded for the final devices. Mo : Al metallization was used for diodes with $T_{jmax} = 150$°C. As shown in Ref. 3, the pellet yield is strongly dependent on postmetallization heat treatment conditions. We found that sintering at 525°C for 15 min in forming gas ensures maximum values for V_{RWM} and the highest field. The back of the wafers were metallized with Ti : Ag and annealed at 400°C for 15 min. Cr : Ni : Ag metallization for Schottky contact was used for diodes intended to operate at $T_{jmax} = 125$°C. Postmetallization heat treatment was optimized at 450°C every 20 min for Cr_2Si formation. The back of the wafer metallization was the same as above.

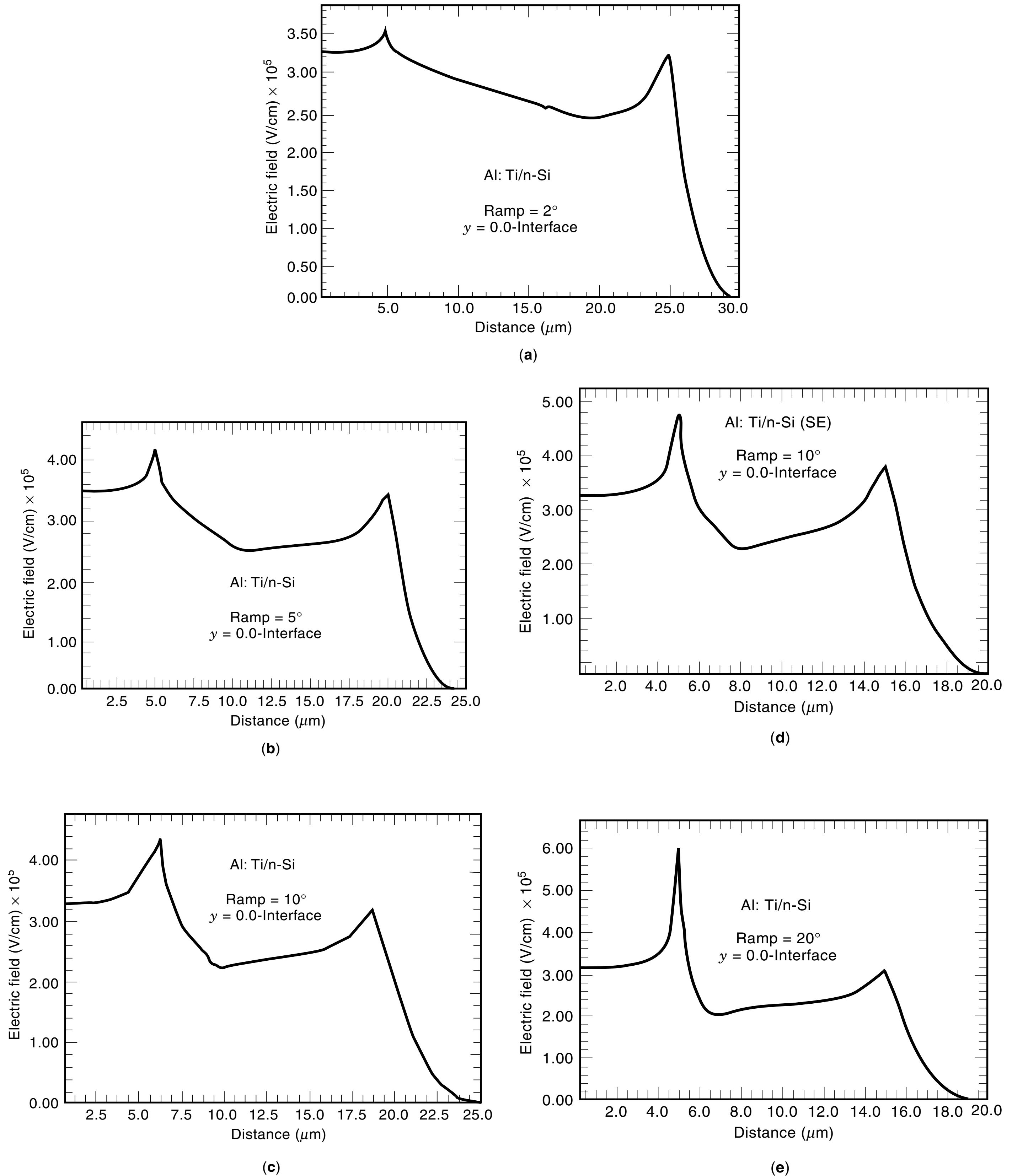
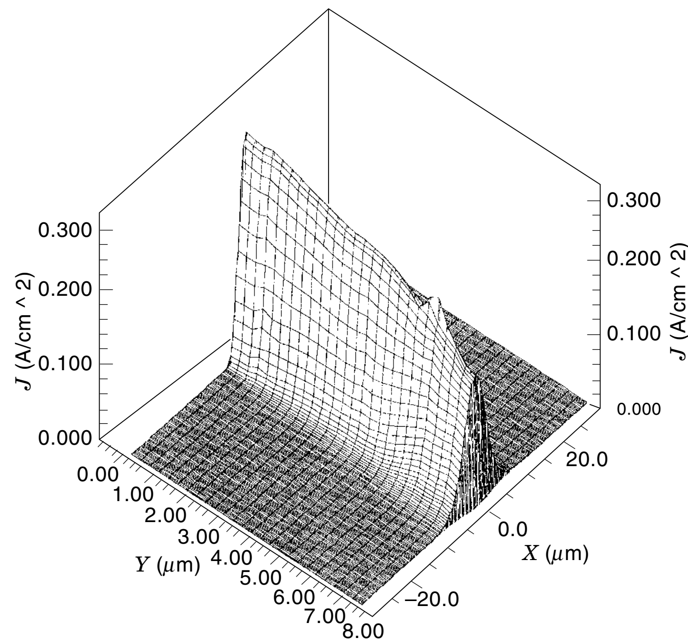
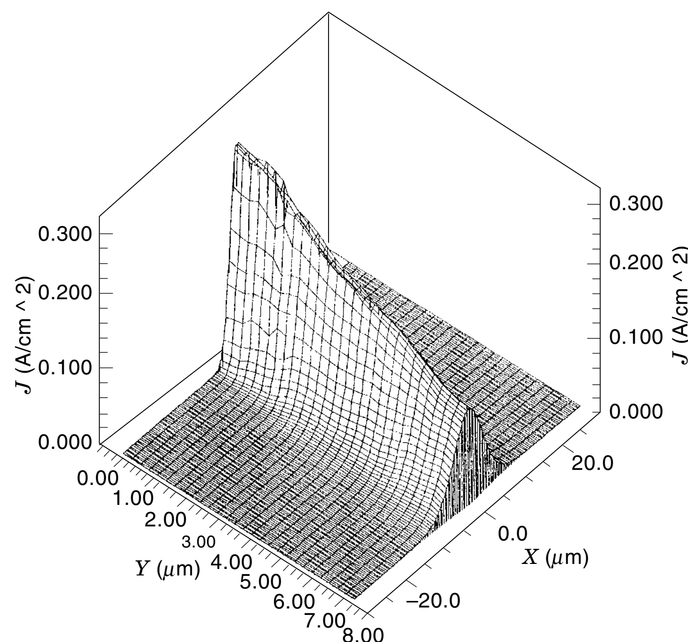


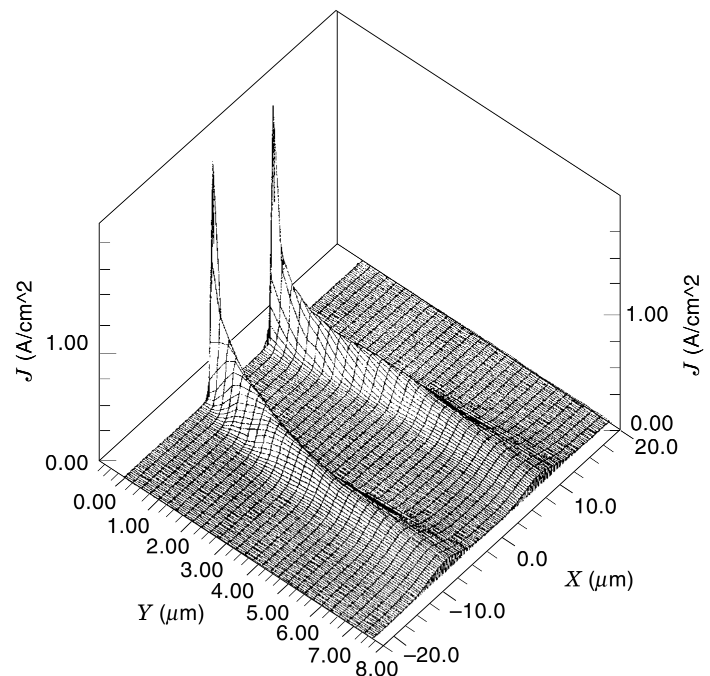
Figure 2. Simulated electric field along SiO_2–Si interface ($x = 0$) for oxide ramp Schottky (ORS) diode with different ramp angles. (a) Ramp = 2° on double epitaxial layer; (b) 5° on double epitaxial layer; (c) 10° on double epitaxial layer; (d) 10° on single epitaxial layer; (e) 20° on double epitaxial layer. When the ramp angle increases, the maximum field (E_{max}) increases as well.



(**a**)



(**b**)



(**c**)

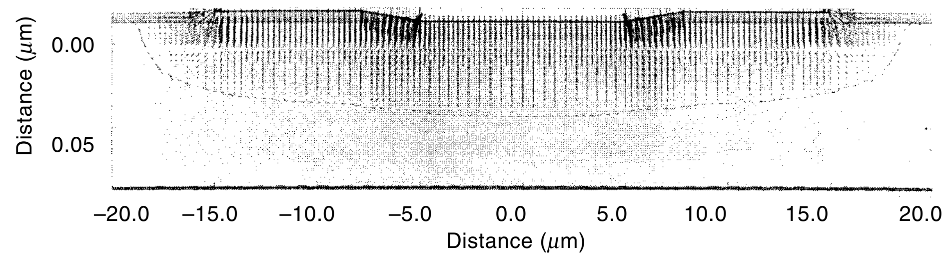
Figure 3. The simulated bidimensional reverse current density at 90 V for oxide ramp Schottky structure with double epitaxial layer. (a) Ramp = 2°, (b) 10°, and (c) 20°. At a small ramp angle, a uniform current density is obtained. For ramp = 20°, a high current density results at the Schottky contact edge, and a corner breakdown voltage is accomplished.

Square-large-area and circular-small-area ORS diodes were fabricated. A very low ramp angle ($\theta = 0.6°$) was measured on these structures. For comparison, a guard ring Schottky diode with similar geometries were prepared. The structure yield was more than 80% as a result of the low-temperature technology process.

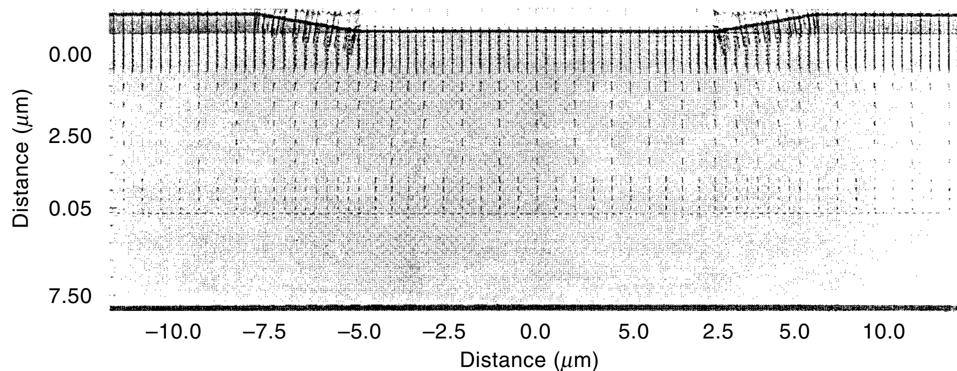
All diodes were encapsulated in the TO 220 case. Forward and reverse current–voltage characteristics and high-frequency (1 MHz) capacitance voltage characteristics were determined at both ambient and higher temperatures.

ANALYTICAL MODEL

In this article, we propose analytical models for electrical characteristics of the Schottky diodes with SE and ramp oxide termination. Figure 6 presents a cross section of the ORS diode used in the modeling. To understand the relation between the metal Schottky contact and the thermal treatment, we take into account the silicide obtained as a result of the chemical reaction between the interface metal and silicon (14,15). The silicide has a geometry similar to that of a diffused p^+n

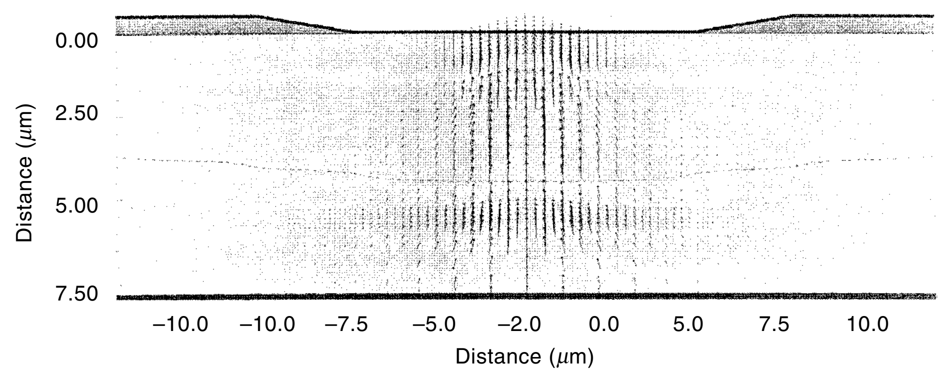


(**a**)

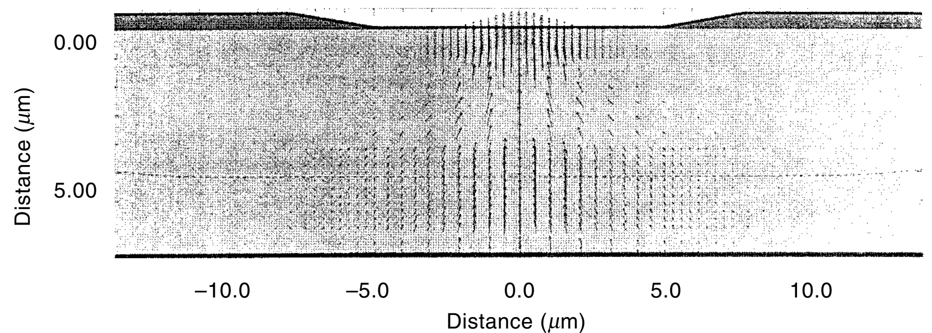


(**b**)

Figure 4. The electric field vectors at 90 V for ORS structure with ramp = 10°. (a) Double epitaxial structure; (b) single epitaxial structure. The high electrical field area of a DE structure extends virtually over the entire active Schottky contact surface, while for an SE structure the high electric field area is confined to a circular contour along the Schottky contact edge.



(**a**)



(**b**)

Figure 5. The total current vectors at 90 V for ORS structure with ramp = 10°. (a) Double epitaxial structure; (b) single epitaxial structure.

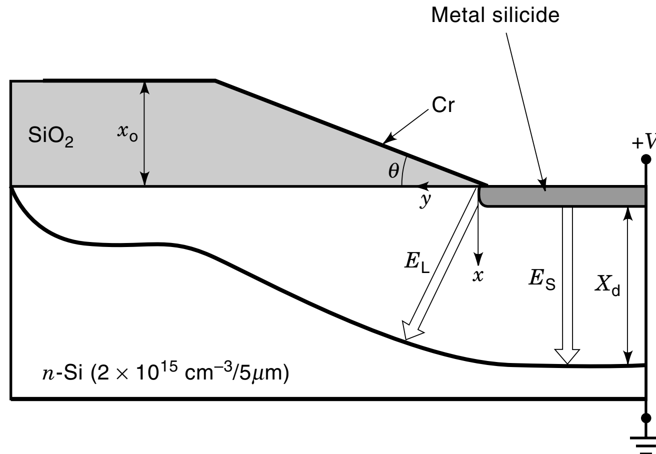


Figure 6. Single epitaxial Schottky structure with oxide ramp termination used in analytical modeling; x_0 is the thickness of oxide (plate portion) and θ is the ramp angle.

junction and the electrical result is to prevent the intensification of the electric field at the silicon–oxide edge, which would tend to reduce premature breakdown (14,15).

We consider a cylindrical curvature of the silicide layer at the contact corner with radius r_j. This shape arises due to the frontal and lateral advancing of silicide in the semiconductor (in epilayer) during its formation. The silicide cylindrical geometry hypothesis is sustained by the very thin thickness of the oxide near the contact window edge.

Electrical Field

The electric field in the contact window has the classical expression of the field at the surface of an ideal Schottky diode (2,3):

$$E_S = \frac{qN_D}{\epsilon_s} \cdot x_d \tag{1}$$

$$x_d = \sqrt{\frac{2\epsilon_s}{qN_d}(V_d - V)} \tag{2}$$

where x_d is depletion region thickness, N_D is the epilayer doping, ϵ_s is the silicon permittivity, V_d is the built-in potential, and $V < 0$ is the applied voltage.

The electric field at the contact corner has two components: a vertical component field (on the x direction) and a lateral one given by

$$E_L(0,0) = \frac{qN_D}{\epsilon_s} x_d \frac{\epsilon_s}{\epsilon_o} tg\theta \tag{3}$$

where θ is ramp angle.

As a result, the maximum electric field (14) is:

$$E_{\max} = E(0,0) = E_S\left(1 + tg^2\theta \frac{\epsilon_s^2}{\epsilon_o^2}\right) \tag{4}$$

appears in the intersection point between the end of ramp and silicide [(0,0) in Fig. 6)].

Figure 7 presents the electrical maximum field versus the reverse voltage ($V = -V_R$) for ramps between 0.5° and 45.5° in 5° steps. For ramps smaller than 5.5°, the maximum electric field is almost the same as the center field, a result which is in good agreement with the MEDICI simulation.

Current–Voltage Characteristics

The device current also has two components: the bulk component and the lateral one. The first component is given by the thermoelectronic emission equation (2,3):

$$I_s = A_s A_n T^2 \exp\left(-\frac{\phi^{\circ}_{Bn} - \alpha E_s}{V_t}\right)\left[\exp\left(\frac{V}{V_t}\right) - 1\right] \tag{5}$$

where A_s is the effective area of contact window ($A_s = l^2$), A_n is the electron Richardson constant, T is the temperature, V_t is the thermal voltage, ϕ°_{Bn} is the electron barrier height at $E_S = 0$, and α is the linear variation coefficient of the barrier with surface electric field (2,3,15)

$$\phi_{Bn} = \phi^{\circ}_{Bn} - \alpha E_S \tag{6}$$

A design equation developed for the lateral current (14) is

$$I_1 = \frac{A_1}{A_s}\frac{I_s}{\beta}\left[\exp\beta - 1 + \frac{2r_j}{l}\left(\frac{\exp\beta}{1 + 4\beta^2/\pi^2} + \frac{\pi}{2\beta}\right)\right] \tag{7}$$

where $\beta = \alpha(E_L - E_S)/V_t$ and $A_1 = 2\pi r_j l$.

Figures 8 and 9 show the forward and reverse current–voltage characteristics of ORS square large-area diodes. Calculated curves, using the above equations and the values of ϕ°_{Bn}, α, and r_j inserted in the figures are in good agreement with the experimental data measured on the SE-ORS diodes with $A_s = 10$ mm². The values of ϕ°_{Bn}, α are very close to those determined for $CrSi_2$/n-Si Schottky contact by other techniques (15). Note that reverse voltage capability and leakage current of the Schottky diodes fabricated using oxide ramp termination are superior to the Schottky diodes with guard ring termination made in similar conditions.

The DE-ORS diodes having the same geometry with SE-diodes show a much higher reverse pulse current handling

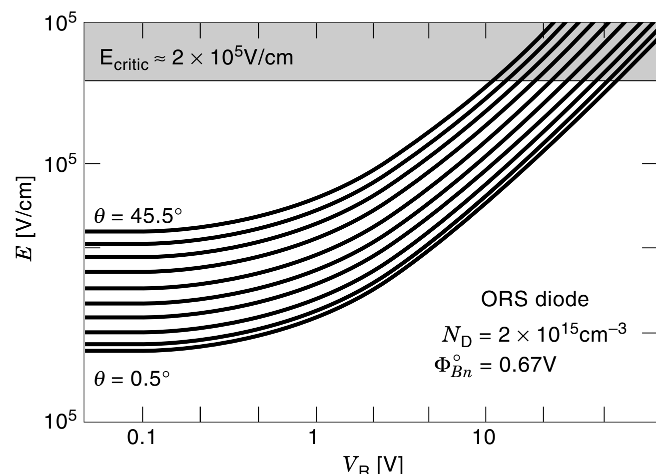


Figure 7. Maximum electric field versus reverse voltage for different ramp angle values calculated with Eq. (4). For $\theta < 5.5°$ $E_{\max} \cong E_S$, in agreement with the MEDICI simulation.

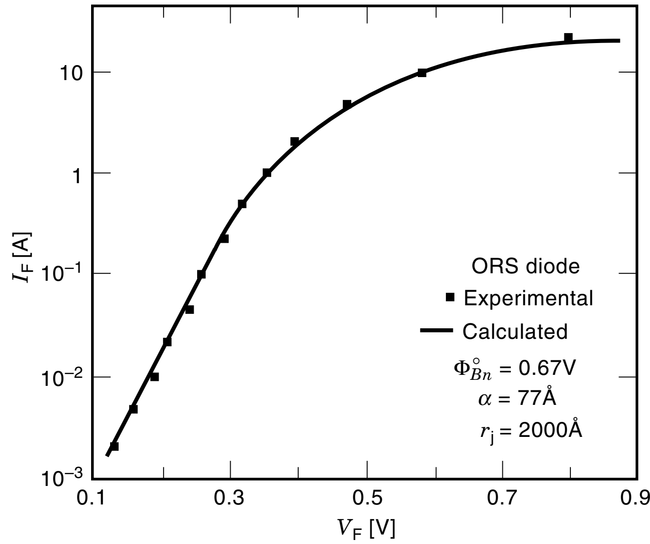


Figure 8. Forward characteristics of ORS diode with 10.1 mm² of area. The experimental data are represented by symbols. The solid curve is calculated with Eqs. (5) and (7).

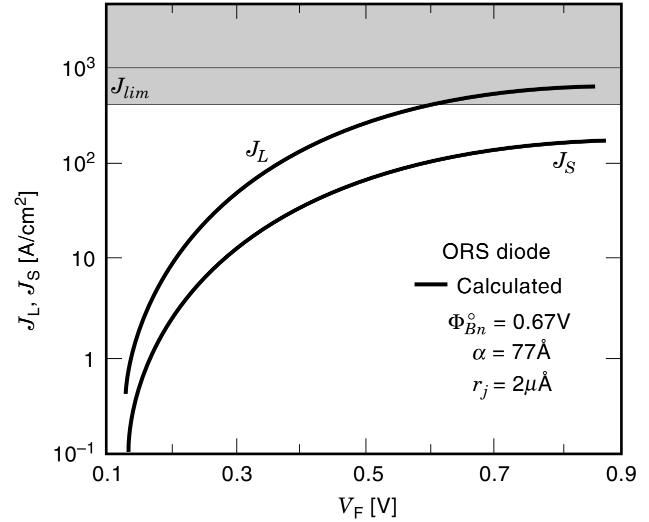


Figure 10. Calculated [using Eqs. (5) and (7)] forward current components versus voltage. For any forward voltage the lateral current density is higher than bulk current density.

capability, with a typical 8.5 A pulse current sustained, compared with 1.2 A measured on SE-ORS diodes (10).

Figure 10 presents the forward voltage dependence of the bulk current density ($J_S = I_S/A_S$) and lateral current density ($J_L = I_L/A_L$), respectively. It is remarkable that the lateral current is always higher than the bulk component in agreement with the MEDICI simulations. As a consequence, the main contribution in the reach of the maximum current density sustained by the device ($J_{\lim}$) is due to lateral current.

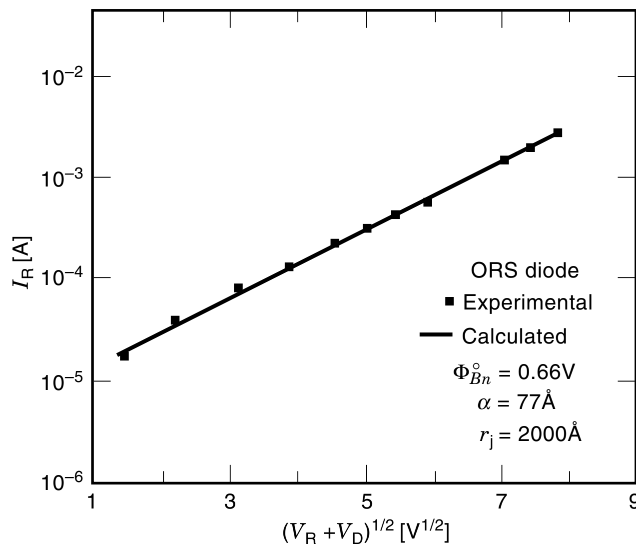


Figure 9. Experimental and calculated reverse characteristics for ORS diode with A_s = 10.18 mm². The theoretical curve is obtained using the same values of ϕ°_{Bn}, α, and r_j parameters as in the forward characteristics.

Capacitance–Voltage Characteristics for Large-Area Diodes

The capacitance of the ORS structure from Fig. 6 has three parallel components. The main component is due to the depletion region of the Schottky contact:

$$C_s = \epsilon_s A_s / x_d \tag{8}$$

The other components that are caused by the structure termination are defined as the parasitic capacities. A parasitic component ($C_{o,r}$) is associated with the ramp oxide region. For the small ramp angles ($\theta < 10°$), the following expression has been derived (14):

$$C_{o,r} \approx 4l \frac{\epsilon_o}{tg\theta} \ln\left[\frac{x_0 + (x_o^2 + x_{d,o}^2)^{1/2}}{x_{d,o}}\right] + 8\frac{\epsilon_o}{tg^2\theta}[(x_o^2 + x_{d,o}^2)^{1/2} - x_{d,o}] \tag{9}$$

for rectangular geometry of the Schottky contact.

The other parasitic component is the MOS overlap capacitance (14) which because the plane oxide region is metal covered (with $A_{o,p}$ area), is given by

$$C_{o,p} = \epsilon_o A_{o,p} / (x_o^2 + x_{d,o}^2)^{1/2} \tag{10}$$

where ϵ_o, x_o are the oxide permittivity and thickness respectively, and $x_{d,o}$ has the expression

$$x_{d,o} = (\epsilon_o/\epsilon_s) x_d \tag{11}$$

The total capacitance is

$$C = C_s + C_{o,p} + C_{o,r} \tag{12}$$

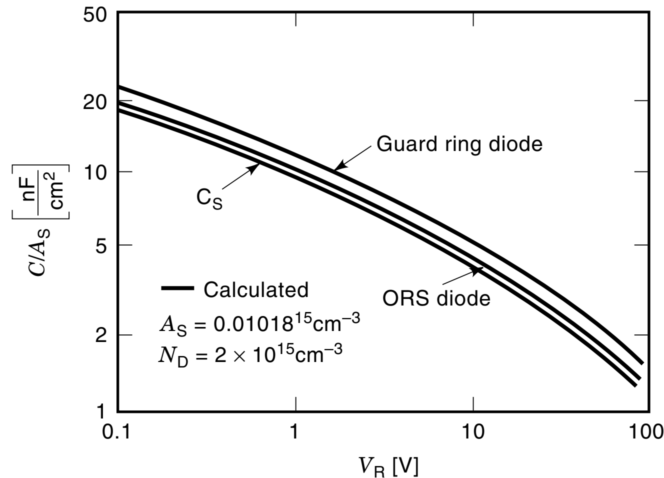


Figure 11. Theoretical total specific capacity (C) and Schottky specific capacity (C_S) as a function of reverse voltage for the ORS diode and Schottky guard ring diode, respectively.

Figure 11 presents the reverse voltage calculated dependence of ORS specific capacitance (C/A_s) and its Schottky component. For comparison a similar curve for the classical ring guard Schottky diode is represented. Both diodes have the same Schottky capacitance, shown in Fig. 11 as well. The parasitic contribution of the termination edge is negligible for large-area ORS diodes. On the other hand, this device has smaller specific capacitance than the guard ring Schottky diode in the whole voltage range.

From Figure 12 one can see that the experimental C–V_R data measured on large square ORS diodes (l = 3.2 mm) are in good agreement with the theoretical curve.

Capacitance–Voltage Characteristics for Small-Area Diodes

In small-area diodes, the contribution of parasitic components (due to diode termination) become important in total capacitance of the diode. In these conditions, we must take into account the oxide charge effect (14). The ramp oxide region capacitance is now given by

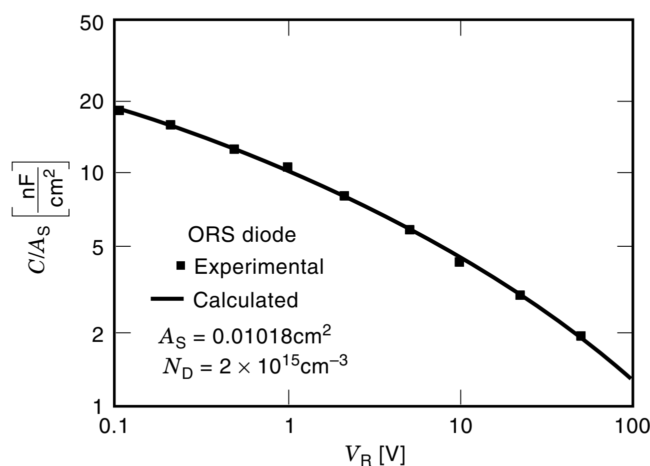


Figure 12. Comparison of theoretical C–V characteristics and experimental data measured on the large area ORS diode.

$$C_{o,r} = \frac{\pi\epsilon_o}{tg\theta}\left(D + 2\frac{x_f}{tg\theta}\right)\ln\left(\frac{x_o - x_f + x_{f,o}}{x_{d,o} - x_f}\right) + 2\frac{\pi\epsilon_o}{tg^2\theta}(x_{f,o} - x_{d,o}) \tag{13}$$

This equation has been obtained for circular Schottky contact (with diameter D), considering a fixed oxide charge of N_f density concentrated at interface Si–SiO$_2$ (14). We used the following notations:

$$x_f = \frac{\epsilon_o N_f}{\epsilon_s N_D}, \quad x_{f,o} = \sqrt{x_o^2 + x_{d,o}^2 - 2x_f x_o} \tag{14}$$

The MOS plane region capacitance is in this case determined by

$$C_{o,p} = \frac{\epsilon_o A_{o,p}}{x_{f,o}} \tag{15}$$

The Schottky component C_s is given by Eq. (8).

Based on the above equations, various calculations were performed to investigate the fixed oxide charge effects. Figure 13 shows the calculated capacitance of a small-area ORS diode as a function of the reverse voltage for different N_f densities. The oxide charge leads a considerable change of the C–V shape and a significant enhancement of total capacitance at low reverse voltage ($V_R < 10$ V).

To verify the validity of the proposed C–V modeling ORS diodes with small diameters (D = 20 μm) were fabricated. A value of 4.7×10^{-12} cm^{-3} for fixed oxide charge was measured on a MOS test structure, simultaneously prepared. The experimental C–V data measured on the ORS diodes closely agree with the theoretical curves of $N_f = 4.5 \times 10^{-12}$ cm^{-3}.

CONCLUSIONS

A ramp oxide terminated Schottky diode has been analyzed which is based on the different etching rate between phospho-

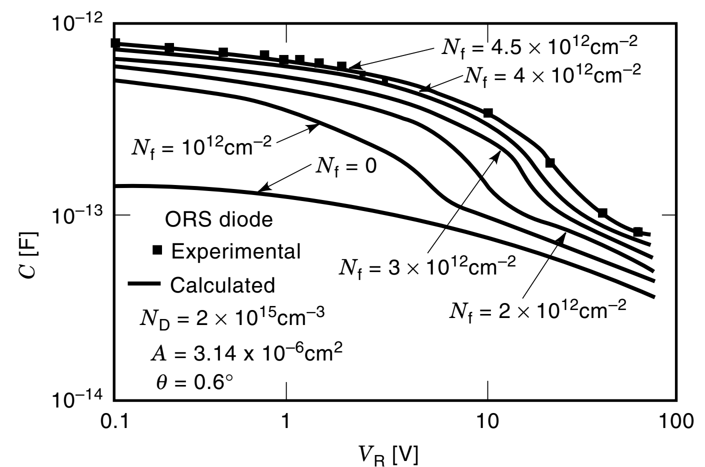


Figure 13. The fixed oxide charge effect on C–V characteristics at small-area ORS diode. The experimental data measured on the circular diode are in good agreement with the calculated curves for N_f = 4.5×10^{12} cm^{-2}.

rus-doped and undoped oxide surrounding the Schottky contact. Electrical characteristics and breakdown properties of ORS structure termination has been simulated, experimented upon, and modeled. The simulation and experimental results demonstrate that in an optimal ORS structure the ramp angle is smaller than 2° and has a double epitaxial layer. In such structures, suppressing the electric field results in enhancement at the contact edge, a volume breakdown, a uniform current density, and occurrence of electric field vectors in the Schottky contact region. A double epitaxial layer was used to increase the forward conduction capability with only a small payoff in the maximum working voltage, and the transient reverse current handling capability of the devices. The technology process for ORS diodes needs only low temperature, which enables high fabrication yield.

The validity of the simple analytical model proposed in this article is confirmed by the model's fit with the experimental data and the simulation results. Modeling has revealed the important contribution of the lateral forward current density for the ORS diode with a silicide Schottky contact. Furthermore it has been shown that the parasitic capacitances of large-area ORS diodes are negligible. Hence the power ORS diode (large-area) will exhibit higher switching performances than the classical guard ring Schottky with the same geometry.

Modeling of C–V characteristics for small-area diodes take into account the oxide charge effect. A good agreement between charge oxide density achieved from C–V curves and well-known MOS methods recommend the ORS diode as a simple test vehicle for determining the fixed oxide charge.

Due to its design simplicity and process robustness compared to other termination techniques, the Schottky oxide ramp ORS diode should find its use in various applications requiring almost ideal breakdown voltages, high power, and high-frequency operation. The ORS diode structure can be used as described in this article, or as a high-voltage termination attached to Schottky diodes of different design in the central area of the structure. For example, the central area of the structure may have a different doping profile from those considered in this article.

BIBLIOGRAPHY

1. B. J. Baliga, Trends in power semiconductor devices, *IEEE Trans. Electron Devices,* **43**: 1717–1731, 1996.
2. E. H. Rhoderick, *Metal Semiconductor Contacts,* Oxford, UK: Clarendon Press, 1978.
3. D. Dascalu, G. Brezeanu, and P. A. Dan, *Metal Semiconductor Contacts in Microelectronics,* Bucharest: Romanian Academy, 1988.
4. A. Rusu, C. Bulucea, and P. Dan, The breakdown voltage of planar Schottky diodes, *Int. J. Electron.,* **5**: 523–534, 1978.
5. B. J. Baliga, High-voltage device termination techniques—A comparative review, *Proc. IEEE,* **129**: 173–179, 1982.
6. B. J. Baliga, Analysis of high-voltage merged *p-i-n*/Schottky (MPS) rectifiers, *IEEE Trans. Electron Devices,* **34**: 271–329, 1987.
7. G. Brezeanu, New termination for planar Schottky structure (PSS), in A. P. Jauho and E. Buzaneva (eds.), *Frontiers in Nanoscale Science of Micron/Submicron Devices,* Dordrecht: Kluwer, 1996, pp. 375–384.
8. M. Badila et al., Impurity lateral Schottky diodes. Simulation and experiment, *Proc. 17th Annu. Semiconductor Conf. CAS,* Sinaia, Romania, 1994, p. 77–80.
9. M. Badila and G. Brezeanu, Field plate termination for Schottky structure, *Proc. 20th Int. Conf. Microelectronics MIEL,* Nis, Serbia, 1995, pp. 391–396.
10. M. Badila and G. Brezeanu, Double epitaxial layer power Schottky diodes with end in the ramp oxide technique, *Microelectronics J.,* **27**: 67–72, 1996.
11. R. Sunkavalli and B. J. Baliga, Dielectrically isolated lateral merged *pin* Schottky (LMPS) diodes, *IEEE Trans. Electron Devices,* **44**: 2011–2016, 1997.
12. *MEDICI Users's Manual,* Technology Modeling Associates Inc., Palo Alto, CA, 1992.
13. W. Kern, *RCA Rev.,* **37**: 55–72, 1975.
14. F. Mitu, Modeling and characterization of high speed devices, Ph.D. Thesis, Univ. Politehnica, Bucharest, Romania, 1996.
15. G. Brezeanu and P. A. Dan, Modeling of gradual interface intimate silicide/Si Schottky contacts, *Solid-State Electron.,* **34**: 95–103, 1991.

MARIAN BADILA
Microtechnology Institute
GHEORGHE BREZEANU
FLORIN MITU
University Politehnica of Bucharest

SCIENTIFIC COMPUTING. See PHYSICS COMPUTING.

SCIENTIFIC VISUALIZATION. See VOLUME VISUALIZATION.

SCINTILLATION. See REFRACTION AND ATTENUATION IN THE TROPOSPHERE.