METAL SEMICONDUCTOR FIELD EFFECT TRANSISTORS

The metal-semiconductor field-effect transistor (MESFET) is one of the field-effect transistors in which the conduction process involves predominantly one kind of carrier, and the current transport between the source and drain electrodes is modulated by a voltage applied to the gate electrode. In the MESFET, a metal-semiconductor rectifying contact is used for the gate. There are a few other field-effect transistors: the junction field–effect transistor (JFET) and the metal-oxide-semiconductor field-effect transistor (MOSFET), where the gates are formed by a p–n junction and a metal-oxide-semiconductor structure, respectively. In the Si device, the MOSFET is usually used because a high-quality insulating oxide (SiO_2) with a low density of interface states can be fabricated. The MOSFET having an insulated gate allows a higher input-voltage swing and higher input impedance than the other field-effect transistors. Compound semiconductors such as GaAs, InP, and InGaAs have higher electron mobilities and maximum drift velocities than Si, so field-effect transistors fabricated from GaAs etc. show higher operating speed and higher frequency performance. In the compound semiconductors such as GaAs, however, there are no good oxides or insulators to make the MOSFET or the insulated-gate field-effect transistor available now, although some good attempts have been reported recently (1). There exist high densities of interface states between the oxide (or insulator) and the compound semiconductor. Therefore, the MESFET structure is usually adopted for field-effect transistors fabricated from compound semiconductors like GaAs.

Historically, the GaAs MESFET was proposed by Mead (2) in 1966 and subsequently fabricated by Hooper and Lehrer (3) using a GaAs epitaxial layer on the semi-insulating GaAs substrate. In 1971, Turner et al. (4) got useful gain up to 18 GHz. In 1973, a first power GaAs MESFET was fabricated with 1.6 W at 2 GHz (5). Around 1980, the GaAs MESFET technology progressed greatly due to the availability of high-quality semi-insulating substrate and ion-implantation processing techniques. In another development, Mimura et al. (6) demonstrated a new type of field-effect transistor called the high electron mobility transistor (HEMT), where an AlGaAs/GaAs heterojunction with doped AlGaAs and non-doped GaAs layers is utilized. In the AlGaAs/GaAs HEMT or heterojunction field-effect transistor (HFET), the Schottky contact is formed on the AlGaAs layer, so this can be regarded as a kind of MESFET. However, we will only describe the normal MESFET (particularly GaAs MESFET) in this article.

Today, the GaAs MESFET is widely used in both high-speed and high-frequency applications. Particularly, it has been the workhorse of the microwave industry for many years (7). The GaAs MESFET is used as the active device for low noise and power amplifiers as well as for oscillators, mixers, and attenuators. Its microwave performance challenges that of HEMT (8). On the other hand, the integration scale of GaAs MESFET-ICs approaches 10^6 transistors on a chip (9), and GaAs-based 32-bit microprocessors are developed (10).

The superior performance of GaAs MESFET is due to the higher electron mobility and the higher electron velocity of GaAs. However, there are several unfavorable phenomena in GaAs MESFET, such as short-channel effects, sidegating effects, frequency-dependent output conductance and transconductance, slow-current transients, and kink phenomena. The short-channel effect is a phenomenon that the threshold voltage of a MESFET shifts with shortening the gate length, and the sidegating effect is a phenomenon that the drain current of the MESFET is modulated when a negative voltage is applied to an adjacent device in ICs. The kink is a phenomenon that the drain conductance shows an abnormal increase at relatively high drain bias. Almost all phenomena listed above are originated from the fact that the semi-insulating substrate (on which the MESFET is fabricated) is achieved by impurity compensation by deep levels, and that high densities of surface states exist on the active layer of GaAs MESFET. However, the detailed mechanisms are not necessarily made clear.

In this article, we first describe the basic operation principle of the MESFET and its current-voltage characteristics that are derived physically. Next, typical device structures of GaAs MESFETs are described, and their high-speed and high-frequency performances are reviewed. Then we describe parasitic effects in GaAs MESFETs, such as substrate conduction, sidegating effects, slow-current transients, low-frequency anomalies, and kink phenomena. Finally, some modeling methods for GaAs MESFETs are presented which are important for circuit design and for understanding physical phenomena in GaAs MESFETs.

BASIC PRINCIPLES

Operation Principle

Figure 1 shows a schematic diagram of a GaAs MESFET. A conductive n-layer is formed on the semi-insulating GaAs substrate which has a high resistivity of $\sim 10^8$ Ωcm. So usually, current does not flow in the substrate region. On the n-layer, two ohmic contacts are provided. One acts as the source and the other as the drain. When a positive voltage V_D is applied to the drain with respect to the source, electrons flow from source to drain. Hence, the source supplies carriers, and the drain acts as the sink.

The third electrode, the gate, forms a rectifying Schottky contact with the n-layer, and so the depletion region exists around the gate. Because the positive voltage is applied to the drain, the depletion layer extends deeper at the drain side. The width of depletion layer can change by applying the gate voltage, so the thickness of conductive channel is varied. Therefore, current from source to drain can be modulated by the gate voltage, leading to the three terminal device.

For a given gate voltage V_G, the channel current increases as the drain voltage increases. Eventually, for sufficient large

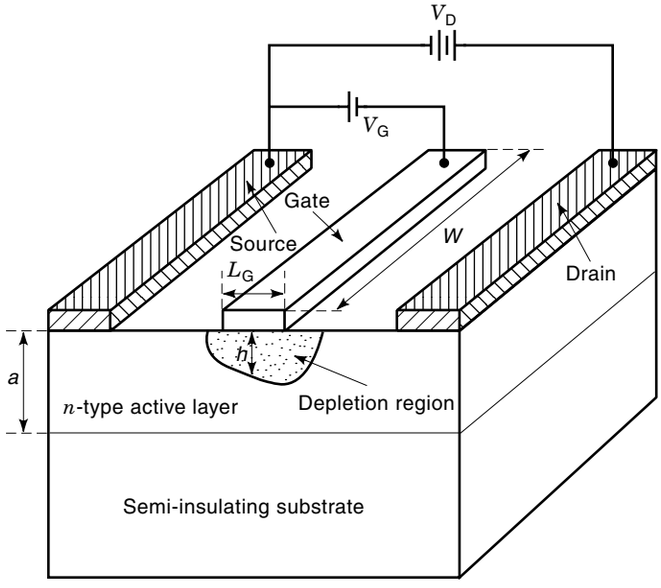


Figure 1. Schematic diagram of a (GaAs) MESFET on the semi-insulating substrate. The depletion region is formed under the gate.

V_D, the current saturates due to the pinching of the channel at the drain side or the electron velocity saturation there. The pinching of the channel means that the n-layer is fully depleted (at the drain side) due to the reverse gate-to-drain voltage. In Fig. 1, the basic device dimensions are the gate length L_G, the gate width W, the channel depth a, and the depletion-layer width h.

The operation of a MESFET is identical to that of a JFET, which was first analyzed by Shockley (11) in 1952. We will next describe current-voltage characteristics of a MESFET that are derived physically.

Current-Voltage Characteristics

Contact Mobility Model. The simplest but most essential method for deriving I–V characteristics of a MESFET is based on that by Shockley (11,12). A long-channel MESFET is considered ($L_G \gg a$), and the following assumptions are adopted: (1) gradual channel approximation, (2) abrupt depletion layer, and (3) constant mobility. As shown in Fig. 2, we consider a region under the gate and assume that the semi-insulating layer is perfectly insulating. Now, we treat a case with uniform doping N_D. Under the gradual channel approximation, the depletion layer width h varies only gradually along the x direction, and it can be obtained by solving the one-dimensional Poisson's equation in the y direction:

$$\frac{d^2\psi}{dy^2} = -\frac{qN_D}{\epsilon} \tag{1}$$

Using the boundary condition that $\psi = V_G - V_b$ at $y = a$ and $\psi = V(x)$ at $y = a - h$, we obtain

$$h(x) = \sqrt{\frac{2\epsilon\{V(x) + V_b - V_G\}}{qN_D}} \tag{2}$$

where V_b is built-in potential at the Schottky contact, and $V(x)$ is the potential at x in the channel region. The depletion widths at the source and drain ends of the gate are

$$h_1 = \sqrt{\frac{2\epsilon(V_b - V_G)}{qN_D}} \qquad (x = 0) \tag{3}$$

$$h_2 = \sqrt{\frac{2\epsilon(V_D + V_b - V_G)}{qN_D}} \qquad (x = L_G) \tag{4}$$

The maximum value of h_2 is equal to a, and in such a case, the drain end of the gate pinches off and is depleted of carriers. The corresponding voltage is called the pinch-off voltage and defined as

$$V_P \equiv \frac{qN_D a^2}{2\epsilon} = V_{DSS} + V_b - V_G \tag{5}$$

where V_{DSS} is the drain voltage at which the pinch-off occurs.

The current density in the x direction along the channel is given by

$$J_x = q\mu N_D E_x = -q\mu N_D \frac{dV}{dx} \tag{6}$$

where the diffusion current is neglected. E_x is the electric field along the x direction, and μ is the electron mobility which is assumed constant. The channel current at x (or the drain current I_D) is then given by

$$I_D = q\mu N_D \frac{dV}{dx}(a - h)W \tag{7}$$

From Eq. (2), we obtain

$$dV = \frac{qN_D}{\epsilon} h\,dh \tag{8}$$

and hence,

$$I_D = \frac{q^2 N_D^2}{\epsilon} \mu W (a - h) h \frac{dh}{dx} \tag{9}$$

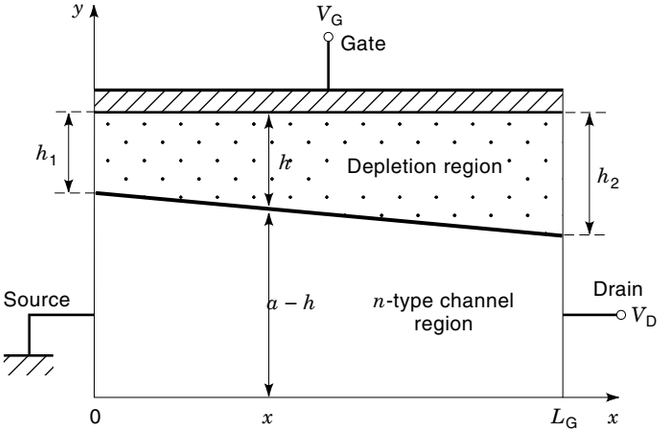


Figure 2. Channel cross-section under the gate of a modeled MESFET. The depletion region extends deeper at the drain side, and hence, the channel becomes thinner there.

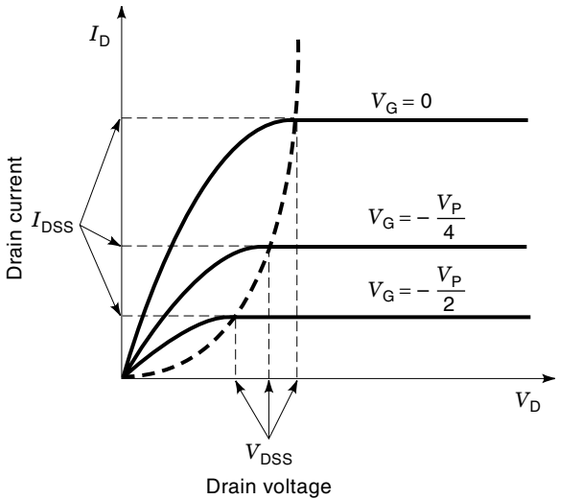


Figure 3. Basic I–V characteristics of a MESFET. The drain current saturates at $V_{DSS} = V_P + V_G - V_b$, and the saturation current I_{DSS} decreases as the gate voltage V_G becomes negative. V_P is the pinch-off voltage, and V_b is built-in potential at the Schottky contact.

Integrating from $x = 0$ ($h = h_1$) to $x = L_G$ ($h = h_2$) yields

$$\int_0^{L_G} I_D\,dx = \frac{q^2 N_D^2 \mu W}{\epsilon} \int_{h_1}^{h_2} (a-h)\,h\,dh \tag{10}$$

Therefore,

$$I_D = \frac{W\mu q^2 N_D^2 a^3}{6\epsilon L_G}\left\{\frac{3}{a^2}(h_2^2 - h_1^2) - \frac{2}{a^3}(h_2^3 - h_1^3)\right\} \tag{11}$$

or

$$I_D = I_P\left[3\frac{V_D}{V_P} - 2\left\{\left(\frac{V_D + V_b - V_G}{V_P}\right)^{3/2} - \left(\frac{V_b - V_G}{V_P}\right)^{3/2}\right\}\right] \tag{12}$$

where

$$I_P = \frac{W\mu q^2 N_D^2 a^3}{6\epsilon L_G} \tag{13}$$

These expressions relate the current up to the point of pinch-off of the channel. At this bias, which occurs when $h_2 = a$, the drain current saturates and remains constant. This current I_{DSS} is given by

$$I_{DSS} = I_P\left[1 - 3\left(\frac{V_b - V_G}{V_P}\right) + 2\left(\frac{V_b - V_G}{V_P}\right)^{3/2}\right] \tag{14}$$

The current-voltage characteristics calculated from Eq. (12) are schematically shown in Fig. 3, where the saturation voltage is given by $V_{DSS} = V_P + V_G - V_b$.

From the current-voltage characteristics, we can obtain important device parameters such as transconductance g_m and drain conductance g_D. In the region before saturation, from Eq. (12), we obtain

$$g_m \equiv \frac{\partial I_D}{\partial V_G} = \frac{3I_P}{V_P}\left\{\left(\frac{V_D + V_b - V_G}{V_P}\right)^{1/2} - \left(\frac{V_b - V_G}{V_P}\right)^{1/2}\right\} \tag{15}$$

$$g_D \equiv \frac{\partial I_D}{\partial V_D} = \frac{3I_P}{V_P}\left\{1 - \left(\frac{V_D + V_b - V_G}{V_P}\right)^{1/2}\right\} \tag{16}$$

In the saturation region, $g_D = 0$ and from Eq. (14), g_m becomes

$$g_m = \frac{\partial I_{DSS}}{\partial V_G} = \frac{3I_P}{V_P}\left\{1 - \left(\frac{V_b - V_G}{V_P}\right)^{1/2}\right\} \tag{17}$$

So g_m decreases when V_G becomes more negative.

The model presented here is useful when understanding the basic principle of the MESFET. However, in itself, this model cannot treat the characteristics beyond the pinch-off. Also, usually, the estimated drain current is rather higher than the experimental one. This is attributed to the fact that the electric-field dependence of electron mobility is neglected here.

Field-Dependent Mobility Model. Lehovec and Zuleeg (13) extend the previous model by considering electric-field dependence of electron mobility. They use the function:

$$\mu_n = \frac{\mu}{1 + \mu|E_x|/v_s} \tag{18}$$

where v_s is the saturation velocity and takes a value of about 10^7 cm/s for GaAs at $T = 300$ K. As shown in Fig. 4, the drift velocity $v = \mu_n E_x$ saturates at high E_x. From Eq. (7), the drain current in this case is given by

$$I_D = qN_D\frac{\mu(dV/dx)}{1 + (\mu/v_s)(dV/dx)}(a-h)W \tag{19}$$

Substituting Eq. (8) into Eq. (19), we obtain

$$I_D\left(1 + \frac{qN_D}{\epsilon}\frac{\mu}{v_s}h\frac{dh}{dx}\right) = \frac{q^2 N_D^2}{\epsilon}\mu W(a-h)h\frac{dh}{dx} \tag{20}$$

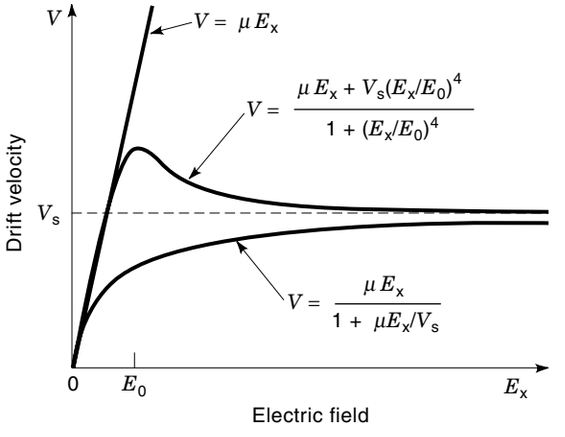


Figure 4. Three kinds of velocity versus electric field characteristics. One ($v = \mu E_x$) is a case of constant mobility, and the other two are cases of field-dependent mobilities where the velocities saturate.

Integrating from $x = 0$ ($h = h_1$) to $x = L_G$ ($h = h_2$) yields

$$I_D = \frac{I_P}{1 + \mu V_D / v_s L_G} \left[3\frac{V_D}{V_P} - 2\left\{ \left(\frac{V_D + V_b - V_G}{V_P} \right)^{3/2} - \left(\frac{V_b - V_G}{V_P} \right)^{3/2} \right\} \right] \quad (21)$$

Comparing Eq. (21) and Eq. (12) shows that the drain current is reduced by a factor of $(1 + \mu V_D / v_s L_G)$ due to the field-dependent mobility.

The above model successfully explains the reduction of the drain current. However, the used mobility model does not include the negative differential mobility observed in GaAs. Often, the electron drift velocity of GaAs is expressed analytically by the following-type function (14), as is also shown in Fig. 4.

$$v = \frac{\mu |E_x| + v_s (E_x / E_0)^4}{1 + (E_x / E_0)^4} \quad (22)$$

where E_0 is a parameter. Please also note that this model is only effective before the current saturates, as is the same in the previous model.

Two-Region Model. Statz et al. (15) developed a model that is effective also beyond current saturation. They used a velocity-field curve as shown in Fig. 5, where the mobility is assumed constant up to a critical field E_C, and the velocity is assumed constant beyond E_C. The MESFET is divided into two regions as shown in Fig. 6. Region I near the source is the constant-mobility region, and the gradual channel approximation described previously is applicable. Region II near the drain is the velocity saturation region, where a conductive channel of finite width is postulated to account for current continuity. The point $x = L_1$, which corresponds to the onset of velocity saturation, is allowed to move depending on the drain voltage V_D. Its position is determined by the location at which the longitudinal electric field E_x equals the critical field E_C. So the two-region model is applicable to operation conditions for all I-V characteristics including the saturation region.

In Region I, an expression of the current is essentially the same as that of Eq. (11) or Eq. (12). Integrating Eq. (9) from

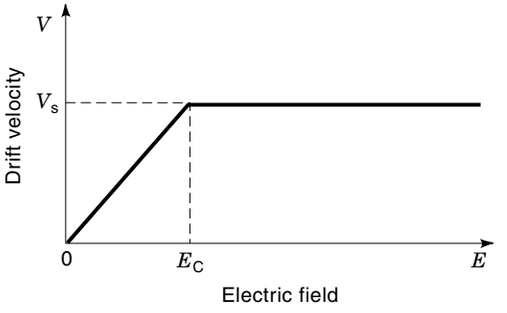


Figure 5. Velocity-field curve used for the two-region model. Below the critical field E_C, the mobility is constant, and the velocity is constant beyond E_C.

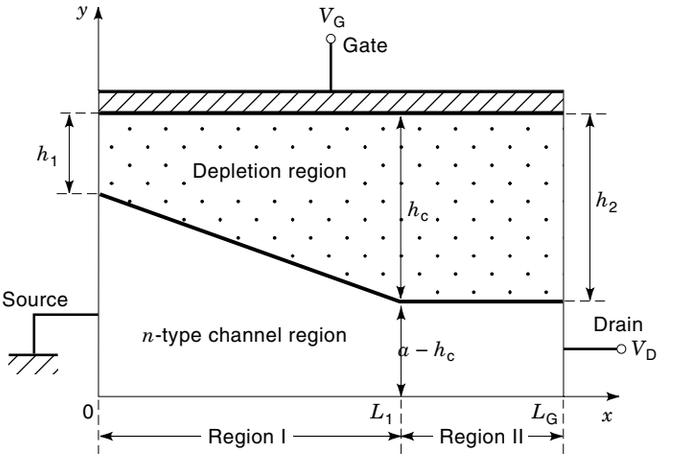


Figure 6. Channel cross-section under the gate for the two-region model. Region I is the constant mobility region, and Region II is the velocity saturation region where the channel thickness is constant.

$x = 0$ ($h = h_1$) to $x = L_1$ ($h = h_c$), we obtain

$$I_D = I_P \frac{L_G}{L_1} \left\{ \frac{3}{a^2}(h_c^2 - h_1^2) - \frac{2}{a^3}(h_c^3 - h_1^3) \right\} \quad (23)$$

where

$$h_c = \sqrt{\frac{2\epsilon (V_{DL1} + V_b - V_G)}{qN_D}} \quad (24)$$

Here, V_{DL1} is the potential at $x = L_1$ in the channel. We can determine L_1 by utilizing current continuity between Regions I and II. In Region II, electrons are assumed to travel at the saturation velocity v_s, and hence,

$$I_D = qN_D v_s (a - h_c) W \quad (25)$$

From Eq. (23) and Eq. (25), we obtain

$$L_1 = \frac{qN_D \mu \{3a(h_c^2 - h_1^2) - 2(h_c^3 - h_1^3)\}}{6\epsilon v_s (a - h_c)} \quad (26)$$

Once the h_c is known, the length L_1 is specified, and the current I_D is determined.

For a given I_D, the potential drop from the source to drain can be obtained by integrating the longitudinal electric field from $x = 0$ to $x = L_G$. In Region I, the potential drop V_{DL1} is, from Eq. (24) and Eq. (3),

$$V_{DL1} = \frac{qN_D}{2\epsilon}(h_c^2 - h_1^2) \quad (27)$$

In Region II, the potential drop V_{DL2} is determined by solving Laplace's equation. By taking the lowest space harmonic, we obtain (15)

$$V_{DL2} \simeq \frac{2a}{\pi} \frac{v_s}{\mu} \sinh \left\{ \frac{\pi}{2a}(L_G - L_1) \right\} \quad (28)$$

The drain voltage V_D is the sum of Eq. (27) and Eq. (28), and hence,

$$V_D = \frac{qN_D}{2\epsilon}(h_c^2 - h_1^2) + \frac{2a}{\pi}\frac{v_s}{\mu}\sinh\left\{\frac{\mu}{2a}(L_G - L_1)\right\} \qquad (29)$$

Eq. (29) and Eq. (26) allow one to determine L_1 and h_c for given V_D and V_G, yielding the current I_D. So $I_D - V_D$ curves as a parameter of V_G are obtained. The two-region model described here has been the basic of several physics-based analytical GaAs MESFET models later developed (16).

In the discussions above, we derived the current-voltage characteristics of a MESFET in closed or analytical forms based on various assumptions. Particularly, we used the gradual channel approximation and assumed the one-dimensional current flow. As the gate length becomes shorter and the drain voltage becomes larger, two-dimensional effects will dominate the device characteristics, and current flow in the depletion layer and in the substrate should be considered. In such cases, two-dimensional numerical simulation is required, where the Poisson's equation and the transport equations are solved simultaneously. Many works on this subject have been done to predict the I–V curves or to understand physical phenomena in GaAs MESFETs (17).

GaAs MESFET STRUCTURES

In the analysis done in the previous section, only the intrinsic region (under the gate) is considered. In real devices, there exist parasitic source resistance and drain resistance which originate from bulk regions between source and gate electrodes and between gate and drain electrodes, respectively. If the source resistance is high and the potential drop there becomes significant, the effective potential drop along the gate junction becomes smaller. So the degree of current modulation by the gate voltage is reduced, leading to a lower transconductance g_m. It should be also noted that high densities of surface states exist on the active layer, and so a surface depletion region is formed between source (drain) and gate electrodes. This contributes to increasing the source resistance.

Therefore, in real GaAs MESFETs, some methods to reduce the source resistance are adopted. There are many kinds of GaAs MESFET structures depending on their desired application. But we may classify GaAs MESFET structures in two main categories—the recessed gate structure and the self-aligned structure, as shown schematically in Fig. 7.

Recessed-Gate Structure

Recessing is a technique for adjusting the pinch-off (or threshold) voltage by reducing the active-layer thickness under the gate while maintaining a relatively low resistance between gate and source (drain) electrodes. This is achieved by using a rather thick n-type active layer in which the actual channel thickness is defined by controlled etching of a trench. The position and the shape of the recess are important design issues.

In power devices, the recess and the position of gate electrode are often asymmetrically located with a shorter distance to the source electrode than to the drain electrode. This has two advantages. It reduces the source resistance to maintain high transconductance g_m. And it increases the drain-to-source breakdown voltage and the gate breakdown (Schottky diode breakdown) voltage by allowing additional expansion

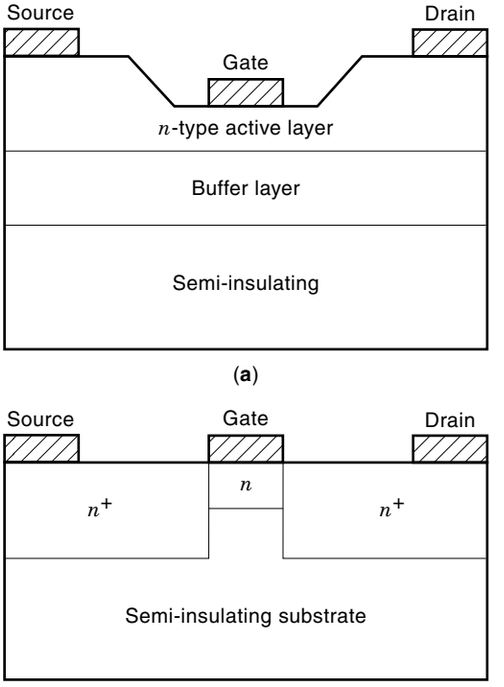


Figure 7. Schematic cross-section of the two main categories of GaAs MESFET structures: (a) recessed-gate structure, (b) self-aligned structure. Both of them have low source resistances.

space for the high-field region at the drain side of the gate. It is recognized that a graded recess is more effective than an abrupt recess in reducing electric field at the recess edge, and it provides higher breakdown voltage (18). As for the details on the breakdown phenomena, please refer to Ref. 18.

For microwave application, the semiconductor layer is typically grown by a molecular beam epitaxy (MBE) method to obtain desired doping profiles. A variety of doping profiles in the active layer may be used—from uniform doping to delta doping. Often, the gate is given a T-shape which combines a short gate length with a large gate metal cross section. The latter leads to a reduced parasitic gate resistance, which is particularly important in microwave devices.

A drawback of the recessed gate technique, especially in the context of ICs, is the limited alignment accuracy of the recess and of the gate electrode. The accuracy of recess etching is also a problem. These inaccuracies lead to non-uniformities in the source resistance, the transconductance and the threshold voltage over a wafer (and from wafer to wafer).

Self-Aligned Structures

The self-aligned gate technique is a method to self-align the source and drain n^+-layers to the gate as shown in Fig. 7(b). This structure is usually realized by first forming the gate region and then utilizing n^+-implantation. This is a planar structure and has a low source resistance and a high transconductance because of the n^+ source region which also reduces the surface-state effects. The self-aligned structure is particularly used for digital FETs, where the active layer is also fabricated by direct ion-implantation into the semi-insulating substrate, and relatively uniform threshold voltage

over a wafer is realized. A drawback of this structure is the low breakdown voltage of the Schottky diode. To overcome this problem, the lightly doped drain (LDD) structure is adopted (19).

The basic feature of the self-aligned gate process is shown in Fig. 8 (20). First, an n-type active layer is formed in the semi-insulating substrate by Si ion-implantation and subsequent annealing. Next, TiW (a refractory metal) is deposited by sputtering and etched to form the gate electrode. The gate

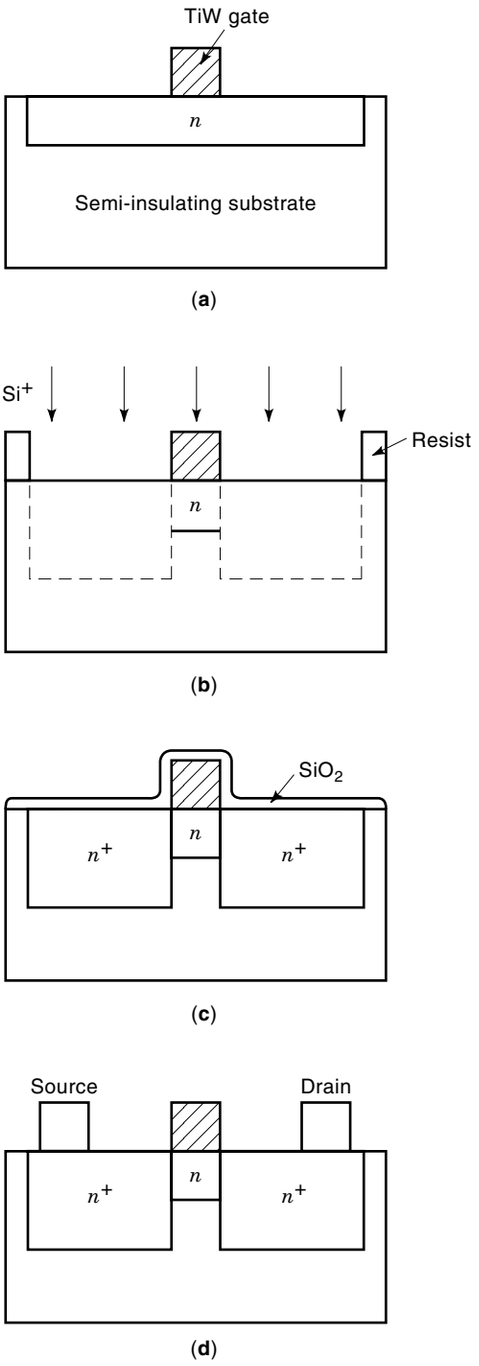


Figure 8. Fabrication process of self-aligned GaAs MESFET using TiW refractory gate, developed by Yokoyama et al. (20).

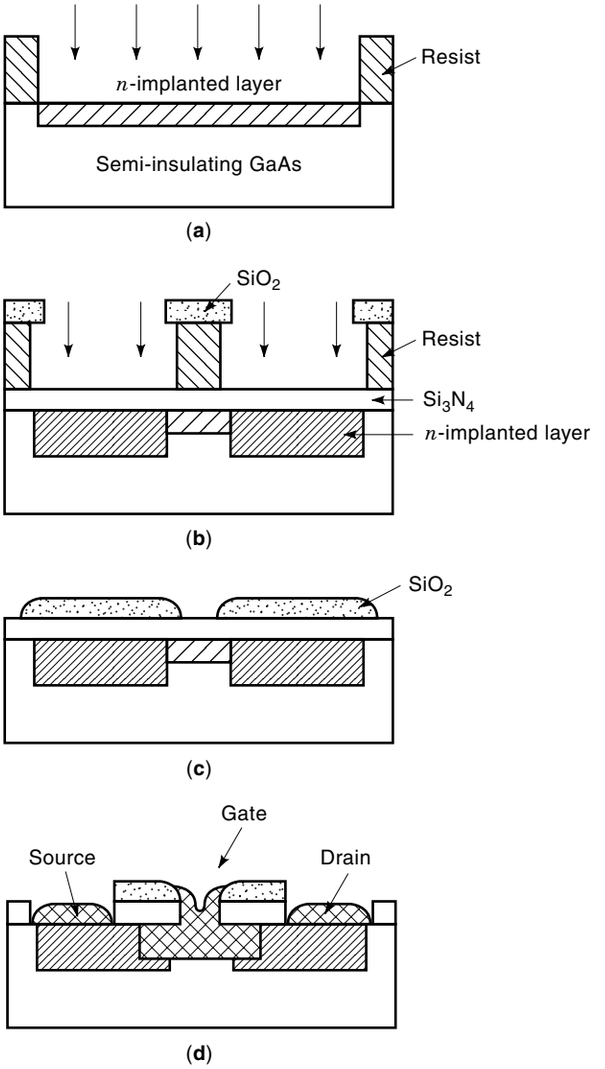


Figure 9. Fabrication process of SAINT MESFET. This process allows any choice of gate metal because the gate metalization is done after the high temperature anneal. (Reproduced with permission from K. Yamasaki, K. Asai, and K. Kurumada, GaAs LSI-directed MESFET's with self-aligned implantation for n+-layer technology (SAINT), *IEEE Trans. Electron Devices,* **ED-29**(11): 1772–1777 (© 1982 IEEE).)

then served as a mask for the subsequent n^+ source and drain implant, which is followed by another annealing stage using a SiO_2 cap. The device is completed using AuGe/Au ohmic contacts formed by liftoff. The gate metal must be capable of surviving the high temperature anneal (about 850 °C) without damaging the Schottky barrier properties. Various alloy metals such as TiW-based alloys and WSi-based alloys have proven suitable for this purpose. These compositions are not very conductive, but this is usually not a severe problem for digital FETs in which the gate width may be only 10 to 20 μm. It would be a severe problem for analog FETs having much wider gate fingers.

Another class of self-aligned process known as SAINT (self-aligned implantation for n^+-layer technology) (21) involves the use of a complex mask structure acting as a "dummy gate" for the n^+ implantation, as shown in Fig. 9.

The process starts by the selective implantation of the active layer and the deposition of Si_3N_4 cap layer. Then, the dummy gate is fabricated from layers of resist and SiO_2, patterned in a T-shape by undercutting the lower resist using plasma etching. The n^+-implantation is followed by the sputter deposition of a layer of SiO_2, a lift-off step, and the annealing of the implanted dopants. Then the ohmic contacts are fabricated. Finally, the remaining Si_3N_4 in the gate area is removed, and the gate metal is deposited. The process allows any choice of gate metalization because the gate metal is placed on the wafer after the high temperature anneal.

In the self-aligned MESFETs with n^+ source and drain regions, current-flow via the semi-insulating substrate between the n^+-layers becomes remarkable when the gate length becomes shorter. So the threshold voltage shifts with shortening the gate length, showing a remarkable short-channel effect. To overcome this problem, so-called BP (Buried p-layer)—SAINT (22) was proposed as shown in Fig. 10. Here, the p-implanted layer is formed under the n and n^+ regions and acts as a barrier for electrons injected into the substrate. In fact, it is shown experimentally and theoretically (23) that the short-channel effect is greatly reduced by introducing the p-layer. However, the high dose buried p-layer may lead to the degradation of device performance due to its parasitic capacitance (24).

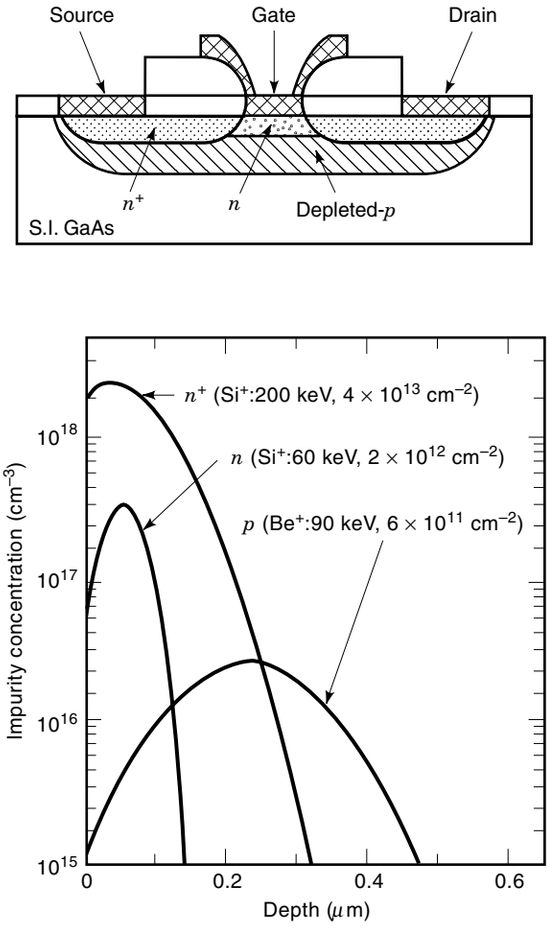


Figure 10. Cross-section view of a buried p-layer SAINT FET and calculated impurity concentration profiles. The p-layer acts as a barrier against electron injection from the channel into the semi-insulating substrate. (Reproduced with permission from K. Yamasaki, N. Kato, and M. Hirayama, Buried p-layer SAINT for very high-speed GAs LSI's with submicrometer gate length, *IEEE Trans. Electron Devices,* ED-32(11): 2420–2425 (© 1985 IEEE).)

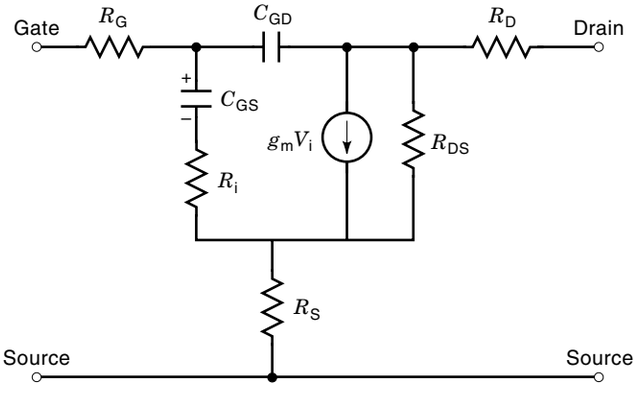


Figure 11. Small-signal equivalent circuit of a MESFET. C_{GS} and C_{GD} are the gate-to-source and gate-to-drain capacitances, respectively. R_i is the charging resistance, and R_{DS} is the output resistance. R_G, R_S, and R_D are the parasitic gate, source, and drain resistances, respectively.

HIGH-SPEED AND HIGH-FREQUENCY PERFORMANCE

How fast the GaAs MESFET operates or switches is an interesting point for a practical viewpoint. In a logic circuit, however, the switching time depends on the load capacitance, and it is not a unique measure of high-speed performance. As to standard high-speed and high-frequency figures of merit for FETs, there are the cutoff frequency f_T and the maximum frequency of oscillation f_{max}. f_T is defined as the frequency at which the short-circuit current gain falls to unify, and f_{max} is the highest frequency at which power gain can be obtained from the FET. These are correlated to the small-signal equivalent circuit of the FET, and they are also easily estimated by microwave measurements.

A typical small-signal equivalent circuit of a GaAs MESFET is shown in Fig. 11 (7,12). From this, the cutoff frequency f_T is derived as

$$f_T \simeq \frac{g_m}{2\pi C_{GS}} \tag{30}$$

where C_{GS} is the gate-source capacitance. The approximate expression for f_{max} is given by

$$f_{max} \simeq \frac{f_T}{2}\sqrt{\frac{R_{DS}}{R_G + R_i + R_S}} \tag{31}$$

where R_{DS} is the output resistance, and R_i is the charging resistance. R_G and R_S are the parasitic gate and source resistances, respectively. f_T is also expressed, by using the transit time through the channel τ, as (12)

$$f_T = \frac{1}{2\pi\tau} \tag{32}$$

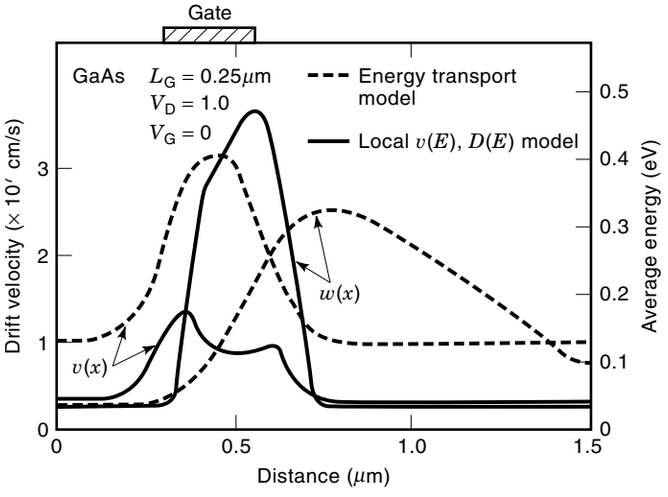


Figure 12. Drift velocity v and average electron energy w as functions of distance along the channel for a 0.25 μm gate-length GaAs MESFET, calculated by using energy-transport model (dashed lines) and quasi-equilibrium model (solid lines). In the case of energy transport model, the velocity becomes much higher than the saturation velocity (10^7 cm/s) under the gate, showing a remarkable velocity-overshoot effect. (Reproduced with permission from R. K. Cook and J. Frey, Two-dimensional numerical simulation of energy transport effect in Si and GaAs MESFET's, *IEEE Trans. Electron Devices,* **ED-29**(6): 970–977 (© 1982 IEEE).)

If we assume that electrons travel under the gate with the saturation velocity v_s, f_T becomes

$$f_T = \frac{v_s}{2\pi L_G} \tag{33}$$

From this, we can say that f_T should become higher as the gate length L_G becomes shorter.

As is understood from Eq. (32) and Eq. (33), f_T depends on how the electrons travel through the channel. There are some theoretical calculations on electron velocity profiles in short-channel GaAs MESFETs. Figure 12 shows such an example (25). According to the model that includes energy transport effects, the electron velocity becomes much higher than the saturation velocity ($\sim 10^7$ cm/s). This so-called velocity overshoot effect is more pronounced in GaAs-based devices than in Si-based devices. Therefore, higher f_T than that estimated by assuming the velocity saturation is expected in short-channel GaAs MESFETs.

Das (26) theoretically estimated f_T, f_{max}, and g_m of a GaAs MESFET with a short gate (0.1 $\sim$ 0.25 μm) by using the concept of charge control (27). Table 1 shows some of the results.

Table 1. Physical Parameters and Estimated Performance of GaAs MESFETs (Ref. (26)).

L_G	L_{GD}	a	N_D	v_S	g_m	f_T	f_{max}
(μm)	(μm)	(nm)	(cm^{-3})	(cm/s)	(mS/mm)	(GHz)	(GHz)
0.25	0.10	48.5	5×10^{17}	1.4×10^7	241	54	128
0.20	0.10	41	7×10^{17}	1.7×10^7	331	77	181
0.15	0.08	36	9×10^{17}	2.1×10^7	461	125	266
0.10	0.07	30	1.3×10^{18}	2.6×10^7	648	213	424

Here, L_{GD} is the gate-drain distance, a is the active-layer thickness, N_D is the donor density in the active layer, and v_s is the saturation velocity. The velocity overshoot was not taken into account explicitly in the calculations, but it was included in the value of v_s as an effective saturation velocity. It was also assumed that the gate was located as far from the drain and as close to the source as possible so that the gate-drain capacitance and the source resistance would be minimized. High values of f_T = 213 GHz, f_{max} = 424 GHz, and g_m = 648 mS/mm are predicted for the gate length L_G of 0.1 μm.

Golio et al. (28) collected and examined the experimental data for f_T, f_{max}, and g_m of GaAs MESFETs published in the literatures between 1966 and 1988. They have projected limits to the ultimate frequency performance which can be realized with GaAs MESFETs. The data projected at L_G = 0.1 μm are f_T = 80 $\sim$ 200 GHz, f_{max} = 300 $\sim$ 1000 GHz, and g_m = 300 $\sim$ 1000 mS/mm. Recently, Feng et al. (8) obtained f_T values of 55 GHz for 0.5 μm, 89 GHz for 0.25 μm, and 109 GHz for 0.15 μm gate-length GaAs MESFETs utilizing ion-implantation technology. These are comparable to those for GaAs-base HEMTs. As for f_{max}, a high value of 120 GHz was reported for a 0.25 μm gate-length GaAs MESFET in Ref. 29.

In the 1980s, GaAs MESFETs for digital ICs were studied extensively. The high-speed performance was characterized by the propagation delay time of the ring oscillator. A delay of 9.9 ps/gate for a 0.4 μm gate-length (BP-SAINT) GaAs MESFET was reported in Ref. 22. The performance of power GaAs MESFETs were also improved in the 1980s. The details are found in Ref. 18.

PARASITIC EFFECTS

The high-speed and high-frequency performance of GaAs MESFETs is due to the high electron velocity of GaAs. However, there are several unfavorable phenomena or parasitic effects in GaAs MESFETs such as short-channel effects, side-gating effects, slow-current transients, low-frequency anomalies (frequency-dependent transconductance and output conductance), and kink phenomena. These phenomenon are originated from the fact that the semi-insulating GaAs substrate (on which the MESFET is fabricated) is achieved by

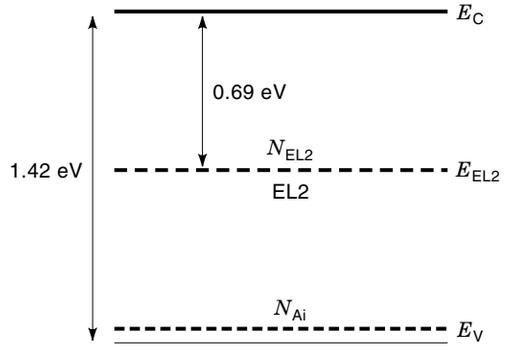


Figure 13. Two-level compensation model for undoped semi-insulating LEC GaAs. N_{EL2} and N_{Ai} are densities of deep donor "EL2" and shallow acceptor, respectively. The deep donors donate electrons to the shallow acceptors, and hence, the ionized EL2 density N^+_{EL2} becomes nearly equal to the shallow acceptor density N_{Ai} under equilibrium.

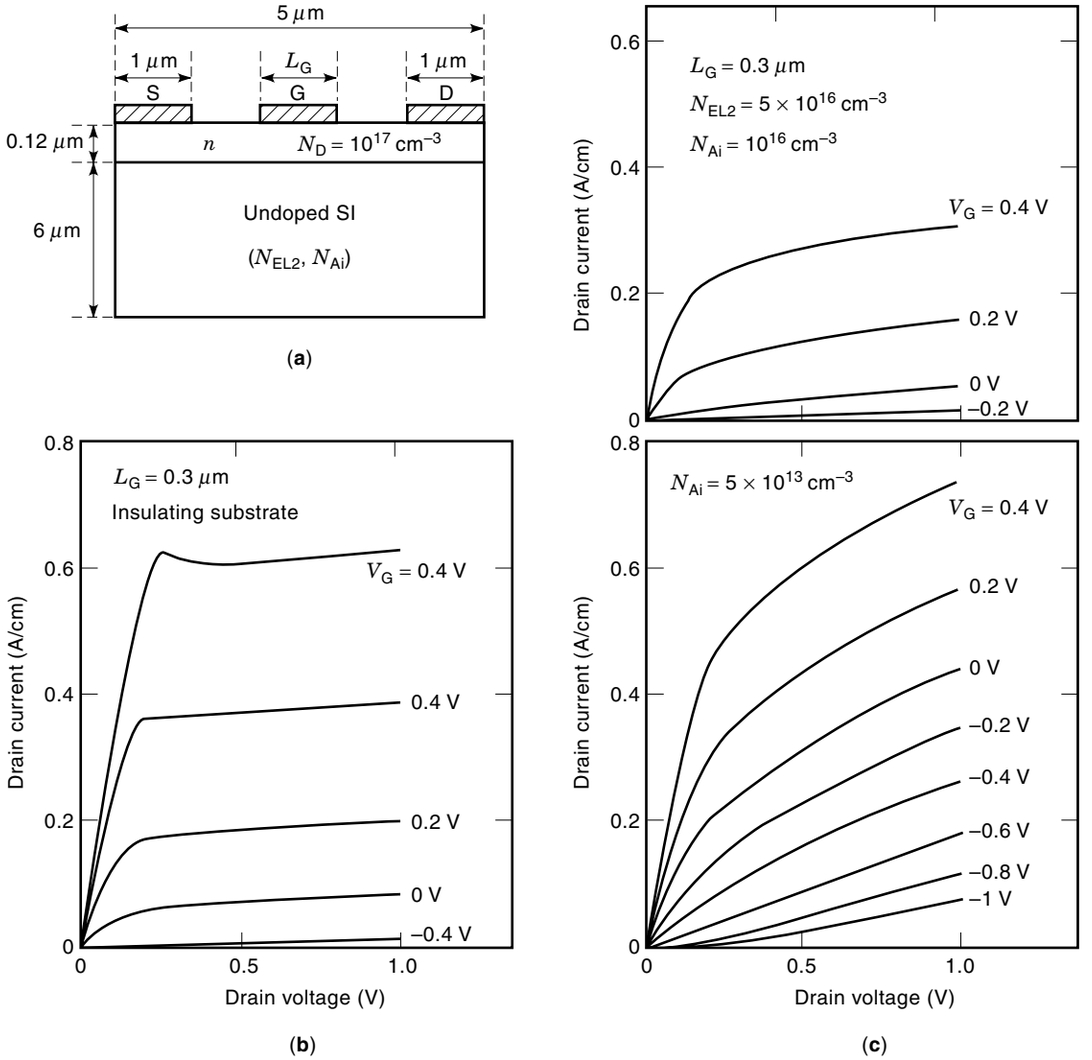


Figure 14. (a) Simulated GaAs MESFET structure. (b) Calculated drain characteristics for a case with perfectly insulating substrate. (c) Calculated drain characteristics for the two cases with different shallow-acceptor densities N_{Ai} in the semi-insulating substrate, where the deep-donor density N_{EL2} is 5×10^{16} cm^{-3}. With the semi-insulating substrate, the drain current does not saturate, particularly for lower N_{Ai}, because the substrate current becomes large (33).

impurity compensation at deep levels (30) and that high densities of surface states exist on the active layer of GaAs MESFETs. We will discuss these phenomena below.

Substrate Conduction

The analysis done before for deriving I–V characteristics of the MESFET is based on the assumption that the semi-insulating substrate is a perfect insulator, and current does not flow through it. But, in fact, the substrate is "semi-insulating" and not a perfect insulator. The semi-insulating nature is achieved by impurity compensation by deep levels. For an example, in the undoped semi-insulating LEC (liquid-encapsulated Czochralski) GaAs, which has been widely used since early 1980s, it is thought that deep donors "EL2" (N_{EL2}) compensate shallow acceptors due to residual carbon (N_{Ai}) (31), as shown in Fig. 13. In this case, the deep donors donate electrons to the shallow acceptors, and hence, semi-insulating properties are realized. In equilibrium, the ionized deep-donor density N^+_{EL2} becomes nearly equal to the shallow acceptor density N_{Ai}, and the ionized deep donors act as trap centers. If the n-layer is attached to the semi-insulating substrate, electrons are injected into the substrate and are captured by the traps. So if the ionized deep-donor density N^+_{EL2} (or N_{Ai}) is low, the trap-filled region (where all traps are filled with electrons) extends deeper into the substrate (32). The resistance in this region is low, and hence, the current can flow through the semi-insulating substrate.

Figure 14 shows examples of I–V characteristics of GaAs MESFETs on the undoped semi-insulating substrate, calculated by two-dimensional (2-D) numerical simulation in which Poisson's equation and continuity equations are solved self-consistently (33). Figure 14(a) is the simulated structure, and Fig. 14(b) corresponds to a case with perfectly insulating substrate. In Fig. 14(c), two cases with different shallow-acceptor

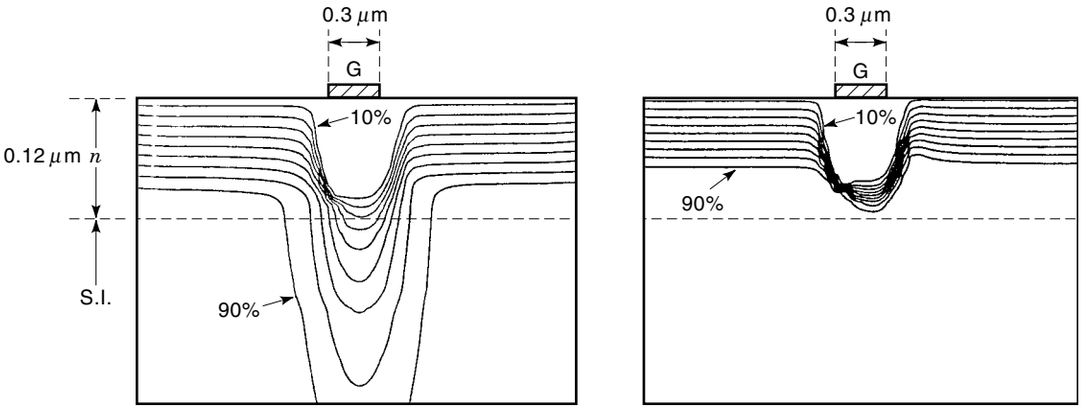


Figure 15. Comparison of current distributions of 0.3 μm gate-length GaAs MESFETs with different N_{Ai} in the semi-insulating substrate, corresponding to Fig. 14(c). V_D = 1 V and V_G = 0 V. $N_{EL2} = 5 \times 10^{16}$ cm^{-3}. (a) $N_{Ai} = 5 \times 10^{13}$ cm^{-3}, and (b) $N_{Ai} = 10^{16}$ cm^{-3}. For lower N_{Ai}, the substrate current component becomes larger, because the barrier for electrons at the channel–substrate interface is less steep.

density in the substrate ($N_{Ai} = 10^{16}$ cm^{-3} and 5×10^{13} cm^{-3}) are shown. The gate length L_G is 0.3 μm, and the field-dependent mobility expressed in Eq. (22) is used. The surface states are not considered in this calculation. In the case with perfectly insulating substrate, the drain current almost saturates with the drain voltage. In the cases with semi-insulating substrates, however, the drain currents do not saturate in general, and increase with the drain voltage, particularly for lower acceptor density N_{Ai} in the substrate. This is because, as shown in Fig. 15, the substrate current component becomes larger for lower N_{Ai}. This increase in substrate current leads to lower transconductance at a given drain current. It should be also noted that in the case with high N_{Ai}, the drain currents become lower than those for the case with perfectly insulating substrate. This is because, as schematically shown in Fig. 16, a space-charge layer is formed at the active layer-substrate interface, and the effective channel thickness becomes thinner for higher N_{Ai}. From the above considerations, we can say that to consider impurity compensation by deep levels in the semi-insulating substrate is important for evaluating I-V characteristics of GaAs MESFETs.

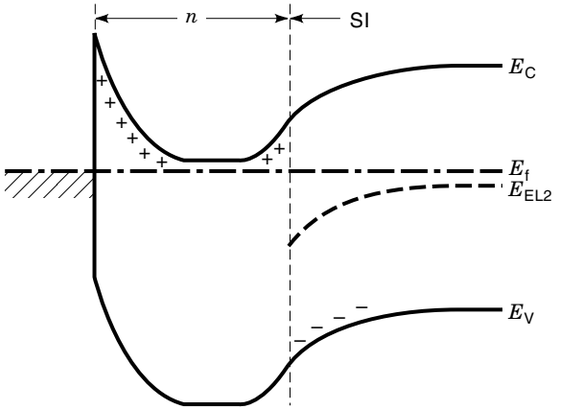


Figure 16. Schematic energy band diagram along the line from gate electrode to the substrate. The space-charge region is formed at the channel–substrate interface, because the semi-insulating substrate is achieved by impurity compensation by deep levels.

As seen in Fig. 14(c), when N_{Ai} is low and the substrate current becomes large, the threshold voltage of GaAs MESFETs shifts toward deeply negative. The shift of threshold voltage becomes more remarkable when the gate length becomes shorter. This phenomenon is one of the so-called short-channel effects. To reduce this, the substrate current must be reduced. For this purpose, the shallow acceptor density N_{Ai} in the semi-insulating substrate should be made relatively high. It is also effective to introduce a buried p-layer or a p-buffer layer because the acceptors in the p-layer should have the same electrical role as acceptors in the semi-insulating substrate. In fact, it is shown experimentally and theoretically that to introduce a buried p-layer (p-buffer layer) is effective to reduce the shore-channel effects in GaAs MESFETs (22,23).

Sidegating Effects

The sidegating effect is a phenomenon that the drain current of a GaAs MESFET is modulated when a negative voltage is applied to an adjacent device in ICs. This was also called the backdating effect because initially the current modulation was studied by attaching an electrode to the backside of the substrate. This effect is detrimental in GaAs digital, analog and microwave ICs because of unintentional electrical interactions between closely spaced devices. Numerous studies have suggested that this effect is caused by modulation of the space-charge region at the interface between the MESFET active layer and the buffer layer or the semi-insulating substrate which is achieved by impurity compensation by deep levels.

Two representative experimental data about sidegating (backgating) effects in the early 1980s are shown in Fig. 17 (34) and in Fig. 18 (35). In Fig. 17, a Cr-doped HB (horizontal Bridgman) semi-insulating substrate was used, and the electrode was attached to the bottom of the substrate. The group X′ corresponded to a case without a buffer layer, and the group A′ and B′ corresponded to cases with different buffer layers. In all three cases, the drain currents decreased without threshold as the substrate bias voltage became negative. The authors detected hole drops due to Cr both in the buffer layer and in the semi-insulating substrate. In Fig. 18, a LEC

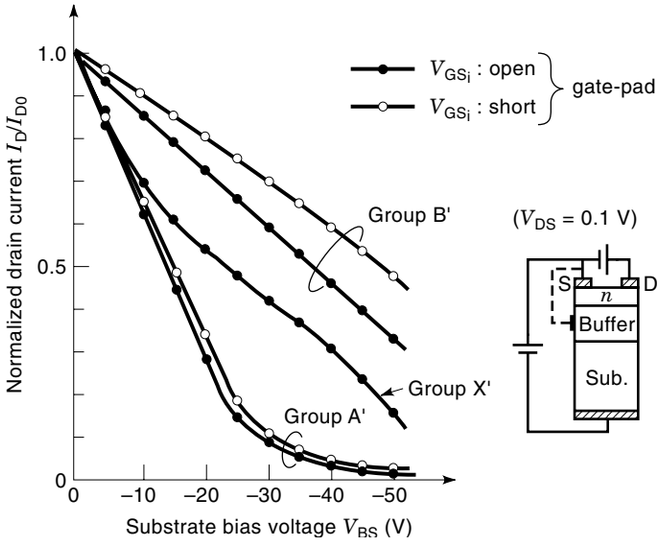


Figure 17. Experimental results of drain-current reduction due to substrate bias. The Cr-doped HB semi-insulating substrate is used. The drain currents decrease without threshold when the substrate bias voltage becomes negative. (Reproduced with permission from T. Itoh and H. Yanai, Stability of performance and interfacial problem in GaAs MESFET's, *IEEE Trans. Electron Devices,* **ED-27**(6): 1037–1045 (© 1980 IEEE).)

Cr-doped semi-insulating substrate was used, and the sidegate (backgate) electrode was attached to the same surface as the MESFET. The substrate current showed ohmic behavior at low voltages and showed a sudden rise at a certain threshold voltage. Just at this voltage, the drain current began to decrease. Thus, the threshold voltage for the sudden increase in the substrate current was exactly the same as the threshold voltage for the sidegating effect. This threshold behavior was typical also for cases of using undoped semi-insulating LEC substrates extensively studied later. The threshold behavior was qualitatively explained by Lampert's carrier injection model (32,36).

The above difference in sidegating behavior for different types of substrates can be explained as follows. In the undoped semi-insulating LEC GaAs, as described before, deep donors "EL2" compensate shallow acceptors, and the deep donor acts as an electron trap because its capture cross section for electrons is much larger than that for holes (30). In the Cr-doped semi-insulating substrate, deep acceptors "Cr" compensate shallow donors, and the deep acceptor acts as a hole trap because its capture cross section for holes is much larger than that for electrons (30). Fig. 19 shows a comparison of calculated energy band diagrams of n–i–n structures with different i-layers (substrates) (37). The left n-layer corresponds to the MESFET active layer. Part (a) is for a case with EL2, and part (b) is for a case with Cr. In (b), the voltage is entirely applied along the reverse-biased n–i junction because electrons as well as holes are depleted there, and hence, the drain current of the MESFET decreases without threshold when negative voltage is applied to an adjacent n-layer. In (a), the voltage is applied along the bulk i-region because electrons are not depleted at the reverse-biased n–i junction because of the electron-trap nature of EL2 (32). Then, the substrate current shows ohmic behavior at low voltages, and the drain current of the MESFET changes little. When the applied voltage becomes so high that the traps are all filled with electrons, the substrate current increases suddenly, and the voltage becomes applied along the reverse-based n–i junction. Therefore, the drain current begins to decrease with threshold in this case. The corresponding voltage is called the trap-fill-limited voltage (36) and given by

$$V_{\mathrm{TFL}} = \frac{qN_{\mathrm{Ai}}}{2\epsilon} d^2 \tag{34}$$

where d is the i-layer thickness. However, the voltage given by Eq. (34) was usually too high as compared to the experimental voltage for threshold, and this model did not necessarily give quantitative explanations.

Recently, it was pointed out that the Schottky pad (of GaAs MESFET) directly attached to the semi-insulating substrate should play an important role in the sidegating effect. Liu et al. (38) studied effects of Schottky contact on the semi-insulating substrate by using the test structure shown in Fig. 20, where the results of sidegating effects are also shown when the Schottky contact (SC) is floating, or its voltage V_{SC} is set to 0 V. It is seen that the current in the n–i–n structure, formed by the MESFET and the sidegate, is very low within the voltage range of the measurements. On the other hand, the current in the Schottky-i–n structure, formed by the Schottky contact and the sidegate, show a sudden increase at a relatively low voltage, indicating a remarkable sidegating effect. The most likely cause of this high leakage current might be the hole injection from the Schottky contact, as has been suggested by computer simulation (39). The existence of the Schottky pad on the semi-insulating substrate could explain, to some extent, the reduction of the threshold voltage for sidegating. However, there are no quantitative models to predict the onset voltage adequately.

To improve the sidegating threshold, two approaches were adopted (40). One was to use isolation implantation techniques such as oxygen, boron, and protons. This technique increased the threshold voltage for sidegating by about a factor of three. The other approach was to shield the MESFET channel from the offending sidegating electrodes. A Schottky metal shield between the sidegate electrode and the FET and a Be-implanted p-type shield tied to the source contact were shown to improve sidegate immunity. Recently, Chen and Smith et al. (41) showed that a new buffer layer grown by molecular-beam epitaxy (MBE) at a substantially low temperature (~200 °C) could greatly reduce the sidegating effect. However, the basic mechanism responsible for its unique semi-insulating property is not yet clarified. Many studies on this so-called LT (low temperature)–GaAs buffer are being made.

Slow Current Transients

GaAs MESFETs are essentially high-speed and high-frequency devices. However, slow current transients are often observed experimentally even if the drain voltage or the gate voltage is changed abruptly. These are called "drain-lag" or "gate-lag" and could seriously limit the performance of power MESFETs as well as pulse operating integrated circuits. For example, gate-lag affects digital circuits such as inverter chains by causing pulse narrowing, which finally leads to function error. It is suggested that these phenomena occur due to the slow responses of deep traps in the semi-insulating substrate or surface states on the active layer.

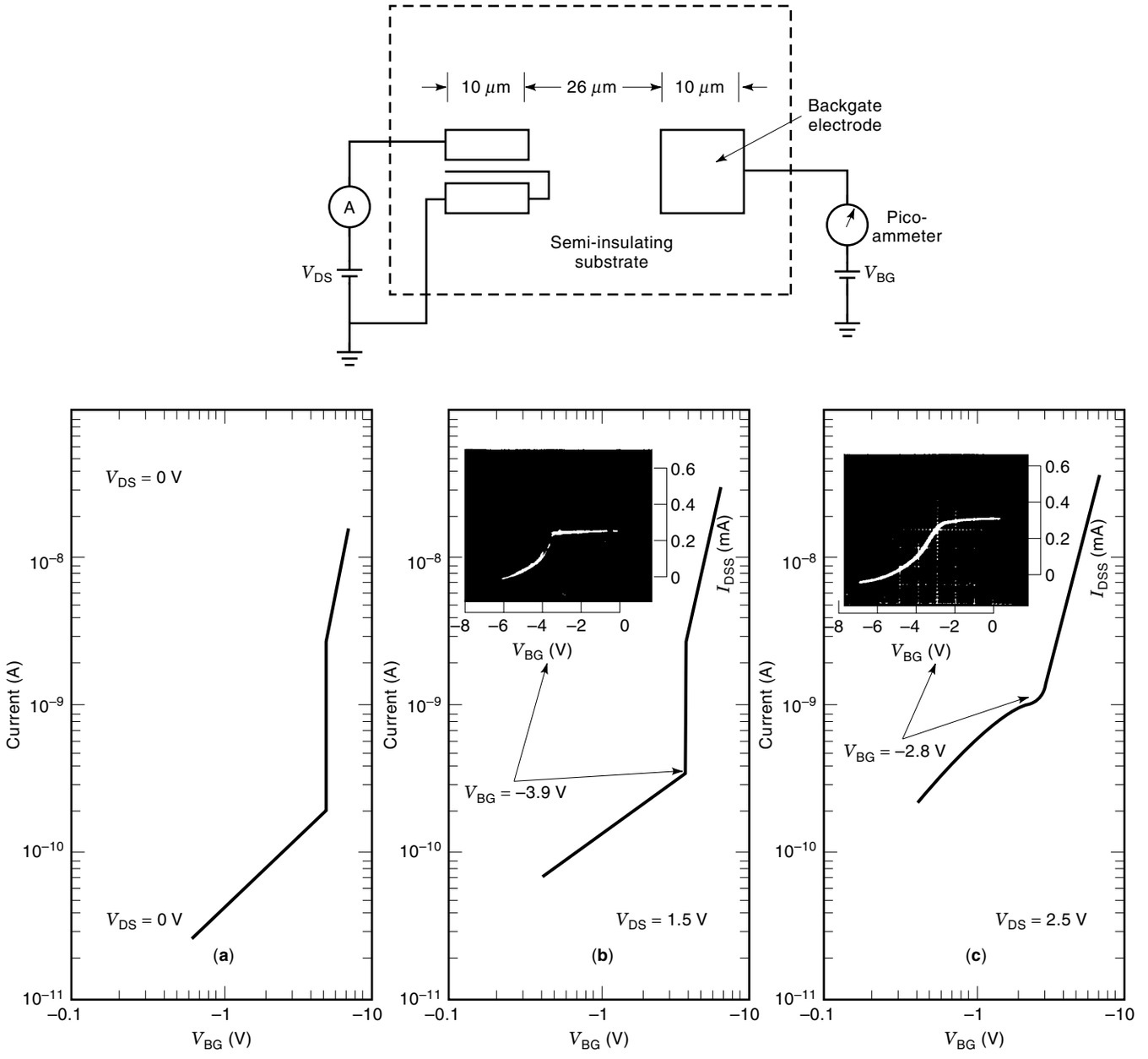


Figure 18. The test structure used for sidegating measurements, and the current-voltage relation of the substrate conduction between the MESFET and the backgate (sidegate) electrode when (a) V_{DS} = 0 V, (b) V_{DS} = 1.5 V, and (c) V_{DS} = 2.5 V. The LEC Cr-doped semi-insulating substrate is used. The sidegating characteristics, I_{DSS} vs. V_{BG} at V_{DS} = 1.5 V and V_{DS} = 2.5 V, are shown by the photographs in (b) and (c), respectively. The sudden increase in the substrate conduction corresponds to the sudden decrease in the drain current. (Reproduced with permission from C. P. Lee, S. J. Lee, and B. M. Welch, Carrier injection and backgating effect in GaAs MESFET's, *IEEE Electron Device Lett.,* **EDL-3**(4): 97–98 (© 1982 IEEE).)

Figure 21 shows an example of drain-lag phenomenon experimentally reported by Mickanin et al. (42). They used a 300 μm wide enhancement-mode GaAs MESFET on undoped semi-insulating LEC substrate. The gate voltage was set to the pinch-off voltage, defined as I_D = 1 μA/μm at V_D = 1 V. As shown in Fig. 21, 10 Hz and 100 kHz drain-voltage pulses from 0 to 5 V were applied, and the drain-current transients were traced. It is seen that the current with a 10 Hz pulse rate shows overshoot behavior. This type of overshoot has been commonly observed by other researchers. The absence of overshoot with a 100 kHz pulse rate indicates that this phenomenon is frequency-dependent. This phenomenon was usually explained by trapping dynamics at the channel-substrate interface or in the semi-insulating substrate. An example of drain-lag phenomena calculated by 2-D simulation is shown in Fig. 22 (43). The device structure is the same as that

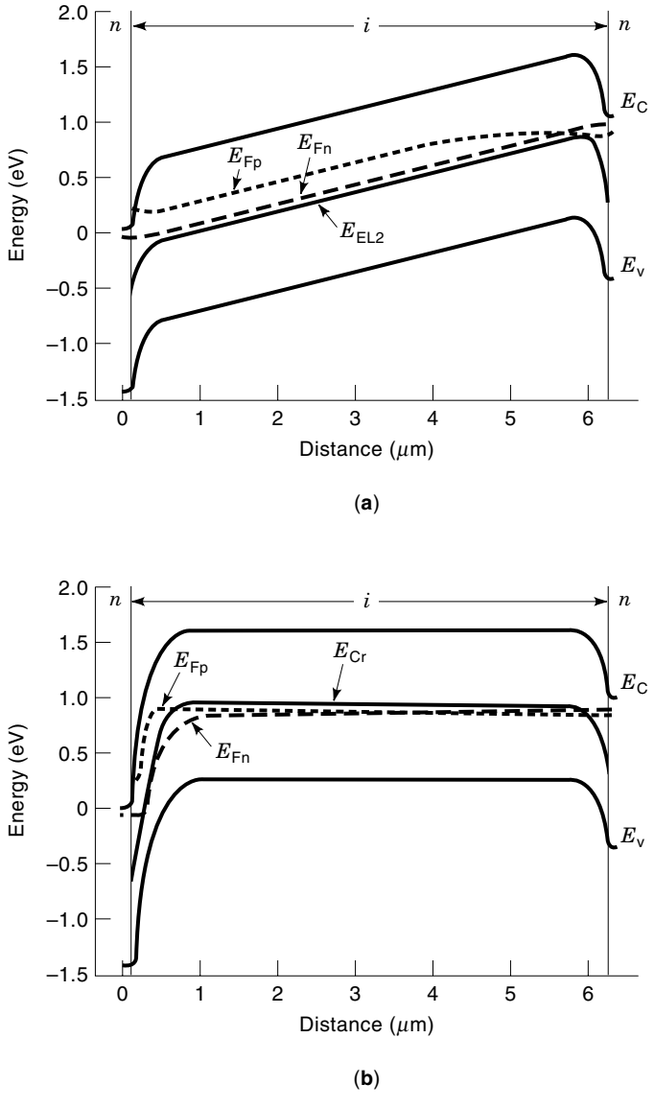


Figure 19. Comparison of calculated energy band diagrams of n–i–n structures with different deep levels in the i-layer. (a) Case with deep donor "EL2" ($N_{EL2} = 5 \times 10^{16}$ cm^{-3}) and shallow acceptor ($N_{Ai} = 10^{16}$ cm^{-3}), and (b) case with deep acceptor Cr ($N_{Cr} = 10^{16}$ cm^{-3}) and shallow donor ($N_{Di} = 10^{15}$ cm^{-3}). "EL2" acts as an electron trap, and "Cr" acts as a hole trap. This difference leads to the difference in the energy-band diagrams (32,37).

in Fig. 14(a). The gate voltage is 0 V, and the drain voltage is changed abruptly from 0 to 1 V or from 1 to 0.5 V. The drain currents become constant temporarily (a "quasi-steady state") around $t = 10^{-11}$ sec, and after some periods, they begin to decrease or increase, reaching real steady-state values. In fact, the current overshoot is observed when the drain voltage is raised. It is interpreted that the quasi-steady state is a state where the deep donors "EL2" in the substrate do not respond to the voltage change, and electrons move under the same ionized-impurity densities as those for $V_D = 0$ V or 1 V. When the deep donors begin to capture or emit electrons, the drain currents begin to decrease or increase, reaching steady-state values. Therefore, the deep donors in the substrate can be also a cause of hysteresis in I–V curves.

Figure 23 shows schematic diagram of gate-lag measurement and $V_{gs(off)}$ dependence of drain current transients recently reported by Kohno et al. (44). They used a single recessed-gate MESFET with the pinch-off voltage of −2.4 V. When the gate voltage was changed from $V_{gs(off)}$ to $V_{gs(on)} = 0$ V, the drain currents remained low for some periods and began to increase gradually between 10^{-4} and 10^{-1} s, reaching steady-state values. As $V_{gs(off)}$ was lower, the gate-lag became more pronounced. The gate-lag phenomenon was usually correlated to the surface states on the active layer. Lo and Lee (45) simulated the gate-lag phenomenon by considering surface states, which were assumed to consist of a pair of deep donors and deep acceptors. The results are shown in Fig. 24. They used a planer MESFET with the threshold (pinch-off) voltage of −2.5 V. Here, the Gate lag rate was defined as $(I_D(t = 250\text{ ms}) - I_D(t = 1\text{ ns}))/I_D(t = 250\text{ ms})$. In fact, as the initial gate voltage was lower, the gate-lag percentage increased. It was understood that the gate-lag arose because the response of surface deep levels were slow. It was also shown that when the initial gate voltage was lower, the negative surface charge density was higher to enhance the gate-lag phenomenon.

To reduce the above lag phenomena, effects of deep traps in the substrate and surface states should be minimized. Canfield et al. (46) used the p-well technology where the p-well potential was constrained by connecting it to the source and showed that the drain-lag was eliminated. To reduce the gate-lag, several methods to minimize the surface-state effects have been proposed, but no conclusive way has been realized.

Low-Frequency Anomalies

Many of the electrical characteristics of GaAs MESFETs shift dramatically in values at relatively low frequencies (<1 MHz) (7). Device parameters which have been observed to shift include output conductance (drain conductance) g_D, transconductance g_m, and device capacitances. As the frequency is increased, the measured output conductance is seen to increase by as much as a factor of two (47). The characteristic frequencies at which this increase occurs ranges less than 10 Hz to about 100 kHz. The transconductance usually decreases with the frequency, and the decrease rate is typically 5 to 30 percent. The frequency dependences of g_D and g_m can be correlated to the drain-lag and the gate-lag, respectively. Therefore, these frequency dependences are attributed to the existence of deep traps in the semi-insulating substrate and surface states on the active layer.

A typical example of measured frequency dependence of g_D in a GaAs MESFET is shown in Fig. 25 by symbols (47). The device was a standard, recessed-gate depletion-made MESFET fabricated on undoped semi-insulating LEC GaAs. The gate length was 1 μm, and the n-channel was formed by ion implantation to a peak concentration of approximately 2×10^{17} cm^{-3}. As seen, the output conductance also indicated temperature dependence. These frequency and temperature dependences of g_D were attributed to deep donor "EL2" in the semi-insulating substrate. By assuming a temperature-dependent time constant of electron emission form EL2:

$$\tau_e \simeq \frac{3.5 \times 10^{-8}}{T^2} \exp\left(\frac{9450}{T}\right) \tag{35}$$

theoretical curves of frequency-dependent g_D were derived. They are shown in Fig. 25 by solid curves. These fit well with the experimental results. It was shown experimentally that

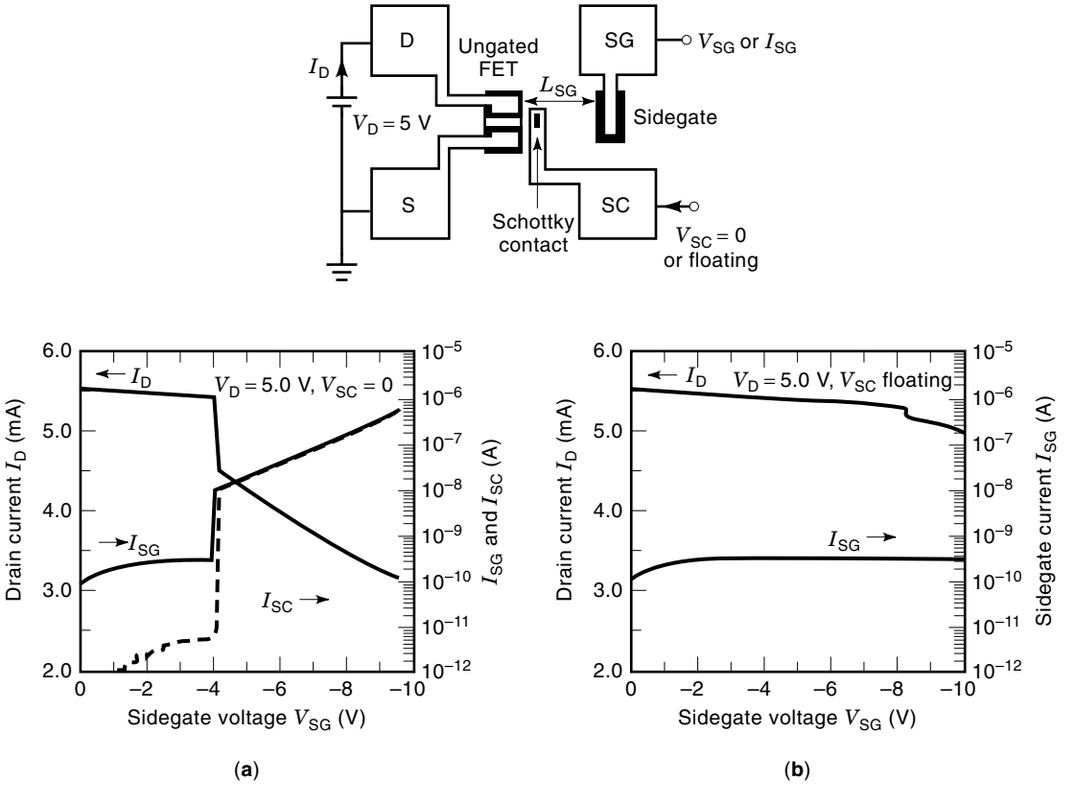


Figure 20. Schematic top view of the test structure used in the measurements, and results of the voltage-controlled sidegating effect measurements. (a) Results measured with V_{SC} = 0, and (b) results measured with V_{SC} floating. With V_{SC} = 0, the sidegating effect is observed at a low sidegate voltage V_{SG}. (Reproduced with permission from Y. Liu, R. W. Dutton, and M. D. Deal, Schottky contact effects in the sidegating effect of GaAs devices, *IEEE Electron Device Lett.,* **13**(3):149–151 (© 1992 IEEE).)

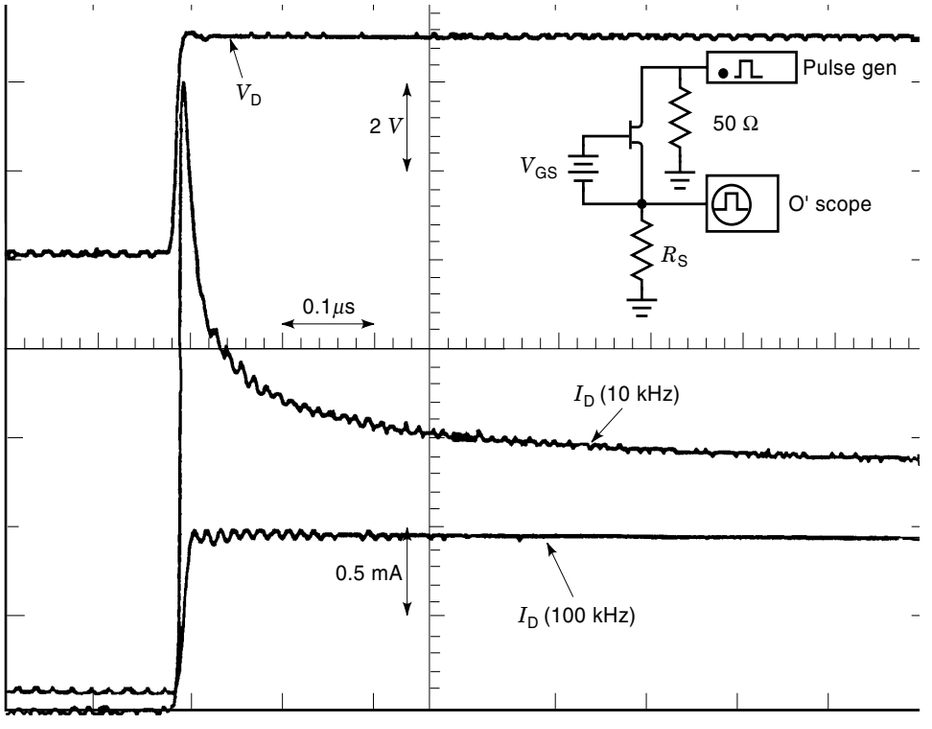


Figure 21. Schematic measurement system of drain-lag and measured waveforms. The upper is the drain voltage pulse. The lower curves show drain current transients at 10 Hz and 100 KHz pulses, respectively. The current overshoot and the subsequent slow transient are observed at the 10 Hz pulse. (Reproduced with permission from W. Mickanin, P. Canfield, E. Finchem, and B. Odekirk, Frequency-dependent transients in GaAs MESFETs: process, geometry and material effects, *IEEE GaAs IC Symposium Technical Digest,* 211–214 (© 1989 IEEE).)

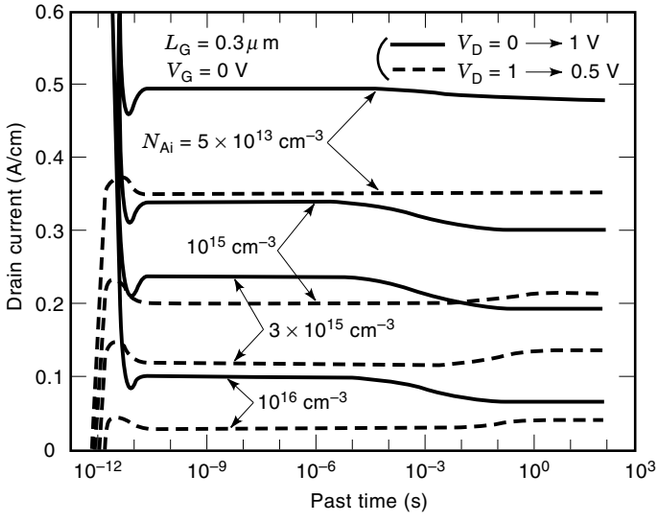


Figure 22. Calculated responses of drain currents for 0.3 μm gate-length GaAs MESFETs on undoped semi-insulating substrate [Fig. 14(a): $N_{EL2} = 5 \times 10^{16}$ cm^{-3}] when V_D steps from 0 to 1 V and when V_D steps from 1 to 0.5 V (43). The current overshoot and the subsequent slow transient are qualitatively reproduced for the former case (solid lines).

by using the *p*-well GaAs MESFET technology, the frequency dependence of output conductance was not observed up to 1 MHz (46).

An example of measured frequency dispersion of transconductance for a GaAs MESFET is shown in Fig. 26 (48). The device was fabricated by Si ion implantation into undoped semi-insulating LEC GaAs. The gate length was 1 μm. Both the drain bias and the superimposed gate modulation signal δv_{gs} were kept small ($\sim$50 mV). (The drain bias was kept low in order to make the assumption that the channel depth is constant, and so the channel region may be treated as a resistance.) As seen in the figure, the transconductance decreased with the frequency and showed dispersion over a limited range of temperature. This behavior was explained by the surface-state dynamics. At temperatures below 150 K, the surface states responded so slowly that they could not follow even the lowest modulation frequency used (10 Hz). As the temperature was raised, their response time decreased, falling within the window of used measurement frequencies. At still higher temperature ($\sim$400 K), the response of the surface states was so fast that the characteristic frequency became much higher than the highest used frequency here (20 kHz), so there was no dispersion again. Zhao et al. (49) developed an analytical model for frequency dependence of transconductance in GaAs MESFETs. Assuming a single surface state ES1 ($E_C - E_{S1} = 0.4$ eV, $N_{S1} = 10^{12}$ cm^{-2}, $\sigma_{S1} = 10^{-11}$ cm^2), he obtained the temperature dependence of transconductance frequency dispersion as shown in Fig. 27. A general agreement is seen between the modeling results and experimental results in Fig. 26.

Kink Phenomena

High-voltage behavior of GaAs MESFETs has always been of interest for microwave applications where the maximum power is limited in part by the breakdown voltage of the device. Recently, it was reported that the GaAs MESFETs showed an abnormal increase in the output conductance (kink phenomenon) at relatively low voltages (3 $\sim$ 4 V) (50,51). This phenomenon may limit the operation voltage of GaAs MESFETs. It was recognized that the kink was associated with impact ionization of carriers in the channel. It was also suggested that the kink was not due to direct gate breakdown but could be regarded as a phenomenon related to the substrate.

An example of measured drain characteristics of GaAs MESFETs reported by Harrison (51) is shown in Fig. 28. The device was a 0.8 μm gate-length self-aligned GaAs MESFET fabricated on undoped LEC semi-insulating substrate. The output conductance in the saturated region showed an increase for $V_D > 3.5$ V. It was shown that in this kink region, the sidegating effect became remarkable. This strongly suggests that the semi-insulating substrate should play an important role in the kink phenomenon. It was proposed that holes which were generated by impact ionization and injected into the semi-insulating substrate were the origin of these phenomena.

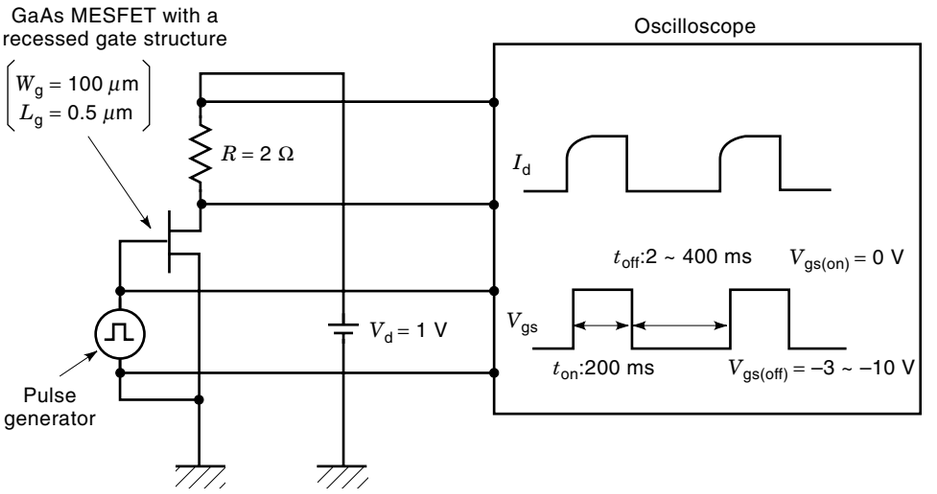
Drain characteristics of a 0.3 μm gate-length GaAs MESFET, calculated by 2D simulation considering impact ionization of carriers, are shown in Fig. 29(a) (52). The simulated structure is the same as that in Fig. 14(a), where the shallow acceptor density in the substrate N_{Ai} is 10^{16} cm^{-3}. The characteristic show kink behavior at $V_D = 3 \sim 5$ V and at $V_D = 10 \sim 15$ V. However, these are not due to direct gate breakdown because the gate current is much lower than the drain current as shown in Fig. 29(b). Figure 30 shows calculated hole density profiles at $V_D = 4$ V and 12 V for $V_G = 0$ V. It is understood that holes generated by impact ionization flow into the substrate and are captured by deep donors "EL2," and hence, the ionized deep-donor density N^+_{EL2} increases. This increase in positive charges in the substrate increases the channel thickness, resulting in the first kink. At $V_D = 12$ V, hole densities in the substrate become very high and comparable to N^+_{EL2}, but the hole current is much lower than the electron current. In this case, we can interpret that the increase in the positive hole charges in the substrate widens the channel thickness, leading to the steep increase in the drain current. It was also ascertained by 2D simulation (53) that the sidegating effects should become remarkable in the kink region. In another work (54), it was suggested that the kink could be reduced by decreasing the acceptor density in the substrate.

MESFET MODELING

Modeling for Circuit Simulation

For circuit design applications, accurate but simple device models are required. Purely physical models such as those described when deriving the *I–V* characteristics are usually not accurate as required for most applications. The inaccuracies arise from the assumptions and approximations required to perform the device analysis. In contrast, empirical models can be accurate enough to fit the experimental data, though large amount of tedious characterization data are often required to obtain the accuracy.

An early and basic empirical model for GaAs MESFETs was proposed by Curtice (55). The current-voltage character-



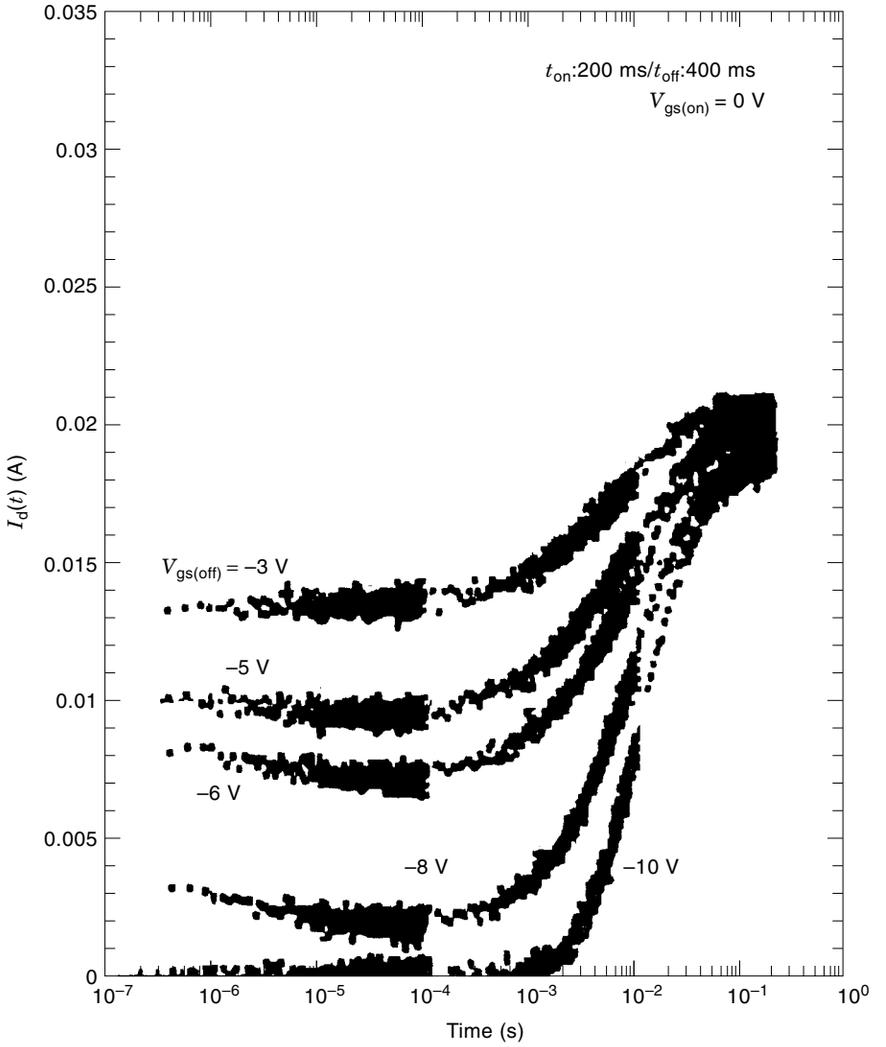


Figure 23. Schematic diagram of gate-lag measurement and measured $V_{gs(off)}$ dependence of drain-current transients. The gate-lag is remarkable when the off-state gate voltage $V_{gs(off)}$ is deeply negative. (Reproduced with permission from Y. Kohno et al., Modeling and suppression of the surface trap effect on drain current frequency dispersions in GaAs MESFETs, *IEEE GaAs IC Symposium Technical Digest,* 263–266 (© 1994 IEEE).)

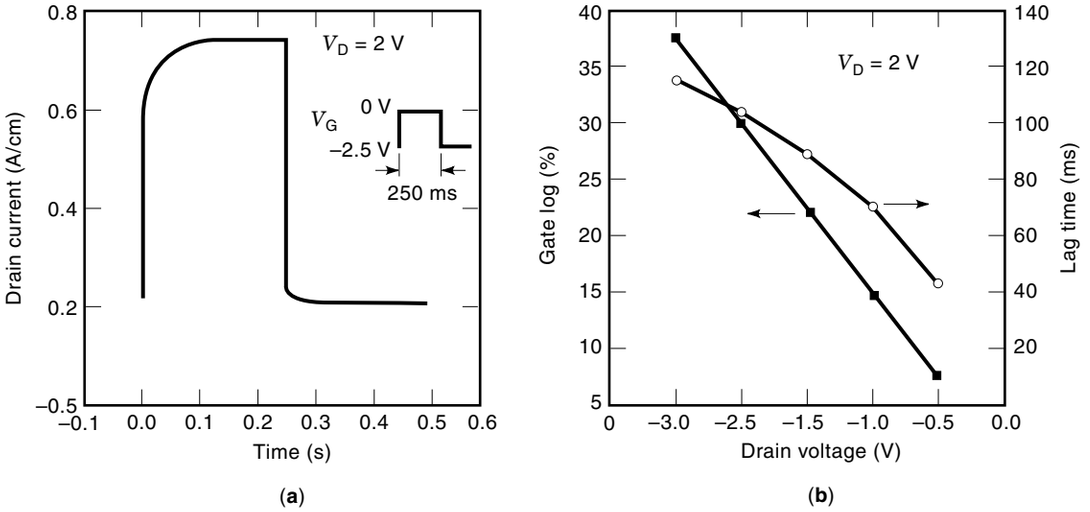


Figure 24. (a) Calculated example of gate-lag phenomenon. (b) Calculated lag percentage and lag time when the gate voltage is changed from −2.5, −2, −1.5, −1, and −0.5 V to 0 V. The gate-lag is enhanced when the off-state gate voltage is more negative. (Reproduced with permission from S. H. Lo and C. P. Lee, Analysis of surface trap effect on gate lag phenomena in GaAs MESFET's, *IEEE Trans. Electron Devices,* **41**(9):1504–1512 (© 1994 IEEE).)

istics were expressed as

$$I_D = \beta(V_G - V_T)^2(1 + \lambda V_D)\tanh(\alpha V_D) \tag{36}$$

where V_T is the threshold voltage or the pinch-off voltage. β, λ, and α are the parameters. Eq. (36) can be separated into three components. The first component $\beta(V_G - V_T)^2$ is used to model the approximately square-law behavior of the I_D–V_G relationship. In the second component $1 + \lambda V_D$, the parameter λ is used to model the drain conductance. The third component $\tanh(\alpha V_D)$ is used because the hyperbolic tangent approximates the I_D–V_D characteristics observed in GaAs MESFETs. α determines the voltage at which the drain current saturates. Curtice and Ettenberg (56) altered the original Curtice model to get a closer fit to the relationship between I_D and V_G. The new equation is

$$I_D = (A_0 + A_1 v_1 + A_2 v_1^2 + A_3 v_1^3)\tanh(\gamma V_D) \tag{37}$$

$$v_1 = V_G\{1 + \beta(V_{D0} - V_D)\}$$

where β and γ are the parameters. V_{D0} is the drain voltage at which the A_i coefficients are evaluated.

Statz et al. (57) developed a model based on Eq. (36). They thought that the square-law approximation of the $I_D - V_G$ relationship was only valid for small values of $V_G - V_T$, and that I_D became almost linear for larger values of $V_G - V_T$. To model this behavior, in place of $\beta(V_G - V_T)^2$, they adopted the

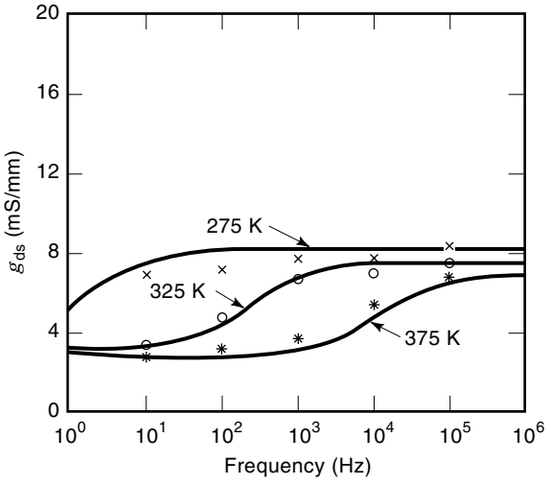


Figure 25. Comparison between the experimentally observed output conductance (×, ○, ∗) and the theoretical curves (solid lines) at three different temperatures for V_D = 3 V and V_G = 0.2 V. The increase in output conductance with frequency is often seen experimentally. (Reproduced with permission from P. C. Canfield, S. C. F. Lam, and D. J. Allstot, Modeling of frequency and temperature effects in GaAs MESFETs, *IEEE J. Solid-State Circuits,* **25**(1):299–306 (© 1990 IEEE).)

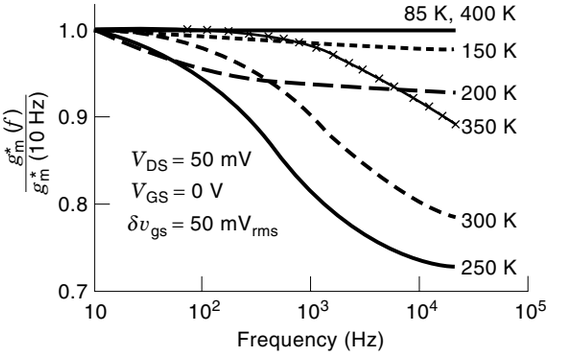


Figure 26. Measured frequency dispersion of transconductance as a function of temperature for a 1 μm gate-length GaAs MESFET. The decrease in transconductance with frequency is often seen experimentally. (Reproduced with permission from S. R. Blight, R. H. Wallis, and H. Thomas, Surface influence on the conductance DLTS spectra of GaAs MESFET's, *IEEE Trans. Electron Devices,* **ED-33**(10): 1447–1453 (© 1986 IEEE).)

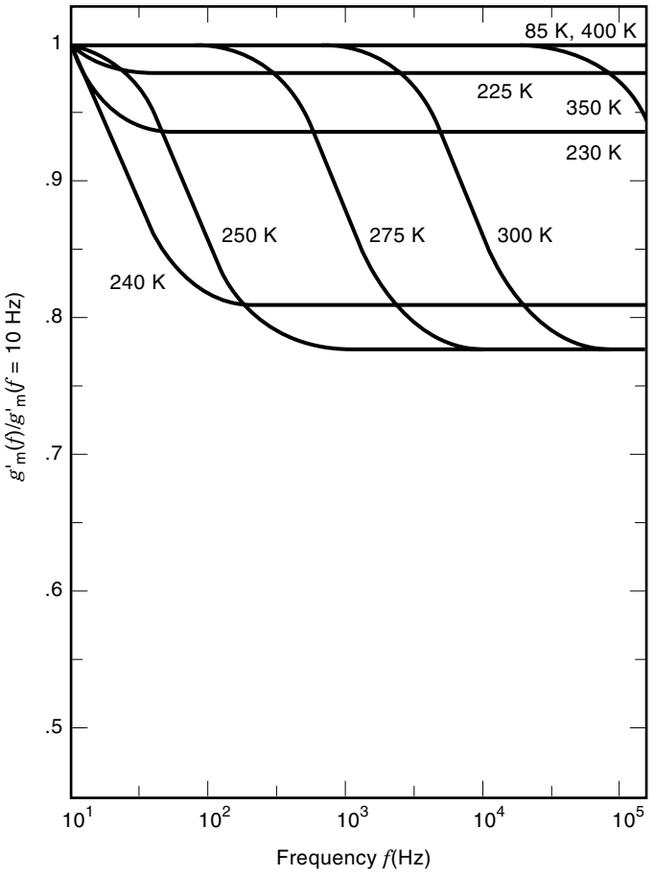


Figure 27. Modeling results of temperature dependence of transconductance dispersion for a single surface state case. A general agreement is seen between these modeling results and the experimental results in Fig. 26. (Reproduced with permission from J. H. Zhao, R. Hwang, and S. Chang, On the characterization of surface states and deep traps in GaAs MESFETs, *Solid-State Electron.,* **36**(12):1665–1672 (© 1993 Elsevier Science Ltd.).)

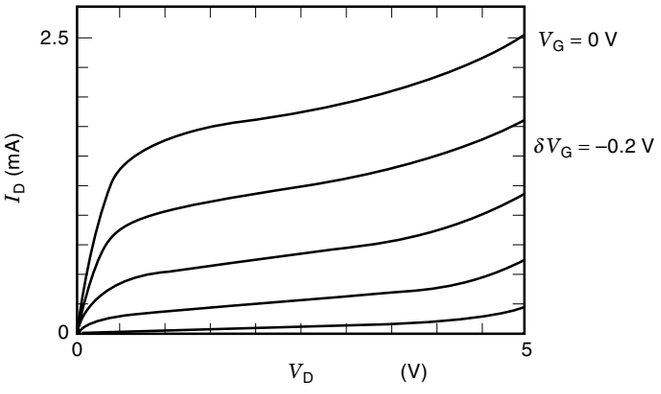


Figure 28. Measured drain characteristics of 0.8 μm gate-length GaAs MESFET, showing the onset of the kink phenomenon at V_D = 3.5 V. (Reproduced with permission from A. Harrison, Backgating in submicrometer GaAs MESFET's operated at high drain bias, *IEEE Electron Device Lett.,* **13** (7): 381–383 (© 1992 IEEE).)

empirical expression

$$\frac{\beta(V_G - V_T)^2}{1 + b(V_G - V_T)}$$

In addition, they found that the tanh function in Eq. (36) consumed considerable computer time. The tanh function below saturation was modified using a polynominal of the form

$$1 - (1 - (\alpha V_D/n))^n$$

with $n = 3$. In the saturated region ($V_D > n/\alpha$), the tanh function was replaced by unity. These modifications led to a new form for the drain current.

For $0 < V_D < 3/\alpha$,

$$I_D = \frac{\beta(V_G - V_T)^2}{1 + b(V_G - V_T)}\left[1 - \left(1 - \frac{\alpha V_D}{3}\right)^3\right](1 + \lambda V_D) \qquad (38)$$

For $V_D \geq 3/\alpha$

$$I_D = \frac{\beta(V_G - V_T)^2}{1 + b(V_G - V_T)}(1 + \lambda V_D) \qquad (39)$$

The model was compared with the experimental data. Figure 31 shows such an example (57). The agreement between the model and the experiment was satisfactory.

Besides the models mentioned above, some other models for circuit simulation such as SPICE were proposed. About these models and the applicability of them, please refer to Ref. 7, where the modeling of device capacitance not mentioned here is also found.

Device Simulation

When the gate length of GaAs MESFETs became short, the analytical one-dimensional approach with several assumptions became inadequate for estimating the I–V characteristics or other device performance. Then, the 2-D numerical simulation that solved Poisson's equation and transport equations self-consistently became used for predicting the device performance and for understanding physical phenomena observed in GaAs MESFETs. Historically, 2-D simulation of GaAs MESFETs was already made in the middle 1970s, in particular for understanding effects of negative differential mobility in GaAs on the device performance.

The so-called drift-diffusion type simulation method is now a mature and standard tool for evaluating the performance of GaAs devices as well as Si devices (17,58). As to recent topics regarding this method, there are numerical simulations of trapping effects on GaAs MESFET performance. If we now treat a GaAs MESFET on undoped semi-insulating LEC substrate including deep donors "EL2," the basic equations for device analysis can be written as follows (33,43).

(a) Poisson's equation

$$\nabla^2\psi = -\frac{q}{\epsilon}(p - n + N^+_{EL2}) \qquad (40)$$

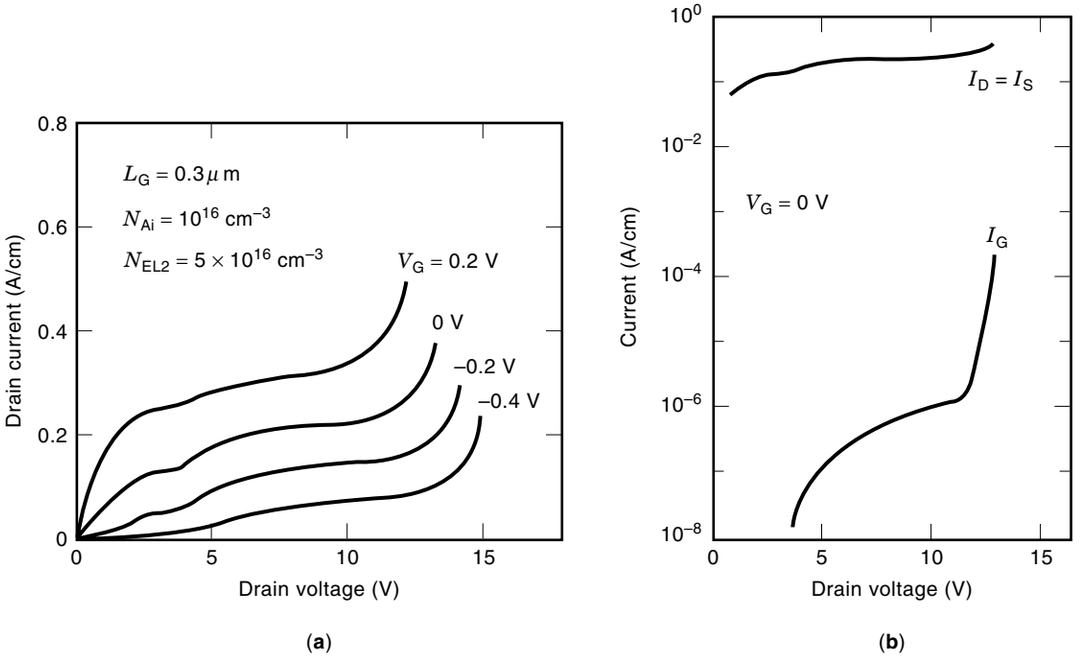


Figure 29. Simulated (a) drain characteristics and (b) terminal currents versus drain voltage curves of 0.3 μm gate-length GaAs MESFET on undoped semi-insulating substrate shown in Fig. 14(a). Two kinks are seen at $V_D = 3 \sim 5$ V and at $V_D = 10 \sim 15$ V (52).

(b) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n - \{C_n N_{EL2}^+ n - e_n(N_{EL2} - N_{EL2}^+)\} \tag{41}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot J_p - \{C_p(N_{EL2} - N_{EL2}^+)p - e_p N_{EL2}^+\} \tag{42}$$

(c) Rate equation for deep levels

$$\frac{\partial}{\partial t}(N_{EL2} - N_{EL2}^+) = \{C_n N_{EL2}^+ n - e_n(N_{EL2} - N_{EL2}^+)\} - \{C_p N_{EL2} - N_{EL2}^+)p - e_p N_{EL2}^+\} \tag{43}$$

(d) Current equations for electrons and holes

$$J_n = -q\mu_n n\nabla\psi + qD_n\nabla n \tag{44}$$

$$J_p = -q\mu_p p\nabla\psi - qD_p\nabla p \tag{45}$$

where N_{EL2}^+ represents the ionized EL2 density, C_n and C_p are electron and hole capture coefficients of EL2, respectively, e_n and e_p are electron and hole emission rates of EL2, respectively, and other symbol have their normal meanings. By solving these equations, the deep-trap effects on the substrate conduction, the sidegrating effects, the slow-current transients, and the frequency-dependent small-signal parameters

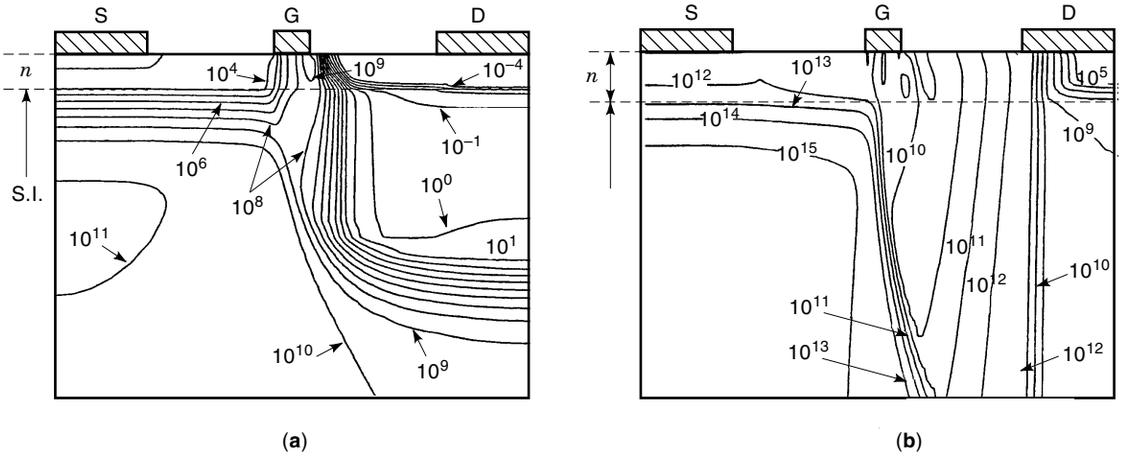


Figure 30. Calculated hole density profiles at (a) $V_D = 4$ V and (b) $V_D = 12$ V, corresponding to Fig. 29. $V_G = 0$ V. Holes generated by impact ionization flow into the substrate and are captured by deep donors "EL2." The increase in N_{EL2}^+ is the origin of the first kink, and the increase in hole charges themselves (b) is the cause of the second kink.

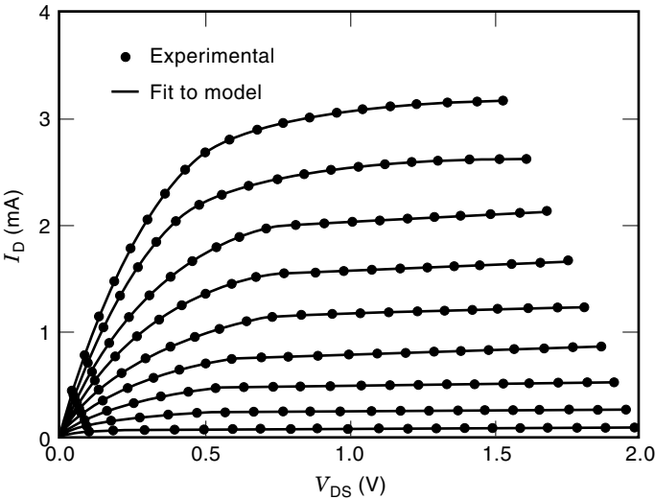


Figure 31. Comparison of modeled and measured drain characteristics of a GaAs MESFET. The very good agreement is observed. (Reproduced with permission from H. Statz et al., GaAs FET device and circuit simulation in SPICE, *IEEE Trans. Electron Devices,* **ED-34**(2): 160–169 (© 1987 IEEE).)

can be analyzed. By modeling the surface states as deep levels, surface-state effects on these phenomena can also be analyzed.

It is well recognized that the drift-diffusion model is inadequate for treating the nonequilibrium carrier transport that becomes important in shorter gate-length GaAs MESFETs. To treat this problem, a hydrodynamic model that uses three conservation equations derived from the Boltzmann transport equation have been adopted (17,25,59). These equations for electrons can be written as

$$\frac{\partial n}{\partial t} + \nabla \cdot (nv) = 0 \tag{46}$$

$$\frac{\partial v}{\partial t} + v \cdot \nabla v = -\frac{qE}{m^*} - \frac{2}{3m^* n}\nabla\left[n\left(w - \frac{m^*}{2}v^2\right)\right] - \frac{v}{\tau_p} \tag{47}$$

$$\frac{\partial \omega}{\partial t} + v \cdot \nabla w = -qv \cdot E - \frac{2}{3n}\nabla \cdot \left[nv\left(w - \frac{m^*}{2}v^2\right)\right] - \frac{w - w_0}{\tau_w} \tag{48}$$

where v is the average electron velocity, w is the average electron energy, and w_0 is the equilibrium value of w. m^*, τ_p, and τ_w are the effective mass, the momentum relaxation time, and the energy relaxation time, respectively, and these are usually given as a function of w. As a more fundamental method to treat the nonequilibrium carrier transport, there is a Monte Carlo simulation method (60). This method is suitable for studying fundamental carrier transports in the device, but may not be suited for device design use because it requires large computer resources.

Finally, it should be pointed out that in the compound semiconductor device fields such as GaAs MESFETs, the simulation results have not necessarily been compared with experimental data. This situation is quite contrary to that in Si devices. To compare the simulation results with experiments will contribute much to refining the models and optimizing the device structures.

BIBLIOGRAPHY

1. F. Ren et al., III–V compound semiconductor MOSFETs using $Ga_2O_3(Gd_2O_3)$As gate dielectric, *IEEE GaAs IC Symp. Tech. Dig.,* 18–21, 1997.
2. C. A. Mead, Schottky barrier gate field-effect transistor, *Proc. IEEE,* **54**: 307–308, 1966.
3. W. W. Hooper and W. I. Lehrer, An epitaxial GaAs field-effect transistor, *Proc. IEEE,* **55**: 1237–1238, 1967.
4. J. Turner et al., *Inst. Phys. Conf. Ser.,* **9**: 234–239, 1971.
5. M. Fukuta et al., Mesh source type microwave power FET, *IEEE Int. Solid-State Circuit Conf. Tech. Dig.,* 84–85, 1973.
6. T. Mimura et al., A new field-effect transistor with selectively doped GaAs/n-Al_xGa_{1-x}As heterojunctions. *Jpn. J. Appl. Phys.,* **19**: L225–L227, 1980.
7. J. M. Golio, *Microwave MESFETs & HEMTs,* Norwood, MA: Artech House, 1991.
8. M. Feng and J. Laskar, On the speed and noise performance of direct ion-implanted GaAs MESFET's, *IEEE Trans. Electron Devices,* **40**: 9–17, 1993.
9. *Vitesse Data Book.*
10. V. Milutinovic (ed.), *Microprocessor Design for GaAs Technology,* New Jersey: Prentice Hall Advanced Reference Series, Engineering, 1990.
11. W. Shockley, Unipolar field-effect transistor, *Proc. IRE,* **40**: 1365–1376, 1952.
12. S. M. Sze, *Physics of Semiconductor Devices,* 2nd ed., New York: Wiley, 1981.
13. K. Lehovec and R. Zuleeg, Voltage-current characteristics of GaAs JFET in the hot electron range, *Solid-State Electron.,* **13**: 1415–1426, 1970.
14. H. W. Thim, Computer study of bulk GaAs devices with random and dimensional doping fluctuations, *J. Appl. Phys.,* **39**: 3897–3904, 1968.
15. H. Statz, H. A. Haus, and R. A. Pucel, Noise characteristics of gallium arsenide field-effect transistor, *IEEE Trans. Electron Devices,* **ED-21**: 549–562, 1974.
16. M. Shur, *GaAs Devices and Circuits,* New York: Plenum Press, 1987.
17. C. M. Snowden and R. E. Miles (eds.), *Compound Semiconductor Device Modelling,* London: Springer-Verlag, 1993.
18. J. L. B. Walker (ed.), *High Power GaAs FET Amplifiers,* Norwood, MA: Artech House, 1993.
19. J. Mikkelson, GaAs digital VLSI device and circuit technology, *IEDM Tech. Dig.,* 231–234, 1991.
20. N. Yokoyama et al., A self-aligned source/drain planar device for ultra-high-speed GaAs VLSIs, *ISSCC Dig. Tech. Papers,* 218–219, 1981.
21. K. Yamasaki, K. Asai, and K. Kurumada, GaAs LSI-directed MESFET's with self-aligned implantation for n^+-layer technology (SAINT), *IEEE Trans. Electron Devices,* **ED-29**: 1772–1777, 1982.
22. K. Yamasaki, N. Kato, and M. Hirayama, Buried p-layer SAINT for very high-speed GaAs LSI's with submicrometer gate length, *IEEE Trans. Electron Devices,* **ED-32**: 2420–2425, 1985.
23. K. Horio et al., Numerical simulation of GaAs MESFET's with a p-buffer layer on the semi-insulating substrate compensated by deep traps, *IEEE Trans. Microw. Theory Tech.,* **37**: 1371–1379, 1989.
24. R. A. Sadler et al., A high yield buried p-layer fabrication process for GaAs LSI circuits, *IEEE Trans. Electron Devices,* **38**: 1271–1279, 1991.
25. R. K. Cook and J. Frey, Two-dimensional numerical simulation of energy transport effect in Si and GaAs MESFET's, *IEEE Trans. Electron Devices,* **ED-29**: 970–977, 1982.

26. M. B. Das, Millimeter-wave performance of ultrasubmicrometer-gate field-effect transistors: a comparison of MODFET, MESFET and PBT structures, *IEEE Trans. Electron Devices,* **ED-34**: 1429–1440, 1987.
27. M. B. Das, Charge-control analysis of MOS and junction-gate field-effect transistors, *Proc. IEE,* **113**: 1240–1248, 1966.
28. J. M. Golio and J. R. J. Golio, Projected frequency limits of GaAs MESFET's, *IEEE Trans. Microw. Theory Tech.,* **39**: 142–146, 1991.
29. R. M. Nagarajan et al., Design and fabrication of 0.25-μm MESFET's with parallel and π-gate structures, *IEEE Trans. Electron Devices,* **36**: 142–145, 1989.
30. G. M. Martin et al., Compensation mechanism in GaAs, *J. Appl. Phys.,* **51**: 2840–2852, 1980.
31. D. E. Holmes et al., Compensation mechanism in liquid encapsulated Czochralski GaAs: Importance of melt stoichiometry, *IEEE Trans. Electron Devices,* **ED-29**: 1045–1051, 1982.
32. K. Horio, T. Ikoma, and H. Yanai, Computer-aided analysis of GaAs *n-i-n* structures with a heavily compensated *i*-layer, *IEEE Trans. Electron Devices,* **ED-33**: 1242–1250, 1986.
33. K. Horio, H. Yanai, and T. Ikoma, Numerical simulation of GaAs MESFET's on the semi-insulating substrate compensated by deep traps, *IEEE Trans. Electron Devices,* **35**: 1778–1785, 1988.
34. T. Itoh and H. Yanai, Stability of performance and interfacial problem in GaAs MESFET's, *IEEE Trans. Electron Devices,* **ED-27**: 1037–1045, 1980.
35. C. P. Lee, S. J. Lee, and B. M. Welch, Carrier injection and backgating effect in GaAs MESFET's, *IEEE Electron Device Lett.,* **EDL-3**: 97–98, 1982.
36. M. A. Lampert and P. Mark, *Current Injection in Solids,* New York: Academic Press, 1970.
37. K. Horio, K. Asada, and H. Yanai, Two-dimensional simulation of GaAs MESFETs with deep acceptors in the semi-insulating substrate, *Solid-State Electron.,* **34**: 335–343, 1991.
38. Y. Liu, R. W. Dutton, and M. D. Deal, Schottky contact effects in the sidegating effect of GaAs devices, *IEEE Electron Device Lett.,* **13**: 149–151, 1992.
39. S. J. Chang and C. P. Lee, Numerical simulation of sidegating effect in GaAs MESFET's, *IEEE Trans. Electron Devices,* **40**: 698–704, 1993.
40. R. Y. Koyama et al., Parasitic effects and their impact on gallium arsenide integrated circuits, *Proc. 5th Conf. Semi-insulating III-V Materials,* 203–212, 1988.
41. C. L. Chen et al., Reduction of sidegating in GaAs analog and digital circuits using a new buffer layer, *IEEE Trans. Electron Devices,* **36**: 1546–1556, 1989.
42. W. Mickanin et al., Frequency-dependent transients in GaAs MESFETs: process, geometry and material effects, *IEEE GaAs IC Symposium Tech. Dig.,* 211–214, 1989.
43. K. Horio and F. Fuseya, Two-dimensional simulations of drain-current transients in GaAs MESFET's with semi-insulating substrates compensated by deep levels, *IEEE Trans. Electron Devices,* **41**: 1340–1346, 1994.
44. Y. Kohno et al., Modeling and suppression of the surface trap effect on drain current frequency dispersions in GaAs MESFETs, *IEEE GaAs IC Symp. Tech. Dig.,* 263–266, 1994.
45. S. H. Lo and C. P. Lee, Analysis of surface trap effect on gate lag phenomena in GaAs MESFET's, *IEEE Trans. Electron Devices,* **41**: 1504–1512, 1994.
46. P. C. Canfield and D. J. Allstot, A *p*-well GaAs MESFET technology for mixed-mode applications, *IEEE J. Solid-State Circuits,* **25**: 1544–1549, 1990.
47. P. C. Canfield, S. C. F. Lam, and D. J. Allstot, Modeling of frequency and temperature effects in GaAs MESFETs, *IEEE J. Solid-State Circuits,* **25**: 299–306, 1990.
48. S. R. Blight, R. H. Wallis, and H. Thomas, Surface influence on the conductance DLTS spectra of GaAs MESFET's, *IEEE Trans. Electron Devices,* **ED-33**: 1447–1453, 1986.
49. J. H. Zhao, R. Hwang, and S. Chang, On the characterization of surface states and deep traps in GaAs MESFETs, *Solid-State Electron.,* **36**: 1665–1672, 1993.
50. H. I. Fujishiro et al., Modulation of drain current by holes generated by impact ionization in GaAs MESFET, *Jpn. J. Appl. Phys.,* **28**: L1734–L1736, 1989.
51. A. Harrison, Backgating in submicrometer GaAs MESFET's operated at high drain bias, *IEEE Electron Device Lett.,* **13**: 381–383, 1992.
52. K. Horio and K. Satoh, Two-dimensional analysis of substrate-related kink phenomena in GaAs MESFET's, *IEEE Trans. Electron Devices,* **41**: 2256–2261, 1994.
53. K. Usami and K. Horio, 2-D simulation of kink-related sidegating effects in GaAs MESFETs, *Solid-State Electron.,* **39**: 1737–1745, 1996.
54. W. Wilson et al., Understanding the cause of IV kink in GaAs MESFET's with two-dimensional numerical simulation, *IEEE GaAs IC Symp. Tech. Dig.,* 109–112, 1995.
55. W. R. Curtice, A MESFET model for use in the design of GaAs integrated circuits, *IEEE Trans. Microw. Theory Tech.,* **MTT-28**: 448–456, 1980.
56. W. R. Curtice and M. Ettenberg, A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers, *IEEE Trans. Microw. Theory Tech.,* **MTT-33**: 1383–1394, 1985.
57. H. Statz et al., GaAs FET device and circuit simulation in SPICE, *IEEE Trans. Electron Devices,* **ED-34**: 160–169, 1987.
58. S. Selberherr, *Analysis and Simulation of Semiconductor Devices,* Wien, Germany: Springer-Verlag, 1984.
59. K. Blotekjaer, Transport equations for electrons in two-valley semiconductors, *IEEE Trans. Electron Devices,* **ED-17**: 38–47, 1970.
60. C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation,* Wien: Springer-Verlag, 1989.

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