OHMIC CONTACTS

Nearly any solid-state device requires at least one ohmic contact. Therefore, ohmic contacts play a major role in the functionality of devices. Metal-semiconductor contacts were first investigated over a century ago by Ferdinand Braun. Today ohmic contacts to semiconductors critically determine the performance, reliability, and scaling requirements of the devices themselves. Currently, electronic circuits and semiconductor materials are much better developed than the contacts themselves. A substantial amount of work on ohmic contacts to semiconductors has been conducted over the past 50 years. New challenges, such as contacts for ultralarge-scale integrated (ULSI) circuits or good ohmic contacts for wide bandgap semiconductors, require a fundamental understanding of the metal-semiconductor interface. State-of-the-art rectifying and ohmic contacts as well as the theoretical background are reviewed in Refs. 1–3.

In practice, a metal-semiconductor contact is considered as ohmic if the voltage drop across it is much smaller than that across the device, regardless of the polarity of the voltage. This does not necessarily imply that the current voltage characteristic of the contact itself is linear (4). Thus, the ohmic contact should not significantly perturb device performance. The quality of an ohmic contact is defined by the specific contact resistivity ρ_C. In general, the requirements on contacts can be summerized as follows:

1. Low contact resistivity
2. Good adhesion
3. High thermal stability
4. High corrosion resistance
5. Bondable top layer
6. Suitable for micropatterning

The required specific contact resistivity depends clearly on the application. Normally an ohmic contact to a semiconductor is fabricated by opening a window in a nonconducting passivation layer (such as an oxide or nitride layer), and a metal layer is deposited by electron-beam evaporation or sputtering. In the case of ULSI circuits the contact resistivity must be as

J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*. Copyright © 1999 John Wiley & Sons, Inc.

small as possible due mainly to the small contact dimensions. On the other hand, larger contact resistivities can be tolerated for larger contacts (e.g., for sensor applications).

Another class of contacts are heterojunction contacts of two types of semiconductors. These semiconductor heterojunctions are important in optoelectronic devices (e.g., solid-state lasers), heterobipolar transistors, and field effect transistors. A heterojunction is a junction formed between two dissimilar semiconductors. They can be either p–n junctions or isotype n–n or p–p junctions. The isotype heterojunctions are majority carrier junctions similar to metal semiconductor junctions. This type of contact is sometimes used to achieve low-resistivity ohmic contacts to wider bandgap semiconductors.

THEORY OF METAL-SEMICONDUCTOR CONTACTS

Ideal Metal-Semiconductor Contacts

Metal contacts to semiconductors can be either ohmic or rectifying (Schottky contacts). Both types of contacts can be described by one model when the contact is ideal. Ideal contacts to semiconductors are characterized by an atomically abrupt interface without surface states and without structural inhomogeneities between a metal and the semiconductor. In this case the current-voltage characteristic of a metal-semiconductor contact is determined by the work function ($q\phi_s$ for the semiconductor and $q\phi_m$ for the metal) and by the electron affinity $q\chi$, which is the energy difference between the conduction band edge and the vacuum level in the semiconductor. The work function is defined as the energy difference between the Fermi level and the vacuum level. The work function is therefore the required minimum energy to remove an electron from the Fermi level E_F to a position outside of the material.

Figure 1 shows the corresponding energy band diagram of an isolated metal adjacent to an isolated n-type semiconductor, assuming that the work function for the metal is larger than the work function of the semiconductor. When the metal and the semiconductor are brought into intimate contact, the Fermi levels of the two materials must be equal in thermal equilibrium. In addition, the vacuum level must be continuous. This can be only achieved by an electron flow from the semiconductor to the metal until thermal equilibrium is reached. The electrons always flow in the direction from a high to a low Fermi level. This process creates a depletion region of ionized donors in the n-type semiconductor surface. Consequently, a space charge region is formed. For this case the barrier height $q\phi_{Bn} = q(\phi_m - \chi)$ is the difference between the metal work function and the electron affinity of the semiconductor. When a voltage is applied between the metal and the semiconductor so that the space charge region increases, the current flow of electrons is suppressed. Due to the fact that a potential barrier for electrons is created there, this kind of contact is rectifying and therefore nonohmic. If a similar situation is considered for the case when the metal work function is smaller than the n-type semiconductor work function, an accumulation layer of electrons at the semiconductor surface is created without a potential barrier for electrons, which leads to an ohmic contact (Fig. 2).

In a similar procedure the ideal contact of a metal to a p-type semiconductor can be described. In this case rectifying contacts can be achieved for $\phi_m < \phi_s$ and ohmic contacts for $\phi_m > \phi_s$. For an ideal metal p-type semiconductor the barrier height $q\phi_{Bp}$ is given by $q\phi_{Bp} = E_g - q(\phi_m - \chi)$, where E_g is the bandgap of the semiconductor.

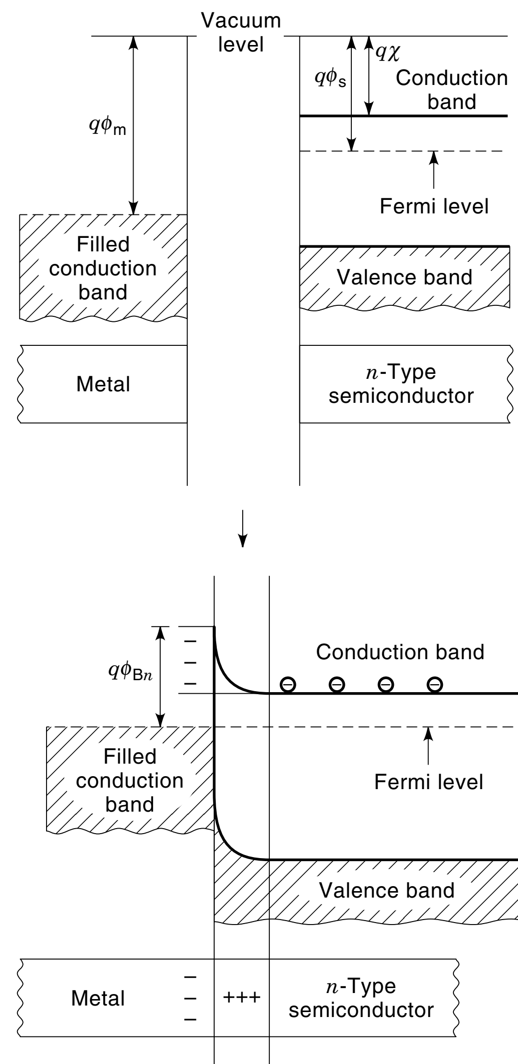

Figure 1. Energy band diagram before (upper part of the figure) and after (lower part of the figure) contact formation of a metal to n-type semiconductor depletion (rectifying) contact. The metal work function is larger than the n-type semiconductor work function.

Contact Barriers Due to Surface States

Contact resistances arise from contact barriers associated with space charges through differences in the work functions, or through the action of surface states, or both. When they arise from surface states, which is often the case, then barriers pre-exist at the semiconductor surface even before a contact is established. Surface state origination can have several causes. The most important ones are the termination and discontinuity of the semiconductor lattice at the surface. In practice the surface states are influenced by absorbed matter (e.g., oxygen or hydrogen). At least some of these additional states can act as carrier traps. If we consider an n-type semiconductor, then some electrons from the bulk of the semiconductor get trapped by the surface states, giving the two-dimensional surface a negative charge before the metal-semiconductor contact is established. Consequently, the adjoining border re-

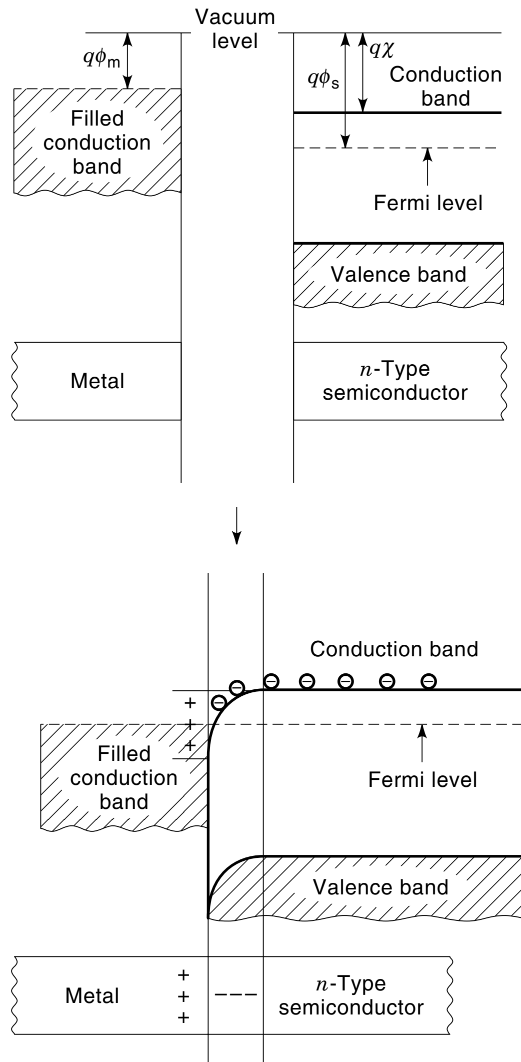

Figure 2. Energy band diagram before (upper part of the figure) and after (lower part of the figure) contact formation of an ohmic metal to n-type semiconductor contact. The metal work function is smaller than the n-type semiconductor work function.

gion to the semiconductor will become positively charged because charge neutrality of the whole system is required. Therefore, the charge density arises from ionized donor centers in an n-type semiconductor within a potential barrier that is no longer compensated by a corresponding electron density. Due to this potential barrier, the contact shows a rectifying behavior. The barrier thickness depends on the donor concentration as well as the barrier height, and this depends on the energy level and number of the surface states. A steady state is reached when the negative charge of the surface is equal to the positive charge in the barrier, both being determined by the same Fermi level. When these levels are densely bunched in a small energy interval, the Fermi level will be bound somewhere in the energy interval. The Fermi level is then "pinned," since its position cannot substantially vary. Empirical measurements of the Schottky barrier height have shown that there is a relationship between the bandgap of the semiconductor and the Schottky barrier height. Following this empirical rule, the Fermi level is pinned at roughly one third of the bandgap for p-type semiconductors and at two thirds for n-type semiconductors (5). In this case the Schottky barrier height is independent of the choice of the metal and the metal work function.

Pinning of the Fermi level is more common in covalent materials than in ionic materials. Silicon, the most prominent strongly covalent bonded material, is dominated by Fermi-level pinning. However, there are materials like SiC where a partial pinning of the Fermi level is observed. These kinds of materials represent an intermediate class of semiconductors depending both on the choice of the metal and surface states. A model that includes the effect of surface states was developed by Crowley and Sze (6). The barrier height for an n-type semiconductor was found to be a linear combination of the metal work function and a quantity $q\phi_0$ (measured from the edge of the valence band), which is defined as the energy below which the surface states must be filled for charge neutrality at the semiconductor surface. The obtained expression is $q\phi_{Bn} = \gamma(q\phi_m - q\chi) + (1 - \gamma)(E_g - q\phi_0)$, where γ is a weighting factor that depends mainly on the surface state density. For the extreme case $\gamma = 0$ the barrier height is $E_g - q\phi_0$ whereas for $\gamma = 1$ the Schottky barrier height $q\phi_{Bn}$ is identical to the ideal metal-semiconductor expression.

Specific Contact Resistivity

Most contacts to common semiconductors are depletion contacts due mainly to the action of surface states. They can, however, display ohmic behaviour with a linear current-voltage characteristic on degenerately doped semiconductors. In the case of a depletion contact the contact resistivity varies exponentially with the Schottky barrier height. Ohmic behavior of a depletion contact can be achieved either when the barrier height is small so that the charge carriers can easily overcome the barrier (thermionic emission) or when the charge carriers are able to surmount the depletion region by quantum mechanical tunneling. Quantum mechanical tunneling is of special importance because practically all ohmic contacts used in integrated circuit technology (mainly made of silicon) are based on this mechanism. The depletion layer width of a metal-semiconductor contact is proportional to the square root of the reciprocal doping concentration. Consequently, the depletion layer width decreases with increasing doping concentration and the tunneling probability increases. When tunneling mainly takes place between the top of the barrier and the Fermi level, the corresponding mechanism is called thermionic field emission. When tunneling mainly takes place around the Fermi level, the tunneling mechanism is called field emission. The two tunneling processes and thermionic emission are sketched in Fig. 3. The Schottky barrier height and shape is a function of the semiconductor doping concentration because charge carriers in the semiconductor are electrostatically attracted toward the metal surface by an induced mirror-image charge of opposite sign in the metal. This effect is called image force lowering. When the doping concentration is increased, the decrease of the depletion layer width ($W_{dep} \propto N^{-1/2}$) proceeds more rapidly than image force lowering ($\Delta\phi_B \propto N^{1/4}$) of the Schottky barrier height. Consequently, when the doping concentration is increased, conduction is dominated by tunneling through a narrowed barrier rather than by thermionic emission over a lowered barrier.

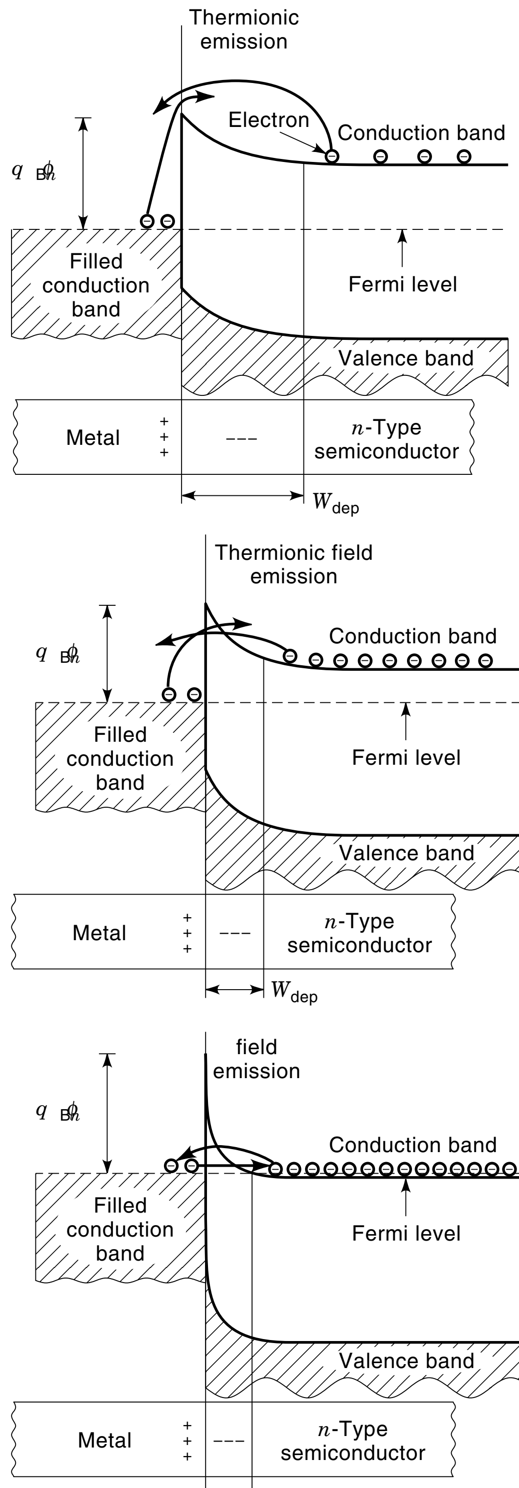

Figure 3. Carrier transport mechanism across the metal (n-type) semiconductor depletion layer junction: by thermionic emission over the top of the barrier (upper part of the figure), by thermionic field emission through the barrier between the top of the barrier and the Fermi level (middle part of the figure), and by field emission through the barrier around the Fermi level (lower part of the figure).

A useful parameter describing the tunneling probability is the characteristic energy E_{00}:

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N}{m\epsilon_0\epsilon_S}} \tag{1}$$

where h is Planck's constant, N the doping concentration, m the effective mass, and $\epsilon_0\epsilon_S$ the dielectric constant. The ratio of kT/E_{00} is a useful measure of the relative importance of the thermionic emission process to thermionic field emission or pure field emission. The constant k is the Boltzmann constant and T the absolute temperature. When E_{00} is high relative to the thermal energy kT, the probability of current transport by tunneling increases. Thus, thermionic emission dominates for $kT/E_{00} \gg 1$, thermionic field emission is dominant for $kT/E_{00} \approx 1$, and for $kT/E_{00} \ll 1$ carrier transport is dominated by field emission.

Depending on the three current transport mechanisms, three asymptotic analytical expressions for the contact resistivity can be obtained. More detailed information concerning the calculation of the specific contact resistivity can be found in Refs. 7–11. The specific contact resistivity ρ_C is defined as

$$\rho_C = \left(\frac{\partial j}{\partial V}\right)^{-1}_{V=0} \tag{2}$$

where V is the voltage and j the current density. This theoretical quantity is independent of the contact size and geometry and holds by definition also for nonohmic contacts. In the case of thermionic emission, the specific contact resistivity is given by

$$\rho_C \propto e^{(q\phi_B/kT)} \tag{3}$$

Obviously, this expression is independent of the doping concentration and valid when the barrier is too thick for tunneling. The specific contact resistivity decreases with increasing temperature and increases exponentially with the barrier height. This mechanism is most prominent at high temperatures and low doping concentrations and describes in its most simple form the contact resistivity of a Schottky contact. For thermionic field emission the specific contact resistivity is (asymptotically) given by

$$\rho_C \propto e\left(\frac{q\phi_B}{E_{00}\coth\left(\frac{E_{00}}{kT}\right)}\right) \tag{4}$$

In the case of field emission the specific contact resistivity is given by

$$\rho_C \propto e^{(q\phi_B/E_{00})} \tag{5}$$

According to these relationships, small contact resistivities can be expected when the doping concentration and the temperature are high and when the barrier height, the effective (tunneling) mass, and the dielectric constant are small. Consequently, the most common and most reproducible way to achieve low-resistivity ohmic contacts is by heavy doping of the semiconductor surface.

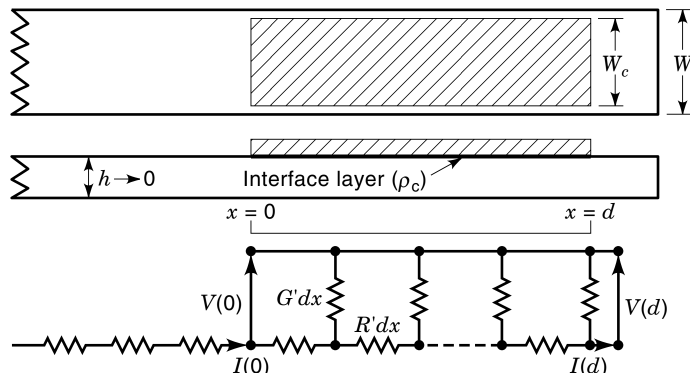

Figure 4. Schematic top view and cross section of an planar ohmic contact with the corresponding equivalent circuit.

The Transmission Line Model for Ohmic Contacts

Most of the ohmic contacts are planar contacts (e.g., for integrated circuits). Consequently, the current distribution at the metal-semiconductor interface is inhomogeneous due to the voltage drop in the semiconductor. This model relates the contact resistance and the geometry-independent specific contact resistivity. It has been established that an ohmic planar contact can be described by a transmission line network (12). Figure 4 shows the contact region of a planar ohmic contact and the corresponding equivalent circuit. This model is based on the assumption that the current lines are normal to the metal-semiconductor interface and that the metal and semiconductor thickness are negligible. Furthermore, it is assumed that the current-voltage characteristic is linear. Each element dx in the equivalent circuit is associated with a certain vertical conductance G' per unit length and a horizontal resistance R' per unit length. Thus,

$$\frac{dV(x)}{dx} = -R'I(x); \quad \frac{dI(x)}{dx} = -G'V(x) \tag{6}$$

with

$$R' = \frac{R_{SC}}{W_C}; \quad G' = \frac{W_C}{\rho_C} \tag{7}$$

where W_C is the contact width. The property R_{SC} is the sheet resistance (in units of ohm/square) directly under the contact and ρ_C is the specific contact resistivity. The sheet resistance under the contact R_{SC} is not necessarily equal to the semiconductor sheet resistance R_S outside the contact area due to contact alloying or sintering effects. By differentiation one gets

$$\frac{d^2V(x)}{dx^2} - \frac{V(x)}{L_T^2} = 0; \quad \frac{d^2I(x)}{dx^2} - \frac{I(x)}{L_T^2} = 0 \tag{8}$$

with

$$L_T = \frac{1}{\sqrt{R'G'}} = \sqrt{\frac{\rho_C}{R_{SC}}} \tag{9}$$

The property L_T has units of length and is called the transfer length. With the boundary conditions $V(0) = V_0$ and $I(0) = 0$, one gets for the voltage

$$V(x) = V_0 \cosh\left(\frac{x}{L_T}\right) - \frac{\sqrt{\rho_C R_{SC}}}{W_C} I_0 \sinh\left(\frac{x}{L_T}\right) \tag{10}$$

and for the current

$$I(x) = I_0 \cosh\left(\frac{x}{L_T}\right) - \frac{V_0 W_C}{\sqrt{\rho_C R_{SC}}} \sinh\left(\frac{x}{L_T}\right) \tag{11}$$

From the equivalent circuit the current is zero for $x > d$. The contact resistance R_C is the quotient of V_0/I_0. Therefore, one gets

$$R_C = \frac{V_0}{I_0} = \frac{R_{SC}L_T}{W_C} \coth\left(\frac{d}{L_T}\right) \tag{12}$$

In a similar way, the contact end resistance R_E can be defined as the voltage drop at the contact end divided by the current $I(0)$. Therefore, one gets

$$R_E = \frac{R_{SC}L_T}{W_C \sinh\left(\frac{d}{L_T}\right)} \tag{13}$$

The specific contact resistivity can be calculated when R_C or R_E are known.

Measurement of the Contact and Contact End Resistance

In the recent literature (e.g., Refs. 1 and 13), a number of test structures have been proposed. The most popular one is sketched in Fig. 5. The three contacts are assumed to have identical contact resistivities and dimensions. They are separated at a distance $l_1 \neq l_2$ from each other. Thus, the resistances R_1 and R_2 are given by

$$R_1 = R_S\frac{l_1}{W} + 2R_C; \quad R_2 = R_S\frac{l_2}{W} + 2R_C \tag{14}$$

Solving these equations for R_C gives

$$R_C = \frac{l_1R_2 - l_2R_1}{2(l_1 - l_2)} \tag{15}$$

A clear disadvantage of this measurement procedure is that the contact resistance is normally small compared with the resistance between the contacts. Therefore, R_C is determined as a small difference of large quantities and is therefore sensitive to experimental errors. One can obtain statistically better results when more than three contacts with different contact separations are used. When the total resistance of the resistor pairs are plotted against the separation distance l, the linear extrapolation of the total resistance to $l = 0$ leads to the contact resistance $2R_C$. The specific contact resistivity can be evaluated from the transmission line model. Another way to determine the specific contact resistivity is the measurement of the contact end resistance. The contact end resistance can be simply measured by forcing a current I between two neighboring pairs of contacts (e.g., between contact 1 and contact

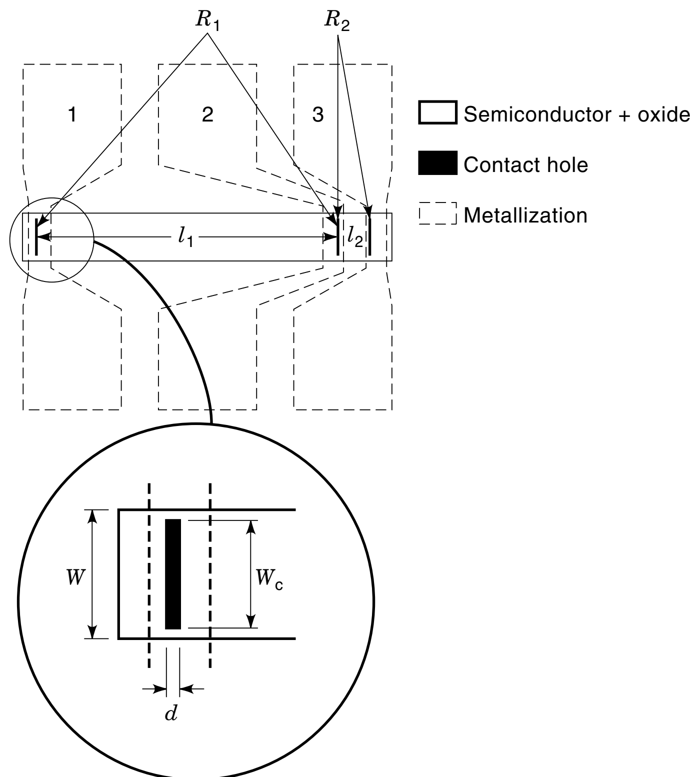

Figure 5. Test structure for the measurement of the contact resistance.

2) and measuring the voltage drop V on a third (e.g., between contact 2 and contact 3) contact, as shown in Fig. 5. The contact end resistance is then simply given by V/I. According to the transmission line model, the contact end resistance measurement is sensitive to the contact length d. The same test procedures can be applied to cylindrical contacts, which allow a simplified fabrication technique (because no insulation of the resistor path is needed) and which eliminate edge effects that exist in the aforementioned structures. For this case the transmission line model has to be modified (1).

PRACTICAL OHMIC CONTACTS TO SEMICONDUCTORS

The most important material for semiconductor devices is clearly silicon. However, other materials, like GaAs, SiC, and diamond, are interesting semiconductors for special applications. Each material has its own drawback due to differences in their physical properties and different affinities for chemical reaction with the metallization. In any case, the characterization and control of the semiconductor surfaces and interfaces plays a key role in developing devices. Typical fabrication technologies and experimentally determined specific contact resistivities are summarized in Table 1.

Metallurgical Aspects

Up until this point in this article the choice of the metallization was dependent only on its work function. However, elemental metallizations have different physical properties; the most important being the resistivity (14), the work function (3), and the thermal expansion coefficient, which are listed in Table 2 for various metals. In practice, metallizations can interact with semiconductor surfaces accompanied with a mass transport across the interface (thermomigration) or they can react with the semiconductor surface to form compounds. The latter effect is sometimes used to lower the specific contact resistivity. Both effects take place at elevated temperatures employed at contact sintering or in high-temperature applications of devices. In the worst case they can lead to a short when shallow p–n junctions for ULSI applications are considered.

Another failure mode is electromigration, which is the metal transport at high current densities. This is most prominent in power devices or highly integrated circuits when scaled down to submicron dimensions. The most simple and cost-effective way to avoid electromigration seems to be to replace the commonly used aluminium metallization with copper. This offers two advantages: (1) The resistivity of copper (1.7 $\mu\Omega$ cm) is lower than the resistivity of aluminum (2.7 $\mu\Omega$ cm), and (2) the electromigration resistance of copper is several orders of magnitude higher than that of aluminum (15). Historically, copper has not been considered for applications

Table 1. Specific Contact Metallurgies and Processes for Various Semiconductors

Semiconductor	Doping/Carrier Concentration (cm^{-3})	Contact Material	Surface Preparation/ Annealing Conditions	Process	Specific Contact Resistivity (Ω cm^2)	Ref.
n-Type Si	1.4×10^{20}	Pt	Good; annealed at 450°C/NR	e-Beam evaporation	6.0×10^{-6}	7
n-Type Si	2.0×10^{20}	Al	Good; annealed at 450°C/NR	e-Beam evaporation	9.0×10^{-7}	7
n-Type GaAs	1.1×10^{17}	Ni/Ge	NR; annealed at 550°C/5 min	NR[a]	3.0×10^{-5}	20
n-Type GaAs	2.0×10^{17}	Pd/Ge	NR; annealed at 550°C/20 min	NR	3.5×10^{-4}	20
n-Type GaN	1.7×10^{19}	Ti/Ag	Good; no anneal	e-Beam evaporation	6.5×10^{-5}	26
n-Type GaN	4.0×10^{17}	Ti/Al/Ni/Au	NR; annealed at 900°C/30 s	e-Beam evaporation	8.9×10^{-8}	29
α (6 H or mixed) n-Type SiC	4.5×10^{17}	Ni	NR; annealed at 1000°C/20 s	e-Beam evaporation	1.7×10^{-4}	30
α (6 H or mixed) p-type SiC	1.8×10^{18}	Al	Good; annealed at 700°C/10 min	e-Beam evaporation	1.7×10^{-3}	30
Polycrystalline p-type diamond	4.9×10^{21}	Al–Si (99 : 1)	O_2 plasma 30 s sputter cleaning; annealed at 450°C/30 min	Sputtering	2.3×10^{-7}	34
Polycrystalline p-type diamond	1.9×10^{21}	Al–Si (99 : 1)	O_2 plasma 30 s sputter cleaning; annealed at 450°C/30 min	Sputtering	1.0×10^{-5}	34

[a] NR: not reported.

Table 2. Physical Properties of Selected Metals for Ohmic Contacts

Metal	Resistivity $\times 10^{-6}$ (Ω cm)	Work Function (eV)	Thermal Expansion Coefficient $\times 10^{-6}$ (1/K)
Ag	1.59	4.42	19
Cu	1.67	4.59	17
Au	2.35	5.20	14
Al	2.65	4.18	25
Mo	5.20	4.21	5
W	5.65	4.55	5
Zn	5.92		35
Ni	6.84	5.15	13
In	8.37	3.97	6
Pt	10.60	5.43	9
Pd	10.80	5.17	
Sn	11.0	4.43	20

in silicon-based devices because of its tendency to diffuse rapidly in silicon and degrade semiconductor device performance. When copper is used as a metallization, a diffusion barrier has to be added between the copper and the substrate to prevent diffusion. A similar need for diffusion barriers results from high-temperature electronic applications.

Most of the practically important metallizations are polycrystalline, which means that metal grains in the micrometer or nanometer range are separated from each other by grain boundaries that have a lower atomic density. When polycrystalline multilayer metallizations are deposited, interdiffusion or reaction between the metallizations or between the metallization and the substrate can result. The diffusion itself in polycrystalline metallizations is controlled by grain boundaries or other defects, which enhance the atomic mobility. An excellent overview concerning diffusion barriers was given by Nicolet (16). Useful diffusion barriers are binary (e.g., TiN) or ternary (e.g., Ti–Si–N) compound metallizations. The idea is thus to change the grain size, microstructure, and composition to avoid diffusion. In the extreme case diffusion barriers can be amorphous. In amorphous metals, there are no grain boundaries or dislocations and the diffusion is dominated by bulk diffusion, which can be orders of magnitude slower than grain boundary diffusion in polycrystalline films (17). Diffusion barriers can also be effective when they consist of nanocrystallites in an amorphous matrix, as long as the volume fraction of nanocrystallites is small and an interconnecting network of grain boundaries is prevented.

Another problem is encountered by mechanical stress. Mechanical stress can determine the lifetime of a contact or an interconnect. This is especially important when a device is exposed to large temperature cycles. The mechanical stress consists of an intrinsic stress component that depends, among many other things, on the lattice constants of the two materials involved and on a thermal stress component. The thermal stress depends on the difference of the thermal expansion coefficients and the Young's moduli. When the thermal expansion coefficients and the Young's moduli are similar, the thermal stress can be minimized.

Ohmic Contacts to Silicon

Ohmic metal contacts to silicon represent the most frequently used type of ohmic contacts. An excellent review concerning contacts to silicon as well as technological aspects is given in Ref. 1. The bandgap of silicon is 1.12 eV and the electron affinity is 4.05 eV (4). Silicon is strongly covalently bonded and the contact behavior is therefore relatively independent of the choice of metal. Even barrier height measurements of different metals on ultrahigh vacuum cleaved silicon surfaces vary only between 0.3 and 0.9 eV (18). However, there is a remarkable scatter in the data presented in the literature depending on the measurement method and the surface cleaning procedure. In practice, specific contact resistivities less than 10^{-7} Ω cm^2 can be achieved at high doping levels (19).

In most silicon-based devices aluminum and some of its alloys are currently the most popular contact systems. Aluminum is an acceptor dopant in silicon and therefore forms a good ohmic contact to heavily doped *p*-type silicon. In the case of heavily doped *n*-type silicon at the semiconductor surface, electrons can surmount the very thin contact barrier by tunneling in both directions. The high donor concentration in the *n*-type silicon substrate ensures that compensation due to aluminum acceptors would only be partial.

Even if all foreign contaminants are successfully removed, a thin native oxide layer with a typical thickness of ≤2.5 nm is always present on a freshly cleaned silicon surface. Aluminum has the ability to react with the thin oxide layer to form aluminum oxide, which is engulfed by aluminum atoms, ensuring a good ohmic contact. Furthermore, the reaction of aluminum with oxide layers outside the contact area ensures good adhesion of the aluminum metallization. Contact sintering is normally performed below 550°C in nitrogen or forming gas for less than half an hour. This results in the formation of an intimate aluminum-silicon contact. However, the heat treatment also results in the dissolution of silicon in aluminum, depending on the time and temperature of the heat treatment. Voids that are left behind can be easily filled with aluminum atoms, leading to thermomigration problems. However, the solubility of silicon in aluminum is relatively small (~1% at 500°C) and it is therefore reasonable to use aluminum-silicon alloys as a metallization with a small amount of silicon (typically 1%) to avoid thermomigration because the thermodynamic driver for further dissolution of silicon in aluminum is reduced.

Several metals can react with silicon by a solid-state reaction to form silicides with metallic properties. So far three metal silicides compounds have been identified: M_2Si, MSi, and MSi_2 (M represents the metal) (18). Normally the unreacted metal is deposited on the silicon substrate. The sample is then annealed to promote interfacial reaction. Thus, the barrier height is independent of the surface properties and only related to the metallurgical reactions. The advantage of silicides are that they can form highly ohmic contacts to single crystal and polycrystalline silicon with a barrier height that decreases almost linearly with the eutectic temperature (4). Furthermore, the thermal expansion coefficient of many silicides is similar to silicon, which minimizes the thermal stress component. Silicide films on silicon can be amorphous, polycrystalline, or can grow as epitaxial films.

Ohmic Contacts to III–V Compound Semiconductors

III–V compound semiconductor materials and the fabrication technology are currently able to produce integrated digital and analog, microwave, and optoelectronic devices. The most

widely used compound semiconductor material is GaAs. Ohmic contacts to III–Vs, especially GaAs, have been discussed in several reviews (20–23). Ohmic contacts to III–V compound semiconductors can be formed by alloying or heavily doping the semiconductor surface. The dependence of the Schottky barrier height and the specific contact resistivity of III–V compound semiconductors on the metal work function are quite complex and not fully understood. GaAs has a bandgap of 1.43 eV and an electron affinity of 4.07 eV (4). Semiconductors like GaAs, InSb, and InP are weakly dependent on the metal work function and are therefore relatively insensitive to the choice of the metal. For other III–Vs like AlN and GaN, the metal work function seems to play an important role for nonalloyed contacts.

Nonalloyed contacts offer the advantage that they preserve the interface morphology because there is no need for a high-temperature treatment after the interface is formed. The typical barrier heights for *n*-type GaAs are between 0.77 and 0.88 eV, independent of the metallization. In the case of *p*-type GaAs, typical Schottky barrier heights are between 0.42 and 0.63 eV. Even for nonalloyed contacts to GaAs, specific contact resistivities $<10^{-6}\ \Omega\ \mathrm{cm}^2$ (24) can be achieved. An alternative way of making ohmic contacts to GaAs is that one of the components of the metallization acts as a doping source to produce a degenerate surface layer. Possible materials would contain Si, Ge, Se, Sn, or Te for *n*-type and Zn, Cd, Be, or Mg for *p*-type semiconductors (21). These alloyed contacts lead to a spatially nonuniform interface. It has been shown experimentally that this leads to an N^{-x} dependence (with $x \approx 1$ for GaAs) of the specific contact resistivity on the doping concentration, which is in contrast to the tunneling theory (25). In general, alloyed ohmic contacts to GaAs and other III–Vs display a complicated interface microstructure that depends, among many other things, on the metallization, stress, defects, and surface damage that strongly affect the specific contact resistivity. The contact formation itself is not completely understood in most cases. Therefore, the contact properties are not easily reproducible.

Another promising III–V candidate is GaN, potentially a material for blue lasers and light-emitting diodes. Only limited information is currently available concerning ohmic contacts to GaN. GaN has a bandgap of 3.4 eV and an electron affinity of 4.1 eV (26). Most interesting is that the barrier height might not be pinned and therefore strongly depends on the work function of the metal (27,28). This is supported by the observation that the Fermi-level pinning is most prominent in III–V compound semiconductors with a low electronegativity difference between the compound elements, whereas materials like AlN with a large electronegativity difference display a strong ionic character (4). Following this approach, the electronegativity difference of AlN is 1.6, that of GaN 1.3, and that of GaAs 0.4. Therefore, it seems reasonable that the specific contact resistivity and ohmic contact formation will depend strongly on the choice of metallization. Contact resistivity measurements on *n*-type GaN revealed that contact resistivities smaller than $10^{-7}\ \Omega\ \mathrm{cm}^2$ can be achieved (29).

Ohmic Contacts to SiC

SiC is currently the most advanced of the wide bandgap semiconductors and in the best position for commercial applications in the near future for high-power, high-frequency, and high-temperature electronics. Polytypism is one of the most unique features of SiC. SiC exists in over 170 polytypes. The number of atoms per unit cell varies from polytype to polytype, which affects the physical properties of different polytypes. The three polytypes of greatest interest are 4 H–SiC, 6 H–SiC, and the cubic form 3 C–SiC.

As already mentioned, SiC presents a semiconductor class with partial Fermi-level pinning and depends therefore partly on the choice of the contact metal. The electron affinity of 3 C–SiC is 4.0 eV and for 6 H–SiC 3.3 eV (30). For ohmic contacts metals with a low work function for *n*-type SiC and metals with a high work function for ohmic contacts to *p*-type SiC should be chosen. Due to the impact of interface states and the defect density of the material itself, it is not easy to predict the barrier heights theoretically. Therefore, specific contact resistivities have to be determined experimentally.

In the case of 3 C–SiC, Schottky barrier heights between 0.16 and 1.4 eV for *n*-type materials have been reported (30). The smallest reported specific contact resistivity to *n*-type materials is less than $10^{-6}\ \Omega\ \mathrm{cm}^2$. Acceptor, *p*-type doping is a recognized problem in SiC that is reflected by higher contact resistivities. For *p*-type materials the lowest reported contact resistivities are in the mid $10^{-2}\ \Omega\ \mathrm{cm}^2$. There is the expected tendency that the contact resistivity drops with increasing doping concentration. Due to the smaller bandgap of 3 C–SiC (2.3 eV), it seems to be easier to achieve low-resistivity ohmic contacts to 3 C–SiC compared with 6 H–SiC, which has a bandgap of 3.0 eV.

For *n*-type 6 H–SiC barrier heights between 0.33 and ~2 eV and for *p*-type 6 H–SiC barrier heights between 1.07 and 1.45 eV have been reported. The barrier heights and the specific contact resistivities are sensitive to the crystal face to which the contact is made. As expected from the tunneling theory, the contact resistivity drops with increasing doping concentration. Currently, contact resistivities of $\leq 10^{-6}\ \Omega\ \mathrm{cm}^2$ can be achieved for the highest doping levels, greater than $4 \times 10^{20}\ \mathrm{cm}^{-3}$ for *n*-type 6 H–SiC. The lowest reported specific contact resistivities to *p*-type 6 H–SiC are in the mid $10^{-5}\ \Omega\ \mathrm{cm}^2$, most likely due to the lower doping concentration in *p*-type materials compared with *n*-type 6 H–SiC.

Another approach to lower the contact resistivity of 6 H–SiC is the use of 3 C–SiC as a contact material. The contact resistivity of nickel contacts to a 3 C–SiC/6 H–SiC heterostructure is at least a factor of 3 smaller compared with a nickel contact without the 3 C–SiC layer (31). The majority of carriers find it easier to surmount two smaller barriers than the equivalent of their sum.

When SiC is used as a basic material for high-temperature electronics, transition metals with high melting points, such as titanium, tungsten, and molybdenum, have to be considered. However, they can react with SiC and can either form silicides or carbides, which can also coexist depending on the temperature. The reaction temperature is usually greater than those for silicon. Not only the temperature but also the amount of time and the metal thickness are important determinants of the resulting phases in metal-SiC systems (30).

Ohmic Contacts to Diamond

Many properties of diamond—like the high breakdown voltage, the large bandgap of 5.48 eV, the deep-lying acceptor

level (0.37 eV above the valence band for lightly doped diamond), and the extreme resistivity range, which can be altered by acceptor, *p*-type doping—make it an interesting material for electromechanical sensors and electronic devices. Large-area diamond can be produced by chemical vapor deposition. However, this material is polycrystalline when not deposited on diamond itself or another material, like cubic boron nitride, with a lattice constant close to diamond. Similar to other semiconductors, the surface pretreatment determines the quality of an ohmic contact to diamond.

The large bandgap and the strongly covalently bonded character of diamond can lead to the assumption that the Schottky barrier height is independent of the work function of the metal and of the electron affinity [tentatively 2.3 eV for (100)-diamond surfaces (32)]. However, the surface treatment plays a significant role. The interaction of diamond with hydrogen has received much attention. Hydrogen can be present in the bulk and at the surface of the as-grown material. To stabilize the material, it is necessary to anneal the sample in argon or dry nitrogen at temperatures around 500°C. Normally a low-resistivity layer is present on as-grown doped and undoped diamond surfaces. This layer can be removed (33) by chemical cleaning with sulfochromic acid or oxygen-plasma treatment, which is necessary to obtain temperature stable interfaces. However, the origin of the surface layer is not clear at present. There are three possible explanations for this surface-conducting layer:

1. Existence of a graphitelike low-resistivity layer
2. Hydrogen passivation of deep levels near the surface
3. Upward band-bending to form an accumulation layer for holes

The band-bending model is most likely to provide an explanation of the surface conducting layer (32). According to these results, the surface of the as-grown hydrogen-terminated samples bends upward for holes to give a low surface resistivity, while the oxygenated surface has a depletion layer for holes. It is therefore reasonable that the aforementioned chemical cleaning procedures lead to oxygenated diamond surfaces and that the Fermi level is pinned at a specific energy. Following the Mead and Spitzer rule (5), the Schottky barrier height of a covalent *p*-type semiconductor should be one third of the bandgap. Therefore, barrier heights in the range of 1.8 eV for diamond can be expected. Reported barrier heights range from 1.1 to 2.2 eV (34). The most conventional way to obtain low contact resistivities is heavy doping of the contact area either by ion implantation or in situ doping during growth. Doping concentrations higher than 10^{21} cm^{-3} have been reported for boron-doped diamond. In qualitative agreement with the theory, the contact resistivity drops with increased doping concentration (34). On the one hand, large barrier heights lead to high contact resistivities. On the other hand, contact resistivities as low as $\sim 10^{-7}$ Ω cm^2 have been reported for Al/Si contacts (35) after annealing at 450°C. The low contact resistivity has been traced back to the formation of SiC at the metal–diamond interface. Similar results were reported for carbide-forming metals like Ti (36) and Mo (37). Tachibana, Williams, and Glass (36) suggested two models that may explain the drop in the contact resistance or the change in the current-voltage characteristic from rectifying to ohmic. The models are based on the assumption that the carbide acts as a defect layer that lowers the metal–diamond barrier height, enhances tunneling, or both. Another model proposed an average decreasing amount of local disorder due to annealing (35). If there is a sufficiently large density of gap states near the Fermi level, then some type of carrier transport can take place with the help of these gap states. However, none of these models have been fully proven. With the metallization of a carbide-forming metal, after carbide formation is removed, small islands of carbide precipitates can be identified at the diamond surface. If these carbide islands conduct better than the surroundings, where no reaction has occurred, then the current density at the metal-diamond interface must be inhomogeneous. Consequently, two different types of carrier transport mechanisms operating in parallel in isolated area segments are distributed uniformly across the interface. Similar to GaAs, the doping dependence can be fitted by a power law dependence (38). Consequently, the second current contribution due to the carbide-island formation in diamond cannot be neglected. Another important point is the use of diffusion barriers to avoid interdiffusion of the contact layer and the bondable top metallization (e.g., Au) at high temperatures. The most frequently used Ti–Au contacts display a strong interdiffusion at temperatures below 450°C (35). TiWN–Au contacts are stable up to temperatures of approximately 450°C. Nitrogen is believed to saturate grain boundaries in the metallization, therefore avoiding the interdiffusion along the grain boundaries. At 600°C TiWN–Au contacts show a similar degradation to Ti–Au contacts.

SUMMARY

Ohmic or rectifying contact behavior depends on the properties of the semiconductor surface to which the contact is made. The choice of metallization plays an important role for more ionic bonded semiconductors such as GaN. Strongly covalently bonded semiconductors, such as Si, GaAs, and diamond, depend only weakly on the choice of the metallization and its work function. This is mainly due to the action of surface states even after a suitable cleaning procedure. These surface states result in a space charge region at the metal–semiconductor interface. In these materials an ohmic contact with a low contact resistivity can be obtained due to heavy doping of the semiconductor surface. When the doping level concentration increases, the depletion layer width decreases and charge carriers can surmount the depletion region by quantum-mechanical tunneling, which leads to a low contact resistivity. Annealing of the contact scheme at elevated temperatures can have significant impact on the contact resistivity due to surface doping effects, solid-state reactions, or structural changes. In many cases the contact resistivity can be significantly reduced after a suitable annealing procedure. The contact resistivity of planar ohmic contacts can be extracted with aid of the transmission line model from suitable test structures. The transmission line model is applicable for all planar ohmic contacts to semiconductors.

Reliable ohmic contacts are highly dependent on the metallization or the metallization scheme. Contact failure due to interdiffusion or solid-state reaction can be avoided when diffusion barriers are used. In order to avoid or reduce diffusion processes it is necessary to change the grain size, microstruc-

ture, and composition of polycrystalline metallizations. The diffusion coefficient in grain boundaries can be orders of magnitude higher than in bulk materials. Consequently, good results can be achieved with amorphous diffusion barriers where no grain boundaries are present.

To summarize, the basic features of ohmic contacts to various semiconductors are well understood. However, contacts for any new application (e.g., for ultralarge-scale integrated circuits or contacts to wide bandgap semiconductors) always pose a new challenge.

ACKNOWLEDGMENTS

The author would like to thank Dr. David Dreifus (Kobe Steel, USA), Dr. Colin Johnston (AEA Technology plc, UK), and Gerald Rutsch (University of Pittsburgh) for critically reviewing the manuscript.

BIBLIOGRAPHY

1. S. S. Cohen and G. Sh. Gildenblat, *VLSI Electronics Microstructure Science Vol. 13: Metal-Semiconductor Contacts and Devices,* New York: Academic Press, 1986.
2. H. K. Henisch, *Semiconductor Contacts: An Approach to Ideas and Models,* New York: Oxford University Press, 1984.
3. E. H. Rhoderick, *Metal-Semiconductor Contacts,* Oxford: Oxford University Press, 1978.
4. M. S. Tyagi, *Introduction to Semiconductor Materials and Devices,* New York: Wiley, 1991.
5. C. A. Mead and W. G. Spitzer, Fermi level position at metal-semiconductor interfaces, *Physical Rev.,* **134** (3A): A713–A716, 1964.
6. A. M. Crowley and S. M. Sze, Surface states and barrier height of metal-semiconductor systems, *J. Appl. Physics,* **36** (10): 3212–3220, 1965.
7. A. Y. C. Yu, Electron tunneling and contact resistance of metal-silicon contact barriers, *Solid State Electronics,* **13**: 239–247, 1970.
8. C. Y. Chang and S. M. Sze, Carrier transport across metal-semiconductor barriers, *Solid State Electronics,* **13**: 727–740, 1970.
9. S. J. Fonash, Current transport in metal semiconductor contacts—a unified approach, *Solid State Electronics,* **15**: 783–787, 1972.
10. G. Brezeanu et al., A computer method for the characterization of surface-layer ohmic contacts, *Solid State Electronics,* **30** (5): 527–532, 1987.
11. K. Shenai and R. W. Dutton, Current transport mechanisms in atomically abrupt metal-semiconductor interfaces, *IEEE Trans. Electron Devices,* **35**: 468–482, 1988.
12. H. H. Berger, Models for contacts to planar devices, *Solid State Electronics,* **15**: 145–158, 1972.
13. D. K. Schroder, *Semiconductor Material and Device Characterization,* New York: Wiley, 1990.
14. R. K. Hoffmann et al., A comparative look at contact systems used in thin film technology, *Hybrid Circuit Technology,* 13–18, October 1985.
15. S. P. Murarka and S. W. Hymes, Copper metallization for ULSI and beyond, *Crit. Rev. Solid State Materials Sci.,* **20** (2): 87–124, 1995.
16. M.-A. Nicolet, Diffusion barriers in thin films, *Thin Solid Films,* **52**: 415–443, 1978.
17. J. D. Wiley et al., Amorphous metallizations for high-temperature semiconductor device applications, *IEEE Trans. Ind. Electron.,* **IE-29**: 154–157, 1982.
18. H. Lüth, *Surfaces and Interfaces of Solids,* Berlin: Springer-Verlag, 1993.
19. D. K. Schroder and D. L. Meier, Solar cell contact resistance—a review, *IEEE Trans. Electron Devices,* **ED-31**: 637–647, 1984.
20. A. Piotrowska, A. G'uivarc'h, and G. Pelous, Ohmic contacts to III–V compound semiconductors: a review of fabrication techniques, *Solid State Electronics,* **26** (3): 179–197, 1983.
21. B. L. Sharma, Ohmic contacts to III–V compound semiconductors. In R. K. Willardson and A. C. Beer (eds.), *Semiconductors and Semimetals,* Vol. 15, New York: Academic Press, 1981.
22. V. L. Rideout, A review of the theory and technology for ohmic contacts to group III–V compound semiconductors, *Solid State Electronics,* **18**: 541–550, 1975.
23. M. N. Yoder, Ohmic contacts in GaAs, *Solid State Electronics,* **23**: 117–119, 1980.
24. K. Shenai, Very low resistance nonalloyed ohmic contacts to Sn-doped molecular-beam epitaxial GaAs, *IEEE Trans. Electron Devices,* **ED-34**: 1642–1649, 1987.
25. N. Braslau, Alloyed ohmic contacts to GaAs, *J. Vaccum Sci. Technology,* **19** (3): 803–807, 1981.
26. J. D. Guo et al., A bilayer Ti/Ag ohmic contact for highly doped n-type GaN films, *Appl. Physics Lett.,* **68** (2): 235–237, 1996.
27. H. Ishikawa et al., Effects of surface treatments and metal work functions on electrical properties at p-GaN/metal interfaces, *J. Appl. Physics,* **81** (3): 1315–1322, 1997.
28. J. S. Foresi and T. D. Moustakas, Metal contacts to gallium nitride, *Appl. Physics Lett.,* **62** (22): 2859–2861, 1996.
29. Z. Fan et al., Very low resistance multilayer ohmic contact to n-GaN, *Appl. Physics Lett.,* **68** (12): 1672–1674, 1996.
30. L. M. Porter and R. F. Davis, A critical review of ohmic and rectifying contacts for silicon carbide, *Materials Sci. Eng.,* **B34**: 83–105, 1995.
31. F. P. Cluskey, R. Grzybowski, and T. Podlesak, *High Temperature Electronics,* Boca Raton, FL: CRC Press, 1997.
32. J. Shirafuji and T. Sugino, Electrical properties of diamond surfaces, *Diamond and Related Materials,* **5**: 706–713, 1996.
33. Y. Mori, H. Kawarada, and A. Hiraki, Properties of metal diamond interfaces and effects of oxygen adsorbed onto diamond surface, *Appl. Phys. Lett.,* **58** (9): 940–941, 1991.
34. M. Werner et al., Electrical characterization of Al/Si ohmic contacts to heavily boron doped polycrystalline diamond films, *J. Appl. Phys.,* **79** (5): 2535–2541, 1996.
35. M. Werner et al., The effect of metallization on the ohmic contact resistivity to heavily B-doped polycrystalline diamond films, *IEEE Trans. Electron Devices,* **42**: 1344–1351, 1995.
36. T. Tachibana, B. E. Williams, and J. T. Glass, Correlation of the electrical properties of metal contacts with the chemical nature of the metal diamond interface. II. Titanium contacts: A carbide forming metal, *Physical Rev.,* **B45** (20): 975–981, 1992.
37. K. L. Moazed, J. R. Zeidler, and M. J. Taylor, A thermally activated solid state reaction process for fabricating ohmic contacts to semiconducting diamond, *J. Appl. Phys.,* **68** (5), 1990.
38. M. Werner, CVD diamond sensors for temperature and pressure. In B. Dischler and C. Wild (eds.), *Low Pressure Synthetic Diamond: Manufacturing and Applications,* Berlin: Springer-Verlag, in press.

MATTHIAS WERNER
VDI/VDE-Technologiezentrum
Informationstechnik GmbH

OHMIC HEATING. See Resistance heating.