BIPOLAR PERMEABLE TRANSISTOR

A permeable base transistor (PBT) is a special transistor type, which operates like a vacuum tube (triode) inside semiconductor material. The transistor has three electrodes: source, gate, and drain, as shown in Fig. 1(a). Between the upper and lower electrode—source and drain—a semiconducting material is sandwiched, in which a metal or metal-like grid is embedded.

By applying a voltage between source and drain, electrons move from the source to the drain electrode. In addition, a smaller voltage between gate- and source-electrode generates an electric field, which controls the electron flux from the source to the drain, like the grid in a vacuum tube. Using ac voltage at the gate input, a significant voltage and current amplification arises at the drain, that is, the small gate voltage controls the large electron current flux from the source to the drain. Due to the small distances between source and drain of less than 1 μm and the resulting high accelerating electric field, the electrons move very fast from the source to the drain contact, meaning they have a small transit time corresponding to a high transit frequency up to 100 GHz. Hence, PBTs are mainly suggested for radio frequency amplifiers.

The following paragraphs describe the architecture of a PBT, taking into account different semiconductor and metal materials, the history of the device, special physical effects, plus a couple of device simulations for optimizing the PBT geometry for high-frequency applications.

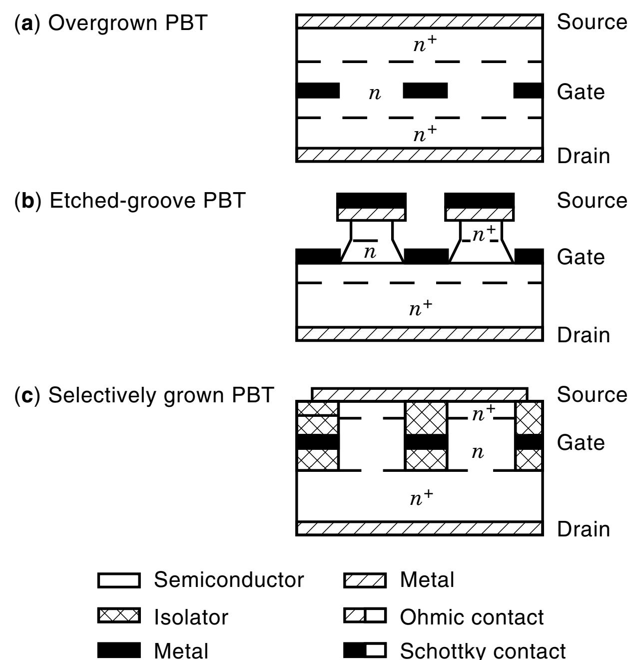

Figure 1. Schematic cross-section of three important PBT geometries with n-type semiconducting material. The thickness of the metal or silicide layer, respectively, is the gate length l_g and the distance between the two dashed lines, which limits the low doped regions, is called channel length h. (a) The overgrown PBT, where the gate is completely buried inside the semiconductor; (b) the etched-groove PBT, where the gate lay in etched grooves on the surface of the semiconductor; (c) the selectively grown PBT, where the channel and the source contact is selectively grown, for example, by chemical vapor deposition of Si, into an etched SiO_2/metal/SiO_2 sandwich.

PBTs are, in principle, vertical MESFETs (metal semiconductor field effect transistor) with extremely short gate lengths. The device structure of PBTs is characterized by a vertical $n^+\ n\ n^+$ or $p^+\ p\ p^+$ layer sequence, respectively, where in the lower doped n-layer (p-layer) a grid-like Schottky gate is embedded or attached (see Fig. 1). The electric field around the gate fingers controls the vertical majority current flux from the source to the drain. The obvious advantage of a PBT over a MESFET is the reduction of transit time due to the shorter gate length and the shorter channel length; the latter means the thickness of the low doped layer. Drift-diffusion and Monte Carlo simulations have predicted for n-type Si- and GaAs-based PBTs an available unity-current-gain f_T frequency as high as 50–130 GHz (1–6). For that reason, PBTs have been proposed for both high-speed logic circuits (7,8) and high-frequency high-power amplifiers or oscillators (9,10). In addition, PBTs were proposed for high-frequency high-voltage operation—for example, as class C amplifiers (9,10). A high unity-current-gain frequency f_T in PBTs is mainly correlated to a short drain–source distance h and a high free electron density inside the channels. These parameters are strongly correlated with the channel and gate finger widths, because only transistors with threshold voltages in the range of zero exhibit high unity-current-gain frequencies. Asymmetric gate positions in long channel PBTs ($h > 600$ nm)—that is, for smaller gate–source distances than gate–drain distances—improve the high-frequency performance and the breakdown behavior (10–13). Only for h values below 200 nm, f_T values above 50 GHz may be expected. A further reduction of the channel length much below 200 nm and an increase of the channel doping concentration above 3×10^{17} cm^{-3} are physically limited by tunneling breakdown at the gate finger edges (14,15).

For a large maximum oscillation frequency f_{max}, parasitic impedances are important—that is, the ratio of the finger width to the finger length b_f/z, low parasitic gate areas, and low series and source resistances. The essential intrinsic parameter for obtaining high f_{max} values is the ratio of the transconductance and the drain conductance $g = g_m/G_{DS}$, as shown in Tables 1 and 2 (1). Only for ratios above 10, f_{max} values in Si and GaAs PBTs were obtained (3,14,16,17). Better g_m/G_{DS} ratios are the only advantage of GaAs over Si PBTs, because in a typical operation point both devices perform in the electron saturation velocity regime, which is approximately equal in both materials. However, due to the Γ–L scattering in GaAs and the resulting negative differential slope in velocity–field curve the dc output characteristics of GaAs PBTs show a better saturation behavior and consequently a smaller drain conductance than do Si PBTs. [Table 1 (18–39); Table 2 (40–50)].

DEVICE ARCHITECTURE AND HISTORY

From the technological point of view, three types of PBTs exist as shown in Fig. 1: (a) the overgrown PBT, where the gate is completely buried inside the semiconductor, (b) the so-called etched-groove type, where the gate fingers lay in etched grooves besides the ridge-like source contacts, and (c) the selectively grown PBT with oxide above and below the metal grid (43). The latter type suppressed considerably the parasitic capacitances above and below the metal grid and is often

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Table 1. Historical Development of Si PBTs

Literature									
Year	Authors (ref. no.)	Gate	l_g (nm)	b_c (nm)	h (μm)	N_D (cm^{-3})	g_m (S/m)	G_{DS} (S/m)	f_T/f_{max} (GHz)
				Etched-Groove Si PBT					
1982	Rathman et al. (18)	W	50	160	—	4×10^{16}	37.5	10	8/10
1982	Chi et al. (19)	—	—	200	1.0	2×10^{15}	36	—	—/—
1984	Rathman et al. (3)	W	60	160	—	4×10^{16}	50	—	9.4/—
1984	Rathman et al. (20)	W	60	160	1.0	4×10^{16}	50	5	10/20
1987	Gruhle et al. (21)	Pt	100	500	1.2	1.5×10^{17}	62	—	—/—
1987	Gruhle et al. (21)	Pt	100	700	2.0	4×10^{16}	45	7	—/—
1988	Miyao, Ohshima et al. (22,23)	$NiSi_2$	13	1000	2.0	1×10^{16}	32	5.2	—/—
1988	Rathman and Niblack (16)	PtSi	60	160	1.0[a]	1×10^{16}	110	5.9	22/26
1990	Gruhle and Beneking (4)	PtAu	70	90	0.1	1×10^{17}	155	60	12/13
1990	Rathman (10)	PtSi	—	160	1.2[b]	6×10^{16}	80	2	22/—
1990	Letourneau et al. (24)	PtSi	20	700	—	—	16	2	—/—
1990	Gruhle et al. (25)	CrPt	—	300	2	3×10^{15}	30	7.8	—/—
1991	Gruhle et al. (26)	PtAu	70	300	0.5	$\approx 10^{17}$	125	11	26/26
				Overgrown Si PBT					
1984	Ishibashi and Furukawa (27)	$CoSi_2$	100	—	—	10^{15}	≈1	2.8	—/—
1986	Ishibashi and Furukawa (28)	$CoSi_2$	100	3000	—	—	2	2.5	—/—
1986	Rosencher et al. (29,30)	$CoSi_2$	90	1000	0.8	3×10^{16}	0.3	0.5	—/—
1988	Glastre et al. (31)	$CoSi_2$	60	300	—	$\approx 10^{15}$	1	0.1	—/—
1989	Ohshima et al. (32,33)	$CoSi_2$	10	500	1.8	2×10^{16}	50	11	—/—
1990	Badoz et al. (34,35)	WSi_2	150	500	—	$\approx 10^{15}$	5	1.3	—/—
1990	Schüppen et al. (36)	$CoSi_2$	60	1500	Sub[c]	8×10^{16}	11	4.7	—/—
1991	Gruhle et al. (14)	$CoSi_2$	5	500	0.7	—	35	17	—/—
1991	Nakagawa et al. (5,37)	$CoSi_2$	10	500	1.8	2×10^{16}	50	11	6/—
1992	Schüppen et al. (38)	$CoSi_2$	40	1000	1.1	2×10^{16}	50	7.8	1.5/0.8
1993	Schüppen et al. (1,39)	$CoSi_2$	40	400	1.0	4×10^{16}	70	8.5	6/1.5

[a]Asymmetric gate position $h_s/h_d \neq 1$.
[b]Here $h_s = 0.25\ \mu$m, G_{DS} calculated from output characteristics, N_D average doping concentrations for nonconstant doping profiles.
[c]Sub, substrate.

Table 2. Historical Development of GaAs PBTs

Literature									
Year	Authors Zitat (Ref. no.)	Gate	l_g (nm)	b_c (nm)	h (μm)	N_D (cm^{-3})[a]	g'_m (S/m)	G'_{DS} (S/m)[b]	f_T/f_{max} (GHz)
				Overgrown GaAs PBT					
1979	Bozler (40)	W	20	200	—	1×10^{16}	25	3.6	—/17
1980	Bozler and Alley (41)	W	30	160	2.3	5×10^{16}	90	13.5	37/10.4
1982	Bozler and Alley (7)	W	30	160	2.3	5×10^{16}	90	12.5	38/30
1982	Alley et al. (42)	W	50	160	—	—	120	—	28/100
1984	Asai et al. (43)	W	30	1250	2.5	2×10^{15}	11	8	—/—
1985	Bozler et al. (17,44)	W	30	160	0.7	1×10^{17}	150	2	35/150
1986	Takanashi et al. (45)	W	70	250	0.7	5×10^{16}	70	5.4	7.5/18
1987	Hollis et al. (46–48)	W	50	160	—	8×10^{16}	200	—	50/220
				Etched-Groove GaAs PBT					
1983	Kohn et al. (49)	Ti	—	500	0.5	7×10^{15}	47	13	—/—
1987	Clarke et al. (50)	—	700	300	3.0	2×10^{17}	92	3.3	13/67

[a]Here N_D values represent average doping concentrations.
[b]Here G'_{DS} values calculated from output characteristics.

called vertical MESFET (51). However, device shown in Fig. 1(c) includes the highest technological demand due to the selective epitaxial growth of the semiconductor in present of metal or silicide, respectively. Until now the best high-frequency performance of Si PBTs was achieved with the etched-groove type. Unity-current-gain frequencies f_T and a maximum oscillation frequency f_{max} of 26 GHz were measured (16,26), whereas in GaAs the overgrown type reached record f_T and f_{max} values of 50 GHz and 220 GHz, respectively (47). In contrast to GaAs, where good PBT performances were achieved by epitaxial overgrowth of a tungsten grid (41), the heteroepitaxy of Si with metals or silicides, respectively, was a severe drawback for overgrown Si PBTs. Significant PBT data were not obtained by $CoSi_2$/Si(111) heteroepitaxy until the end of the 1980s (Table 1) (33). Until now, the highest published unity-current-gain frequency f_T for overgrown Si(100) PBTs with a buried $CoSi_2$ gate is 6 GHz, fabricated by high-dose ion implantation of Co into Si and subsequent rapid thermal annealing (36,38,52–54). The same results were achieved by MBE grown Si/$CoSi_2$/Si layers (5).

The idea of the PBT arose from the static induction transistor (SIT), where a p^+ gate was embedded in n-type material (55), and the metal-gate transistor was proposed by J. Lindmayer in 1964 (56). However, the PBT in the present form was first realized using a tungsten grid in GaAs by C. O. Bozler in 1979 (40) Tables 1 and 2 sum up the historical development of Si and GaAs PBTs, respectively, by showing the main experimentally obtained device parameters—that is, the geometry, the transconductance, the drain conductance, and the measured high-frequency performance.

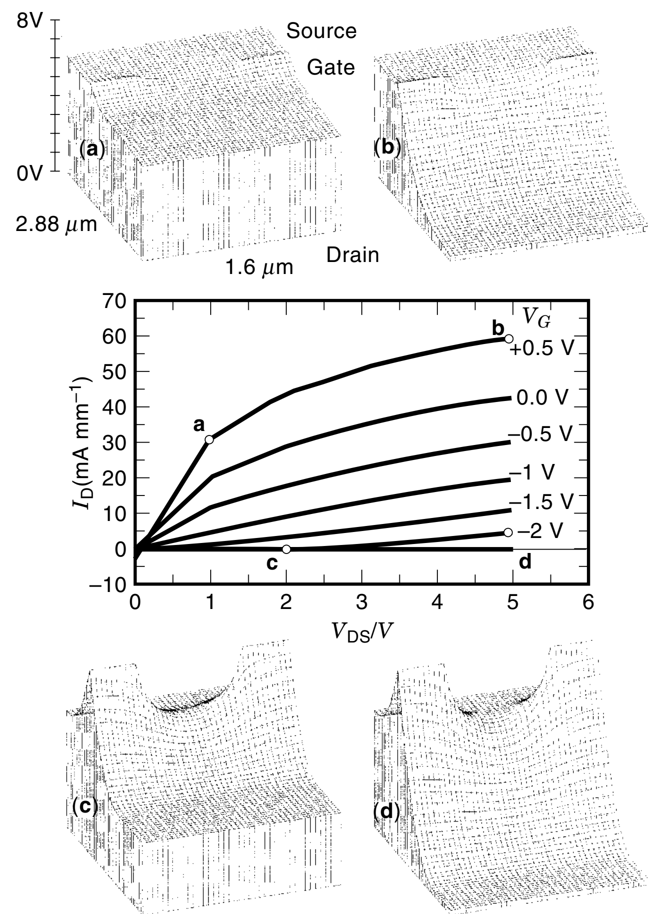

Figure 2. Output characteristics and corresponding potential distribution at the gate fingers of a typical PBT (15). (a) Low-current regime, (b) saturation region, (c) pinch-off, (d) punch-through.

SPECIAL PHYSICAL EFFECTS IN PBTs

In the following paragraph, special physical effects of PBTs were investigated by overgrown n-type silicon-based PBTs. PBTs are unipolar devices and they operate like vertical short-channel MESFETs with the following advantages:

- The extremely short gate length (<100 nm) is defined by the thickness of the metal or silicide layer and not by lithography as in MESFETs.
- Very short channel lengths (<500 nm) are easily obtainable not by lithography, but by the thickness of an epitaxial layer.
- Low gate resistances with long gate widths (>300 μm) are attainable by ridge-like gates without need for airbridges and T gates.
- The vertical structure easily permits three-dimensional integration.

The basic disadvantages of PBTs are the so-called short-channel effects, which lead to unwanted high drain conductances. In addition, the parasitic space-charge regions above and below the gate fingers increase the gate capacitances, so that small finger widths are necessary for reaching good high-frequency performances. Instead of the physical gate length l_g as in MESFETs with long gates ($l_g \geq 2$ μm), an effective gate length l_{eff} controls the main current flux from source to drain in PBTs (10). Since the geometric gate length l_g is much smaller than the depletion layers in the main current flux direction (see Fig. 2), the parasitic space-charge regions at the gate edges cannot be neglected; on the contrary, they themselves determine the effective gate length l_{eff}, which is a function of the channel doping and the applied voltages: $l_{eff} = f(N_D, l_g, V_{DS}, V_G)$.

As expected, the PBT works like a MESFET for medium currents and low drain–source voltages V_{DS} (Fig. 2a). However, also in the saturation regime (Fig. 2b) the drain current is a function of both the gate and the drain-source voltage. For negative gate voltages or zero gate voltages and smaller gate spacings, respectively, the channel is pinched off (Fig. 2c). In this regime a depletion layer and a potential barrier exists between source and drain. By increasing the drain–source voltage V_{DS}, the electron concentration at the source side of the space-charge regions grows up and electrons are injected into the depletion layer, which is very thin between the gate fingers. If the pass time of the carriers through the space-charge region is smaller than the relaxation time, electrons can cross the depletion layer without charge compensation by recombination or by relaxation, respectively. Then the drain current is space-charge-limited and triode-like characteristics are observed, as can typically be seen in the lower part of the PBT output characteristics (Fig. 2d), predominant for low channel doping concentrations (52).

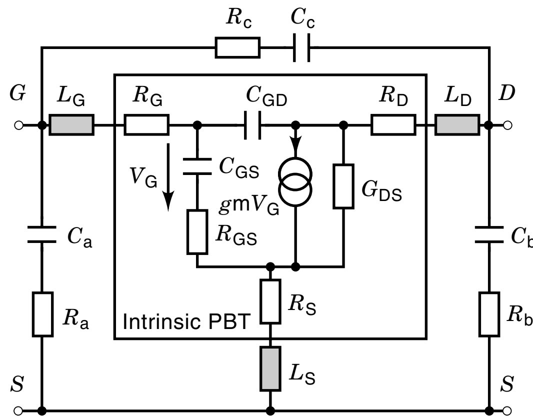

Figure 3. Small-signal equivalent circuit of a PBT in source configuration, including both the intrinsic transistor, which is similar to a standard MESFET equivalent circuit, and the external parasitic impedances.

In contrast to MESFETs, in PBTs tunneling is the predominant breakdown mechanism for reasonable channel doping concentrations, due to the high curvature of the electric field lines at the gate finger edges (14). Only for very short channels the space-charge regions around the gate fingers are limited by the high doped source and drain layers, and avalanche breakdown becomes possible. Another typical phenomenon in PBT operation is the spillover effect, which means the local enhancement of electron concentration in the low doped channel for short n^+nn^+ structures (57). In this case the diffusion tails from each nn^+ transition are superimposed. For typical channel lengths h between 200 nm and 1000 nm the spillover effect do not affect the PBT behavior for choosing appropriate doping in the range of 5×10^{15} cm^{-3} to 3×10^{17} cm^{-3}; thus shorter channel lengths require a higher doping concentration. On the other hand, the spillover effect leads to an enhanced electron concentration in short channels without decreasing the mobility. This may improve the channel conductivity and consequently the PBT performance.

In order to frame a matched small-signal high-frequency equivalent circuit (EC) of a PBT, the device is compared with a planar MESFET. The intrinsic lumped elements are shown in Fig. 3 (41). This EC differs from that of a MESFET only by the drain-source capacitance C_{DS}, which considers the parasitic substrate capacitance in the MESFET model, but does not exist in PBTs. Vojak and Alley (58) neglect for simplification in their EC also the gate–source resistance. However, for the extrinsic device the parasitic pad impedances have to be taken into account (Fig. 3). Besides the dc transconductance g_m and the drain conductance G_{DS} the main interesting transistor parameters are the unity-current-gain frequency f_T, and the maximum oscillation frequency f_{max}. After Ref. 41 f_T can be written as

$$f_T = \left.\frac{\Delta I_D/\Delta V_G}{2\pi\,\Delta Q_T/\Delta V_G}\right|_{V_{DS=const}} = \frac{g_m}{2\pi\,(C_{GS}+C_{GD})} \qquad (1)$$

Q_T is the total stored charge around the gate fingers. For the intrinsic EC in Fig. 2, f_{max} may be expressed as (59)

$$f_{max} \approx \frac{\sqrt{g_m}}{4\pi C_{GS}} \frac{1}{\sqrt{\dfrac{C_{GD}}{C_{GS}}R_G + \dfrac{G_{DS}}{g_m}\left(R_{GS} + \dfrac{R_G+R_S}{1+g_m R_S}\right)}} \qquad (2)$$

This equation will be used further on to estimate the maximum oscillation frequency f_{max}.

PBT DESIGN

For optimizing the PBT performance the following technological dimensions and parameters are adjustable (Fig. 4):

- Gatelength l_g
- Channel doping $N_D = f(y)$
- Channel length h (h_d, h_s)
- Channel width b_c
- Gate finger width b_f
- Gate finger length z
- Number of parallel gate fingers i
- Total gate area A_G

What are physically and technologically reasonable limits for these variable intrinsic PBT parameters? To answer this question, a couple of drift-diffusion simulations and analytical estimations were performed (see Ref. 1). In the following section we consider how the f_T and f_{max} values depend on the adjustable PBT parameters for a given operation point. Of course, the high-frequency performance depends on the material—Si or GaAs—and on the bias conditions, but a typical operation point of a silicon PBT as class A amplifier lays in the range of the data chosen here, with $V_G = 0 - 0.3$ V and $V_{DS} = 2$ V. For that reason, note that the results do not show always the absolute highest attainable frequencies, but they give the right tendencies for the device parameters.

Gate Length l_g

In order to gain shorter carrier transit times as in planar MESFETs, a gate length below 100 nm is certainly reasonable. By simulations in the present and in previous works (e.g., Ref. 41) it has been shown that the gate length for values less than 100 nm have nearly no influence on the high-frequency behavior of PBTs, i.e. the unity-current-gain fre-

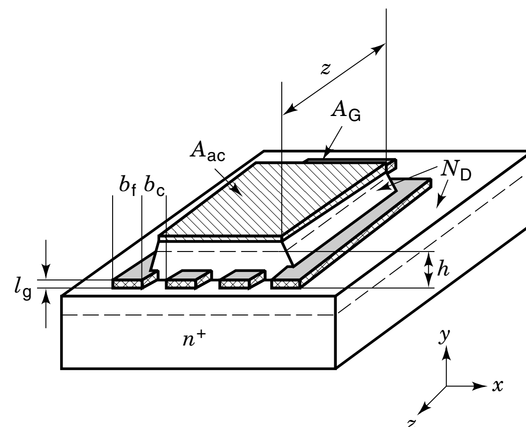

Figure 4. Typical realistic three-dimensional PBT structure of an overgrown type, considering the parasitic gate area. The main important transistor parameters are shown.

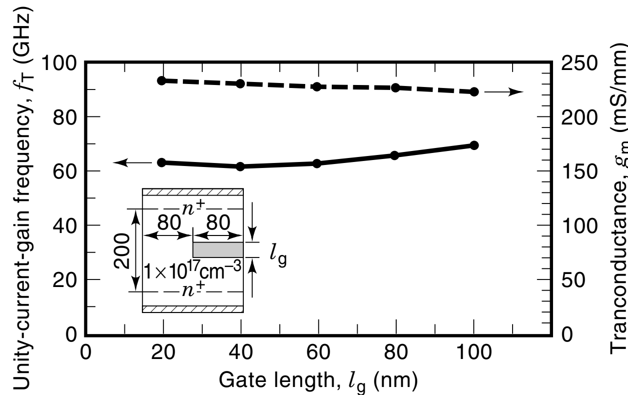

Figure 5. Simulation of transit frequency f_T and transconductance g_m versus gate length for a channel length h = 200 nm (dimensions in nanometers), demonstrating that between 20 nm to 100 nm gate length f_T and g_m are nearly independent from the gate length.

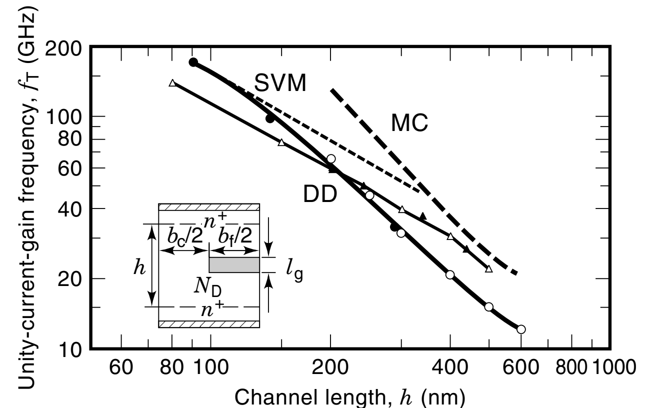

Figure 7. f_T versus channel length h. The parameters are shown in Table 3. ——— DD: drift-diffusion; --- MC: Monte Carlo simulation; ——— SVM: saturated velocity model, Si PBTs. These curves demonstrate the good agreement between different simulations, but also they proof the statement that for optimizing the transit frequency the channel length h is the main important parameter.

quency f_T (Fig. 5). However, for a suitable gate resistance and for preventing tunneling breakdown at very low voltages the gate length should not be shorter than 30 nm (14). Hence gate lengths l_g between 30 nm and 100 nm are appropriate values.

Channel Doping Concentration N_D

To investigate the influence of the channel doping concentration N_D, a PBT structure with two different channel lengths (h = 200 nm, 400 nm), constant gate finger width (b_f = 200 nm), and constant channel width (b_c = 200 nm) was simulated. For longer channels (e.g., h = 400 nm in Fig. 6), the unity-current-gain frequency increases with increasing doping concentration, as expected from MESFET results, but for short channel lengths in a PBT (e.g., 200 nm), the dependence of f_T on N_D is negligible. This is due to the spill-over effect in shallow n^+-n-n^+ structures (8,57), which leads to an enhanced electron concentration in the lower doped channel. The curves in Fig. 6 give a first hint for the effect of the channel length h on f_T.

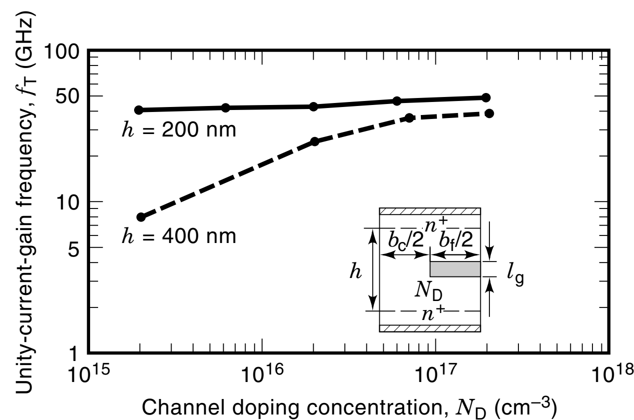

Figure 6. f_T versus channel doping concentration N_D with h as parameter ($b_c = b_f$ = 200 nm). The curve for h = 400 nm increases the higher the channel doping is, as expected. However, for short channels, for example, h = 200 nm, the transit frequency becomes approximately independent of the doping concentration in the channel, due to the electron spillover effect into the channel owing to the high doped emitter and collector regions.

Channel Length h

An important parameter for optimizing the high-frequency performance of PBTs is the channel length h. This is demonstrated by the drift-diffusion (DD) and Monte Carlo (MC) simulations and measurements of different authors in Fig. 7. The chosen parameters and operation points are listed in Table 3. Despite the different assumptions and operation points, there obviously exists an approximately linear relation between h and f_T for a double logarithmic plot f_T versus h, proving that the essential PBT parameter is its channel length h. For h values below 200 nm, unity-current-gain frequencies of 100 GHz are available in overgrown Si PBTs. Channel lengths much below this value are technologically not appropriate since breakdown and tunneling have to be taken into account. Nevertheless, for well-operating PBTs the channel width b_c and the doping concentration have to be chosen in a way that pinch-off is attainable. In longer channels (h > 600 nm) the gate–source distance h_s determines the high-frequency performance (10), but from simulations with (h = 600 nm) the gate position in the channel has nearly no effect on f_T. Comparing the results with those of Ref. 10 shows that enhancing the gate–drain distance reduces f_T with respect to a symmetric device with equal gate–source spacing. However, the breakdown voltage is increased. For high-frequency power applications, doping profiles with asymmetric gate positions in the channel are certainly reasonable as shown in Ref. 10.

Channel Width b_c

For a constant doping profile the unity-current-gain frequency increases for smaller channel widths, as can be seen in Fig. 8, but for very short widths b_c the frequency f_T drops. Then the channel is pinched off for the doping concentration and the operation point chosen here. The solid curves in Fig. 8 do not consider the different threshold voltages V_T; that is, the PBTs with large b_c values can never be pinched off, whereas the channels in the PBTs with small b_c cannot be

Table 3. Parameters of the Curves in Fig. 7

Symbol	Authors	(Ref. no.)	Simulation	N_D (cm^{-3})	l_g (nm)	b_c (nm)	b_f (nm)	V_G (V)	V_{DS} (V)
△	Gruhle	(8)	DD[a]	1×10^{12}	≈0	$h/2$	$h/4$	0	1.5
○	Ohshima et al.	(5)	DD	1×10^{17}	10	400	400	0	3
----	Ohshima et al.	(5)	MC[b]	1×10^{17}	10	400	400	0	3
●	Schüppen et al.	(1)	DD	3×10^{17}	40	$2h$	h	0	1
▲	Schüppen et al.	(1)	DD	3×10^{17}	40	$2h$	h	0.2	2

[a]DD, drift-diffusion simulation.
[b]MC, Monte Carlo simulation.

opened. Considering this situation, it is more reasonable to compare PBTs with threshold voltages V_T of approximately zero; that is, the channel doping concentration was enhanced with decreasing channel width for the dashed lines in Fig. 8 and the calculations in Fig. 9. Then the transistors with different b_c values operate approximately in the same regime. Surprisingly, in this case the transit frequency is in a wide range nearly independent of the channel width b_c. The reason for this behavior results from the short channel lengths (e.g., h = 200 nm). Then the ratio of the transconductance and the gate capacitances become nearly independent of the channel doping concentration N_D due to the spillover effect.

Gate Finger Width b_f

The gate finger width does not influence the transconductance, but the parasitic drain and source capacitances (i.e., the optimum b_f should be infinitesimally small. This is of course impossible to fabricate. For wide grid periodicities $b_c + b_f$ a small gate width would increase f_T, but note that f_{max} diminishes at the same time, because of the higher gate finger resistance. The simulations show that for small grid periodicities (≤600 nm) the gain from asymmetric b_f to b_c values is nearly negligible. In Fig. 9, f_{max} was estimated for PBTs with $V_T \approx 0$ and 1 mm total gate width using Eq. (2). The calculations of g_m, G_{DS}, and ($C_{GS} + C_{GD}$) were simulated and physically reasonable parasitic resistances were assumed, as shown in the figure caption of Fig. 9. The dashed curves indicate that the maximum oscillation frequency cannot be influenced either by the channel width b_c nor by the finger width b_f for $h = b_c = b_f$ and the parasitics assumed here. Surprisingly, for short channel lengths it seems that f_{max} is enhanced with rising b_c. This phenomenon may be attributed to the smaller gate capacitances at lower doping concentrations in connection with a constant channel transit time, whereby the approximately constant transit time or unity-current-gain frequency f_T, respecitively, is due to the spillover effect as mentioned above.

In order to find the best lateral PBT dimensions, some analytical estimations were performed and compared with the simulated data. The gate area is related to the number of parallel gate fingers i, the length of each gate finger z, the channel width b_c, and the gate finger width b_f as follows:

$$A_G = A_{ac} + A_0 \approx zi(b_c + b_f) + A_0 \tag{3}$$

A_{ac} is the active transistor area (i.e., drain or source area, respectively), and A_0 is the parasitic gate area. For the calculations the saturated-velocity model (60) and pinch-off condition in an optimum operation point were assumed. For $C_{GS} \geq 3C_{GD}$ the f_T is nearly independent of the capacitance ratio C_{GS}/C_{GD} and can be written as a function of the lateral geome-

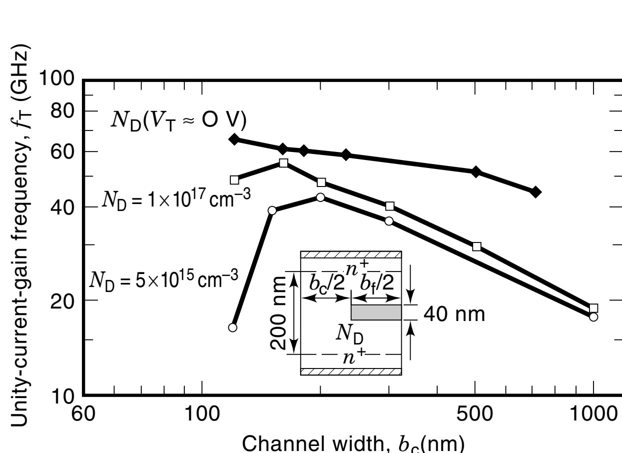

Figure 8. f_T versus channel width b_c for various N_D values. The uppermost curve is simulated for zero threshold voltage, which seems to be the best case for PBTs in terms of high f_T values. For constant doping profiles the transit frequency depends strongly on the channel width.

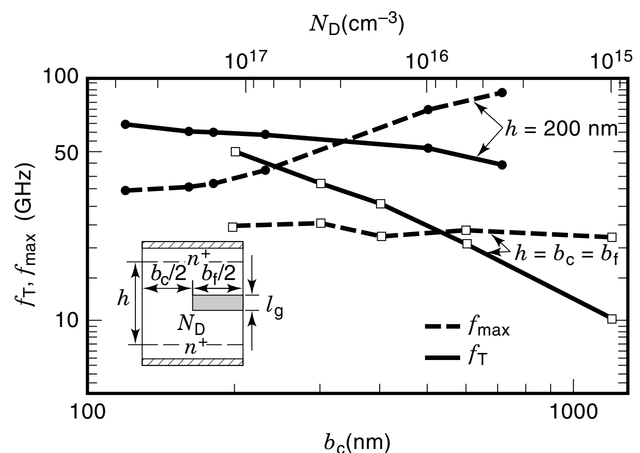

Figure 9. Simulated f_T as a function of b_c and N_D for $V_T \approx 0$ and estimated $f_{max} = f(b_c, N_D)$ for $i \cdot z$ = 1 mm, $R_G = R_S$ = 5 Ω, R_{GS} = 2 Ω, and $c \geq 3$, using simulated data and Eq. (2). Surprisingly, high f_{max} values can be obtained also for a 600 nm channel width for short channel length and relatively low channel dopings.

try parameters:

$$f_T \approx \frac{3v_{sat}}{4\pi} \cdot \frac{iz}{iz(b_c + b_f) + A_0} \tag{4}$$

This approximation leads to reasonable f_T values for small channel lengths ($h \leq 400$ nm), as can be seen by the comparison of the saturated-velocity model (SVM) with simulations in Fig. 7.

The plot of the transit frequency versus the number of parallel gate finger i for different finger length z obtained from Eq. (3) are shown in Fig. 10. For a given parasitic gate area A_0 the unity-current-gain frequency f_T rises with increasing number of gate fingers i. In addition, for PBTs with small active areas (e.g., for digital applications), it is more effective to use a few longer gate fingers than to use a lot of small fingers, because each additional finger contributes a parasitic area to A_0. For these assumptions, f_T will only be a function of the grid periodicity ($b_f + b_c$). The dotted lines in Fig. 10 indicate the maximum f_T values for two different grid periodicities and $z \to \infty$.

In order to optimize the maximum frequency of oscillation f_{max}, the transit frequency should be high and the gate resistance must be kept low. Therefore, obviously, each gate finger must not be too long and the number of parallel gate fingers not too small. For obtaining a more quantitative understanding of the problem, f_{max} from Eq. (2) can be written with $g = g_m/G_{DS}$, $c = C_{GS}/C_{GD}$, and $R_{GS} = R_S = 0$ as

$$f_{max} = \frac{1}{2}\sqrt{f_T f_{GE}}\,\frac{(1 + c^{-1})}{\sqrt{c^{-1} + g^{-1}}} \tag{5}$$

That means that the maximum frequency of oscillation is proportional to the geometric average of the cut-off frequency f_{GE} of input low-pass filter and the unity-current-gain frequency f_T. Neglecting the Miller capacitance, the cut-off frequency of the input low pass filter may be given by

$$f_{GE} = \frac{1}{2\pi(C_{GS} + C_{GD})R_G} \tag{6}$$

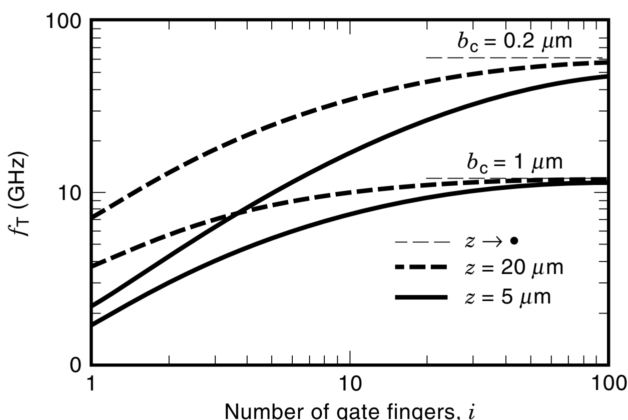

Figure 10. f_T versus the number of parallel $CoSi_2$ gate fingers i for $b_c = b_f$ and $A_0 = 50\ \mu m^2$ (1). The shorter the gate finger width the higher the part of the parasitic gate area, hence, the dependence of the number of gate fingers on the transit frequency is for short gate fingers higher than for longer ones.

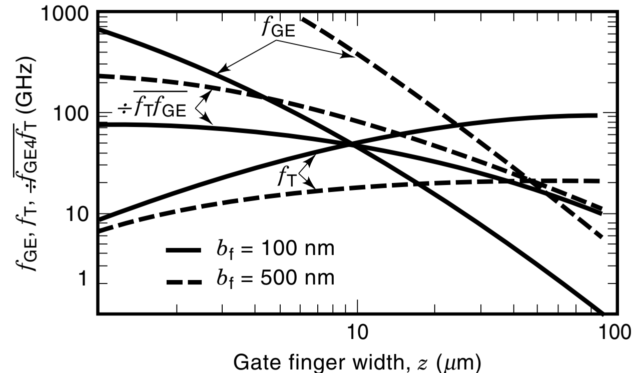

Figure 11. f_T, cutoff frequency of the input low-pass f_{GE}, and $\sqrt{f_T, f_{GE}}$ versus the gate finger width (1). The square root of the transit frequency and the frequency limit of the input low-pass filter is strongly correlated with f_{max}, showing that gate finger lengths above 10 μm are reasonable for good RF performance of PBTs.

For $z \gg b_f$ the gate resistance R_G of a typical Si/$CoSi_2$/Si PBT is estimated by

$$R_G = \frac{1}{i}\,\rho_{CoSi_2}\,\frac{z}{l_g b_f} \tag{7}$$

Parallel circuits of many gate fingers reduce the absolute gate resistance. This is an important advantage of PBTs over planar FETs or HEMTs (high-electron-mobility transistors), where technologically fussy air bridges and T gates have to be used for reducing the gate resistances. Despite the 40 nm gate length and 200 nm gate finger width, a gate resistance of 5 Ω can be achieved with 40 parallel fingers of 10 μm length. This corresponds to a gate resistance per gate width of 12 Ω/mm, whereas T gates typically yield values of 250 Ω/mm (61).

Plots of f_{GE} and f_T as a function of the gate finger length z are shown in Fig. 11. The curves of $\sqrt{f_{GE}(z) f_T(z)}$, which is proportional to f_{max}, indicate that the highest f_{max} lay in the left part of the crossover of the $f_T(z)$ and $f_{GE}(z)$ function. For gate finger lengths z smaller than 10 μm ($b_f = 100$ nm), f_{max} becomes nearly constant. Surprisingly, but in accordance with previous calculations (Fig. 9), f_{max} reaches higher values for larger gate finger widths b_f. A simple calculation in Ref. 1 leads to the following expression, which describes the correlation of z and $b_f = b_c$:

$$z < b_f\sqrt{\frac{l_g}{4\epsilon\rho_{CoSi_2} v_{sat}}} \tag{8}$$

Note that Eq. (8) becomes independent of the parasitic gate area and the relation of the gate capacitances. This is an important boundary condition for obtaining PBTs with high f_{max} values.

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