RADIATION EFFECTS

Significant damage occurs to semiconductor devices exposed to ionizing and other types of radiation. Since the 1960s, considerable work has been done to investigate the effects of radiation on semiconductor devices. Some of the earlier work on the effects of radiation on semiconductor devices focused on

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radiation-induced damage in minority carrier devices (e.g., bipolar transistors) caused by displacement damage and on transient radiation effects caused by high dose rate pulses of ionizing irradiation. A large portion of this early work originated from studies of the effects of nuclear explosions on semiconductor devices. Displacement damage occurs as a high-energy particle, for example, a proton or neutron, collides with an atom in a material. The high-energy particle can knock an atom from its lattice site to an interstitial site creating a vacancy/interstitial pair. This results in deep and shallow trap sites in the material that can compensate for majority carriers, cause carrier removal, and act as generating, recombining, and trapping centers. Displacement effects are important primarily for minority carrier and optoelectronic devices. A high dose rate pulse of ionizing radiation generates many electron-hole pairs in a short time. Photocurrents are generated that cause temporary loss of stored information or disrupt functional operation of an IC (dose rate upset). In some cases, the resulting high currents can cause permanent damage in a device.

In 1964, Hughes and Giroux (1) found that MOS devices are very sensitive to ionizing irradiation. Prior to this work, it was commonly believed that ionizing irradiation had little effect on MOS devices. After the initial work by Hughes and Giroux, a large amount of work investigated the mechanisms for ionizing radiation effects in MOS devices and methods for hardening MOS devices to ionizing irradiation. Total dose ionization degradation occurs as energetic particles (e.g., protons, electrons, X rays, gamma rays) ionize atoms in the material creating electron-hole pairs. Ionizing radiation induces significant charge buildup in oxides (e.g., the gate oxide of a MOS transistor or the field oxide of a MOS or bipolar IC) causing large threshold-voltage shifts and decreases in carrier mobility for MOS transistors and decreases in gain for bipolar transistors. This results in large increases in the static power supply of an IC, degradation in timing, and potentially loss of functionality. Total dose ionizing radiation often results in permanent or long-term degradation. There are many potential environments that expose devices to ionizing irradiation. Two of the most studied ionizing radiation environments are those of a nuclear explosion and space.

In addition to causing total dose ionization degradation and displacement damage, energetic particles, such as protons, alpha particles, and heavy ions in space, also cause single-event effects (SEEs). As a single high-energy particle (e.g., energetic heavy ion, proton, alpha particle, or neutron) strikes a material, it generates a dense plasma of electron-hole pairs along the path of the particle, which triggers a variety of SEEs. Single-event effects are classified into two types: *soft errors,* which cause no permanent damage and are correctable, and *hard errors,* which result in permanent damage to the device. A single event upset (SEU) is an example of a soft error, where only the logic state of the circuit is changed. SEUs were first observed in space in 1975 (2). Soft errors often are corrected by reloading the original information into a memory element or by restarting an algorithm in a CPU. If the error rate caused by single-event upsets is too high, performance degradation and even system failure results. Hard errors are observed in circuits where high electric fields are present across insulating layers, such as nonvolatile memories and thin gate oxides. Here, permanent damage is induced by energy deposition in a small region of the dielectric after the passage of a high-energy particle. This effect is termed single-event gate rupture (SEGR). Protons and heavy ions also trigger high-current conditions that result in circuit failure. Examples of this type of hard error are single-event latchup (SEL) in silicon-controlled rectifiers (SCRs) and CMOS and bipolar ICs, single-event snap-back (SES) in *n*MOS devices, and single-event burnout (SEB) in power transistors.

The early studies of radiation effects on electronic devices were funded primarily through military programs. Government funding constituted a significant portion of the funding for advanced semiconductor device development and government agencies influenced device development. Consequently, the major focus was on investigating the effects of and hardening devices to radiation from nuclear environments and on improving device performance to displacement, total dose ionization, and high dose rate pulse effects. Single-event effects were relatively unimportant because devices were relatively simple and operated at high voltage levels. Hardening devices was relatively straightforward. Many commercial semiconductor suppliers worked with government laboratories to manufacture radiation-hardened devices.

Today, the emphasis of radiation-effects studies has changed dramatically. With the end of the cold war, government funding for studies of nuclear radiation effects has dropped substantially. Commercial IC development is rapidly progressing and government funding constitutes only a small fraction of the money spent on advanced semiconductor development. As such, individual government agencies have little influence on commercial IC development. Only a few commercial IC suppliers are willing to work with government laboratories to manufacture radiation-hardened devices.

Meanwhile, the number of commercial and military space programs has increased dramatically. The complexity of ICs in space systems (both commercial and military) is rapidly advancing. As a result, now more emphasis is placed on single-event effects. As dimensions of integrated circuits (ICs) continue to shrink and power-supply levels decrease, less radiation-induced charge is required to upset electronics, and present-day ICs are becoming more susceptible to single-event effects. Single-event effects are no longer a problem only for devices in space systems. Naturally occurring terrestrial radiation also induces single-event upsets on earth and in low-altitude aircraft. As electronic technologies continue to advance, radiation-induced effects on IC reliability are becoming increasingly important even for commercial electronics used on earth.

The reduction in government funding and the number of suppliers of radiation-hardened devices has also increased the use of nonhardened, commercial, off-the-shelf (COTS) components in space systems. The total dose irradiation margin between device failure and system requirements is often small for COTS devices. This makes methods for ensuring device hardness in space based on laboratory measurements increasingly more important. Now a larger fraction of government funding is spent on developing techniques for improving hardness assurance test guidelines.

Because of the changing emphasis of radiation-effect studies, we focus the following discussion on those effects pertinent to space and terrestrial radiation, namely, single-event and total dose ionization effects. Emphasis is placed on those effects relevant to MOS transistors and ICs. MOS devices constitute a major portion of the electronics of nearly all modern space systems. The material covers radiation effects in both

commercial and hardened devices. Although we focus on MOS technology, the effects of radiation-induced charge buildup in MOS oxides can be applied to understanding radiation effects in other types of device technologies. For example, recent work has shown that the amount of gain degradation of bipolar transistors increases as the dose rate of the radiation source decreases (3–5). The cause of the increased degradation at low dose rate is related to the buildup of trapped positive charge and interface traps in oxides over the base region of *n–p–n* transistors (6,7) and the buildup of traps along the base/oxide interface of *p–n–p* transistors (4,5,8). The effects of charge buildup on gain degradation are unique to bipolar transistors, but defects responsible for degradation of bipolar oxides are similar to those responsible for degrading MOS oxides.

To place the discussion of radiation effects in its proper context, first we give an overview of space and terrestrial radiation environments. Single-event effects are covered next, beginning with a discussion of the charge collection mechanisms that are the basis for all single-event effects. Then circuit issues relevant to single-event effects, including both soft and hard errors, are presented. The final topic is total dose ionization effects. The mechanisms for total dose effects are first reviewed, followed by a discussion of charge buildup in ICs. We close with a review of present methods for improving total dose hardness.

SPACE AND TERRESTRIAL RADIATION

The particle flux in natural radiation varies widely in composition from the earth's surface to the interplanetary environment of space probes. In space, only protons and heavy ions have sufficient mass and energy to cause soft errors, whereas both protons and electrons contribute to total dose damage. In the terrestrial environment, cosmic rays and secondary particle showers cause upsets in ground-based electronics and in aircraft electronics. A detailed understanding of the radiation environment is necessary to estimate device reliability and, ultimately, the useful lifetime of a system.

In this section we describe the radiation environment in more detail, including a description of the dependence of the particle flux on energy, spacecraft altitude, inclination, and shielding. Understanding these dependencies and building accurate models of the environment experienced by spacecraft is important for error rate predictions. We also discuss the influence of the near-earth environment on terrestrial and low-altitude radiation.

Definition of Terms

Before proceeding, it is important to define a few commonly used terms to describe space and terrestrial radiation. As a particle passes through a material it loses energy by collisions with the electrons (electronic stopping) and nuclei (nuclear stopping) of the target material (9). The rate of energy loss per unit path length, dE/dx, from both mechanisms is called the total stopping power and is expressed in units of erg/cm. Mass stopping power is the energy loss per unit mass per area, $1/\rho\, dE/dx$, where ρ is the density of the target material. In single-event effects studies, we normally consider the amount of energy transferred per unit path length to a given material, where linear energy transfer (LET) is given in units of MeV/mg/cm^2 (or MeV-cm^2/mg). LET considers only the energy deposited along or near the particle's path, whereas stopping power considers all energy lost to the material. This distinction is important when considering energy deposition and collection on a microscopic scale, where track structure may be important. In most cases, however, mass stopping power is used to estimate LET, and the terms are used synonymously in the remaining text. The dependence of LET on energy has a peak, which is roughly equal to the atomic number of the ion in silicon. A carbon atom, for example, has a peak LET of about 6 MeV-cm^2/mg, and LET decreases on either side of this peak. The energy at the peak increases with the mass of the ion.

In many environments, particle flux is isotropic and strikes a system from any direction. Here it is defined as the number of particles per square meter per second impinging on a unit sphere from all directions. When flux is anisotropic, it is defined as the number of particles passing through the center of a sphere from a unit solid angle. This measure has units of number per square meter-steradian-seconds, and is, by definition, 4π smaller than the isotropic flux. Fluence is simply the flux integrated over time and is given in units of number per square meter or number per square meter-steradian for isotropic or anisotropic fluence, respectively.

Total-dose ionization irradiation is normally specified in units of rad or gray (Gy); 1 rad = 100 Gy. A rad is equal to 100 ergs of energy deposited per gram of material. The energy deposited must be specified for the material of interest. For example, for a MOS transistor, total dose is measured in units of rad(Si) or rad(SiO_2). For a space satellite, the average dose rate can vary over a wide range, from less than 10^{-6} to mid 10^{-3} rad(Si)/s. For a five-year space mission, these dose rates correspond to a total-dose range of less than 1 krad(Si) to more than 5 Mrad(Si).

Natural Space Radiation

Natural space radiation consists of a steady-state component and a transient component. The former consists of energetic, charged particles trapped within the earth's radiation belts, the solar wind, and very energetic galactic cosmic rays that originate outside our solar system. The steady-state environment changes over a period of years as it is moderated by solar activity and by precession of the earth's magnetic field with respect to the earth's axis of rotation. The transient environment is influenced primarily by energetic solar events, such as coronal mass ejections (CMEs), solar flares, and solar storms. This section discusses the major factors in the steady-state and transient environments that influence the performance of integrated circuits and semiconductor devices in space.

The Earth's Radiation Belts. Energetic, charged particles in the near-earth environment are trapped in the earth's magnetic field forming regions that are called the van Allen radiation belts after James van Allen, who designed the first instruments to measure and analyze the earth's radiation belts (10). The structure of the earth's magnetic field, the magnetosphere, defines the shape of the radiation belts, which to first order, can be described as a series of concentric shells of decreasing magnetic flux with increasing altitude. Each shell (called L shells) is given as a dimensionless number in units

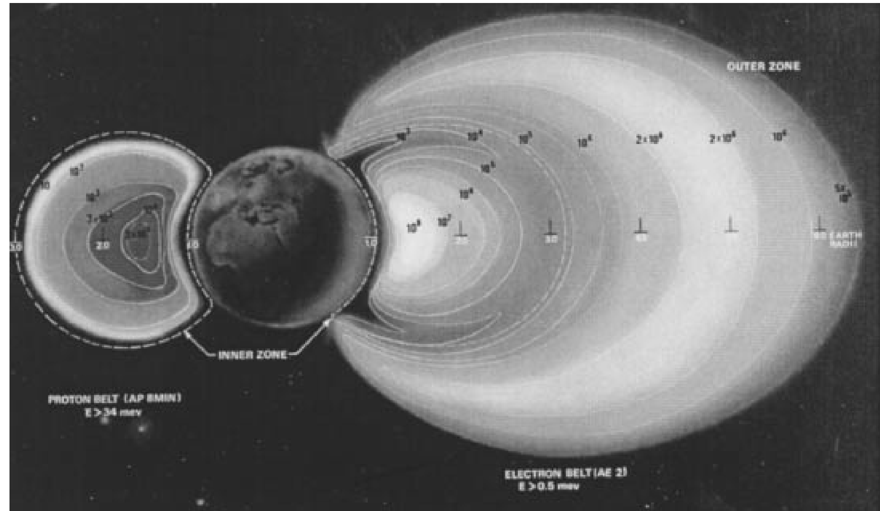


Figure 1. Density of the van Allen radiation belts formed by the earth's magnetosphere. The proton belt has a single peak at about 1.5 Re, and the electron belt is double peaked at 1.4 Re and 4.9 Re. Note that the belts are actually toroidal but are separated here for clarity.

of earth radii (Re = 6371 km). Because the magnetic field lines in a dipole field converge at the north and south magnetic poles, the distance between L shells decreases at polar latitudes, whereas the shells extend farthest at the magnetic equator, which is tilted 11° from the earth's geographic equator. A more detailed description of the earth's magnetosphere and its effect on the radiation environment can be found in Ref. (10).

The radiation belts, depicted in Fig. 1, begin at an altitude of about 1,000 km at the magnetic equator. The most abundant particles are electrons and protons. However, some low-energy heavy ions are also found. The distribution of trapped protons with energy greater than 10 MeV consists of one region that peaks at about 5,000 km and extends to about 18,000 km (3.8 earth radii). Higher energies are confined to the lower L shell. So, for example, the >400 MeV distribution extends only from L =1.2 to 2. Normal intensities for proton flux are on the order of 10^6/cm^2-s. The electron belts are divided into *inner* and *outer* radiation belts. The inner belt peaks at approximately 4,000 km and extends to about 9,600 km (2.8 earth radii) whereas the outer belt ranges from 11,500 km to about 70,000 km (12 earth radii). In low-earth orbit (LEO), spacecraft encounter both inner belt electrons and protons, whereas in geosynchronous orbit (GEO), about 35,775 km, primarily outer belt electrons are encountered. The most intense total dose radiation environment is at half geosynchronous orbit, about 17,500 km.

The South Atlantic Anomaly. Above the Atlantic Ocean off the South American coast the magnetosphere dips toward the earth causing a region of increased proton flux, called the South Atlantic anomaly (SAA). This region extends as low as 500 km. The proton flux of particles with energy greater than 30 MeV is 10^4 times more intense at 1,000 km in the SAA than at comparable altitudes over other regions of the earth. At higher altitudes the magnetosphere is more uniform and the proton flux depends only on the L shell.

Galactic Cosmic Rays. Galactic cosmic rays (GCR) originate outside the solar system and propagate throughout all space. The relative composition of the GCR flux depends highly on the ion species, as shown in Fig. 2 (11). Its composition is roughly 85% protons, 14% alpha particles, and 1% heavy nuclei, and spans more than 11 orders of magnitude in flux. Note that there are four orders of magnitude difference in the intensity of iron, the most abundant high LET heavy ion, and protons. The flux for each species peaks at energies of 100 to 1000 MeV/nucleon, then tails off to energies as high as 100 GeV/nucleon (12). At these energies it is virtually impossible to shield circuits from heavy ion strikes. The galactic cosmic ray flux provides a steady background radiation on the order of tens of particles per square centimeter-second that, because of their high LET, must be considered in spacecraft system design to ensure survival.

Solar Flares. Solar flares contain high fluxes of protons, electrons, and some energetic heavy ions, and generally last from hours to days (13). Because these fluxes are orders of magnitude higher than the steady-state flux of the radiation

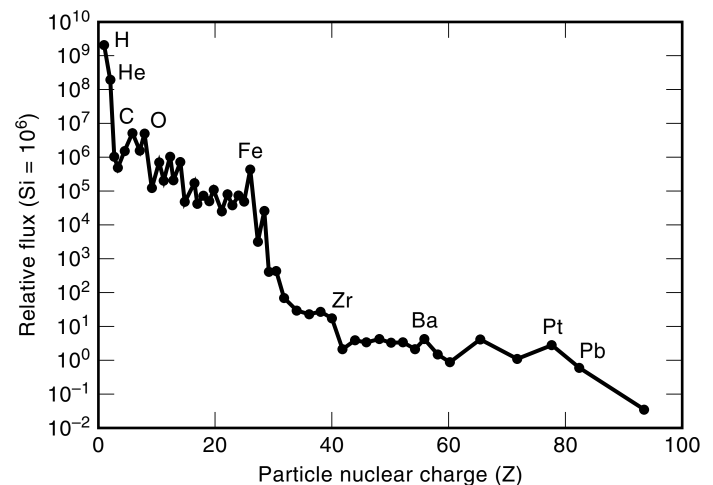


Figure 2. Galactic cosmic ray particle spectrum as a function of mass. Protons and helium ions are the most abundant elements, but there are a significant number of heavier elements up to Fe. Due to their high LET, even the low flux of ions heavier than Fe must be considered (11).

belts and the GCR flux, peak error rates in satellites are dominated by solar protons and heavy ions. Proton fluence during a large flare can exceed 10^{10} p/cm^2, and can have energies greater than 100 MeV. Depending on the energy spectrum of a given flare, solar protons extend to altitudes as low as 5 earth radii. Flares also inject energetic particles into the earth's radiation belts, some of which are trapped and form new radiation belts persisting for months (14). Early researchers thought that large flares were anomalous events. Now it is known, however, that the fluence distribution of flares forms a continuum that is well described by an extreme value distribution (15), which predicts a 10% chance per year of a large flare during the seven active years of the 11-year solar cycle.

Coronal mass ejections (CMEs) are solar events in the sun's chromosphere that eject large quantities of highly ionized gas into interplanetary space and have an associated magnetic bubble (16). When this magnetic bubble hits the earth's magnetosphere the resulting shock accelerates charge particles into the radiation belts. For large CMEs, the magnetosphere is significantly perturbed, reducing the magnetic shielding experienced by satellites. Magnetic storms are perturbations of the magnetosphere, can persist for hours to days after a large transient, and are associated with CMEs, flares, and changes in the embedded solar magnetic field. The solar wind is a steady stream of protons, electrons, doubly ionized helium, and a small quantity of heavier ions that emanate from the sun's outer atmosphere and permeate throughout the solar system and beyond (17). While the solar wind has an average variation that follows solar activity, it can change by orders of magnitude in a period of hours during CMEs and flares. Electrons dominate the total dose contribution from the solar wind. However, their energies are in the eV to keV range and are easily stopped by thin shields. CMEs and the solar wind do not contribute significantly to total dose or SEE in spacecraft systems. However, they can cause significant charging on exposed dielectric surfaces. After a critical charge is reached, these insulators destructively discharge. Dielectric charging must be considered in overall system design.

Dependencies. In earth orbit, the contribution of the GCR and solar-flare fluxes to the total particle flux depends on solar activity. The galactic component, for example, is affected by the screening effect of the solar wind. As solar activity decreases, the galactic component increases. On the other hand, the interplanetary and flare components increase with solar activity because they are composed primarily of particles originating in the sun. The change in the integral LET spectra (total flux of particles with LET greater than or equal to a given LET) as a function of solar activity is shown in Fig. 3 for a spacecraft in geosynchronous orbit. These particular curves were calculated for 25 mils of aluminum. The lowest intensity (curve a) occurs at the solar maximum excluding solar flares. This represents the absolute minimum in a geosynchronous orbit. The environment at solar minimum (curve b) describes the environment for approximately 40% of the time. This is the pure galactic cosmic ray spectrum. If we add solar flares to this, the 90% environment results (curve c). Alternatively, we say that the environment is more severe than curve (c) only 10% of the time. This curve, called Adams' 10% worse-case environment, has been used quite frequently to represent the space environment in error rate calculations (18).

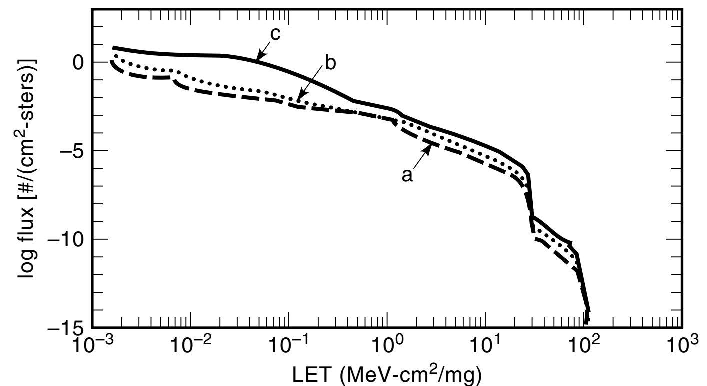


Figure 3. The integral LET spectra under (a) solar maximum conditions; (b) solar minimum conditions; and (c) the Adams' 10% worst-case environment. Integral LET curves give the flux for all particles with a given LET or less (20).

With the development of improved solar flare models, however, now in the solar minimum environment with a separate model for solar flares is considered the best estimate of the worst-case environment (19).

The earth's magnetosphere screens out particles below a specific energy determined by the particle's magnetic rigidity, which is defined as the momentum per unit charge, and the local field strength. The magnetic field deflects particles with lower rigidity and prevents their further penetration. Near the equator the earth's magnetic field screens all but the most energetic ions, whereas the particle flux at the poles is not significantly attenuated.

The penetration range of cosmic rays in a material depends on their energy. Therefore, the skins of a spacecraft and electronic boxes provide some degree of shielding to electronic components. The degree to which a spectrum is affected by shielding depends on the hardness of the spectrum. Additional shielding may prove effective against low energy components but is relatively ineffective in reducing hard components, such as high-energy protons and the galactic cosmic ray spectrum. For example, the GCR spectrum is only marginally reduced for aluminum thicknesses in the 2 to 10 g/cm^2 range (300 mils to 1.45 in. thicknesses). Only when shielding is on the order of 50 to 100 g/cm^2 is this spectrum appreciably attenuated (20). Spacecraft walls are normally about 100 mils thick. Recent honeycomb construction to reduce weight provides even less shielding.

The combined contribution of trapped electrons, protons, and solar flare protons to ionizing dose accumulated to a spacecraft is shown in Fig. 4 as a function of altitude and aluminum shielding thickness. Two peaks are evident: the first at 3,000 km is caused primarily by trapped protons, whereas the second peak at 17,000 km is caused by trapped electrons. As shielding thickness increases from 100 to 300 mils, the first peak decreases by a factor of 3, whereas the second peak decreases more than 60-fold. This clearly illustrates the effectiveness of shielding against electrons and the difficulty of shielding against high-energy protons. As an example of how this information is useful for ensuring survival of a space-based system, consider the annual dose accumulated to a system in three different orbits with 100 mils of aluminum shielding. A spacecraft in a low earth orbit of 800 km receives an annual dose of only 300 rad(Si), whereas a

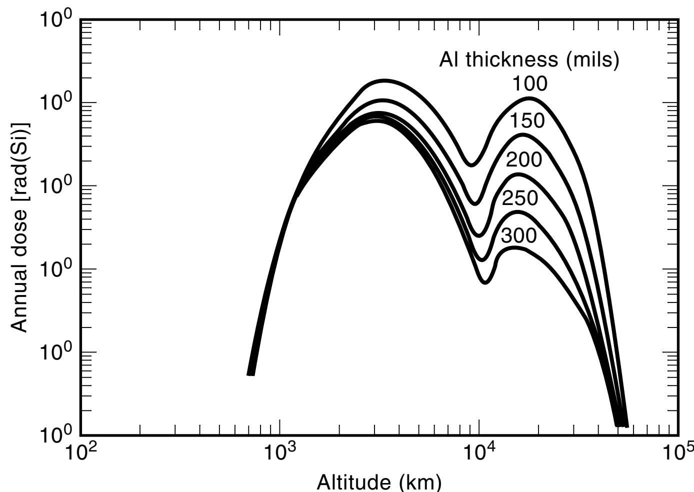


Figure 4. Annual ionizing dose accumulated as a function of altitude with shielding thickness from 100 mils to 300 mils of aluminum.

spacecraft in geosynchronous orbit at 35,000 km receives about 10 krad(Si) per year. A system in half-geosynchronous orbit, 17,500 km, receives a dose in excess of 100 krad(Si) per year. For a ten-year design lifetime these three systems require electronics that can survive doses of 3, 100, and 1000 krad(Si), respectively. Clearly, the design issues for a low-earth orbit are much more tractable than those for a system in the middle of the radiation belts.

Terrestrial Radiation. As galactic cosmic rays interact with the earth's upper atmosphere, they produce a shower of secondary particles that includes protons, neutrons, pions, muons, electrons, and photons. The density of secondaries depends highly on altitude, latitude, longitude, and the variation of the primary GCR flux with solar activity. It peaks at an altitude of about 15 km, just above commercial airplane altitudes and decreases at lower altitudes because of absorption and thermalization processes that remove secondaries (21). The neutron flux in the energy range from 1 to 10 MeV has a maximum at an altitude of 18.3 km (60 kft), but is significant as low as 9 km (30 kft). Taber and Normand (22) have shown a strong correlation between the upset rate observed in a 64 kbit memory and measured neutron flux as a function of altitude (Fig. 5). Note that the error rate has been scaled by a factor of 10^7 to plot it on the same graph. Similar correlations have been demonstrated as a function of latitude. Secondary protons are considered a possible cause for in-flight SEU. However, their latitude dependence does not correlate with the measured data.

SEUs are also observed at ground level and their frequency and distribution are consistent with terrestrial cosmic rays. Ziegler (21) showed that the frequency of errors in large computer memory systems, for example, scales linearly with altitude of the city in which they are located. In a test of both SRAM- and DRAM-based systems, a 13 time increase in error rate was observed as altitude increased from sea level to 10,000 ft (Leadville, CO). Similarly, error rate decreased as concrete absorber thickness increases. More recently, Lage (23) showed that SEUs reduced by terrestrial cosmic rays present a lower limit to system error rates after other sources of bit errors, such as package alphas, have been considered.

Terrestrial cosmic-ray-induced upset poses a significant challenge to the reliability of future systems. Although error correction and detection (EDAC) techniques are successful for mitigating upsets in memory systems, the possibility that new upset mechanisms will surface with next-generation technologies, such as logic upsets, cannot be discounted. New materials used for improved performance in advanced IC technologies can also introduce new sources of particle flux. Solder bump interconnects in flip-chip packaging can be a source of alpha particles if high purity lead is not used. Now the effect of technology and design changes on SEU is a first-order consideration for next generation ICs.

SINGLE-EVENT EFFECTS

The field of single-event effects (SEE) deals with the response of semiconductor devices and ICs to the passage of a single energetic atomic particle, such as a highly accelerated proton or a heavily ionized iron nucleus. There is a wide variety of effects, but the classic effect is termed single-event upset (SEU) and describes the corruption of information stored in solid-state memory devices. As an energetic particle transits the semiconductor material, it deposits energy in the lattice atoms, generating a dense plasma of free electrons and holes as the lattice atoms are ionized (holes are the absence of an electron and act electrically like a positively charged particle). When this excess charge is collected across a high field region, such as a *p–n* junction in a semiconductor device, a current pulse results that the device can interpret as a valid signal. For memory devices, this event can change stored information. For complex ICs, such as microprocessors, it can result

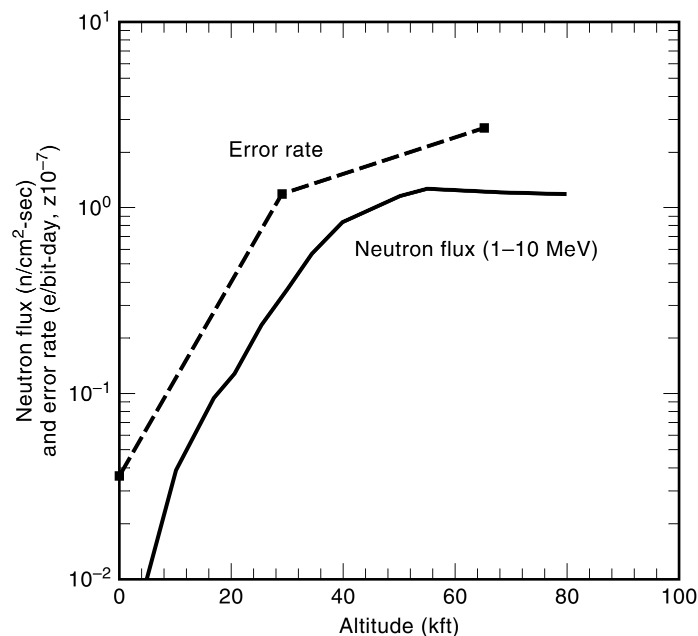


Figure 5. Single event upsets measured in a 16 kbit SRAM as a function of aircraft altitude and neutron flux. The interaction of galactic cosmic rays with the upper atmosphere generates secondary showers of energetic nucleons whose flux peaks at about 60 kft. SEU in avionics are well correlated with the neutron flux of the secondary showers (22).

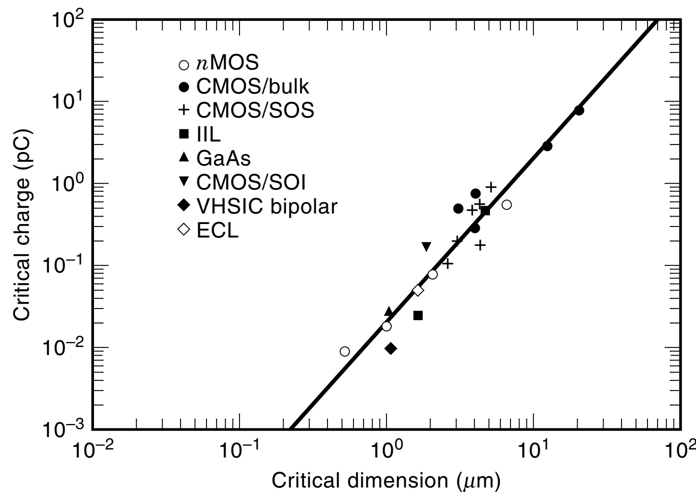


Figure 6. Critical charge as a function of critical dimension for various technologies. Historically, power law dependence has been observed (27).

in improper execution of a program and even in the processor locking up.

SEU was first observed experimentally in 1975, when Binder et al. (2) attributed bit-flips in bipolar J-K flip-flops in a communication satellite to galactic cosmic rays. A few years later, May and Woods (24) observed upsets in dynamic random-access memories (DRAMs) caused by alpha particles from the decay of radioactive material in ceramic packages. That same year, Pickel and Blandford (25) reported soft errors in nMOS DRAMs in space. Proton- and neutron-induced upsets were observed by Guenzer and co-workers in 1979 (26). Since that time, upsets have been observed in many satellite systems and are a major design consideration for any space-based system.

Single-event effects have traditionally been a concern only for semiconductors used in space environments, where devices are exposed to a high flux of radiation. The continuing decrease of feature size in ICs and the commensurate decrease in charge representing information has led to increased SEU sensitivity. The universality of this trend was noted by Petersen and Marshall (27), who observed a power law dependence of critical charge to upset as a function of technology feature size for a wide variety of technologies (Fig. 6). At technology scaling levels of 0.5 μm and below, they predicted that critical charge would decrease to less than 5 fC. In fact, now upsets due to terrestrial cosmic rays are being observed in large memory systems at sea level (28) and in avionics systems at altitudes from 30 to 60 kft (29). Recently, Johnston (30) noted that data from submicron IC technologies suggest that this trend may not continue unabated, because chip manufacturers have added capacitance to memory designs to reduce alpha-particle sensitivity.

The field of SEE encompasses a wide range of disciplines including high-energy physics, cosmic ray physics, solid-state physics, electrical engineering, IC processing, circuit design and analysis, system architecture, and computer modeling. Despite the breadth of overlap among many areas of research, a working knowledge of the important effects can be obtained by mastering a few concepts from these diverse areas.

SEE Mechanisms

The underlying processes that determine SEE sensitivity are charge deposition and charge collection in semiconductor materials. Charge deposition processes were discussed briefly in the introduction. Here, we discuss in more depth the charge collection processes that ultimately determine whether a device experiences an upset or destructive SEE after an energetic particle strike.

The dense plasma of electrons and holes generated along the track of a heavy ion strike are collected through a variety of mechanisms. Charge collection in the semiconductor itself includes drift collection in high electric field regions and diffusive charge collection outside field regions. These processes are illustrated in Fig. 7(a). Charge carriers generated in the initial depletion region are separated by the existing electric field and are rapidly collected. Holes are swept to the p-type side of the junction, and electrons are swept to the n-type side of the junction, resulting in a current pulse. The charge plasma surrounding the ion track can be dense enough to perturb the initial electric field lines of the junction, so that it reaches well beyond the extent of the original depletion region of the p–n junction into the more lightly doped side of the junction. As equilibrium is reestablished, the extended field collapses, sweeping additional charge into the junction where it is collected. This is the field funnel process first explained by Hsieh (31) using 2-D simulation, and subsequently described analytically by McLean and Oldham (32). Dodd et al. (33), provided a graphic depiction of this process using 3-D modeling. These prompt charge collection processes occur on

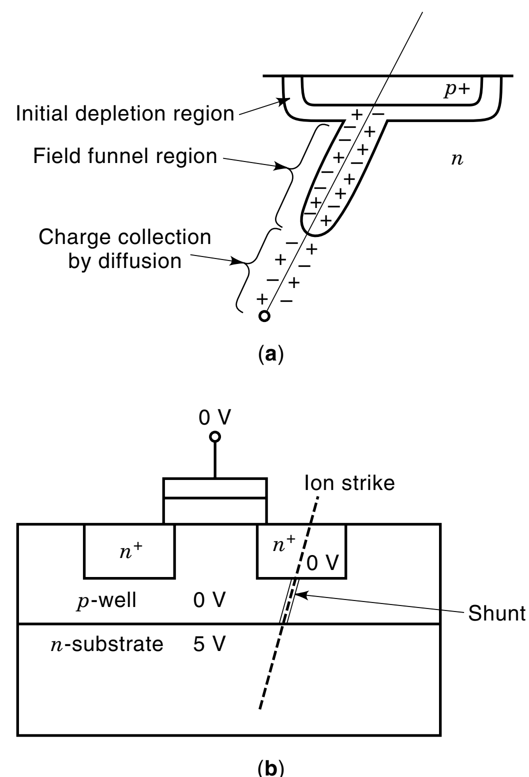


Figure 7. Charge collection mechanisms include photocurrent collection due to (a) drift in the depletion and field funnel regions and diffusive charge collection; and (b) shunt charge collection when regions of like doping are connected by a plasma shunt.

the order of 10 to several 100 ps, depending on doping levels in the substrate and are faster than circuit response times in present technologies.

Outside the high field regions of the junction and the field funnel, charge is collected by diffusive processes driven by concentration gradients in quasi-neutral regions of the semiconductor, as described by Kirkpatrick (34) for single-event upset. This process occurs later and extends to as long as 10 ns, which is on the order of the circuit response time or slower. The shape of the charge collection transient can be a first-order concern for determining upset sensitivity, depending on the technology and circuit design. This is discussed further in the next section.

In some IC technologies, parasitic three-layer *n–p–n* and *p–n–p* structures are formed that are sources of shunt current or bipolar gain when charge is generated in the base region. In the first case, a heavy ion strike can connect regions of similar doping that are separated by a region of opposite doping, as seen in Fig. 7(b). A charge can flow between like regions when a potential difference exists. This *shunt* effect was observed by Hauser et al. (35), in CMOS test structures and by Sexton et al. (36) in pass transistors in a CMOS technology. Bipolar gain results when the initial charge generated in the base turns on a parasitic bipolar transistor that subsequently injects much more charge in the circuit than was originally deposited by the heavy ion. Although this effect has been observed only in specialized cases to date, this mechanism may dominate as technologies scale to deep submicron levels in coming years (37). Similar structures occur in silicon-on-insulator (SOI) technologies and can result in an increased SEU sensitivity when the body region is allowed to float (38).

The region from which charge is collected is called to as the sensitive volume (SV). As the previous discussion indicates, multiple mechanisms contribute to charge collection making it difficult to define a SV clearly. Additionally, circuits sensitive to the rate at which charge is collected have a SV that varies with circuit operation. In spite of these complexities, the SV concept is widely used because of the intuitive insight it gives to the underlying physical processes, and it is useful as a mathematical construct in error rate prediction methodologies (discussed in the Error Rate Prediction section).

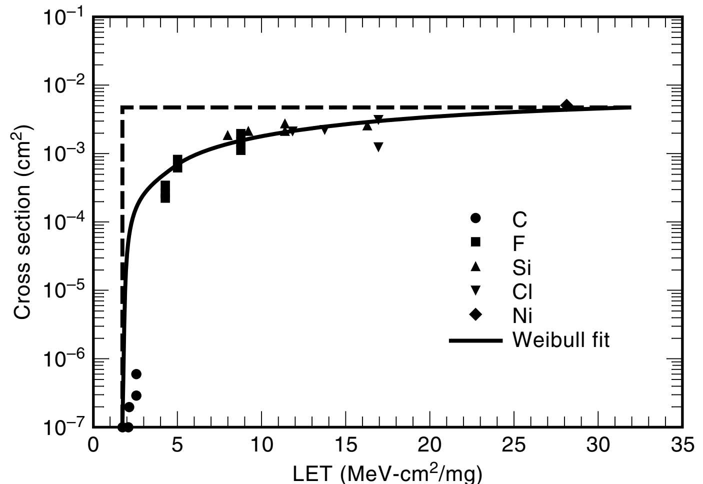


Figure 8. A typical upset cross-sectional curve is compared to an ideal curve. The ideal curve has an abrupt threshold and a well-defined saturation cross section, whereas measured curves show a gradual threshold and an ambiguous saturation cross section.

Single-Event Upset

The sensitivity of an IC to single-event upset (SEU) is expressed as the ratio of number of upsets to the total particle fluence, that is, # upsets/(# particles/cm^2). Because this term has units of square centimeters, it is called the error cross section. Experimental cross-sectional data are normally plotted as a function of LET for particles striking the IC normal to the surface. Two key parameters are determined from cross-sectional curves: the threshold LET for upset, L_0, and the saturation cross section, σ_{sat}. The threshold LET is a measure of the minimum LET required to upset the most sensitive region of the chip, whereas the saturation cross section should equal the total area of the sensitive regions of the chip. These parameters are used to estimate the error rate for a given IC in a specific environment. In Fig. 8 we show an ideal and a measured cross-sectional curve for a typical commercial memory chip. The ideal cross-sectional curve (dashed line) is a step function with a well-defined threshold and saturation cross section. Below the threshold, no cell upsets, whereas above the threshold, all sensitive cells upset.

For a real device, however, there is a distribution of thresholds due to variation of charge collection across a cell and cell-to-cell variation in sensitivity, resulting in a smoothly increasing cross section with LET. As LET increases, more regions of the device are sensitive to upset. The measured cross section increases until all sensitive regions upset and the cross section curve saturates. Cross-sectional curves are sometimes plotted as a function of linear charge deposited (LCD) with x-axis units of picocoulombs per micrometer (for silicon, 1 MeV-cm^2/mg is equivalent to 0.0104 pC/μm). Measured upset curves such as this are taken over a range of LET, where LET is increased by using higher Z ions (for C to Ni ions used here, LET ranges from 2.5 to 28 MeV-cm^2/mg). LET is also varied by increasing the angle of the ion strike relative to the surface normal, thereby increasing the path length through the SV and increasing the amount of charge deposited in the SV. This results in a higher "effective LET," given by:

$$L_{\text{eff}} = L_0 \cos\theta \tag{1}$$

where L_0 is the ion LET at normal incidence and θ is angle of incidence relative to the surface normal. The effective LET approximation has been used extensively in the past for large geometry devices that have large, flat sensitive volumes. It breaks down, however, as device geometries shrink and the dimensions of the SV are nearly equal. In this case, a more involved correction for the angle of incidence is required (39). Also shown in Fig. 8 is a fit to the data based on the Weibull distribution function (solid line), which is often used in reliability estimating techniques.

Dynamic circuits, such as dynamic RAM (DRAM) cells, depend for proper operation on charge storage on a circuit node or in a region of silicon. For a DRAM, the amount of charge necessary for proper circuit operation is a function of the sensitivity of the sense amplifiers, the memory cell capacitance, and the bit line capacitance. A one-transistor DRAM memory

cell is shown schematically in Fig. 9. Information is stored on capacitor C_{cell}, which is written and refreshed through the access transistor. When the cell is subsequently accessed by turning this transistor on, the bit line is pulled down, and the complement state of the cell is sensed on the bit line. The critical charge representing a bit of information on capacitor C_{cell} can be as small as 0.1 to 0.5 pC. This is equivalent to only 5×10^5 to 3×10^6 electrons. If an ion strike results in charge collection to the memory node of about the same order of magnitude as the original charge on the node, a bit error occurs. In subsequent refresh cycles the error is maintained, because the new state of the memory cell appears to be valid information. The primary consideration for dynamic circuits like this is whether the collected charge exceeds the critical charge required to represent a logic state on the memory node. If the critical charge is exceeded, an upset occurs. Ref. 40 discusses DRAM upset in more depth.

In static circuits, such as a CMOS static RAM (SRAM) or D-latch, upset is controlled by the rate at which charge is collected. A schematic diagram of a six-transistor (6-T) memory cell is shown in Fig. 10. Each series connection of an n- and p-channel transistor forms an inverter whose input is the common gate and whose output is the common drain. When the output of each inverter is coupled to the input of the other inverter, a bistable memory element is formed. In this diagram feedback resistors are shown in the cross-coupling links. Feedback resistors (R_{FB}) are used to slow the response of the circuit to the ion strike, thereby hardening the memory to upset, but there is a commensurate performance penalty. Following an ion strike to the off-biased drain of transistor $P1$ (labeled "ion strike" in the figure), a current spike is observed on the drain node of the inverter formed by transistors $N1$ and $P1$. If charge is collected by the drain of $P1$ faster than it is removed by the unstruck n-channel transistor $N1$ (called the restoring transistor), the node voltage rises to a diode drop above V_{DD} (see the lower left waveform in Fig. 10) and an upset may occur.

Whether an upset occurs depends on the competing processes of removing excess charge at the struck node and changing the state of the opposing inverter of the memory cell (41). The time required for the struck node to recover to one-half the voltage swing at the node is defined as the recovery time t_R. The time required to switch the opposing inverter formed by transistors $N2$ and $P2$ is defined as the decoupling time t_{DC} (see the lower right waveform in Fig. 10). Upset occurs in this analysis if t_R is greater than t_{DC}. Memory cells are hardened to SEU by adding feedback resistors in the cross-coupling link between inverters (shown as R_{FB} in the figure). This effectively increases t_{DC} and gives the cell more time to remove excess charge before responding to the transient.

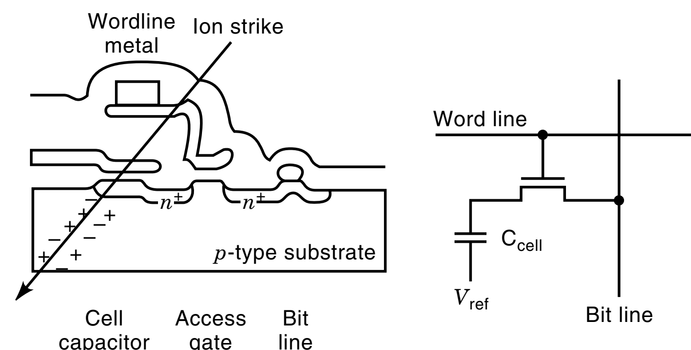


Figure 9. Circuit schematic of a one-transistor DRAM memory cell. Information is stored as charge on the capacitor C_{cell} and is accessed through the single transistor.

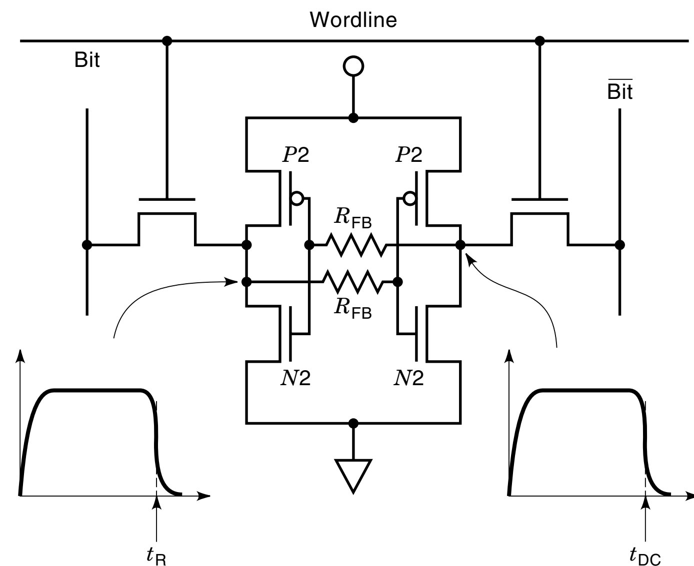


Figure 10. Logic diagram and circuit schematic for a six-transistor CMOS SRAM memory cell. The cross-coupled inverters form a bistable memory element. Each inverter is composed of a series connected n- and n-channel transistor. The voltage transients following a heavy ion strike to an "off" biased p-drain are shown. Feedback resistors R_F are inserted in the cross-coupling links to reduce SEU sensitivity (41).

As packing density increases, the charge deposited by a single ion strike is collected by the sensitive volumes of more than one memory cell and multiple bits are upset. Zoutendyk et al. (42) first observed this phenomenon experimentally, called multiple bit upset (MBU), and it has since been measured in many different technologies. MBU has also been observed in closely spaced trench capacitor storage cells used in advanced DRAMs. In this case upset was attributed to a shunt connecting two adjacent storage regions (43). Most EDAC implementations are able to detect and correct one bit upset in a single word and detect two bit upsets without correction in a word. If a memory chip is laid out so that multiple bits in a single word are topographically adjacent, MBU defeats these EDAC schemes. More complex EDAC approaches can be applied, but these require additional bits of memory and much more error correction overhead. The better approach is to ensure at the chip design level that logical bits in a word are not located physically close to each other.

Hard Errors

Single-Event Latchup. The single most important effect that designers of space-based systems must consider is catastrophic damage resulting from single event latchup (SEL). Latchup is a high current condition that results from thyristor (also known as a silicon controlled rectifier, or SCR) action in four-layer structures. Latchup creates a low-resistance path from power supply to ground in CMOS ICs, which are vulnerable to this failure condition because of the complemen-

tary structure required for this technology (44). As shown in Fig. 11, a pair of coupled parasitic bipolar transistors are associated with the *p*-well structure. A vertical *n*–*p*–*n* transistor is formed from the *n*-type substrate, *p*-well, and *n*-channel source, whereas the *p*-well, *n*-type substrate, and *p*-channel source form a lateral *p*–*n*–*p* transistor. The lumped-parameter equivalent circuit is shown on the right-hand side of the figure.

Latchup is triggered in SCR structures by excess current in the base of the lateral *p*–*n*–*p* transistor. When sufficient current flows in the substrate (across R_s), the emitter base junction of the *p*–*n*–*p* transistor is forward biased and it injects a large current into the *p*-well. This current induces a voltage drop in the *p*-well (across R_w) which turns on the vertical *n*–*p*–*n* transistor. As the *n*–*p*–*n* transistor turns on, it reinforces the initial current in the substrate, and a regenerative condition exists which results in high current and low resistance. The holding voltage for latchup is on the order of 1 V. Latchup in early devices was triggered on the order of hundreds of nanoseconds, and destructive burnout occurs on the order of hundreds of microseconds (45). The threshold for latchup decreases with increasing temperature and power supply voltage (46). Latchup susceptibility in advanced technologies is addressed by Johnston (47). During SEL measurements, latchup cross section is calculated in the same manner as upset cross section, that is, the number of latchups divided by the fluence to latchup, and is plotted as cross section versus LET.

Single-Event Gate Rupture. Another major consideration for designers is a catastrophic failure known as single-event gate

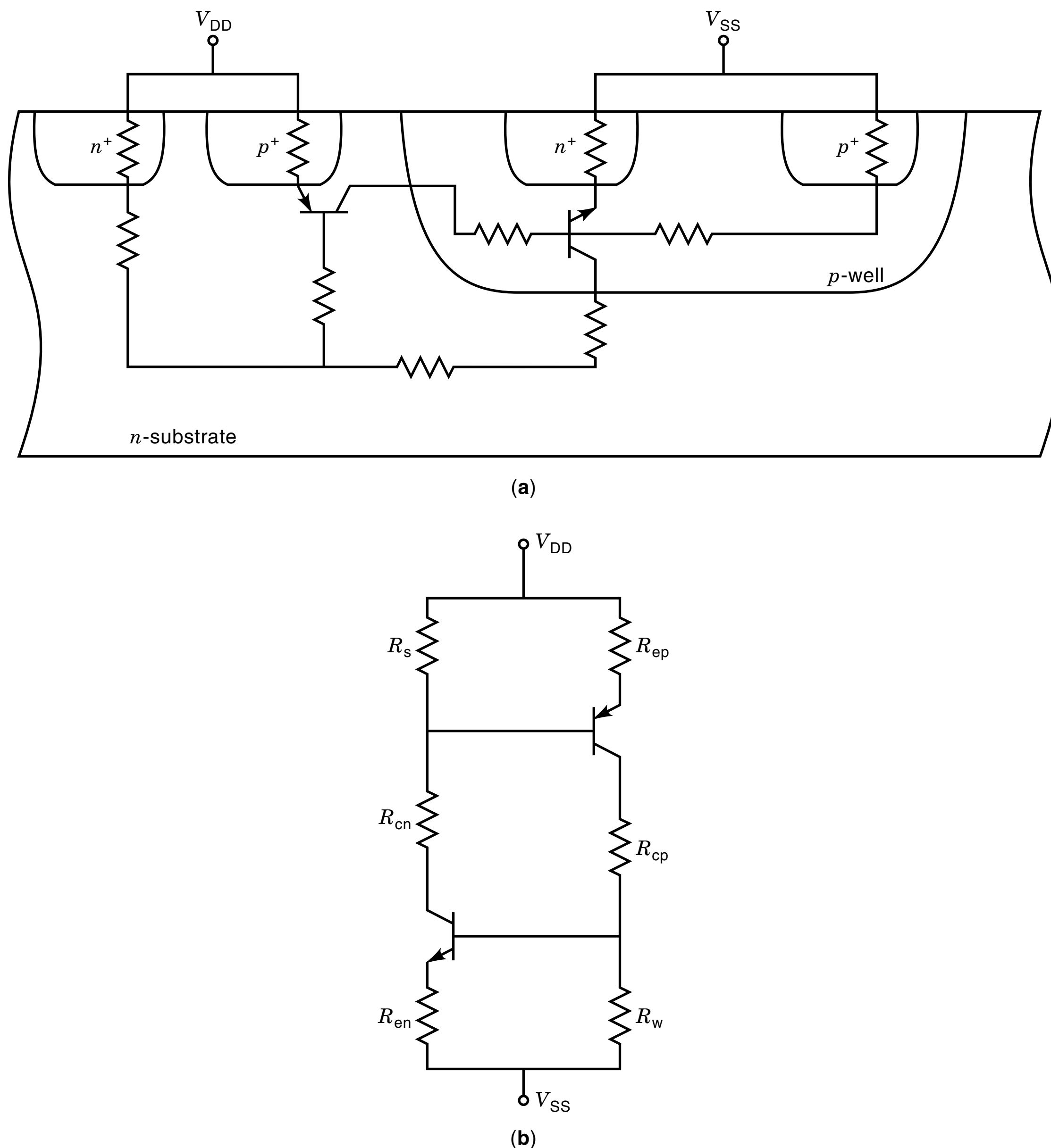


Figure 11. Cross section of a CMOS technology showing (a) the vertical *n*–*p*–*n* and lateral *p*–*n*–*p* parasitic transistors formed in this *p*-well technology; and (b) a circuit schematic indicating how the parasitic elements are electrically connected (44).

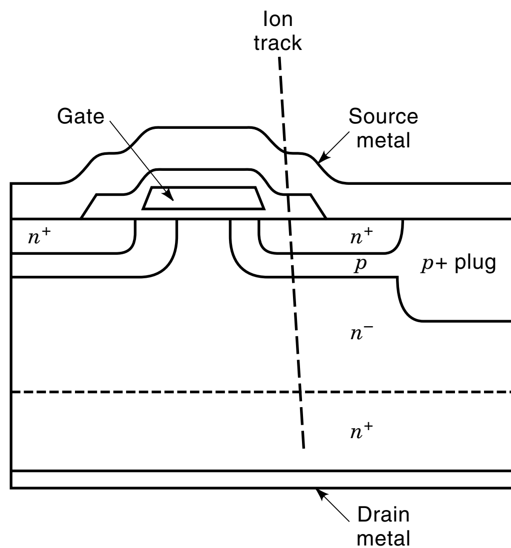


Figure 12. Cross section of a typical power MOSFET structure.

rupture (SEGR) (48,49). This effect occurs under conditions of high field, as happens during a write or clear operation in a nonvolatile SRAM or EEPROM. It has recently become a concern for advanced technologies as oxide thicknesses scale below 10 nm and oxide fields increase above 5 MV/cm (50). As a heavy ion passes through the dielectric, a highly conductive plasma path is formed that allows the capacitor formed by this structure to discharge. If sufficient energy is stored on the capacitor because of high electric fields, excessive heating during discharge creates a thermal runaway condition (48). Temperatures are high enough to cause the dielectric to melt and the overlying conductive layers to evaporate.

In a power MOSFET, the requirement for a standoff voltage on the order of 100s of volts is satisfied by dropping this potential over the thickness of the silicon substrate. A typical cross section of a power MOSFET is shown in Fig. 12. In normal operation, the MOSFET gate induces a channel between the source and drain regions. Current flows from the source to the drain near the surface and then is collected in the heavily doped substrate. The lightly doped epi layer doping and thickness determine the on resistance of the device. As a heavy ion passes through the substrate, the large bias on the drain is electrically coupled into the oxide electric field, resulting in gate rupture at voltages well below the rated standoff voltage. This mechanism is described in detail by Brews et al. (51). Figure 13 shows the set of V_{GS} and V_{DS} biases that result in SEGR as a function of various heavy ions for a power MOSFET rated to 70 V with a 50 nm gate oxide. The data cover an LET range from 3 MeV-cm^2/mg for F to 82 MeV-cm^2/mg for Au. The control data shown in the graph (open circles and dashed line) denote nominal rupture voltages with no heavy ion exposure, which are -40 V and 73 V for V_{GS} and V_{DS}, respectively. During exposure to heavy ions, however, the V_{GS} at which SEGR occurs decreases as V_{DS} increases. An empirical equation that fits this dependence has been developed by Wheatley et al. (49):

$$V_{GS} = 0.84[1 - \exp(-L/17)]xV_{DS} - \frac{50}{1 + L/50} \tag{2}$$

where V_{GS} is the gate bias at which rupture occurs, V_{DS} is drain to source voltage, and L is the incident ion LET. This equation correctly fits the observed trend of decreasing V_{GS} with increasing V_{DS} and LET. The first term describes the coupling of drain bias from the substrate into the gate, and the second term accounts for the effect of the ion passing through the oxide itself. Fits to this equation are shown as solid lines in Fig. 13. Each line denotes the safe operating range for this part as a function of heavy ion. Note that the safe operating range decreases for increasingly heavy ions (higher LET). The manufacturer's recommended derating for SEGR is shown as a dotted line in Fig. 13. This represents a 50% decrease in maximum V_{GS} and V_{DS} to account for SEGR.

The industry trend toward increasing electric fields as oxide thickness and feature size scale down in advanced technologies raises the concern that SEGR may be a limiting factor for integrated circuits (ICs) in space applications. It has been suggested that, as devices scale to 0.25 μm and below, SEGR by Fe ions will occur, leading to a large increase in catastrophic failures in space hardware. Sexton et al. (50) found that, as oxide thickness decreases below 10 nm, the increasing breakdown strength of the oxides results in a higher than expected gate voltage for rupture, contrary to earlier predictions. Their results suggest that advanced technologies will be more SEGR resistant than expected at a given electric field. They caution, however, that SEGR will continue to be a significant concern for devices that operate with a gate oxide electric field above 5 MV/cm.

Single-Event Burnout (SEB). Destructive failure resulting from heavy ion exposure is observed in bipolar power transistors and in power MOSFETS (52–54). In this phenomenon, the excess current generated by the passage of a heavy ion triggers a secondary photocurrent that overheats the device and causes catastrophic failure. In power MOSFETS, a parasitic n–p–n bipolar transistor exists between the epi layer (collector), the p-type body (base), and the n-type source (emitter) (see Fig. 12). When a heavy ion passes through this

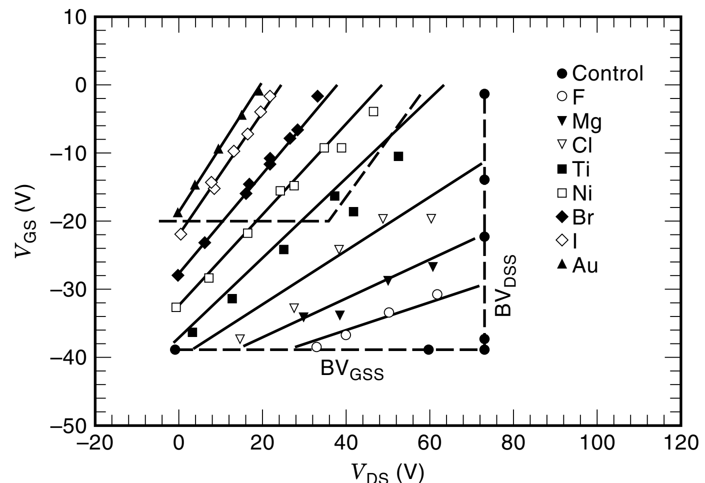


Figure 13. Dependence of single-event gate rupture as a function of drain-source bias, gate-source bias, and ion species. Breakdown voltages without ion irradiation are shown as a dashed curve (control), and the manufacturer's suggested derating in space is shown by the dotted curve. (49).

parasitic transistor, excess current is generated in the base region. Excess hole current flows toward the body contact, raising the local potential along the base–emitter junction. If sufficient current flows to raise this potential to the turn-on voltage of this junction, the base–emitter junction becomes forward biased and turns on the n–p–n transistor. Following turn-on, the transistor enters a second breakdown condition where thermal runaway reinforces the mechanism caused by avalanching at the epi–substrate junction. This condition has been called current-induced avalanche (CIA) (55). If the external circuit provides sufficient current, local overheating in a portion of the device occurs, destroying the device. A definite threshold voltage is required for burnout to occur, and this is often well below the normal breakdown voltage for the device. Fischer (54) has measured failure threshold voltages ranging from 22% to 90% of the rated breakdown voltage for devices from several manufacturers.

Snapback. Snapback is a high-current, low-resistance condition that occurs only in n-channel transistors. It has an *IV* characteristic that is similar to latchup and exhibits a negative-resistance region and a low-resistance region. Like latchup, it is triggered by external stimuli that inject sufficient current into the p-well to make the n-source forward biased. Snapback initiation has been observed by avalanche-induced breakdown at the n-drain (56), by excess photocurrents generated during moderate dose-rate gamma irradiation (56), and by heavy-ion strikes to sensitive n-drain or n-channel regions (57).

A significant difference between latchup and snapback is that the holding voltage is on the order of several volts depending on channel length and doping levels, much higher than the 1 V holding voltage seen in latchup. Snapback is sustained only when the load circuit on the n-channel device provides sufficient holding current. For CMOS ICs, the load devices are p-channel transistors. Because holding current is on the order of milliamps, snapback is normally observed in output buffers and internal bus drivers.

Proton-Induced Effects. Because of the small stopping power for protons, insufficient charge is generated to induce SEE at current levels of sensitivity. Interaction of a proton with the semiconductor lattice, however, generates secondary particles with higher LET that cause SEE (58). Elastic scattering of target nuclei, for example, deposits enough energy to cause soft errors. Of more importance, however, is the contribution to upset from inelastic scattering events, where the incident proton reacts with the target nucleus. About one of every 10^5 protons experiences an inelastic collision with the target lattice. As the composite nucleus decays, it emits alpha particles and lower energy protons. In addition, the daughter nucleus recoils with enough energy to cause upset through direct ionization. The composite nucleus also decays through a spallation reaction, where the compound nucleus breaks up into two heavy fragments, both of which recoil and deposit energy. Researchers have observed proton-induced upset, latchup, and burnout. To date, no instance of SEGR is attributed to protons.

SEU Mitigation. Depending on the application, a low rate of SEU is acceptable in systems. Error detection and correction (EDAC) circuitry and software are often included to handle these errors (59,60). Some examples of EDAC include use of parity bits, Reed-Solomon encoding, and Hamming codes. If errors occur too frequently, however, the error handling architecture of a system is overwhelmed and system failure results. In mission-critical applications, such as circuitry for a satellite attitude control system, SEU hardened devices must be used to reduce the probability of system failure.

Special design and fabrication techniques are available to harden circuitry to SEU. Circuit design techniques include increasing the size of transistors to remove excess charge faster (61), and the use of redundant circuits and voting logic to determine the correct state (62). Feedback resistors and capacitance are added to internal nodes of memory cell to reduce sensitivity to transients (63). All of these techniques incur some degree of performance penalty. Increased size carries a density penalty, and adding redundant circuitry increases chip power and reduces functional density. Feedback resistors and capacitors reduce the speed of the device.

A more direct approach to SEU mitigation centers on reducing the amount of charge collected following a heavy-ion strike. A prime example of this approach is the use of silicon on insulator (SOI) substrates. The SEU tolerance of a nonhardened SRAM design is greatly increased by simply fabricating the design in a SOI-based technology. Figure 14 is a cross section of a mesa-etch SOI transistor. The active silicon channel region is an *island* built on top of an insulating layer (buried oxide) instead of a silicon substrate. Because SOI/MOS transistors are fabricated on an insulating layer, the amount of p–n junction area and the sensitive volume are greatly reduced, thereby making SOI/MOS ICs far superior to bulk silicon ICs for single-event upset. Because there are no possible parasitic bipolar transistors between n- and p-channel transistors and consequently, no four-layer structures, it is also impossible to latchup SOI-based technologies. SOI transistors operate in two modes, partially depleted and fully depleted. Partially depleted transistors are defined as transistors whose the silicon thickness is greater than the maximum depletion width formed by the conducting channel. In fully depleted transistors, the conducting channel and

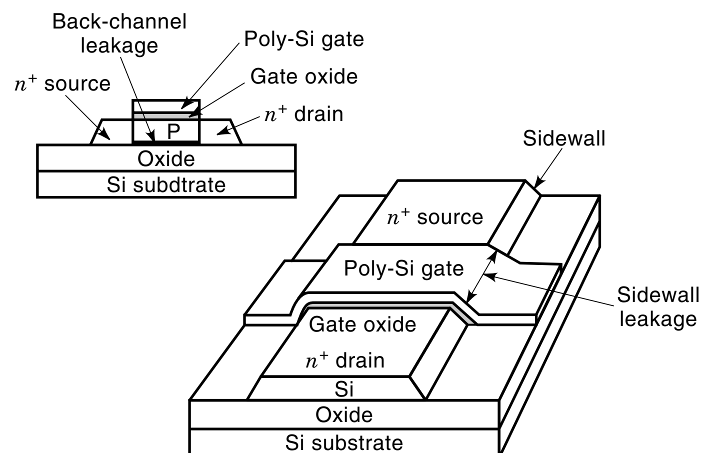


Figure 14. Cross section of a mesa-etched SOI transistor. The active silicon channel is built on top of an insulating oxide leading to a lower sensitive charge-collection volume and reduced p–n junction area. These properties make SOI ICs superior to bulk-silicon ICs for single-event upset and high dose rate pulsed-irradiation hardness.

depletion region extend throughout the thickness of the silicon layer. The presence of a region of nondepleted silicon between the edge of the depletion region and the silicon/buried oxide interface in a partially depleted technology provides a place where excess charge builds up unless body ties are provided to connect this region to a voltage reference (e.g., normally a transistor source diffusion). For partially depleted SOI technologies, body ties or other means of removing excess charge in the floating body are required for optimum SEU tolerance. In a fully depleted technology, excess charge in a floating body is greatly reduced because it is swept out by the high fields in this region. In this case, body ties are not required to obtain high SEU tolerance.

Error Rate Prediction

Error rate predictions are based on estimating the particle flux expected for a given part during its lifetime and a measurement of the SEE sensitivity of the part. The environment has been discussed earlier. Part sensitivity is often described in terms of its critical charge Q_c, defined as the minimum collected charge necessary to upset a circuit. (For simplicity it is assumed that collected charge and deposited charge are equal. When this condition does not apply, other corrections are required.) This concept is easily applied for dynamic circuits because the collected charge negates the stored charge at a node. However, in the case of CMOS latches and memory cells, a critical charge is more difficult to define because these circuits are sensitive to the *rate at which charge is collected,* and charge collection is modulated by the circuit response. Here critical charge is estimated by considering the circuit's response and integrating only charge collected when the circuit is vulnerable to upset. This approach was taken by Dodd and Sexton (64), who clearly demonstrated the need to differentiate between deposited and collected charge. See Ref. (65) for an excellent review of various error rate prediction methodologies that have been used and recommended approaches.

For error rate calculations, the problem is one of determining the probability that any ion, from the full spectrum of ions available, which has a given LET or greater, passes through the SV at any angle so that it deposits sufficient energy to cause upset. Because flux is isotropic, we must consider all possible path lengths. The longer the path through the sensitive volume, the more energy (charge) is deposited. In other words, with longer path length, ions with lower LET cause upset. Mathematically, error rate is determined from

$$R(E_{\mathrm{C}}) = A_{\mathrm{P}} \int \Phi[L_t(s, E_{\mathrm{C}})] f(s)\, ds \qquad (3)$$

where the integration is performed over the distribution of all path lengths s through the SV. In this equation A_p is the average projected area of the SV, Φ is the LET spectrum for a given environment, L_t is the threshold LET for any path s and Q_C, and $f(s)$ is the distribution of pathlengths through the SV.

This form of the error rate calculation has the following underlying assumptions: (1) the shape of the SV is described by an RPP; (2) ion LET is constant through the SV; (3) track structure can be ignored; (4) charge collection by diffusion from outside the SV can be ignored; (5) the SV is augmented by a funnel length which is invariant with ion LET or energy; (6) all charge generated within the SV is collected; and (7) there is a sharp threshold for upset. Because the measured cross-sectional curve is not a step function but has a gradual rise from an onset threshold, current practice is to integrally weight the error rate based on the measured data. Mathematically, this is described by

$$R = \int R(E) f(E)\, dE \qquad (4)$$

where the integral is performed from the measured onset threshold to saturation, and $f(E)$ is a probability density function that describes the experimental data.

Error rate calculations using Eqs. (3) and (4) are readily performed by using an error rate code, such as CREME96 (66), or a commercially available software package called SPACERAD (67). Both of these codes include the latest environment models, and can include shielding models. The latter also includes utilities that take into account discontinuities that arise in the data set because of the geometry of the SV, as described by Connell et al. (68).

Error rate calculations from proton-induced upset proceed along a different path. Here the measured sensitivity of a part is given as a function of particle energy, so that the error rate is simply the integral of error cross section over the fluence of particles with energy sufficient to cause upset. Mathematically, this is given by

$$R(E) = \int_0^\infty \sigma(E)\Phi(E)\, dE \qquad (5)$$

where $\sigma(E)$ is the error cross section and $\Phi(E)$ is the proton spectrum of the environment. Note that no path length calculation involving and assumed RPP is required because the nuclear reaction of the proton in the SV is assumed to be isotropic and independent of angle. Further, the statistics of the proton interaction are included in the $\sigma(E)$ data. For further information, the reader is referred to Ref. (69).

TOTAL-DOSE IONIZATION EFFECTS

As mentioned in the introduction, MOS devices were first shown to be affected by ionizing irradiation in 1964 (1). In the two decades following this initial work, significant progress was made in understanding the mechanisms for radiation-induced charge buildup in MOS oxides. During this period, it was commonly believed that short-time laboratory irradiations performed at moderate dose rates would overestimate device damage in space caused by charge annealing from long-time space exposures. However, in the mid-1980s it was shown that devices could actually fail at lower dose rates in space than in standard laboratory measurements because of different buildup and annealing rates for the different components of radiation-induced charge. These observations resulted in considerable interest in defining new and better hardness assurance test guidelines for space.

In this section, we review the mechanisms for radiation-induced charge buildup in MOS oxides. The effects of charge buildup in gate, field, and SOI buried oxides on IC performance are described. Mechanisms for the time-dependent buildup and neutralization of radiation-induced charge leading to different failure levels and mechanisms in different radiation environments are highlighted. Techniques for reduc-

ing radiation-induced charge (device hardening) are also discussed.

Basic Mechanisms

As described in the Natural Space and Terrestrial section above, electronics in space systems orbiting the earth are exposed to high fluxes of very energetic particles. These particles include electrons and protons. Although electrons are not important for single-event effects, the electron flux in space causes significant total-dose damage due to ionization effects. Therefore, for total-dose effects, both the flux of electrons and protons must be considered. Manufactured systems, including high-energy particle accelerators and some types of IC processing equipment (e.g., X-ray lithography radiation sources and scanning electron microscopes), can also expose electronics to high ionizing radiation levels.

As a MOS oxide is exposed to high-energy ionizing radiation, electron-hole pairs are created uniformly throughout the oxide. The carriers generated by ionizing irradiation induce buildup of charge in the oxide which leads to device degradation. Figure 15 (70) is a schematic band diagram of a MOS capacitor under positive gate bias and depicts the mechanisms by which ionizing irradiation induces charge buildup in an oxide. Under a positively applied bias, as shown in Fig. 15, radiation-generated holes transport to the Si/SiO_2 interface. Holes are trapped near the interface creating a positive, oxide-trapped charge. As a result of the hole transport and trapping process, hydrogen liberated in the oxide drifts to the Si/SiO_2 interface to form interface traps. The total threshold-voltage shift ΔV_{th} for a transistor is given by the sum of the threshold-voltage shifts due to interface-trap and oxide-trapped charge. Therefore,

$$\Delta V_{\mathrm{th}} = \Delta V_{\mathrm{ot}} + \Delta V_{\mathrm{it}} \tag{6}$$

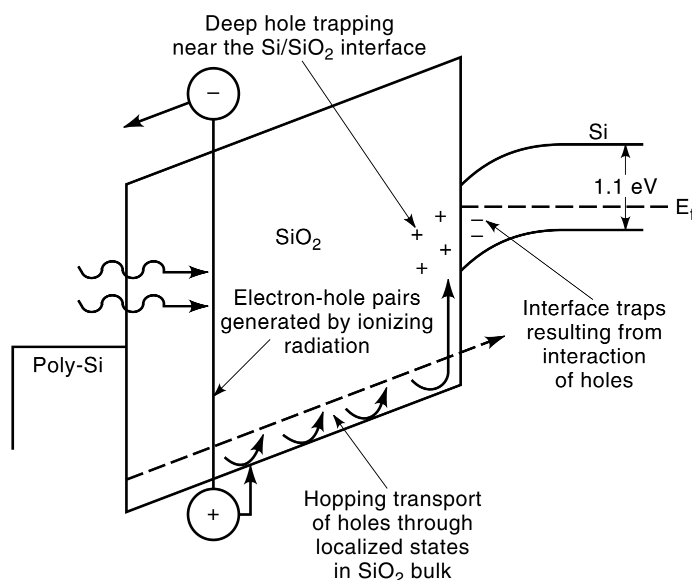


Figure 15. Schematic band diagram of a MOS capacitor under positive bias illustrating the mechanisms for radiation-induced charge buildup. Positive oxide-trapped charge occurs because hole trapping and interface-trap buildup results from the release of hydrogen during the hole transport and trapping process (70).

where ΔV_{ot} and ΔV_{it} are the threshold-voltage shifts due to oxide-trapped and interface-trap charge, respectively. Now the mechanisms for these charge components are discussed in detail.

Oxide-Trapped Charge. Immediately after electron–hole pairs are generated, some fraction of the generated electrons recombine with generated holes. The fraction of electron–hole pairs that escape *initial* recombination is called the electron–hole yield. The electron–hole yield depends on the electric field in the oxide and the energy and type of incident particle (70). For a thermal gate oxide, electrons that escape initial recombination are rapidly swept to the gate electrode (within picoseconds) (71,72) under positive bias, as illustrated in Fig. 15, and do not contribute to radiation-induced charge buildup. Those holes that escape initial recombination move toward the Si/SiO_2 interface at a much slower rate. Holes are believed to transport through the Si/SiO_2 by polaron hopping through localized states in the oxide (73,74). The time that it takes holes to hop through the oxide depends on temperature, electric field, and oxide thickness (73–76).

As the holes reach the vicinity of the Si/SiO_2 interface, some fraction of the holes become trapped in the oxide near the Si/SiO_2 interface. This trapped charge results in a positive charge buildup in the oxide and is called oxide-trapped charge. The positive charge buildup causes a negative, oxide-trapped charge, threshold-voltage shift that is calculated from

$$\Delta V_{\mathrm{ot}} = \frac{-1}{C_{\mathrm{ox}} t_{\mathrm{ox}}} \int_0^{t_{\mathrm{ox}}} \rho(x)\,dx \tag{7}$$

where C_{ox} is the oxide capacitance, t_{ox} is the oxide thickness, and $\rho(x)$ is the spatial distribution of the net charged oxide traps in the oxide. For standard thermal oxides, most of the trapped holes are located close to the Si/SiO_2 interfaces (77). For SOI buried oxides and other specially processed oxides, hole traps are often distributed throughout the bulk of the oxide (78–82).

The microscopic nature of several oxide-trap point defects in thermally grown oxides has been identified by electron paramagnetic resonance experiments (83,84). The most important of these is called the E′ center. At least nine variations of the E′ center have been detected. Most E′ centers are characterized by an unpaired electron highly localized on a silicon atom bonded to three oxygen atoms. The chemical notation for the generic E′ center is given by $\uparrow \mathrm{Si}{\equiv}\mathrm{O}_3$ or $\bullet \mathrm{Si}{\equiv}\mathrm{O}_3$.

Once holes are trapped, they are neutralized by electron tunneling from the silicon (85–88) and by thermal emission of electrons from the oxide valence band (86,89–91). In addition to the neutralization of oxide traps by electron tunneling or thermal emission, oxide-trap charge is also compensated for as electrons are trapped at electron-trap sites associated with the trapped holes. Oxide-trapped charge neutralization occurs over very long periods, from seconds to years. In some cases, the rate of oxide-trapped charge neutralization is relatively large, whereas for some technologies little or no oxide-trapped charge neutralization has been observed. The rate of neutralization by thermal emission of electrons depends on temperature. The rate of neutralization by electron tunneling depends on the distance of the oxide traps from the Si/SiO_2 interface and the electric field in the oxide.

Combining the effects of hole trapping and neutralization, the amount of oxide-trapped charge and its associated threshold-voltage shift ΔV_{ot} are time-dependent. For short periods after a pulse of irradiation, little neutralization of trapped charge occurs and the magnitude of ΔV_{ot} can be very large. For long periods after a pulse of irradiation, considerably more neutralization occurs and the magnitude of ΔV_{ot} may be small. Similarly, for devices exposed to ionizing irradiation in space, where the dose rate is very low, neutralization of oxide-trapped charge occurs constantly during irradiation and ΔV_{ot} may always be small. The time dependence for trapped-hole neutralization at room temperature is illustrated in Fig. 16 (92) where the voltage shift due to oxide-trap charge, ΔV_{ot}, is plotted versus time for hardened n-channel polysilicon gate transistors irradiated to 100 krad(SiO_2) at dose rates from 6×10^9 to 0.05 rad(SiO_2)/s and then annealed at room temperature. The bias during irradiation and annealing was 6 V, and the gate oxide thickness of the transistors was 60 nm. The largest voltage shift (~ -1.45 V) was for short periods after the highest dose rate irradiation. For the lowest dose rate irradiation (0.05 rad(SiO_2)/s), the maximum voltage shift of approximately -0.4 V occurred after irradiating transistors to 100 krad(SiO_2). During annealing, the decrease in ΔV_{ot} follows a logarithmic time dependence. At each dose rate, ΔV_{ot} falls on the same straight line. Thus, the rate at which ΔV_{ot} is neutralized is dose-rate independent.

The fraction of holes trapped and the rate of neutralization depend on processing conditions. The percent of trapped holes varies from a few percent for specially processed hardened oxides to 100% for commercial oxides. One processing step that significantly affects the amount of radiation-induced oxide-trapped charge is the temperature of processing steps after gate oxide deposition (93). Figure 17 illustrates the effect of annealing temperature on oxide-trapped charge buildup. ΔV_{ot} is plotted versus annealing temperature for polysilicon gate capacitors with an oxide thickness of 46 nm irradiated to 1 Mrad(SiO_2). ΔV_{ot} was measured shortly after irradiation. For temperatures above 850°C, increasing annealing temperature results in a large increase in ΔV_{ot}. The cause of the large increase in ΔV_{ot} with increasing temperature is the outward diffusion of oxygen from the oxide during annealing that creates oxide traps (94).

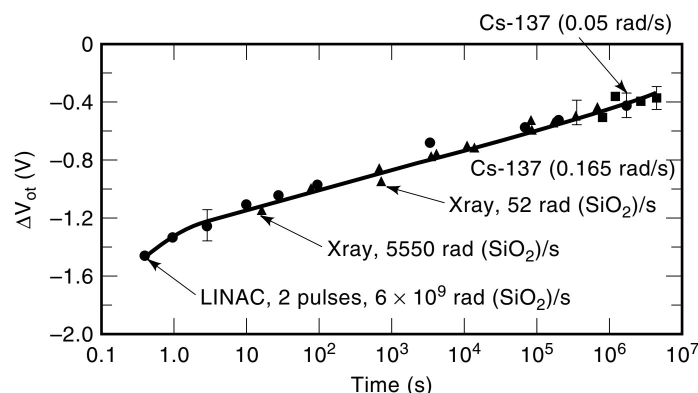


Figure 16. Neutralization of oxide-trapped charge occurs after irradiation, leading to a logarithmic decrease in the magnitude of ΔV_{ot} with time (92).

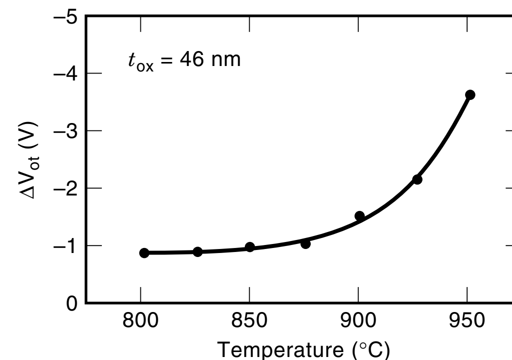
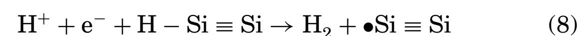


Figure 17. The increase in radiation-induced, oxide-trapped charge voltage shift with the annealing temperature after gate deposition during device fabrication. Processing temperatures above 850°C increase the amount of radiation-induced, oxide-trapped charge (93).

Interface Traps. As holes are trapped near the Si/SiO_2 interface and as holes transport to the interface, H^+ ions are released in the oxide. Under a positive bias as shown in Fig. 15, these hydrogen ions can drift to the Si/SiO_2 interface. Once the H^+ ions reach the interface, they react to form interface traps (95–101). The physical reaction to produce an interface trap is likely (102–104):



$$H^+ + e^- + H - Si \equiv Si \rightarrow H_2 + \bullet Si \equiv Si \tag{8}$$

where $H{-}Si{\equiv}Si$ denotes a silicon atom bonded to one hydrogen atom and backbonded to three silicon atoms and $\bullet Si{\equiv}Si$ denotes a silicon atom with a dangling bond (interface trap). The microscopic structure of the radiation-induced interface trap has been identified by electron paramagnetic resonance measurements as the P_b center (84). A P_b center is a trivalent silicon defect site similar to the E′ center except that the P_b center is backbonded by three silicon atoms.

The magnitude of interface-trap buildup depends on the amount of hydrogen used in ambient gases for annealing and oxidation following gate deposition (105). Fig. 18 is a plot of

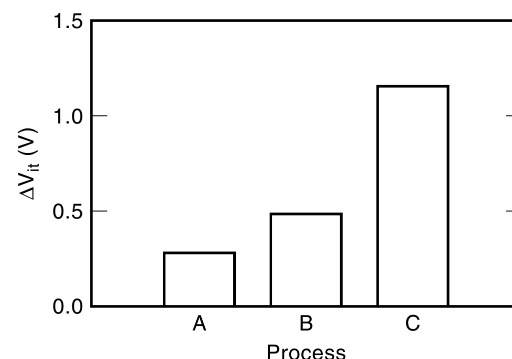


Figure 18. The effect of the amount of hydrogen used in the ambient gases of high-temperature annealing and oxidation following gate deposition during device fabrication on radiation-induced interface-trap charge. Capacitors fabricated using process A were processed using the least amount of hydrogen, and capacitors fabricated using process C were processed using the highest amount of hydrogen. Increasing the amount of hydrogen during device fabrication increases the amount of radiation-induced interface traps (105).

threshold-voltage shift ΔV_{it}, due to interface traps for capacitors fabricated using annealing in ambients containing varying amounts of hydrogen. The capacitors fabricated by process A were processed using the least amount of hydrogen and the capacitors fabricated by process C were fabricated using the greatest amount of hydrogen. The capacitors had an oxide thickness of 101 nm and were irradiated to 100 krad(SiO_2). The capacitors fabricated using the greatest amount of hydrogen had the largest radiation-induced, interface-trap charge, voltage shifts.

Interface traps at the Si/SiO_2 interface are amphoteric and are either donor or acceptor traps. Traps in the upper half of the bandgap typically are acceptors, that is, if the Fermi level at the interface is above the trap energy level, the trap accepts an electron from the silicon and is negatively charged. Acceptor traps are most important for n-channel transistors. Thus, for n-channel transistors, interface traps are predominantly negatively charged. Interface traps in the lower half of the band gap are typically donors, that is, if the Fermi level at the interface is below the trap energy level, the trap donates an electron to the silicon and is positively charged. Donor interface traps are most important for p-channel transistors. Thus, for p-channel transistors, interface traps are predominantly positively charged. If the Fermi level is near midgap, acceptor traps in the upper half of the band gap are empty, donor traps in the lower half of the band gap are filled, and the net interface-trap charge is close to zero. Because interface traps are located at the Si/SiO_2 interface, they rapidly respond to changes in applied bias.

The voltage shift due to interface-trap charge is given by

$$\Delta V_{it} = \frac{-qN_{it}}{C_{ox}} \tag{9}$$

where q is the charge of an electron and N_{it} is the number of charged interface traps. Because interface traps for n-channel transistors are predominantly negatively charged, ΔV_{it} is positive for n-channel transistors. Similarly, interface traps for p-channel transistors are predominantly positively charged and ΔV_{it} is negative for p-channel transistors.

The rate of interface-trap charge buildup depends on the kinetics of hydrogen transport and interaction in the oxide and at the interface. This causes the buildup of interface traps to occur over long periods of time (compared to that of oxide-trapped charge buildup). The saturation of interface-trap buildup can take thousands of seconds to occur. Figure 19 indicates the slow buildup of interface traps following pulses of ionizing irradiation (101). Plotted is the radiation-induced increase in the density of interface traps ΔD_{it}, for capacitors irradiated to 75 krad(Si) using a 10 MeV electron linear accelerator (LINAC) at dose rates from 1.3×10^7 to 1.4×10^9 rad(Si)/s. Capacitors were irradiated using short 10 μs pulses with a repetition rate of 4 Hz. The dose rate is determined from the total dose divided by the total irradiation time. At the highest dose rate, the buildup follows an approximate linear with log time response from 3 s to 3000 s. Interface-trap buildup does not begin to saturate until more than 10^5 s after irradiation. Unlike oxide-trapped charge, interface traps do not undergo neutralization or annealing at room temperature. Thus, the maximum amount of interface-trap buildup occurs after interface-trap buildup is saturated, that is, $>10^5$ s for these capacitors.

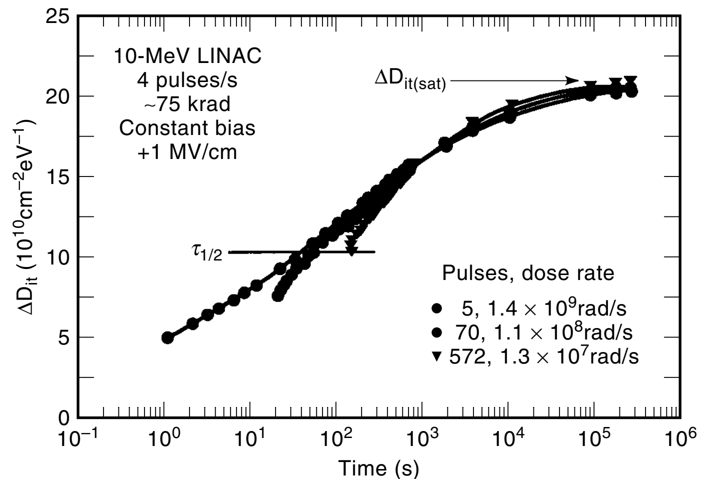


Figure 19. The increase in the density of interface traps following pulses of ionizing irradiation. The buildup of interface traps does not saturate until more than 10^5 s after irradiation for these devices (101).

Total Threshold-Voltage Shift. Recall that for an n-channel transistor, ΔV_{it} is positive and ΔV_{ot} is negative. Therefore, ΔV_{it} and ΔV_{ot} compensate for each other, as seen in Eq. (6). Because the time scales for ΔV_{it} buildup and ΔV_{ot} buildup and neutralization are different, the amount of compensation and hence, ΔV_{th}, is time-dependent. For short periods after a pulse of irradiation, ΔV_{ot} dominates the threshold-voltage shift and ΔV_{th} is large and negative. For long periods after a pulse of irradiation or for low-dose rate exposures (e.g., space), ΔV_{it} may dominate the threshold-voltage shift and ΔV_{th} may be large and positive. For a p-channel transistor, both ΔV_{ot} and ΔV_{it} are negative, they add together, and the radiation-induced threshold-voltage shift is always negative. Figure 20

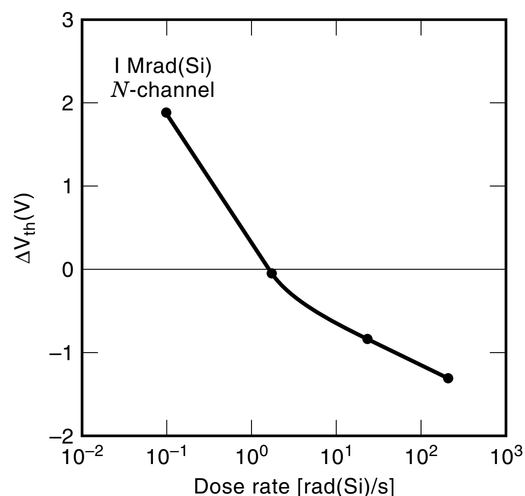


Figure 20. Radiation-induced, n-channel transistor threshold-voltage shift versus dose rate of the radiation source. At high dose rates (short times), the threshold voltage shift is dominated by oxide-trapped charge, and the threshold voltage shift is negative. At low dose rates (long times), the threshold voltage is dominated by interface-trap charge and the threshold-voltage shift is positive (106,107,109).

illustrates the change in ΔV_{th} with time (dose rate) for n-channel transistors (106,107). ΔV_{th} is plotted versus dose rate for transistors irradiated to 1 Mrad(Si). For low dose-rate exposures (long times), interface-trap buildup dominates, and ΔV_{th} is large and positive. For higher dose-rate exposures (shorter times), oxide-trapped charge dominates, and ΔV_{th} is large and negative.

In addition to causing a change in threshold voltage, a buildup of radiation-induced interface traps also decreases carrier mobility. The degradation μ in carrier mobility with interface-trap charge buildup follows the general relationship (108)

$$\mu = \frac{\mu_0}{1 + \alpha \Delta N_{it}} \tag{10}$$

where μ_0 is the preirradiation mobility and α is a constant. Equation 10 is valid under most conditions, except for short periods (<0.1 s) after a pulse of irradiation (109). At short periods after irradiation (~0.01 s), there is a significant concentration of oxide-trapped charge close to the Si/SiO_2 interface which affects, and in some cases dominates, the degradation in mobility. As electrons tunnel from the silicon into the oxide and neutralize oxide charge close to the interface, the effect of charged hole traps on mobility becomes increasingly less important.

Border Traps. Some oxide traps are located close enough to the interface that they exchange charge with the silicon on the time frames of an electrical measurement. These oxide traps act electrically like interface traps but in fact are oxide traps. Oxide traps close to the interface that act electrically like interface traps are called border traps (110). For an oxide trap to behave like a border trap, it must be within ~3 nm of the Si/SiO_2 or gate/SiO_2 interface (70,85,110,111). Note that all oxide traps are likely to act as border traps for oxide thicknesses less than 6 nm (gate oxides of advanced IC technologies).

Circuit Effects

In this section, we describe how the buildup of oxide-trapped and interface-trap charge in different types of oxides affects the performance of MOS ICs. The electrical response of a MOS IC is affected by radiation-induced charge buildup in gate and field oxides. The electrical response of a SOI MOS IC is also affected by radiation-induced charge buildup in the buried oxide and radiation-induced interface-trap and oxide-trapped charge buildup in gate and field oxides. For each type of oxide, the mechanisms for charge buildup are similar to that described previously. For some oxides (e.g., SOI buried oxides), substantial electron trapping also occurs.

The type of oxide that dominates the radiation-induced electrical response depends on processing and design conditions. As late as the early 1980s, gate oxides normally dominated IC response. For these technologies, the gate-oxide thickness was relatively thick, and simple radiation-hardening techniques such as p^+ guard bands (discussed later) were used to isolate transistors. For today's advanced MOS technologies, however, field oxides normally dominate IC response. This is especially true for commercial technologies primarily because of the inherent improvement in gate-oxide hardness as advanced technologies go to thinner gate oxides (discussed later) and because p^+ guard bands (and other simple radiation-hardening transistor isolation techniques) are not compatible with high-density circuits. Whether IC response is dominated by gate or field oxides, however, the time-dependent nature for the buildup and neutralization of oxide-trapped charge and the buildup of interface-trap charge also makes IC response time-dependent. As a result, IC parametric degradation and failure mechanisms depend on the dose and dose rate of the radiation environment.

Gate-Oxide Effects on IC Response. As illustrated in Fig. 20, the radiation-induced, threshold-voltage shift for n-channel transistors is either positive or negative. At high dose rates, the threshold voltage is usually dominated by oxide-trapped charge, and the threshold-voltage shift is negative. As the radiation dose increases, the magnitude of the threshold-voltage shift increases negatively. This results in a dramatic increase in the OFF state leakage current (drain-to-source current I_{DS}, measured at zero gate-to-source voltage V_{GS}) of individual transistors and a large increase in the static power supply current I_{DD} of an IC. If the increase in I_{DD} is high enough, functional failure occurs.

At low dose rates, the threshold voltage is dominated by interface-trap charge. If this is the case, the threshold voltage is large and positive. [Oxide-trapped charge dominates the electrical response even at low dose rates for some technologies (112).] A large, positive, threshold-voltage shift decreases transistor drive. Coupled with a decrease in carrier mobility caused by the increase in number of charged interface traps, the decrease in transistor drive causes degradation in IC timing parameters and potentially causes IC functional failure.

Neutralization of oxide-trapped charge and the buildup of interface-trap charge with time also affect IC electrical performance with time. In short periods after a pulse of radiation, the magnitude of the threshold-voltage shift of a n-channel transistor is at its maximum value, causing the largest increase in I_{DS} (and I_{DD}). The threshold voltage shifts positively as oxide-trapped charge is neutralized. This decreases I_{DS}. Thus, an IC that fails I_{DD} specifications shortly after a pulse of irradiation may pass I_{DD} specifications at longer periods. However, as oxide-trapped charge continues to be neutralized (either at long periods after a pulse of irradiation or during low dose rate exposure) and interface traps continue to build up, at some point transistor response begins to be dominated by interface-trap charge and ICs may begin to fail due to timing-related issues. The change in transistor threshold voltage from negative to positive with time after irradiation is often called the rebound effect (113). To summarize, initially after a pulse of irradiation, ICs may fail due to high leakage currents, in moderate periods after irradiation (or for moderate dose rate exposures) ICs may pass all specifications, and in long periods after irradiation (or for low dose rate exposures) ICs may fail due to timing-related issues. The change in IC parametric and functional behavior with time makes it difficult to predict or assess IC failure in low dose-rate, satellite environments from moderate dose-rate laboratory measurements. Radiation test guidelines have been written to account for rebound effects (114,115).

Optimization of several processing conditions is used to harden gate oxides to total-dose ionizing irradiation. The radiation-induced buildup of both oxide-trap and interface-trap charge decreases with slightly less than a t_{ox}^2 dependence

(107). For thin oxides (<20 nm), the amount of radiation-induced, oxide-trapped charge decreases at an even faster rate. Fortunately, this results in increasing gate-oxide hardness with decreasing oxide thickness. Thus, as commercial technologies advance to thinner gate oxides, the effects of gate oxides on IC radiation hardness become increasingly less important. As mentioned previously, minimizing the temperature of annealing and oxidation and the use of hydrogen after gate deposition also decreases the amount of radiation-induced, oxide-trapped charge and interface-trapped charge, respectively.

Field- or Sidewall-Oxide Effects on IC Response. Radiation-induced charge buildup in field oxides often dominates the total-dose electrical response of commercial IC devices. Field oxides are much thicker than gate oxides and are often processed by a variety of deposition techniques that lead to significant radiation-induced charge trapping. Figure 21 is a cross section of a typical commercial field oxide (116). As radiation-induced, oxide-trapped charge builds up in the field oxide, the positive charge inverts *p*-channel surfaces creating a leakage path between the source and drain of an *n*-channel transistor and between adjacent *n*-channel transistors. If the charge buildup is large enough, large leakage currents result, and a large increase in I_{DD} occurs. Because positive charge buildup causes *n*-type silicon regions to go toward deeper accumulation (turn-off harder), edge leakage is not a problem in *p*-channel transistors. Similar types of increases in leakage current also occur for mesa-etched SOI transistors. The leakage path for sidewall leakage is similar to that for field-oxide leakage described before.

Similar to that for a gate-oxide transistor, field-oxide and sidewall induced leakage current is large at short periods after a pulse of irradiation and then decreases at long periods. For low dose-rate exposures, leakage current may be small at all times because of oxide-trapped charge neutralization. In fact, it is possible for some commercial ICs to fail IC leakage current specifications during moderate dose-rate laboratory radiation testing, but pass IC leakage current specifications during exposure in space. Conversely, ICs that pass laboratory radiation testing may fail at higher dose rates. This makes radiation hardness testing extremely difficult.

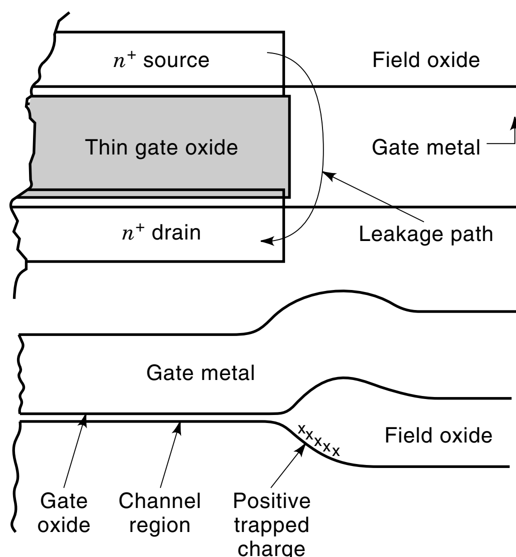


Figure 21. Leakage paths for radiation-induced charge buildup in a field oxide. Radiation-induced, positive-oxide trapped charge inverts underlying *p*-type surfaces causing leakage current to flow from the source to the drain of an *n*-channel transistor (116).

Methods for hardening field and sidewall oxides include processing, layout, and design techniques. Selective implantation is used to heavily dope mesa-etched SOI transistor sidewalls, thereby reducing sidewall leakage current (117–119). Similarly, implanting a p^+ guard band around the edges of an *n*-channel transistor greatly increases the amount of the radiation-induced charge required to invert *p*-channel surfaces and reduce the importance of field oxides. Unfortunately, a p^+ guard band greatly increases the area of a transistor.

Buried-Oxide Effects on IC Response. Buried oxides are inherent in SOI technology and constitute the major difference between the total-dose response between bulk-silicon and SOI devices. Both holes and electrons are trapped in separation by implanted oxygen (SIMOX) buried oxides. Positive charge buildup in the buried oxide near the back-channel silicon interface forms a conducting channel between the source and drain of partially depleted *n*-channel transistors. This increases the OFF state leakage current of *n*-channel transistors similar to that for parasitic field-oxide transistors. The amount of leakage current is only weakly affected by gate bias for partially depleted transistors. Radiation-induced charge buildup has a much stronger effect on fully depleted transistors than on partially depleted transistors. In addition to causing increased leakage current, radiation-induced charge buildup also affects the threshold voltage of fully depleted transistors. Positive oxide-charge buildup in the buried oxide depletes the back-channel interface and decreases the front-channel threshold voltage. The threshold voltage is also affected by the buildup of interface-trap charge at the back-channel/buried oxide interface.

Several methods have been developed to reduce or eliminate the effects of radiation-induced charge buildup in the buried oxide on SOI transistor radiation hardness. One method that completely eliminates buried oxide effects is the use of gate-all-around transistors (120). In these transistors the gate oxide completely surrounds the body region (both top and bottom), and no back channel exists. Variation of implanting and annealing conditions used to form SIMOX SOI substrates is also used to reduce radiation-induced charge buildup. For example, buried oxides formed using supplemental implant (121–123) and multiple implanting and annealing (124) show less radiation-induced degradation than buried oxides formed with a single implant and annealing. Supplemental implant wafers are formed by implanting wafers to approximately the desired level and then reimplanting the wafers using a small additional dose. Multiple implant wafers are formed by implanting wafers in incremental steps and annealing the wafers at high temperature after each step. Methods that modify the back-channel have also been used to reduce the effect of the buried oxide on radiation hardness. One simple method that is commonly used is increasing the back-channel doping near the back-channel/buried oxide interface, making it more difficult to invert the back-channel interface (125–127).

SUMMARY AND CONCLUSIONS

The harsh environment of space causes significant degradation to electronics and can lead to system failure. The types of degradation range from permanent failure due to total-dose ionizing irradiation and single-event hard errors to temporary loss of information caused by single-event upsets. The mechanisms for degradation and failure levels depend on many factors including device type, system design and application, and radiation environment.

As IC technologies continue to advance, they are more susceptible to terrestrial radiation-induced effects. Terrestrial irradiation causes single-event upsets in advanced IC devices reducing their reliability. Methods for hardening ICs to single-event effects have been known for a long time. However, most of these techniques require implementing circuit and/or device changes that degrade IC electrical performance and/or yield and are not suitable for high-performance commercial devices. Thus, new techniques or other IC technologies (e.g., SOI) are required to reduce the effects of terrestrial irradiation on IC reliability.

IC response to ionizing radiation has a complex time dependence. The time dependence of oxide-trapped charge buildup and neutralization and the buildup of interface traps make it difficult to ensure device hardness in space environments on the basis of laboratory measurements. Considerable work has been done to improve radiation hardness assurance test guidelines, and now test guidelines are available that account for time-dependent, radiation-induced charge buildup. Still, more work needs to be done to increase understanding of the mechanisms for charge buildup and device degradation so as to further improve hardness assurance test guidelines, especially for device types that exhibit nonstandard MOS radiation-induced behavior (e.g., bipolar devices).

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BIBLIOGRAPHY

1. H. L. Hughes and R. A. Giroux, *Electronics,* **37**: 58, 1964.
2. D. Binder, E. C. Smith, and A. B. Holman, *IEEE Trans. Nucl. Sci.,* **NS-2**: 2675–2690, 1975.
3. E. W. Enlow et al., *IEEE Trans. Nucl. Sci.,* **NS-38**: 1342–1351, 1991.
4. D. M. Schmidt et al., *IEEE Trans. Nucl. Sci.,* **NS-42**: 1541–1549, 1995.
5. R. D. Schrimpf, *IEEE Trans. Nucl. Sci.,* **NS-43**: 787–796, 1996.
6. D. M. Fleetwood et al., *IEEE Trans. Nucl. Sci.,* **NS-43**: 2537–2546, 1996.
7. R. N. Nowlin et al., *IEEE Trans. Nucl. Sci.,* **NS-39**: 2026–2035, 1992.
8. D. M. Schmidt et al., *IEEE Trans. Nucl. Sci.,* **NS-43**: 3032–3039, 1996.
9. J. F. Ziegler, in J. F. Ziegler (ed.), *The Stopping and Ranges of Ions in Matter,* New York: Pergamon, 1980, p. 6.
10. J. Barth, in N. Van Vonno (ed.), *IEEE Nuclear and Space Radiation Effects Conference Short Course,* New York: IEEE, 1997.
11. R. A. Mewaldt, *Proc. Interplanet. Part. Environ.* , Pasadena, CA, 1987, pp. 121–132; available as *JPL Publ.* **88-28**: 1988.
12. J. H. Adams, Jr., R. Silberberg, and C. H. Tsao, *NRL Memo. Rep. 4506:* 1981.
13. J. Feynman and S. B. Gabriel, *IEEE Trans. Nucl. Sci.,* **NS-43**: 344–352, 1996.
14. M. S. Gussenhoven, E. G. Mullen, and D. H. Brautigam, *IEEE Trans. Nucl. Sci.,* **NS-43**: 353–368, 1996.
15. M. A. Xapsos et al., *IEEE Trans. Nucl. Sci.,* **NS-43**: 2772–2777, 1996.
16. D. V. Rheames, *Rev. Geophys., Suppl.,* **33**: 585, 1995.
17. Solar Wind.
18. J. H. Adams, Jr., *IEEE Trans. Nucl. Sci.,* **NS-29**: 2095–2100, 1982.
19. E. L. Petersen, *IEEE Trans. Nucl. Sci.,* **NS-43**: 2805–2813, 1996.
20. J. H. Adams, Jr., *IEEE Trans. Nucl. Sci.,* **NS-30**: 4475–4480, 1983.
21. J. F. Ziegler, *IBM J. Res. Develop.,* **40**: 19–39, 1996.
22. A. Taber and E. Normand, *IEEE Trans. Nucl. Sci.,* **NS-40**: 120, 1993.
23. C. Lage et al., *Proc. IEDM,* 1993, pp. 821–824.
24. T. C. May and M. H. Woods, *IEEE Trans. Electron Devices,* **ED-26**: 2–9, 1978.
25. J. C. Pickel and J. T. Blandford, Jr., *IEEE Trans. Nucl. Sci.,* **NS-25**: 1166–1171, 1978.
26. C. S. Guenzer, E. A. Wolicki, and R. G. Allas, *IEEE Trans. Nucl. Sci.,* **NS-26**: 5048, 1979.
27. E. L. Petersen and P. W. Marshall, *J. Radiat. Eff.: Res. Eng.,* **6**: 1–23, 1988.
28. E. Normand, *IEEE Trans. Nucl. Sci.,* **NS-43**: 2742–2750, 1996.
29. E. Normand, *IEEE Trans. Nucl. Sci.,* **NS-43**: 461–474, 1996.
30. A. Johnston, *4th Eur. Conf. Radiat. Their Eff. Devices Syst.,* Cannes, France, 1997.
31. C. M. Hsieh, P. C. Murley, and R. R. O'Brien, *IEEE Electron Devices Lett.,* **EDL-2** (4): 103–105, 1981.
32. F. B. McLean and T. R. Oldham, *IEEE Trans. Nucl. Sci.,* **NS-29**: 2018–2023, 1982; T. R. Oldham and F. B. McLean, *IEEE Trans. Nucl. Sci.,* **NS-30**: 4493–4500, 1983.
33. P. E. Dodd, F.W. Sexton, and P. S. Winokur, *IEEE Trans. Nucl. Sci.,* **NS-41**: 2005–2017, 1994.
34. S. Kirkpatrick, *IEEE Trans. Electron Devices,* **ED-26**: 1742–1753, 1979.
35. J. R. Hauser et al., *IEEE Trans. Nucl. Sci.,* **NS-32**: 4115–4121, 1985.
36. F. W. Sexton et al., *IEEE Trans. Nucl. Sci.,* **NS-37**: 1861–1868, 1990.
37. P. E. Dodd et al., *IEEE Trans. Nucl. Sci.,* **NS-43**: 2797–2804, 1996.
38. L. W. Massengill et al., *IEEE Trans. Nucl. Sci.,* **NS-40**: 1804–1819, 1993.
39. L. W. Connell, F. W. Sexton, and A. K. Prinja, *IEEE Trans. Nucl. Sci.,* **NS-42**: 2026–2034, 1995.
40. L. W. Massengill, *IEEE Trans. Nucl. Sci.,* **NS-32**: 577–593, 1996.
41. H. T. Weaver et al., *IEEE Trans. Nucl. Sci.,* **NS-43**: 1281–1286, 1987.
42. J. A. Zoutendyk, L. D. Edmonds, and L. S. Smith, *IEEE Trans. Nucl. Sci.,* **NS-36**: 2267–2274, 1989.

43. J. S. Chern et al., *IEEE Trans. Electron Devices,* **ED-33**: 822–834, 1996.
44. B. L. Gregory and B. D. Shafer, *IEEE Trans. Nucl. Sci.,* **NS-30**: 293, 1979.
45. F. N. Coppage and D. C. Evans, *IEEE Trans. Nucl. Sci.,* **NS-24**: 2226, 1977.
46. A. H. Johnston and B. W. Hughlock, *IEEE Trans. Nucl. Sci.,* **NS-37**: 1886–1893, 1990.
47. A. H. Johnston, *IEEE Trans. Nucl. Sci.,* **NS-43**: 505–521, 1996.
48. T. F. Wrobel, *IEEE Trans. Nucl. Sci.,* **NS-34**: 1262–1268, 1987.
49. C. F. Wheatley, J. L. Titus, and D. I. Burton, *IEEE Trans. Nucl. Sci.,* **NS-41**: 2152–2159, 1994.
50. F. W. Sexton et al., *IEEE Trans. Nucl. Sci.,* **NS-44**: 2345–2352, 1997.
51. J. R. Brews et al., *IEEE Trans. Nucl. Sci.,* **NS-40**: 1959–1966, 1993.
52. J. H. Hohl and K. F. Galloway, *IEEE Trans. Nucl. Sci.,* **NS-34**: 1275–1280, 1987.
53. A. E. Waskiewicz et al., *IEEE Trans. Nucl. Sci.,* **NS-33**: 1710–1713, 1986.
54. T. A. Fischer, *IEEE Trans. Nucl. Sci.,* **NS-34**: 1786–1791, 1987.
55. T. F. Wrobel et al., *IEEE Trans. Nucl. Sci.,* **NS-32**: 3991–3995, 1985.
56. A. Ochoa, Jr. et al., *IEEE Trans. Nucl. Sci.,* **NS-30**: 4127–4134, 1983.
57. R. Koga and W. A. Kolasinki, *IEEE Trans. Nucl. Sci.,* **NS-36**: 2367–2374, 1989.
58. E. L. Petersen, *IEEE Trans. Nucl. Sci.,* **NS-28**: 3981–3986, 1981.
59. C. L. Chen and M. Y. Hsiao, *IBM J. Res. Develop.,* **28**: 124–134, 1984.
60. S. Karp and M. K. Gilbert, *IEEE Trans Aerosp. Electron. Syst.,* **29**: 310–316, 1993.
61. A. E. Giddings et al., *IEEE Trans. Nucl. Sci.,* **NS-32**: 4159–4163, 1985.
62. L. R. Rockett, Jr., *IEEE Trans. Nucl. Sci.,* **NS-35**: 1682–1687, 1988.
63. F. W. Sexton et al., *IEEE Trans. Nucl. Sci.,* **NS-37**: 1861–1868, 1990.
64. P. E. Dodd and F. W. Sexton, *IEEE Trans. Nucl. Sci.,* **NS-42**: 1764–1771, 1995.
65. J. C. Pickel, *IEEE Trans. Nucl. Sci.,* **NS-43**: 483–495, 1996.
66. A. J. Tylka et al., *IEEE Trans. Nucl. Sci.,* **NS-44**: 2150–2160, 1997.
67. SPACERAD is a trademark of the Space Radiation Associates, 1430 Willamette Street, Suite 1, Eugene, OR 97401.
68. L. W. Connell et al., *IEEE Trans. Nucl. Sci.,* **NS-42**: 73–82, 1995.
69. E. L. Petersen, *IEEE Trans. Nucl. Sci.,* **NS-43**: 496–504, 1996.
70. F. B. McLean, H. E. Boesch, Jr., and T. R. Oldham, in T. P. Ma and P. V. Dressendorfer (eds.), *Ionizing Radiation Effects in MOS Devices and Circuits,* New York: Wiley, 1989, pp. 87–192.
71. R. C. Hughes, *Appl. Phys. Lett.,* **26**: 436–438, 1975.
72. R. C. Hughes, *Phys. Rev. Lett.,* **30**: 1333–1336, 1973.
73. F. B. McLean and G. A. Ausman, Jr., *Phys. Rev. B,* **15**: 1052–1061, 1977.
74. F. B. McLean and G. A. Ausman, Jr., *J. Appl. Phys.,* **47**: 1529–1532.
75. H. E. Boesch, Jr., J. M. McGarrity, and F. B. McLean, *IEEE Trans. Nucl. Sci.,* **NS-25**: 1012–1016, 1978.
76. H. E. Boesch, Jr. et al., *IEEE Trans. Nucl. Sci.,* **NS-25**: 1239–1245, 1978.
77. P. M. Lenahan and P. V. Dressendorfer, *J. Appl. Phys.,* **55**: 3495–3499, 1984.
78. H. E. Boesch, Jr. et al., *IEEE Trans. Nucl. Sci.,* **NS-37**: 1982–1989, 1990.
79. C. A. Pennise and H. E. Boesch, Jr., *IEEE Trans. Nucl. Sci.,* **NS-37**: 1990–1994, 1990.
80. H. E. Boecsh, Jr., T. L. Taylor, and G. A. Brown, *IEEE Trans. Nucl. Sci.,* **NS-38**: 1234–1239, 1991.
81. C. A. Pennise and H. E. Boesch, Jr., *IEEE Trans. Nucl. Sci.,* **NS-38**: 1240–1246, 1991.
82. R. E. Stahlbush et al., *IEEE Trans. Nucl. Sci.,* **NS-39**: 2086–2097, 1992.
83. P. M. Lenahan and P. V. Dressendorfer, *IEEE Trans. Nucl. Sci.,* **NS-29**: 1459–1461, 1982.
84. P. M. Lenahan and P. V. Dressendorfer, *IEEE Trans. Nucl. Sci.,* **NS-30**: 4602–4604, 1983.
85. T. R. Oldham, A. J. Lelis, and F. B. McLean, *IEEE Trans. Nucl. Sci.,* **NS-33**: 1203–1209, 1986.
86. P. J. McWhorter, S. L. Miller, and W. M. Miller, *IEEE Trans. Nucl. Sci.,* **NS-37**: 1682–1689, 1990.
87. S. Manzini and A. Modelli, in J. F. Verweij and D. R. Wolters (eds.), *Insulating Films on Semiconductors,* Amsterdam: Elsevier/North-Holland, 1983, pp. 112–115.
88. M. Schmidt and K. Koster, Jr., *Phys. Status Solidi B,* **174** (1): 53–66, 1992.
89. G. F. Derbenwick and H. H. Sanders, *IEEE Trans. Nucl. Sci.,* **NS-24**: 2244–2247, 1977.
90. P. J. McWhorter, S. L. Miller, and T. A. Dellin, *J. Appl. Phys.,* **68**: 1902–1909, 1990.
91. B. Ballard and G. Barbottin, *Instabilities in Silicon Devices,* Vol. 2, New York: Elsevier, 1989, p. 32.
92. D. M. Fleetwood, P. S. Winokur, and J. R. Schwank, *IEEE Trans. Nucl. Sci.,* **NS-35**: 1497–1505, 1988.
93. J. R. Schwank and D. M. Fleetwood, *Appl. Phys. Lett.,* **53**: 770–772, 1988.
94. W. L. Warren et al., *IEEE Trans. Nucl. Sci.,* **NS-41**: 1817–1827, 1994.
95. C. M. Svensson, in S. T. Pantelides (ed.), *The Physics of SiO_2 and Its Interfaces,* Elmsford, NY: Pergamon, 1978, pp. 328–332.
96. F. B. McLean, *IEEE Trans. Nucl. Sci.,* **NS-27**: 1651–1657, 1980.
97. N. S. Saks, R. B. Klein, and D. L. Griscom, *IEEE Trans. Nucl. Sci.,* **NS-35**: 1234–1240, 1988.
98. N. S. Saks and D. B. Brown, *IEEE Trans. Nucl. Sci.,* **NS-37**: 1624–1631, 1990.
99. N. S. Saks and R. W. Rendell, *IEEE Trans. Nucl. Sci.,* **NS-39**: 2220–2228, 1992.
100. M. R. Shaneyfelt et al., *IEEE Trans. Nucl. Sci.,* **NS-37**: 1632–1639, 1990.
101. M. R. Shaneyfelt et al., *IEEE Trans. Nucl. Sci.,* **NS-39**: 2244–2251, 1992.
102. D. L. Griscom, *J. Appl. Phys.,* **58**: 2524–2533, 1985.
103. N. S. Saks, D. B. Brown, and R. W. Rendell, *IEEE Trans. Nucl. Sci.,* **NS-38**: 1130–1139, 1991.
104. D. L. Griscom, *J. Electron. Mater.,* **21**: 763–767, 1992.
105. J. R. Schwank et al., *IEEE Trans. Nucl. Sci.,* **NS-34**: 1152–1158, 1987.
106. P. S. Winokur et al., *IEEE Trans. Nucl. Sci.,* **NS-33**: 1343–1351, 1986.
107. J. R. Schwank, in L. W. Massengill (ed.), *1994 IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1994, pp. ii, 62.
108. F. W. Sexton and J. R. Schwank, *IEEE Trans. Nucl. Sci.,* **NS-32**: 3975–3981, 1985.
109. F. B. McLean and H. E. Boesch, Jr., *IEEE Trans. Nucl. Sci.,* **NS-36**: 1772–1783, 1989.

110. D. M. Fleetwood, *IEEE Trans. Nucl. Sci.,* **NS-39**: 269–271, 1992.
111. J. M. Benedetto et al., *IEEE Trans. Nucl. Sci.,* **NS-32**: 3916–3920, 1985.
112. D M. Fleetwood, P. S. Winokur, and T. L. Meisenheimer, *IEEE Trans. Nucl. Sci.,* **NS-38**: 1552–1559, 1991.
113. J. R. Schwank et al., *IEEE Trans. Nucl. Sci.,* **NS-31**: 1434–1438, 1984.
114. D. M. Fleetwood et al., *IEEE Trans. Nucl. Sci.,* **NS-36**: 1963–1970, 1989.
115. D. M. Fleetwood et al., *Radiat. Phys. Chem.,* **43** (1/2): 129–138, 1994.
116. T. R. Oldham et al., *IEEE Trans. Nucl. Sci.,* **NS-34**: 1184–1189, 1987.
117. M. Haond and O. LeNeel, *Solid State Technol.,* **34**: 47–52, 1991.
118. L. S. Napoli et al., *IEEE Trans. Nucl. Sci.,* **NS-29**: 1707–1711, 1982.
119. J. L. Leray, *Microelectron. Eng.,* **8** (3/4): 187–200, 1988.
120. J. P. Colinge et al., *Proc. IEDM,* 1990, pp. 595–599.
121. R. J. Lambert, T. N. Bhar, and H. L. Hughes, *Appl. Phys. Lett.,* **64**: 3291–3292, 1994.
122. R. E. Stahlbush, H. L. Hughes, and W. A. Krull, *IEEE Trans. Nucl. Sci.,* **NS-40**: 1740–1747, 1993.
123. H. E. Boesch, Jr., T. L. Taylor, and W. A. Krull, *IEEE Trans. Nucl. Sci.,* **NS-40**: 1748–1754, 1993.
124. S. Cristoloveanu et al., *2nd Eur. Conf. Radiat. Their Eff. Devices Syst.,* 1993, pp. 373–377.
125. J. L. Levy et al., *IEEE Trans. Nucl. Sci.,* **NS-35**: 1355–1360, 1988.
126. G. E. Davis et al., *IEEE Trans. Nucl. Sci.,* **NS-32**: 4432–4437, 1985.
127. B.-Y. Tsaur et al., *IEEE Electron Devices Lett.,* **EDL-3**: 195–197, 1982.

Reading List

D. B. Brown (ed.), *IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1991.

D. M. Fleetwood and R. Gaillard (eds.), *IEEE Trans. Nucl. Sci.,* **NS-43**: 1996.

IEEE Transactions on Nuclear Science, December issues.

A. H. Johnston (ed.), *IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1993.

T. P. Ma and P. V. Dressendorfer (eds.), *Ionizing Radiation Effects in MOS Devices and Circuits,* New York: Wiley, 1989.

L. W. Massengill (ed.), *IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1994.

R. L. Pease (ed.), *IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1996.

J. C. Pickel (ed.), *IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1998.

J. R. Schwank (ed.), *IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1995.

F. W. Sexton (ed.), *IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1992.

N. Van Vonno (ed.), *IEEE Nuclear Space Radiation Effects Conf. Short Course,* New York: IEEE, 1997.

J. F. Ziegler and G. R. Srinivasan (eds.), *IBM J. Res. Develop.,* **40** (1): 1996.

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