SCHOTTKY BARRIERS

The Schottky barrier, one of the earliest and simplest semiconductor interfaces studied, consists of a metal in contact with a semiconductor. It is named after Walter Schottky, who in the 1930s developed a comprehensive theory of such contacts, and traced their properties to the electrical barrier that forms at the metal–semiconductor (MS) interface. If the barrier height is relatively large, the current–voltage (*I*–*V*) characteristics exhibit an asymmetrical rectifying behavior, while a symmetrical linear *I*–*V* response results from a low barrier. The rectifying MS contact is called the Schottky diode, whereas the nonrectifying device is simply referred to as an ohmic contact.

The first observation of asymmetrical conduction in solids was made by Ferdinand Braun in 1874, when he studied the properties of metal contacts to metallic sulfides (later identified as semiconductors). The subsequent advent and rapid growth of radio communication led to widespread use of these contacts as “point contact” diode detectors. These naturally occurring semiconducting minerals suffered from high levels and variable distribution of impurities, which made the devices rather unreliable. Reproducible, high-quality MS interfaces had to await the post-World War II development of synthesized semiconductors of extremely high purity (such as Ge and Si) and the use of vacuum deposition techniques. Exhaustive studies of an enormous assortment of metal-semiconductor contacts over the past four decades have led to a better—though still incomplete—understanding of the mechanism of barrier formation. Other phenomena (such as carrier transport) are well understood, and Schottky contact technologies may be considered mature for most semiconductors.

Due to its inherent high speed, the Schottky diode is widely used in micro- and millimeter-wave detection and mixing, while the Schottky interface itself is a key element in important amplifying devices such as the MEtal Semiconductor Field Effect Transistors (MESFET) and the more recent heterostructure FET (HFET), as well as in a variety of radiation detectors. Commonly used metals generally form high barriers on *n*-type semiconductors, and this is also the usually desired situation in devices due to the higher mobility of elec-

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trons. The ohmic contact with negligible voltage drop across itself is essential for all external and internal connections to the elements of semiconductor devices; the theory of the Schottky barrier is also of relevance to the choice of metals for ohmic contacts.

THEORY OF SCHOTTKY BARRIER FORMATION

It is important to distinguish between two different types of MS interfaces: (1) those prepared on semiconductor surfaces freshly formed (by cleaving, or sputtering and annealing, or in-situ epitaxy) in ultrahigh vacuum (UHV, with pressures $< 10^{-10}$ torr) and, hence, unexposed to the ambient; and (2) those prepared on chemically etched surfaces with the metallization done under simple high vacuum (pressure $\approx 10^{-6}$ torr). The former are of great importance in basic studies of Schottky barrier formation. These involve mono- and submonolayer coverage of the metal on freshly cleaved semiconductor surfaces and in-situ evaluation of the barrier height as well as microscopic interactions between the metal and the semiconductor through sophisticated surface analytical tools. All practical Schottky barriers are formed on chemically etched surfaces and result in extremely reproducible electrical characteristics. Regardless of the specific MS interface, it turns out that the same physical models generally apply. This is true even for the special case of reacted metal-semiconductor contacts such as between metallic silicides and silicon. The silicide Schottky barriers are of interest from both fundamental and practical viewpoints, as the MS interface here is buried inside the semiconductor bulk, thus obviating the deleterious influence of surface oxides and other contamination.

We will consider here two basic models, the earlier one due to Schottky and the later one inspired by Bardeen's postulation of the surface states. Exhaustive reviews of the physical models and experimental data on the Schottky barrier may be found in Refs. 1–3.

THE INTIMATE SCHOTTKY CONTACT MODEL

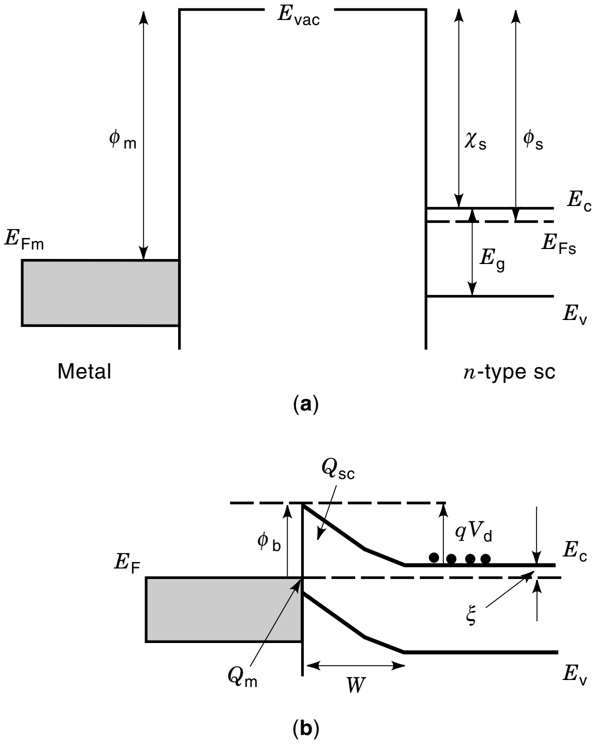

Figure 1. Electron energy band diagram of a metal and an n-type semiconductor under thermal equilibrium; (a) before contact and (b) after contact. The work function of the metal ϕ_{m} is assumed to be greater than the semiconductor electron affinity χ_{s}.

This model, originally proposed by Schottky as well as Mott, assumes an intimate interface between the metal and the semiconductor with no interfacial layer between the two. Consider a metal with work function ϕ_{m} greater than the electron affinity χ_{s} of an n-type semiconductor. Figure 1 (a) shows the electron energy line-up in the metal and the semiconductor before contact. When the contact is made [Fig. 1 (b)], the work function (or, equivalently, electronegativity) difference forces a momentary net flow of electrons from the semiconductor to the metal until the MS system as a whole reaches thermal equilibrium with a single constant Fermi energy E_{F}. The consequences of this process are twofold: (1) an energy barrier ϕ_{b} separating the electrons in the metal from the empty conduction band states of the semiconductor at the interface; and (2) a space charge or depletion region of width W on the semiconductor side of the interface. The electrical properties of the Schottky barrier arise principally from this space charge layer. The positive charge in the latter (Q_{sc}), consisting of ionized donors, compensates the negative electron charge in the metal (Q_{m}). Correspondingly, the space charge region develops a band bending qV_{d} in a manner similar to that in a p–n junction. From Fig. 1, the Schottky barrier height $\phi_{\text{b}}^{\text{n}}$ and (zero-bias) band bending qV_{d} or diffusion potential V_{d} are readily shown to be

$$\phi_{\text{b}}^{\text{n}} = \phi_{\text{m}} - \chi_{\text{s}} \tag{1}$$

$$qV_{\text{d}} = \phi_{\text{m}} - \phi_{\text{s}} \tag{2}$$

The space region width W is given by

$$W = [2\epsilon_{\text{s}} V_{\text{d}}/qN_{\text{D}}]^{1/2} \tag{3}$$

where ϵ_{s} is the dielectric permittivity of the semiconductor, q the electron charge, magnitude, and N_{D} the bulk donor concentration.

It is possible to form Schottky barriers on p-type semiconductors also, in which case we need $\phi_{\text{m}} < \phi_{\text{s}}$, and the Schottky barrier height $\phi_{\text{b}}^{\text{p}}$ (for holes, measured from E_{Fm} to E_{v} at the interface) becomes

$$\phi_{\text{b}}^{\text{p}} = E_{\text{g}} + \chi_{\text{s}} - \phi_{\text{m}} \tag{4}$$

Equations (1) and (4) predict a linear dependence of barrier height on metal work function, with a slope parameter $S_{\phi} = |d\phi_{\text{b}}/d\phi_{\text{m}}|$ equal to unity. However, experimental values of S_{ϕ} are significantly less than unity for most semiconductors, thus requiring a more elaborate model postulating the presence of an interfacial layer *and* interfacial charge. The first proposal for the interfacial charge was made by Bardeen, who recognized that the discontinuity of the crystal lattice at the surface would give rise to surface states or traps located physically at the semiconductor surface and energetically within the bandgap.

Addition of Eqs. (1) and (4) yields the relation

$$\phi_b^n + \phi_b^p = E_g \tag{5}$$

for any metal-semiconductor combination. While Eqs. (1) and (4) invariably fail to describe experimental results on Schottky barriers, the Schottky barrier heights of similarly prepared contacts on n-type and p-type semiconductors often add up to the bandgap as given by Eq. (5) for a variety of semiconductors and metals.

The MIS Schottky Contact Model

The MIS Schottky model incorporates the following changes to the intimate Schottky contact model: (1) an (ultrathin, tunnelable) interfacial layer (I) of thickness δ between the metal and the semiconductor; and (2) interface traps of density D_{it} (cm^{-2} eV^{-1}) located at the IS interface and with occupancy controlled by the metal Fermi energy E_{Fm}. By Gauss's law, a surface charge density Q_{it} in the interface traps would give rise to a potential (Δ/q) across the I-layer as shown in Fig. 2. The resulting realignment of the semiconductor band bending then alters the barrier height, making it less dependent on the metal work function. In view of the electrical transparency of the I-layer, note that the Schottky barrier height is still given by the difference between the semiconductor conduction band edge at the surface and the Fermi energy in the metal. With the additional source of charge, the charge neutrality condition becomes

$$Q_m + Q_{it} + Q_{sc} = 0 \tag{6}$$

It is convenient to define a "neutral level" ϕ_o for the interface traps, such that the net interface trap charge Q_{it} is zero when E_{Fm} lies at ϕ_o. From the band diagram of Fig. 2, using Gauss's law and a few simplifying assumptions, it can be shown (see Ref. 2, p. 20) that

$$\phi_b^n = \gamma(\phi_m - \chi_s) + (1-\gamma)(E_g - \phi_0) \tag{7}$$

where $\gamma = \epsilon_i/(\epsilon_i + q\delta D_{it})$. Now the slope parameter $S_\phi = \gamma < 1$, and decreases monotonically with increase in the interface trap density D_{it} and interface layer thickness δ. In the extreme case when $(\delta D_{it}) \rightarrow \infty$, $\phi_b^n = (E_g - \phi_o)$ = constant, independent of the metal work function ϕ_m—the so-called Bardeen limit. This situation is also referred to as (surface) Fermi level pinning, because E_{Fn} is now pinned to the neutral level ϕ_o of the interface traps. If, on the other hand, $(\delta D_{it}) \rightarrow 0$, then Eq. (4) reduces to Eq. (1), which applies to the (intimate) Schottky limit.

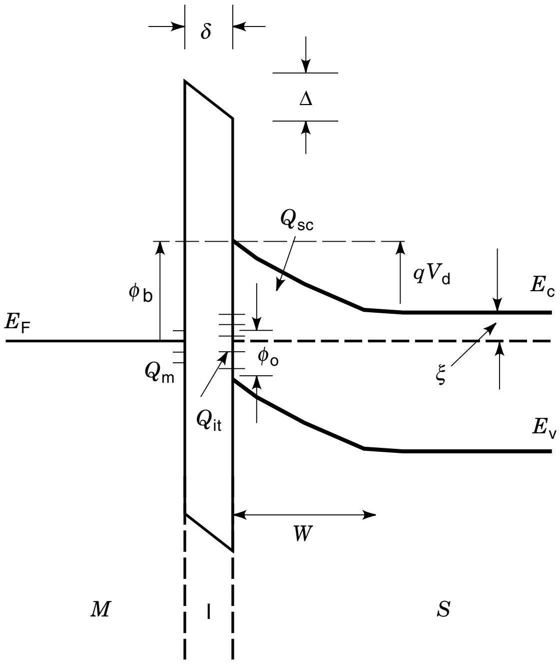

Figure 2. Electron energy band diagram for the MIS Schottky model under thermal equilibrium, with an ultrathin, tunnelable interfacial layer I.

If we use an upper limit of δ = 20 Å for a good Schottky diode and assume an $\epsilon = 4\,\epsilon_o$, the Bardeen limit is approached for $D_{it} \gtrsim 10^{13}$ cm^{-2} eV^{-1}. Using a surface atomic density of 10^{15} cm^{-2} for a solid, this corresponds to about one interface trap for every 100 surface atoms. Such a high level of interface trap density contrasts with $D_{it} < 10^{10}$ cm^{-2} eV^{-1} obtained for the high-quality thermal SiO_2/Si interface used in Si MOS technology.

Experimental verification of Eq. (7) requires deposition of metals of widely differing work function on identically prepared samples, rather than compiling data reported by different authors in the literature. Such studies on Si have yielded a γ in the range 0.15–0.22 depending evidently on surface preparation (4). However, phenomena such as metal–semiconductor reaction, interfacial strain, and aging effects could profoundly influence the MS interface, so strict adherence of relations such as Eq. (7) should not be expected for all metal–semiconductor combinations. The principal success of the model is in explaining semiquantitatively those trends observed in measurements.

An expression similar to that in Eq. (7) can be derived for the MIS Schottky barrier on a p-type semiconductor, and again ϕ_b^n and ϕ_b^p add up to the bandgap E_g of the semiconductor as with the intimate Schottky model [see Eq. (5)]. Experimental data on a number of semiconductors confirm this trend (Ref. 2, section 2). Thus a high barrier height on an n-type semiconductor implies a low barrier on the p-type. A practical conclusion from the MIS Schottky model, as with the intimate Schottky model, is that high barrier heights require metals of large work function for n-type materials and small work function metals for p-type materials. Measured barrier heights are typically in the range 0.6 eV–0.8 eV for n-type Si, and 0.75 eV–0.95 eV for n-type GaAs. Clearly, the higher the bandgap E_g the higher will be the expected Schottky barrier height.

The stipulation of the I-layer in this model is a logical one for Schottky barriers formed on chemically etched semiconductor surfaces. Most semiconductors form a native insulating oxide, 10 Å–20 Å thick, on inevitable exposure to room ambient before the samples are introduced into the vacuum chamber for metallization. The MIS model, however, could also be applied to UHV-prepared intimate contacts because an atomic level separation between Q_m and Q_{it} is all that is needed to simulate the I-layer; here the two sheet charges essentially constitute an atomic dipole.

The origin of the interface traps has been a subject of some controversy over the years, with at least two distinct schools of thought: (1) The unified defect model, where the surface Fermi level is pinned at discrete acceptor- and donor-like defect states induced by the metal deposition; and (2) the continuum metal induced gap states (MIGS) that arise from the decay of the metal electron wavefunctions into the semiconductor, as originally proposed by Heine in 1965. Recent studies of both UHV and chemically etched samples appear to favor the MIGS theory although some anomalies persist, requiring an additional secondary mechanism of metal deposition-induced defect states. These issues have been reviewed at length by Mönch (3,5).

The MIS Schottky model is most effective in giving a qualitative explanation for the observed weak dependence of barrier height on the metal work function. Quantitative, predictive interpretations using Eq. (7) are beset not merely by second-order phenomena, such as metal-semiconductor interdiffusion, but the more basic problem of choosing the right value for the work function ϕ_m. The work function of a solid contains surface as well as volume contributions, and both the intimate and MIS Schottky models tacitly assume that ϕ_m and χ_s do not change (at least differentially) when the metal and the semiconductor are brought into contact. This may not be true in practice, so other parameters of the metal such as electronegativity have been proposed over the years for correlating to barrier height. Other empirical correlations studied include the heat of formation of silicides, effective work function, and the interfacial crystal structure. Detailed discussions of these aspects can be found in an article by Werner and Rao (4) on silicon, and in the review by Brillson (6) on other types of semiconductors.

CARRIER TRANSPORT

The current flow across the Schottky barrier may be visualized as an extension of electron emission from a metal to vacuum. As seen in Fig. 1 (a), the energy barrier for this process is the metal work function ϕ_m, which constitutes the activation energy for over-the-barrier thermionic emission current (proportional to exp $-(\phi_m/kT)$). With the metal in contact with the semiconductor [Fig. 1(b) or Fig. 2], the effective barrier for electron emission changes to the Schottky barrier height ϕ_b, as empty states are available in the conduction band of the semiconductors to receive the emitted electrons. Further, unlike vacuum, the semiconductor is also a source of electrons for emission back into the metal. Most importantly, we can control this latter flow by applying a voltage V of proper polarity—the so-called forward bias where the n-type semiconductor is negatively biased—that raises the conduction (and valence) band edge upwards by an amount qV relative to thermal equilibrium. As shown in Fig. 3, the energy barrier for electrons in the semiconductor reduces from qV_d to $q(V_d - V)$, which results in an exponential increase of current with the applied voltage. The path for this over-the-barrier-thermionic emission is shown as (a) in Fig. 3.

The current–voltage (I–V) characteristics of a Schottky barrier are then dominated by the thermionic emission process, with the following expression for current:

$$I = I_0[\exp(qV/nkT) - 1] \tag{8}$$

I_0 is the so-called saturation current given by

$$I_0 = A \cdot A^{**} \cdot T^2 \exp -(\phi_b/kT) \tag{9}$$

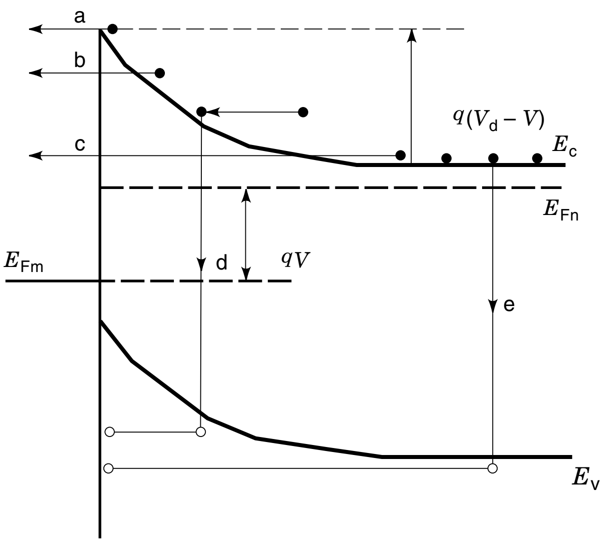

Figure 3. The band diagram of a metal/n-type semiconductor interface under an applied forward bias voltage V, displaying the various carrier transport mechanisms.

where A is the area of the Schottky contact, A^{**} is the modified Richardson's constant, which is dependent on the semiconductor band structure, k is Boltzmann's constant and T is the temperature in kelvins. Equation (8) also contains the so-called ideality factor "n," which has a value slightly greater than unity. This n-factor is a consequence of second-order effects such as the image-force reduction of the Schottky barrier height, and the presence of any interfacial layer that drops part of the applied voltage and thus reduces the voltage across the semiconductor. High-quality, intimate Schottky barriers made on moderately doped semiconductors can have $n \lesssim 1.01$, while increased doping and presence of I-layers can raise the value to as high as 1.1.

According to Eq. (8), the log I vs V plot should be linear for $V \gtrsim 3\,kT$, with the zero-voltage extrapolation giving the saturation current I_0. Using Eq. (9) and assuming the value of A^{**} (112 A/cm^2/K^2 for n-Si and 4.4 A/cm^2/K^2 for n-GaAs), one can then extract the value of the Schottky barrier height ϕ_b. In the reverse direction, that is, for $V < 0$, the current will remain constant at the saturation value I_0 (typical range $10^{-10} - 10^{-6}$ A/cm^2) until the junction breaks down under large reverse bias. It is evident that Eq. (8) represents highly asymmetrical I–V characteristics, leading to the use of the Schottky barrier as a rectifier in the Schottky diode.

Thermionic emission is the dominant transport mechanism at room temperature and above for Schottky barriers formed on moderately doped, single-crystal semiconductors, but a number of other mechanisms are also simultaneously present. Most of these are parallel processes and are illustrated in Fig. 3: Process (b) represents the thermionic field emission or thermally assisted tunneling process, where the electron climbs part way up the barrier thermally and tunnels through the rest; process (c) is field emission or direct tunneling across the entire barrier; process (d) is recombination in the depletion region; process (e) is recombination in the semiconductor bulk of injected minority holes.

Thermionic field emission and field emission become important as the dopant concentration is increased [with corresponding reduction in depletion width W, Eq. (3)] or temperature is reduced, and they have I–V relations similar in form to Eq. (8), but with an n-factor increasing substantially above unity. In the extreme case of field emission, the (nT) product becomes a constant, giving a temperature-independent slope for the log I–V plots. In highly defective or disordered materials such as amorphous and polycrystalline semiconductors, one sometimes observes nonthermionic characteristics even at room temperature and at doping levels where direct field or thermionic field emission is impossible. These are attributed to "multistep" tunneling through impurity and defect levels in the depletion region.

Recombination in the depletion region (process d) and hole injection (process e) are identical to the phenomena that occur in a p–n junction. The former gives an additional current component similar to Eq. (8), but with an ideality factor n that is usually close to 2. If the corresponding I_0 is larger than that for thermionic emission, this component will show up as a shoulder in the log I–V plots under low forward bias. The (minority) hole injection component has a form similar to that in Eq. (8), but with $n = 1$. As the corresponding I_0 is invariably orders of magnitude lower than that for the majority electron thermionic emission, minority carrier injection into the semiconductor is only rarely observed in Schottky barriers, corresponding to unusually large barrier heights and high forward bias. Note that the electrons injected from the n-type semiconductor into the metal are still majority carriers in the metal, unlike those injected from the n- to the p-side of a p–n junction. Thus there is no minority carrier storage in the Schottky diode, making it an extremely fast switching device.

All the current flow mechanisms identified in the preceding are parallel processes. However, the thermionic emission process itself is in series with diffusion of majority electrons from the bulk towards the interface. Nevertheless, except in some very low mobility semiconductors, the rate-limiting step is thermionic emission, not diffusion. Thermionic emission and diffusion limits in a Schottky barrier are analogous to water flow in a pipe limited by the orifice and internal bulk friction, respectively. Further details of current flow in a semiconductor may be found in Ref. 2.

BARRIER HEIGHT MEASUREMENTS

The most commonly used technique for measuring the Schottky barrier height is the I–V measurement. As noted earlier, extrapolation of the forward log I–V plot yields I_0, which is related to ϕ_b through Eq. (9). A simple room-temperature I–V measurement will suffice here if the value of A^{**} is assumed. However, the barrier height measured includes the effect of image force, a reduction on the order of 0.01 eV–0.04 eV depending on the material and doping. The error due to uncertainties in the value of A^{**} (due to the interfacial layer, etc.) is small (<0.02 eV for a factor of 2 change in A^{**}) due to its logarithmic influence on ϕ_b. For any meaningful interpretation of the log I–V data using the thermionic emission theory, it is important to verify that the linear region extends over at least two decades of current and that the n-factor is less than 1.1.

An added degree of freedom in Schottky barrier measurement can be gained if the I–V measurements are made at different temperatures, typically at room temperature and above where thermionic emission is likely to dominate. Then an activation energy plot of log (I/T^2) vs $1/T$ should yield a straight line, whose slope gives the barrier height and the y-axis intercept yields the value of A^{**}. This approach hence does not require any knowledge of the Richardson's constant, and is particularly effective for the assessment of Schottky barriers containing intentionally introduced I-layers for barrier height control.

Another frequently used electrical measurement is based on the depletion capacitance $C = \epsilon_s (A/W)$, which is a function of applied voltage V through Eq. (3) [modified by replacing V_d with $(V_d - V)$ under bias]. To avert the influence of strong conduction under forward bias, the capacitance–voltage (C–V) measurement is usually done under reverse bias (i.e., $V < 0$). Assuming the dopant concentration is constant, a plot of $[1/C^2]$ versus V will then give a straight line with an x-axis intercept at V_d. Figures 1 and 2 show the relation between V_d and ϕ_b; however, by including the effect of carriers at the depletion region edge through a correction term kT, one obtains the relation

$$\phi_b = qV_d + \xi + kT \qquad (10)$$

For intimate Schottky contacts on uniformly doped substrates, the agreement between I–V and C–V determined barrier height is quite close. However, the C–V technique fails to yield the correct barrier height with I-layers of substantial thickness and interface traps that may respond to the ac measurement signal. Incidentally, the slope of the $1/C^2$ plot gives the doping concentration N_D, which turns out to be valid even for nonuniform doping. A convenient way of obtaining the doping profile of a semiconductor wafer is to use a mercury contact as a *temporary* Schottky barrier.

One of the most direct measurements of Schottky barrier height involves photoexciting the electrons in the metal over the barrier. This *internal* photoemission process requires photons of energy $h\nu$ laying between ϕ_b and E_g to avert fundamental absorption in the semiconductor. The photoyield Y (photoelectron per absorbed photon) is given approximately by

$$Y \simeq B[h\nu - \phi_b]^2$$

where B is a constant. A plot of $Y^{1/2}$ versus $h\nu$ gives a straight line with an x-axis intercept at ϕ_b. As with I–V measurements, this barrier height includes the image force reduction effect. The variable wavelength illumination needed for this measurement may be obtained using a high-intensity white light source and a monochromator. If the illumination is on the metal side, the thickness of the metal should be small ($\approx$100 Å) because otherwise the photoexcited, *hot* electron with its limited mean free path cannot reach the interface.

MATERIAL SYSTEMS

Schottky barriers may be formed on literally any semiconductor, and in most cases it is easier to obtain a high barrier on n-type than on p-type material. There are exceptions such as InP, where the barrier height on n-type material is very low, seriously limiting the application potential of this important optoelectronic semiconductor in MESFETs. Most practical applications of Schottky contacts require a high barrier to minimize the leakage current I_0 and this coupled with the higher electron mobility makes *n*-type semiconductors the preferred choice for Schottky-based devices.

The choice of the metal is also based on metallurgical considerations involving interfacial stability. Metal-semiconductor interdiffusion may occur at high operating temperatures and current densities, so practical contacts may involve multilayers, and refractory and other metals and their alloys. Metallic silicides (e.g., PtSi, Co_2Si) are particularly attractive Schottky contact materials for Si as well as compound semiconductors and are widely used.

The technique of metal deposition is also crucial in determining the barrier height. Thermal evaporation in high vacuum ($<10^{-6}$ torr) is the most innocuous method for Schottky barrier formation, while sputtering and related ion-beam/plasma techniques introduce defects close to the MS interface and significantly modify the Schottky barrier height (7).

SCHOTTKY BARRIER MODIFICATION

Modification and control of the Schottky interface have been the subject of intense interest over the past two decades, both from fundamental and practical viewpoints. The interest in basic studies stems from the possibility of "passivating" the interface traps with suitable chemical treatment so that one may achieve the Schottky limit. Studies have also focused on introducing insulating as well as semiconducting nanoscale interlayers (e.g., Al/Si/GaInP, Metal/Si_3N_4/Si) to form deliberate MIS structures for barrier modification (8). Interface doping can also be used to alter ϕ_b. An elegant practical technique is that proposed by Shannon (9). By using a very shallow ($\approx$100 Å) implanted layer between the metal and the semiconductor, the shape of the barrier is altered, thereby changing the effective barrier height. If the implanted species are of the same conductivity type as the substrate, the increased electric field and thinning of the barrier near the top causes carrier tunneling. This effectively reduces barrier height. With an implant of the opposite conductivity type, the dopant compensation causes electric field reversal near the top, thereby increasing barrier height.

Recent contributions to the understanding of Schottky barriers have come about from the study of *epitaxial* silicide/Si interfaces where the crystallographic effects are very much in evidence. A very interesting result is the difference in barrier height of 0.13 eV between $NiSi_2$ and Si(111) depending on whether both have the same orientation or are rotated 180° about the $\langle 111 \rangle$ direction.

A closer inspection of the electrical and structural properties has also forced one to consider the inherent inhomogeneities at Schottky interfaces. The spatial potential fluctuations effectively yields a distributed system of parallel Schottky barriers of varying barrier heights. Hence, the net carrier transport can be profoundly influenced through the exponential dependence of current on ϕ_b [see Eqs. (8), (9)]. These issues are discussed at length in Ref. 4.

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SCHOTTKY DIODES. See Photonic crystals.

SCHOTTKY GATE FIELD EFFECT TRANSISTOR. See Metal semiconductor field effect transistors.