STATIC INDUCTION TRANSISTORS

The static induction transistor (SIT) is a three-terminal semiconductor device. Similarly to other active devices [like the bipolar-junction transistor (BJT) or the junction field-effect transistor (JFET)], in a SIT the current flow between two terminals (the source and the drain) can be controlled through the third terminal (the gate).

The SIT has been originally conceived as a solid-state analog of the vacuum-tube triode. The device is normally on, and a reverse bias applied to the gate is used to modulate the drain-source current. In this mode of operation the steady-state current drawn from the gate is negligible, and the SIT can be considered as a voltage-controlled device, like the JFET. A SIT, however, can also be designed to operate with a forward bias applied to the gate terminal (in this case, the device is called bipolar-mode SIT or BSIT). In this mode of operation a significant current flows through the gate of the SIT and the device becomes current-controlled, similar to a BJT. The BSIT is generally designed as a normally off device and is characterized by a much larger current-handling capability with respect to SIT.

The static induction thyristor (SIThy) also belongs to the family of static-induction devices. Similar to SIT, the SITh can be designed either as a normally on or a normally off device. Its behavior is however similar to the one of a gate turn-off thyristor (GTO). In the on state the SIThy shows very large current-handling capabilities, even for high-voltage de-

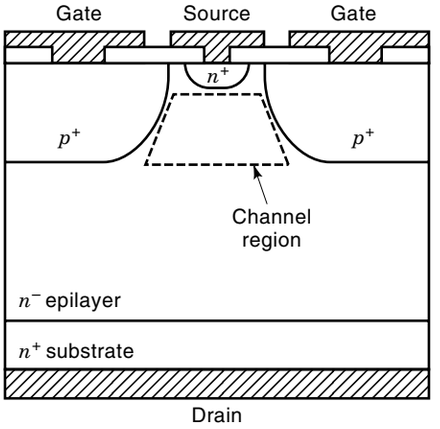

Figure 1. Elementary cell of a SIT realized with surface-gate technology, with the channel region pointed out. The remaining part of the epilayer is the drift region of the device.

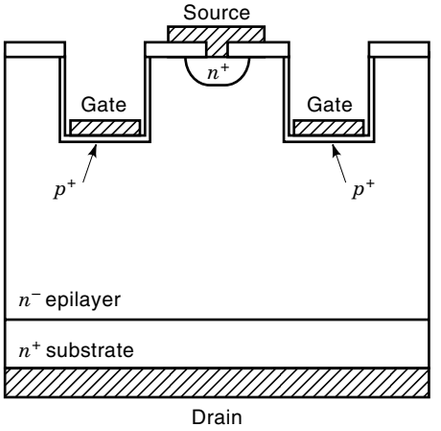

Figure 3. Cross section of a recessed-gate SIT. The vertically walled gate regions improve device performances.

vices, without the need of supplying forward gate current. The SIThy can be turned off by applying a large negative current pulse to the gate.

Although SIT devices have been proposed to realize digital Very Large Scale Integrated Circuits (VLSI), such as logic functions and memory, the main application of SITs is in the field of power electronics. Because of its interesting electrical characteristics, such as negative temperature coefficient, high switching speed, reduced stray capacitance, and good linearity, the SIT has been used in high-power AM/FM transmitters, induction heating systems, and linear amplifiers. Bipolar-mode SIT devices, due to the reduced on-state voltage drop, can be applied in high-voltage power circuits (switching power supplies and lamp ballast). SIThy are used for traction applications (motor control) and in very high-power conversion systems.

SIT STRUCTURE AND CHARACTERISTICS

Figure 1 shows the elementary cell of a surface-gate SIT. A discrete device is composed of many elementary cells in parallel. The surface-gate device can be realized with a simple planar technology and is mostly suited for bipolar-mode applications. The device is fabricated starting from a lowly doped n-type epitaxial region grown on the top of an highly doped n^+ substrate. The p^+ gate and the n^+ source regions are then realized on the top of the epilayer. The region between the source and the gate junctions is indicated as the *channel region* of the device, while the *drift region* is the one from the bottom of the gate and the substrate. The SIT is a short-channel device, since the channel length is comparable to the average channel width.

The basic structure of a buried-gate SIT is shown in Fig. 2. In this case, after the p^+ gate diffusion into the lightly doped epilayer, a second epitaxial growth of n-type silicon is performed to realize the buried grid. Contact to the buried gate is obtained by etching down to the p^+ grid or by diffusing a contact region from the upper surface.

Figure 3 shows a cross section of a recessed-gate SIT. Here, preferential silicon etching is used to form vertically walled grooves in which the gate regions are located. This process can achieve a self-aligned gate and source regions.

Figure 4 shows typical output characteristics of a SIT device. Different from long-channel JFET devices, the output

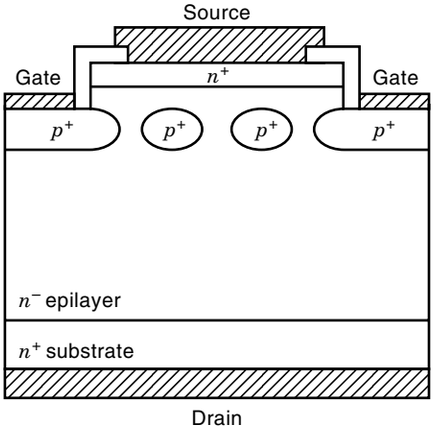

Figure 2. Basic structure of a buried-gate SIT. The gate region is contacted after etching the upper surface of the device.

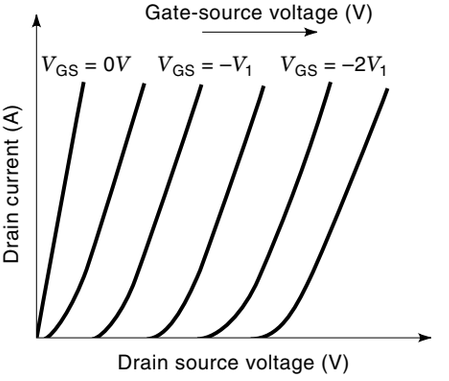

Figure 4. Typical triode-like output characteristic of a SIT device. The drain current increases continuously with the drain voltage and is controlled by applying a reverse voltage on the gate terminal.

curves of the SIT do not show an evident saturation region. Instead, the drain current continuously increases with increasing drain voltage. This behaviour is similar to the one of a vacuum-tube triode, and the non-saturating SIT *IV* curves are referred as *triode-like* characteristics.

For zero gate bias the device is on and the source-drain current is limited by the series of channel and drift region resistances (this is the device on resistance R_{ON}). By increasing the reverse gate bias, the depletion layers surrounding the gate-channel junctions grow, up to the point at which they touch each other. In this condition a potential barrier is created in the channel, which limits the electron current flow between source and drain. Because of the short-channel SIT structure, the height of the potential barrier depends not only on the reverse voltage applied on the gate but also on the drain-source voltage. In particular, by increasing the drain-source voltage the potential barrier height is lowered and the drain current increases continuously, resulting in triode-like characteristics. In addition to the on-resistance, other important parameters for a SIT device are the drain-gate breakdown voltage BV_{DGO}, the source-gate breakdown voltage BV_{SGO}, and the dc blocking gain G_B, given by:

$$G_B = V_{DS}|V_{GS}| \quad \text{for} \quad I_D = \text{small value} \tag{1}$$

If the device is to be used as a switch, the maximum drain-source voltage is given by: $V_{DS,max} = BV_{DGO}(1 - 1/G_B)$, assuming $BV_{SGO} > BV_{DGO}/G_B$.

For linear applications, most important SIT parameters are the voltage amplification factor μ defined as:

$$\mu = -\Delta V_{DS}/\Delta V_{GS} \quad \text{for} \quad I_D = \text{constant} \tag{2}$$

and the transconductance g_m is given by:

$$g_m = \Delta I_D/\Delta V_{GS} \quad \text{for} \quad V_{DS} = \text{constant} \tag{3}$$

The differential output impedance $r_0 = \mu/g_m$ is generally smaller in SIT devices with respect to long-channel JFET structures.

The switching speed and the high-frequency operation of the device are limited by the parasitic gate-drain and gate-source capacitances, C_{GD} and C_{GS}. Because of the reduced values of these capacitances, the high frequency response of SIT devices is good, compared with other power semiconductor devices.

SIT OPERATION

Figure 5 shows a plot of the potential distribution in a surface-gate SIT device, with a reverse gate bias larger than the pinch-off voltage. The potential distribution shows a saddle point in the channel region, where the potential barrier is located. The barrier height can be modulated by the two applied potentials gate-source and drain-source. As the two control terminals act in perpendicular directions, the potential distribution and then the overall device operation are fundamentally two-dimensional. The device current is due to the transport of electrons from source to drain and is exponentially related to the height ψ_B of the potential barrier:

$$I_D = I_0 \exp(-\psi_B/V_T) \tag{4}$$

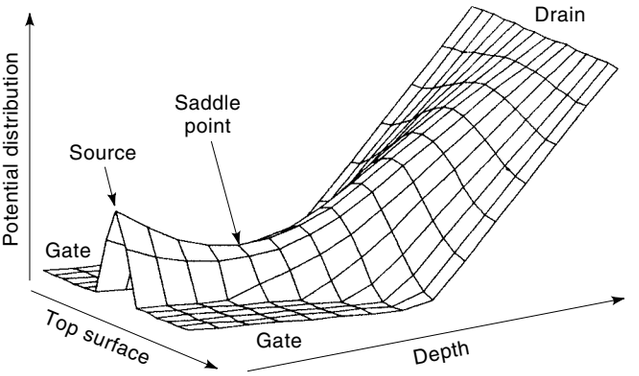

Figure 5. Potential distribution in a surface-gate SIT. Note the saddle point into the channel region, where the potential barrier is located which controls the current flow from source to drain.

In this equation V_T is the thermal voltage kT/q, where k is the Boltzmann constant, T is the absolute temperature, and q is the electronic charge. The coefficient I_0 in Eq. (4) is not a constant, but depends on the shape of the potential distribution in the neighbourhood of the saddle point. The value of ψ_B should be obtained from a two-dimensional solution of the Poisson's equation which gives the potential distribution in the device. In a first-order approximation, it can be assumed that ψ_B is linearly dependent from drain-source and gate-source voltages:

$$\psi_B \approx -\eta V_{GS} - (\eta/\mu)V_{DS} + C \tag{5}$$

Where C is a constant, μ is the voltage amplification factor, and η takes into account the dependence of the potential barrier on V_{GS}. By substituting Eq. (5) into Eq. (4) we can observe that the drain current is exponentially dependent on both gate and drain voltages. Actually, the output SIT curves show an exponential behaviour only in the low-current range. For large drain current values, the carrier concentration due to electrons flowing across the potential barrier becomes comparable to the epilayer doping. In these conditions, while an increase in the drain voltage has the tendency to lower the potential barrier, the effect of the associated increase in the drain current is opposite. In fact, the charge due to mobile electrons in the channel tends to increase the potential barrier height. This electrostatic feedback results in the departure of the SIT output characteristics from the low-current exponential behaviour predicted by Eqs. (4) and (5) to the almost linear curves of Fig. 4.

The blocking gain and the voltage amplification factor of a SIT device are strongly dependent on the aspect ratio of the channel region: that is, the ratio between channel length and width. A large value for the channel aspect ratio results in better control of the potential barrier by the gate potential, and hence in a larger blocking gain. The device technology also plays a major role in determining the values of G_B and μ. In surface-gate devices, the cylindrical shape of the junction boundary results in low channel aspect ratio with reduced blocking gain. Better performances are obtained by using either buried-gate or recessed-gate technologies.

When the SIT is used as a switch, it is important to minimize the power losses in the on state, and hence the R_{ON} value. The on resistance is due to the sum of the channel re-

gion and of the drift region resistances:

$$R_{ON} = R_{CH} + R_{DRIFT} \tag{6}$$

In the ideal case in which the current flow extends over the entire device area A, the drift region resistance is given by:

$$R_{DRIFT} = W/(qN_D\mu_n A) \tag{7}$$

where μ_n is the electron mobility, while W and N_D are the thickness and the doping of the drift region, respectively. The actual value of R_{DRIFT} can be much larger than predicted by Eq. (7), due to uneven current distribution in the drift region. The parameters W and N_D are designed as a function of the drain-gate breakdown voltage BV_{DGO}. A high BV_{DGO} value requires a thick and lightly doped epitaxial layer, resulting in a large drift resistance.

The channel region resistance strongly depends on the channel aspect ratio. Increasing the channel length or reducing its width results in fact in a worsening of the R_{CH} value. Therefore, a trade-off exists between blocking gain and on-resistance, limiting the SIT performances as a switching device.

BIPOLAR-MODE SIT (BSIT)

A SIT can be operated in the bipolar-mode by forward biasing the gate with respect to the source. In high-voltage devices, where low doping of the epitaxial layer is needed to achieve large BV_{DGO}, this easily results in high-level injections in both channel and drift regions that are filled with an electron-hole plasma. In this way, the device-on resistance can be largely reduced, improving the current-handling capability of the device. This advantage is paid for by a reduced switching speed, as a significant time is needed to extract the excess carrier from the epilayer to turn off the device. Furthermore, a more complex gate driving circuit is required, since a significant gate current is needed to conductivity modulate the epilayer region.

Because of the conductivity modulation effect, the channel aspect ratio of BSIT devices can be largely increased without sensible degradation of the on resistance. This allows the realization of normally-off devices. In a normally-off BSIT the built-in voltage of the gate-epilayer junction is able to create a significant potential barrier into the channel even for zero gate-source voltage and for a drain-gate voltage as large as BV_{DGO}. This is a highly desirable feature for a switching device, since in this case there is no need of negative gate bias to turn off the device.

The buried-gate structure is not suited for bipolar operation, due to the large gate series resistance. Better performances are achieved using recessed gate and surface gate devices. In surface gate BSIT, in particular, normally-off operation can be achieved by allowing the two gate diffusions to touch each other into the channel region.

Figure 6 shows typical output characteristics of a BSIT device. The controlling parameter is the gate current. Note that the output curves are no more triode-like, but are instead very similar to the one of a BJT device, with a very low on-state voltage. One of the most important parameters for a BSIT device is the current gain defined as:

$$\beta = I_D/I_G \quad \text{for} \quad V_{DS} = \text{constant} \tag{8}$$

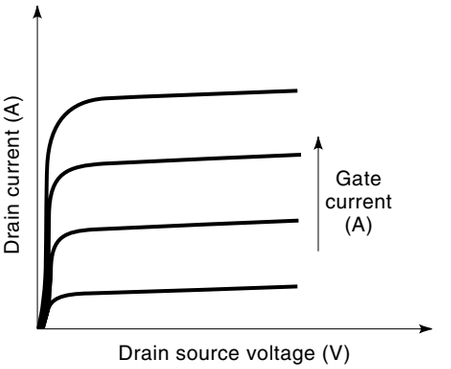

Figure 6. Typical output characteristic of a BSIT device. The curves are very similar to the one of a BJT device, showing a very low on-state saturation voltage.

The value of β is strongly dependent on the drain current. The current gain can be very large at low drain currents, while at large current values β decreases as $1/I_D$.

Figure 7 shows the behavior of the electric field and of the carrier concentration in a forward-biased BSIT, along a vertical axis going from source to drain, passing in the center of the channel region. Two regions can be defined, subdivided by the abscissa x_1.

In the first region, from the source end to x_1, high-injection conditions hold with almost equal electron and hole concentration:

$$p(x) \approx n(x) \gg N_D \tag{9}$$

The conductivity of this region is equal to:

$$\sigma_{mod} = q(\mu_n + \mu_p)n(x) \tag{10}$$

and is therefore much higher than the epilayer conductivity: $q\mu_n N_D$. This phenomenon is known as *conductivity modulation* and is responsible for the reduced voltage drop on the first region.

The charge concentration decreases linearly up to the abscissa x_1 where the hole concentration becomes smaller than

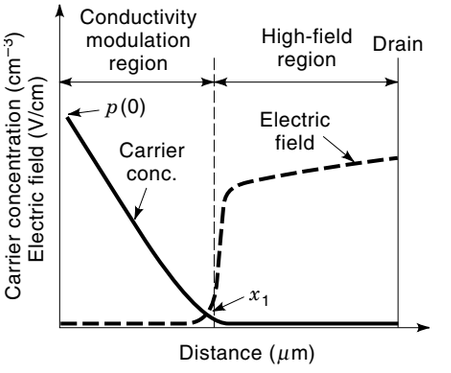

Figure 7. Carrier concentration (solid line) and electric field (dashed line) in a forward-biased BSIT. Note the low electric field in the conductivity modulated region. The drain voltage drops mainly in the high-field region.

the epilayer doping N_D. The drain current is proportional to the slope of carrier concentration $p(0)/x_1$ while the gate current must supply carriers that recombine in the conductivity modulated epilayer and also minority carriers that recombine in the highly doped gate and source diffusions.

In the second region, from x_1 to the drain end, the holes are practically absent due to the high electric field that repels them from the drain region, while the electrons drift toward the drain. The drain-source voltage drops mainly across this second region.

When the BSIT is in saturation, all the epilayer is in conductivity modulation regime: that is, off abscissa x_1 reaches the epilayer-substrate junction. This explains the very low on-state voltage drop exhibited by BSIT devices.

Like the BJT, the BSIT switching speed is limited by its bipolar-mode operation. The device turn-off takes place in two phases. In the first one, a little change in the drain current is observed, although a reverse current is extracted from the gate terminal. This is the storage time of the device, needed to remove the excess carrier stored in the epilayer. The second phase of the BSIT turn-off process is much faster, and is characterized by the fall time needed to decrease the drain current up to zero. During this phase a sensible power dissipation occurs, as the device experiences both large drain voltages and currents.

STATIC INDUCTION THYRISTOR (SIThy)

The basic structure of a SIThy is very similar to the one of a SIT device. The main difference is the substrate doping that is *p*-type in a SIThy, while it is *n*-type in a SIT device.

In absence of gate bias, the SIThy operates like a *pin* rectifier, in which the anode corresponds to the *p*-doped drain and the cathode to the *n*-type source. The device, therefore, is able to block a negative voltage applied between drain and source. A positive V_{DS} value brings the device in forward conduction. In this state, the device is able to conduct a large current with a reduced voltage drop. Like a *pin* diode, the forward conduction curve of a SIThy is characterized by a knee voltage of about 0.7 V.

The device is in the forward blocking mode when a sufficiently large negative voltage is applied between gate and source terminals. A potential barrier is created in the channel region which modulates the current flow between source and drain. The device behavior in this operating condition is very similar to the one of a SIT, with triode-like characteristics, and a blocking gain G_B can be defined as in Eq. (1).

The SIThy is able to be switched from conduction mode to the forward blocking mode (forced gate turn-off). During forced turn-off, a large negative current pulse must be supplied to the gate of the device, in order to remove minority carriers stored in the channel region, before creating a potential barrier into the channel. An important parameter characterizing the forced-gate turn-off process is the turn-off current gain, defined as:

$$G_T = I_D/I_{GP} \tag{11}$$

where I_{GP} is the extracted gate current.

The turn-off speed of the device is limited by the time needed to extract minority carrier from the epilayer. When the forced gate turn-off process begins, an initial storage time is observed, in which the drain current remains almost constant, while excess carriers are extracted from the epilayer of the device. Then, a depletion layer forms in the channel region, a potential barrier builds up, and the drain current begins to decrease. However, the stored charges in the epilayer are not completely removed by the gate current during the storage time. The remaining charge in the device must then decay by recombination, with a characteristic time equal to the carrier lifetime in the epilayer τ. This causes a long decay tail in the drain current waveform, decreasing the speed of the SIThy. The carriers lifetime in the epilayer is thus an important design parameter for SIThy devices. Increasing τ yields a larger epilayer conductivity modulation and hence a reduced on-state voltage drop. On the other hand, a large τ value results in a long turn-off time and in increased switching losses. To overcome the tradeoff between turn-off time and on-state voltage drop, local lifetime control techniques using proton or helium irradiation have been proposed.

BIBLIOGRAPHY

B. J. Baliga, The asymmetrical field controlled thyristor, *IEEE Trans. Electron Devices,* **ED-27**: 1262–1268, 1980.

B. J. Baliga, Bipolar operatoin of power junction field effect transistors, *Electron. Lett.,* **16**: 300–301, 1980.

B. J. Baliga, Barrier controlled current conduction in field controlled thyristors, *Solid-State Electron.,* **24**: 617–620, 1981.

B. J. Baliga, Electron irradiation of field controlled thyristor, *IEEE Trans. Electron Devices,* **ED-29**: 805–811, 1982.

B. J. Baliga, High voltage junction-gate field-effect transistor with recessed gates, *IEEE Trans. Electron Devices,* **ED-29**: 1560–1570, 1982.

B. J. Baliga, *Modern Power Devices,* New York: Wiley, 1987.

S. Bellone et al., A quasi one-dimensional analysis of vertical FET devices operated in the bipolar mode, *Solid-State Electron.,* **26**: 403–413, 1983.

C. Bulucea and A. Rusu, A first-order theory of the static induction transistor, *Solid-State Electron.,* **30**: 1227–1242, 1987.

Y. Mochida, J. Nishizawa, and T. Ohmi, Characteristics of static induction transistor: effects of series resistance, *IEEE Trans. Electron Devices,* **ED-25**: 761–767, 1978.

J. Nishizawa, T. Ohmi, and H. L. Chen, Analysis of static characteristics of a bipolar-mode SIT (BSIT), *IEEE Trans. Electron Devices,* **ED-29**: 1233–1244, 1982.

J. Nishizawa et al., A low loss high speed switching device: the 2500-V 300-A static induction thyristor, *IEEE Trans. Electron Devices,* **ED-33**: 507–515, 1986.

J. Nishizawa et al., A double gate type static induction thyristor, *IEEE Trans. Electron Devices,* **ED-34**: 1396–1405, 1987.

J. Niswizawa, T. Terasaki, and J. Shibata, Field-effect transistor versus analog transistor (static induction transistor), *IEEE Trans. Electron Devices,* **ED-22**: 185–197, 1975.

P. Plotka and B. Wilamosky, Interpretation of exponential type drain characteristics of the static induction transistor, *Solid-State Electron.,* **23**: 693–694, 1980.

P. Spirito, A. G. M. Strollo, and A. Caruso, Two-dimensional analysis of the IV characteristics of normally off bipolar-mode FET devices, *Solid-State Electron.,* **33**: 1401–1417, 1990.

J. M. C. Stork and J. D. Plummer, Small geometry depleted base bipolar transistors (BSIT)—VLSI devices?, *IEEE Trans. Electron Devices,* **ED-28**: 1354–1363, 1981.

A. G. M. Strollo, Trade off between blocking gain and on resistance in static induction transistor, *Solid-State Electron.,* **38**: 309–315, 1995.

A. G. M. Strollo and P. Spirito, A self-consistent model for the SIT DC characteristics, *IEEE Trans. Electron Devices,* **ED-38**: 1943–1951, 1991.

ANTONIO G. M. STROLLO
University of Naples