THYRISTOR TYPES

A thyristor is a semiconductor switch consisting of four alternately doped *pnpn* layers. Thyristors are typically available to control voltage and current from ~100 V to 10,000 V and from 1 A to >3000 A (rms), and vary in size from <5 mm to >125 mm chip diameter. The most common thyristor is the semiconductor-controlled rectifier (SCR). The SCR is a three-terminal thyristor device with anode, cathode, and gate terminals. Thyristors are also available within integrated circuits (ICs), particularly in telecom applications.

The symmetric SCR blocks voltage in both directions and can be turned on by applying a small current to the gate cathode junction, thereby closing the switch in the anode-to-cathode or forward direction. The SCR differs in operation from the three-layer bipolar junction transistor (BJT) in *latching* after gating and the buildup of sufficient *latching current.* The SCR stays latched on until its anode-to-cathode current (gate open) is reduced below a *holding current* limit. The thyristor also differs from the transistor in displaying bistable action that depends on *pnpn* regenerative feedback.

A thyristor can be unidirectional or bidirectional, have from two to six leads (Fig. 1), and be triggered from a voltage blocking state to a conducting state by gate current; by light (photon) energy (e.g., from a laser); by a voltage change *dv/dt*, as in the reverse-switching rectrifier (RSR); or by two-terminal breakover, as in the diac and the Shockley diode). The triac and silicon bilateral switches are examples of bidirectional thyristors that conduct current in either direction.

A unique property of the thyristor is *regeneration,* herein defined as simultaneous electron and hole injection from the cathode and anode emitters respectively. The SCR gate current acts to initiate electron injection from the cathode emitter. After electrons transit the narrow *p* base, they enter the wide *n*-base and initiate hole injection from the anode emitter, thereby resulting in charge neutrality, regeneration, and latch-on. Anode current delay results from the time required for electrons to transit the thin *p*-base, which can be reduced by (dual) gating the cathode and anode emitters simultaneously.

Reverse-switched *dynistors* (RSDs, from the I. V. Grekhov–A. F. Ioffe Institute, Russia) are two-terminal thyristors with shorted anode emitters. Dynistors are designed to turn on by passing reverse current from cathode to anode, thereby modulating the central junction prior to the first current zero crossing. Dual gating from both anode and cathode emitters can be achieved by optical, *dv/dt,* or dual gate triggering and can result in high *di/dt* capability.

The history of *pnpn* thyristors can be traced back to the invention by Schockley, in the early 1950s of the Hook collector transistor, now called the Shockley diode. Moll et al. of Bell Labs published an article on *pnpn* transistor switches in 1956 (1). In the late 1950s R. A. York, aware of the Bell Labs work, initiated a commercial effort at the General Electric (GE) Company that would eventually result in the first wide-

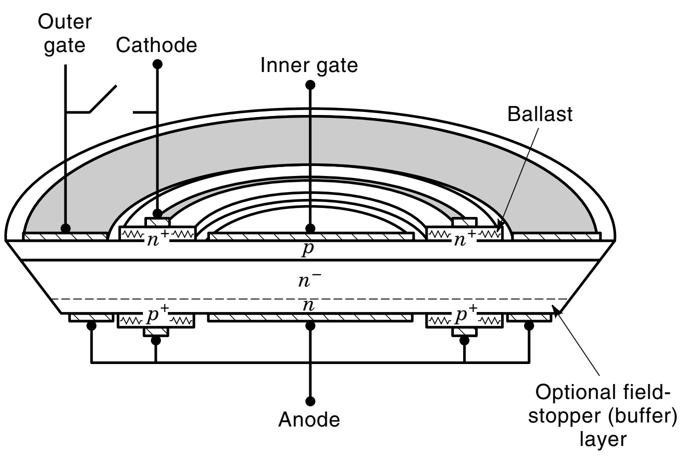


Figure 1. The programmable reverse-conducting thyristor.

spread production and application of thyristors. Shockley and Gibbons also recognized the potential of *pnpn* hook collector devices as high-speed-turn-on switches, later to be called *pulse power thyristors* (PPTs), with an article (2) in 1958.

Construction

Thyristors are typically made from the highest-quality float-zoned silicon, but have also been made from GaAs and SiC. Most high-power thyristors have deep-diffused parallel-plane central junctions that terminate at beveled (mesa) surfaces (Fig. 2). High-voltage thyristors are made from single-crystal, high-resistivity n-type silicon that is doped by the nuclear transmutation of some of the Si atoms to phosphorus. Nuclear transmutation produces Si substrates with exceptional resistivity uniformity and has recently led to thyristors that can block over 10,000 V. The planar process has also been used to build low-power devices where all three junctions terminate at the surface (the GE C13 and C106). The Si-controlled switch (SCS-C13) uses the planar process to bring all four layers to the top surface, thereby enabling the connection of terminals to all of them. Triac thyristors have anode and cathode patterns on both sides of the wafer, which enables them to control ac power.

Passivation of thyristors for low leakage current has been a continuing challenge. Materials such as glass (GE #351), polymers (polyimide siloxanes), SiN, diamondlike carbon (DLC), SiPOS (oxygen-rich polysilicon), silicones (RTVs), oxides, and combinations have been used after suitable surface beveling and cleaning. A major passivation difficulty is associated with mechanical stress and passivant-induced surface charge, which is usually electronegative and tends to invert the underlying high-resistivity n-base region near the passivation surface. Inversion results in *channeling,* or high leakage current, especially if moisture is allowed to penetrate to the Si surface.

Thyristors are usually limited to $<125°C$ due to leakage current and the potential for thermal runaway. However, diodes that block equivalent voltage are rated to $\approx 200°C$. Recently, thyristors have been designed with shorter emitters on both sides of the chip, thereby enabling diodelike blocking performance to $>200°C$. Temperature excursions during allowable surge performance can approach the metal–Si eutectic melting point, $\approx 577°C$. Traditionally the surge-current limit is calculated by the empirical relation $N = (300/\Delta T)^9$, where N is the number of expected cycles before failure is expected, and ΔT is the temperature excursion (K) per cycle.

GENERAL APPLICATIONS

The control of power is the most common and cost-effective use of the traditional SCR, because the current reverses polarity each cycle, thereby enabling low-cost SCRs to phase-control the power to a load such as a lamp, without having to interrupt the current. Thyristors should be considered wherever high blocking voltage and current must be controlled. However, recent semiconductor switches such as metal–oxide–semiconductor field-effect transistors (MOSFETs), insulated-gate bipolar transistors (IGBTs), and MOS-controlled thyristors (MCTs) should be considered for high-frequency ($>$20 kHz) switching, particularly for inverters, choppers, and electric motor control. Thyristors are the most cost-effective closing-switch and on-state devices. They also have the potential to be the optimum opening and closing switch for $>$1200 V applications. Continuing thyristor technology progress is realizing the unfulfilled potential of the thyristors for unlimited turn-on di/dt, as well as optimum turnoff performance with respect to the reverse-biased safe operating area (RBSOA).

The 1998 demand for power semiconductor devices (over 1 W) exceeds \$13 billion per year and is growing at $\approx$13%. BJTs, IGBTs, thyristors, and power diodes satisfy the bulk of this demand. IGBTs are currently favored in new applications for medium-power, medium-frequency applications. However, recent progress in applying thyristor technology to inverters, motor control, pulse power, and choppers may eventually displace many IGBT devices, particularly where discrete and/or integrated MOS devices are used for thyristor control. The thyristor is the most cost-effective technology to block high voltage with minimal on-state losses.

Turnoff performance is the primary weaknesses of the traditional SCR. Inverter SCRs are designed to minimize the turnoff recovery time t_q in resonant or forced commutated inverter circuits. Presently, IGBTs must be considered competitive with inverter SCRs in medium-power ($<$1200 V, $<$200 A) applications.

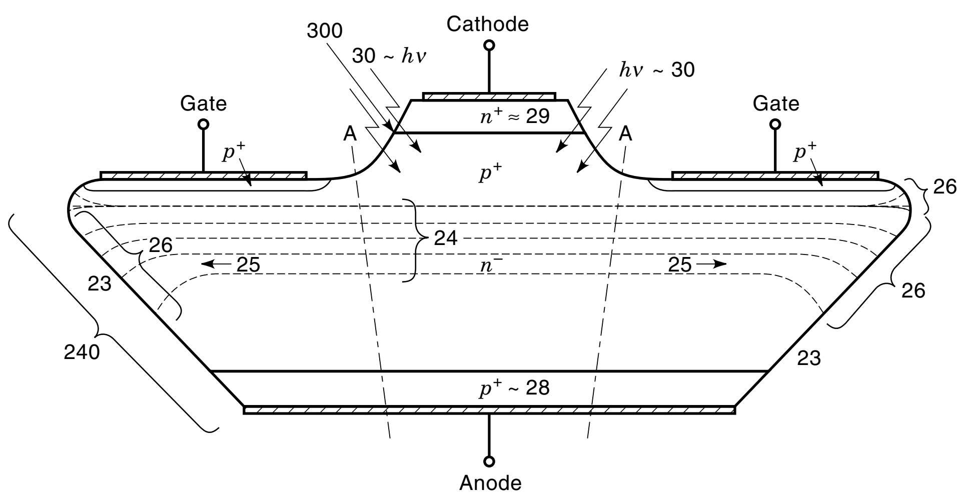


Figure 2. Positive-beveled thyristor.

OPEN-BASE RECOVERY PROBLEMS

Gate turnoff thyristors (GTOs) and MCTs are designed as opening-switch thyristors, but suffer low RBSOA performance capability. All popular opening-switch power semiconductors, such as IGBTs, GTOs, and MCTs, suffer open-base recovery (OBR) problems. These problems are associated with the finite time required for trapped-electron–hole recombination in the open bases, and are manifest as tail current and high switching losses. In contrast, rectifier diodes and some narrow-base BJT devices recover by sweeping untrapped charge from the junction during reverse recovery, with a resultant *square RBSOA.* This means the device is able to interrupt its rated current, to rated voltage, without the use of costly snubbers (i.e., parallel capacitors).

AVAILABLE TYPES

The following summary describes various commercially available thyristor technologies.

Phase-control thyristors are designed to maximize the silicon area for use as active emitter area at 50 Hz to 60 Hz ac. The devices have large shorted emitters (for high dv/dt) with small center gates, and depend on the low plasma spreading velocity to turn on emitter areas remote from the center gate. Phase-control SCRs are typically constructed by diffusing a symmetric *pnp* followed by a selective n^+ (n^+ means heavy n doping) on the cathode side. The cathode is defined by a selective silicon etch or by oxide masking. The device is then metallized, and the metal selectively etched using photomasks, thereby separating the cathode from the gate metallization. Initial conduction is typically confined to an area immediately surrounding the gate pad, and later spreads to the entire emitter area. If di/dt exceeds specified limits, the initial on area will be too small to support the current, and small di/dt melt holes will develop in the vicinity of the gate cathode periphery and destroy the device. Researchers have extensively examined the spreading velocity by viewing radiative recombination of the spreading hole–electron plasma. Despite comprehensive research, the high base spreading resistance of conventional phase control devices results in low (e.g., less than 200 A/μs) di/dt withstand capability of phase-control SCRs.

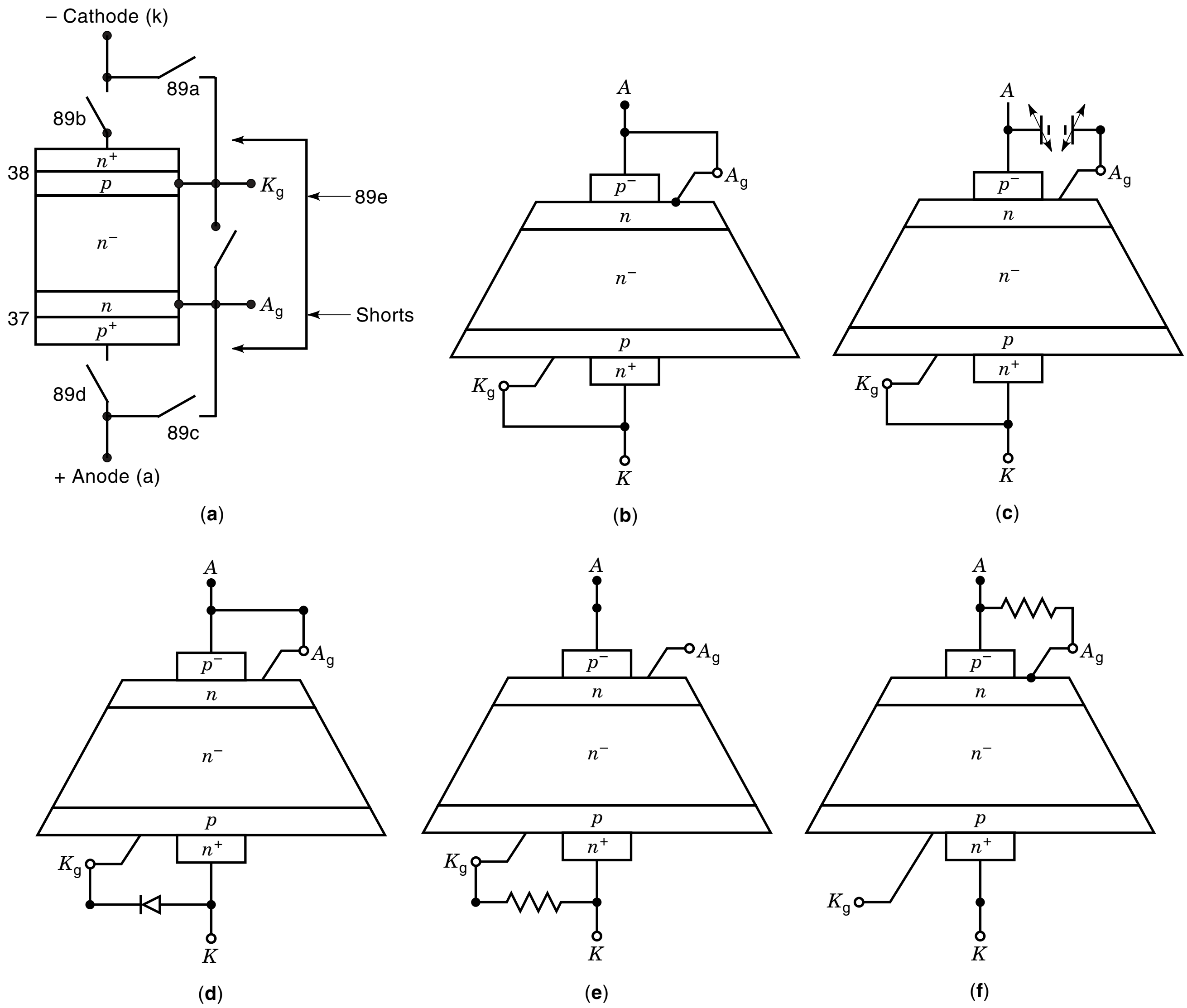
Inverter thyristors have distributed or interdigitated gates (for high di/dt), similar to transistor emitter patterns. These interdigitated thyristors utilize larger initial areas of the emitter for faster turn-on, and enable short turnoff times. For faster turnoff, heavy gold or platinum diffusion and/or electron radiation reduce the carrier lifetime in the open *n*-base, thereby reducing thyristor turnoff times (t_q). Unlike transistors, inverter thyristors have heavily shorted emitters to prevent latchup when voltage is being reapplied (that is, dv/dt withstand capability). These inverter design features allow thyristors to be used at high (up to 50 kHz) repetition rates, but at the expense of high forward voltage drop, which limits performance and accelerates the onset of thermal runaway.

Gate assist turnoff (GATO) *and gate turnoff* (GTO) *thyristors* have unshorted *npn* regions that are designed like high-speed transistors, where the gate is used for charge-control turnoff functions. In GATO closing switches, the gate is used to extract charge from the gate–emitter junction during the t_q (zero-current interval) and the reapplied dv/dt-switching interval. This allows high-repetition-rate performance without the adverse tradeoff between turnoff time and on-state voltage in lifetime-controlled inverter SCRs. The disadvantage of GATO operation is the requirement for negative gate bias and current during the off-state and commutation dv/dt intervals, and the complexity of the triggering circuitry.

GTO's are similar to GATOs but must be lifetime-controlled to act as opening switches. GTOs are made with both symmetric and asymmetric (*n*-buffer field-stopper layer) structures, and without cathode shorts. Asymmetric GTOs are made both with and without (transparent emitter) anode shorts. The best turnoff gains for GTOs ($I_a/I_g \approx 5$) are obtained with shorted-anode, asymmetric structures, but most must be continuously gated to remain on. So far, some of the highest-di/dt pulse-power closing-switch thyristors (PPCSTs) have been GTO-type structures. These GTO emitter structures are ideally suited to receive and distribute high turn-on gating currents. If opening is not required, the highest possible hole–electron lifetimes will lead to the lowest possible on-state voltage and turn-on time. Therefore, the GATO is perhaps the best conventional semiconductor switch structure for pulse-power applications.

MOS-Controlled Thyristors (MCTs) are integrated arrays of paralleled GTO cells (on the order of 20 μm spacing), with complementary FETs connected from anode to gate and gate to cathode. All of the cells have turnoff FETs that act as gate–cathode shunts during turnoff and during the off state. Some of the MCT cells have integrated high-voltage turn-on DMOS-FETs connected from anode to gate. For those turn-on cells having their own anode–gate FET, the upper-base spreading resistance under the emitter is low, and good gate–emitter injection is assured for good di/dt. However, not all cells have turn-on FETs, and their area utilization (60%) is not as good as with GATOs (>85%). Furthermore, gate-yield considerations limit the active area to about 1 cm^2. High-current, high-voltage applications are therefore better served by GATO, GTO, or DGT designs, even though the turnoff function is not required.

In the past, thyristors have not been optimized to serve as both closing and opening switches for square RBSOA performance, that is, turnoff at full current and voltage without snubbers. As a result, designers have sought circuit solutions such as forced commutation for turnoff, resonant topologies (soft switching for low-RBSOA switches), saturable reactors to limit di/dt, snubbers to limit reapplied dv/dt, and expensive gate drives to accommodate GTOs with low turnoff gain. Long turnoff tail currents due to open-base recovery of the wide-base *pnp* is endemic to most power semiconductor opening switches. The MCT has addressed many of these difficulties, but also suffers from open-base recovery (low RBSOA), is difficult to scale up to large areas with good yield, and has a low active-to-total area ratio. Moreover, turn-on FETs associated with MCTs must block the full device voltage and must be sized proportionally to the 2.5 power of the blocking volt age. Thus, it would be desirable to provide the industry with power electronic switching devices that can serve as both closing and opening switches at unlimited di/dts and without snubbers or saturable reactors. Baliga (3,4) has further refined the operation of MOS-gated thyristors by integrating MOS control for single-side emitter switching, and by controlling the base resistance (BRTs). The best DMOS polarities for



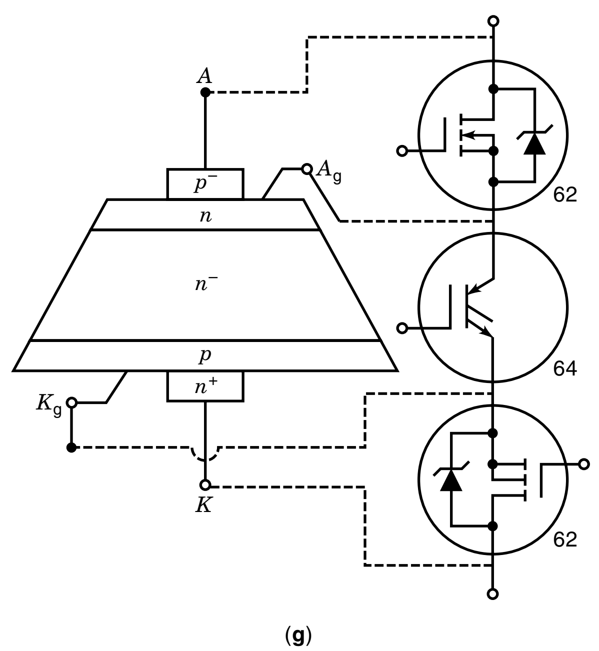


Figure 3. (a) General switching concepts for thyristor control. (b) *pin* diode configuration. (c) Silicon-controlled switch. (d) Reverse-conducting thyristor. (e) Anode-gated thyristor. (f) Cathode-gated thyristor. (g) Dual-gated MOS-controlled thyristor.

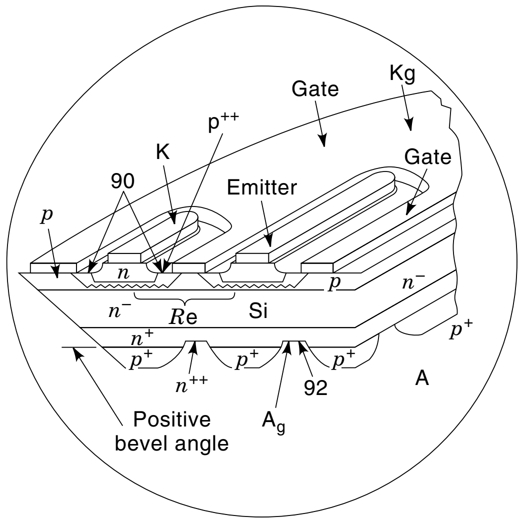


Figure 4. Two-sided thyristor.

MCT turnoff are *n*-channel, which requires a *p*-base for the GTO cell. Unfortunately, the MCT *p*-base has a much lower RBSOA capability than the traditional *n*-base, thereby leading to an adverse tradeoff.

Dual-Gated Thyristors (DGTs), with four terminals, enable control of all thyristor junctions. Figures 3 and 4 illustrate the variety of devices that are possible with ohmic contacts to all four layers of a mesa-type thyristor, and how to transition from one to the other. Figure 5 illustrates a method of transitioning the conducting thyristor to a recovering reverse-biased *pin* diode. Semiconductor switching devices can be constructed to be capable of almost unlimited di/dt by simultaneous electron–hole injection from both anode and cathode emitters, by reduced spreading resistance under the emitter, and by providing a continuous and narrow solder-bumped gate–cathode structure. High di/dt has many desirable ramifications in power applications. Dual gate contacts offer thyristor devices having improved ambient temperature performance. Existing thyristor junction temperatures (T_j) are limited to approximately 125°C. By employing asymmetric semiconductor structures and edge-bevel-area gain reduction techniques such as positive beveling and electron beam irradiation, significantly higher junction temperatures, on the order of 200°C, can be achieved. A four-leaded semiconductor device having an anode, anode gate, cathode, and cathode gate is illustrated in Fig. 6. By selectively connecting the anode and anode gate leads and/or the cathode and cathode gate leads (and/or by opening the emitter leads), DGTs can be operated or transitioned in a number of different modes. For example, the DGT can transition from a conducting *pnpn* thyristor to a *pin* diode, enjoying the square-RBSOA capability of the diode. The DCT can also operate as a semiconductor-controlled switch (SCS), as a reversibly triggered conducting thyristor, as an anode-gated GTO, as a cathode-gated GTO, or as an anode–cathode-gated SCR. The DGT can operate as an MCT that is controlled from both anode and cathode sides, using optimum *n*-channel DMOSFETS for emitter shunts, and *n*-channel IGBTs to connect anode and cathode gates for the most efficient amplifying-gate turn-on of both anode and cathode emitters.

Both the *npn* and *pnp* portions of the DGT are efficient bipolar junction transistors (Fig. 6) which can be used independently. Access to all four thyristor layers results in much better device control, higher hole–electron lifetimes, and better turnoff performance because open-base recovery with the attendant hole–electron recombination tail of the wide-base

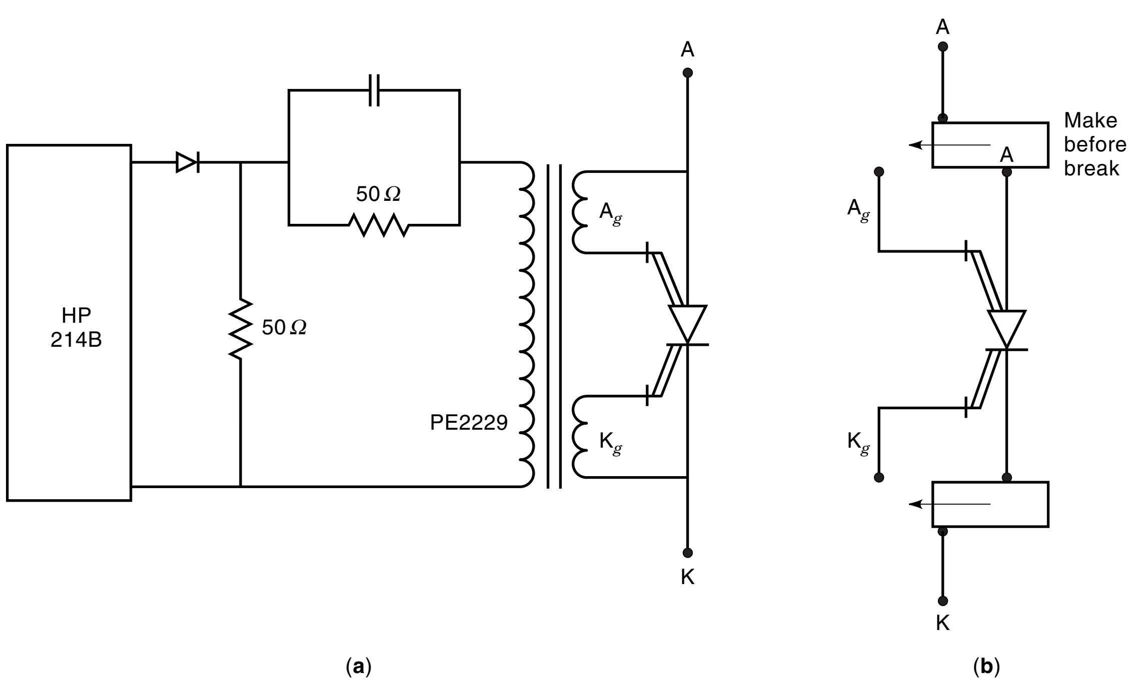


Figure 5. Two methods of turning off the DMCT.

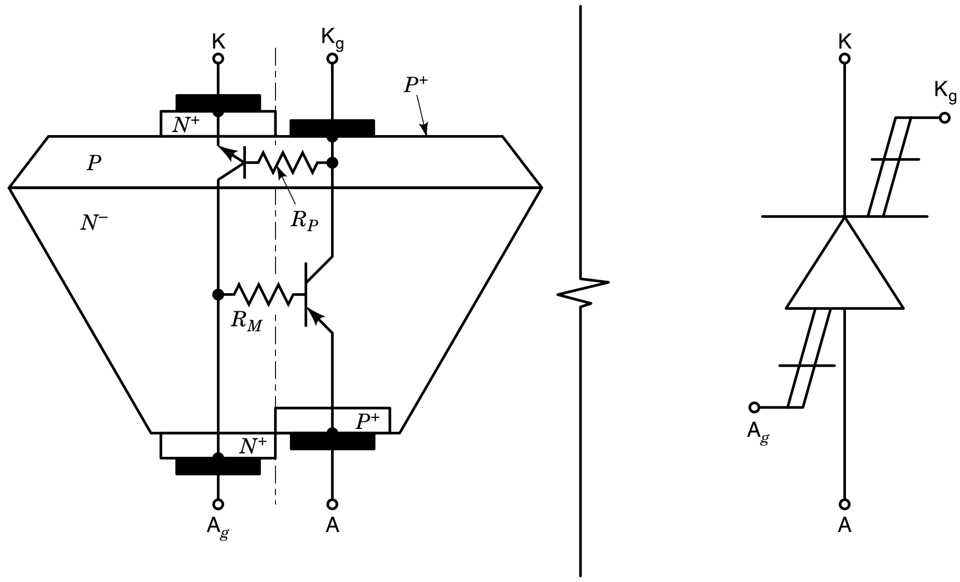


Figure 6. The *npn–pnp* model of the thyristor.

pnp and *npn* is avoided. With contacts to all four layers and a narrow and continuous emitter, the conducting *pnpn* structure can transition to a recovering (reverse-biased) *pin* diode by connecting both gates to their respective emitters. Thus, the external circuit will sweep charge from the recovering large-area central junction, rather than depending on open-base hole–electron trapped charge recombination as in conventional IGBTs, MCTs, or three-leaded GTOs. Open-base recovery is associated with low RBSOA, that is, a need for snubbers, high on-state and turnoff dissipation, low repetition rate, and low controllable current density, all of which can be avoided in the DGT.

Two-sided turnon triggering is typically required for fast turn-on; that is, ohmic contacts are provided to both anode and cathode gate regions of an asymmetric thyristor structure. High di/dt turn-on gating is achieved by connecting the anode and cathode gates together with a smaller *pilot* IGBT, resulting in simultaneous injection from both anode (holes) and cathode (electrons) emitters (Fig. 7).

Slow lateral plasma spreading, typical of SCRs, is avoided by use of a long continuous serpentine emitters on both sides of the chip, surrounded on both sides by gate metallization (Fig. 1). The lateral dimension from the center of the emitter to the gate metal edge is everywhere constant and shorter than 1 diffusion length. Unlike phase-control SCRs, turn on of the DGT will utilize the entire area of the serpentine emitter at the instant of turn-on, thereby enabling an indefinitely

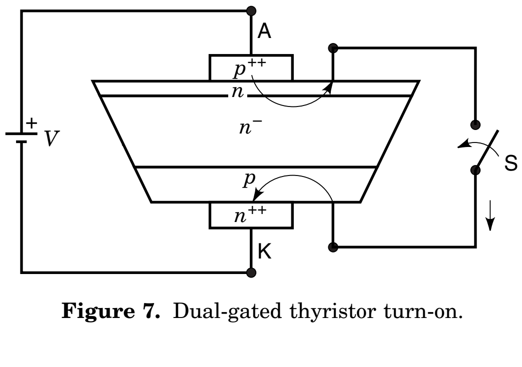


Figure 7. Dual-gated thyristor turn-on.

high-di/dt performance without failure. Triggering is effected by simply closing a FET (IGBT) switch (Fig. 7).

Pulse power thyristors (PPTs) operate at high emitter current densities of $>5 \times 10^4$ A/cm^2 with di/dt >20 kA/μs. Additionally, series stacks of chips are used to discharge capacitors from >35 kV. PPT chips can be series connected to block high voltage in increments of >3.3 kV, in packages only slightly larger than the chips, thereby enabling low-stray-inductance pulse power circuits, or pulse-forming networks (PFNs).

PPT thyristor design typically involves:

- Low-inductance stripline packaging
- Use of low-stray-inductance PFNs
- Hermetic passivation at the chip level
- Triggering for 20 kA/μs
- Characterizing the PPTs for pulse power operation in applications such as radar modulators, electromagnetic launchers, food and water purification, and as solid-state replacements for thyratrons, ignitrons, spark-gap switches, and mechanical switches.

A unique feature of pulse-power thyristor design is the absence of an adverse tradeoff between closing-switch and opening-switch thyristor design. Both closing- and opening-switch designs benefit from the narrow serpentine emitters on both sides of the chip, ohmic contact (and leads) to all four layers, and thick gate metal contacts and low spreading resistance under both anode and cathode emitters. Pulse-power opening-switch thyristors (PPOSTs) only differ from pulse-power closing-switch thyristors (PPCSTs) by having some sort of lifetime control (such as Au–Pt diffusion and/or electron radiation); that is, the same process used to make *pin* diodes faster via less stored charge. High-temperature voltage-blocking performance is another advantage of having contacts (leads) to all four layers of thyristors. When both anode and cathode gate leads are connected to their respective emitters (via resistors or active FET switches), the PPT has the same voltage-blocking performance as a *pin* diode. That is, PPTs will be capable of blocking voltage to >200°C, in comparison with 125°C for the traditional 3.3 kV thyristor. Access to all four *pnpn* layers enables both emitter switching and MCT switching for diodelike RBSOA, the best SOA known. Simply connecting the two PPT gates together (Fig. 7) also enables efficient turn-on and self-limiting di/dt.

TEMPERATURE CONTROL

Heat transfer and temperature control of semiconductors is a much more tractable problem than that of thyratrons, spark gaps, vacuum switches, or ignitrons. Typically two-sided cooled thyristors have a much lower thermal impedance than tube-type devices, thereby enabling a higher rms current. The Coulomb transfer characteristic typically used to rate tube-type switches is not as meaningful for thyristors. The typical device of 4 in. (10 cm) diameter can conduct several thousand amperes of direct current (dc). Unlike tubes, the low thermal impedance of thyristors enables the temperature to be maintained at a steady state. Tube-type switches typically have a much higher on-state resistance as well as a higher thermal impedance than solid state-devices, which severely limits their charge transfer capabilities in comparison with PPTs.

Thyristors were developed in the late 1950s to replace 200 V to ≈2000 V thyratrons. Light-fired thyristor stacks to >50 kV are now generally available. Radar transmitters also benefit from PPT technology for improved performance and higher efficiency.

TRIGGERING

Triggering DGTs is much simpler than for tube-type devices or traditional thyristors. For example, with both anode and cathode gates, a small high-voltage IGBT device (or small opto-PPT) can be used to simply connect the anode and cathode gates together, thereby forward-biasing both anode and cathode emitters for fast turn-on. The main power supply is therefore used for triggering; where the trigger current also serves as load current. As the main PPT modulates, less voltage is available for trigger current, so it automatically decreases the current after the critical di/dt turn-on stress interval is over, a very convenient feature. As voltage-triggered devices, the IGBTs will enable transformer-isolated triggering of multichip stacks using low-rated (≈5 V · μs) pulse transformers.

Traditionally, phase-control thyristor di/dt specification limits address a failure mode where the turn-on current is pinched to a small filament, causing a small di/dt melt hole along the edge of the gate–emitter junction closest to the gate region. With an adequate gate drive, PPTs do not fail in the traditional di/dt mode. Rather, the finite PPT switch turn-on time will act to self-limit di/dt in PFN discharge circuits, where stray inductance is a second-order effect in determining di/dt.

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TIME-DEPENDENT MAGNETIC REVERSAL. See MAGNETIC MEDIA, MAGNETIZATION REVERSAL.

TIMED GRAPHS. See DISCRETE EVENT SYSTEMS.

TIME DIVISION MULTIPLE ACCESS. See DEMULTIPLEXING EQUIPMENT.

TIME-DOMAIN. See TIME-DOMAIN NETWORK ANALYSIS.