TRAPS

Traps are the defects which can capture mobile charge carriers. In microelectronic devices, traps appear in the bulk of dielectric, at the dielectric/semiconductor interface, and within semiconductors. This article will focus on traps in the dielectric. Readers interested in interface traps and traps in semiconductors should read the article entitled SURFACE STATES and DEEP LEVEL TRANSIENT SPECTROSCOPY, respectively.

For the modern semiconductor industry, silicon dioxide (SiO_2) and silicon are the most widely used dielectric and semiconductor, respectively. Here we will concentrate on the trap in the SiO_2 prepared on silicon here. Readers interested in the trap in silicon nitrides may find more information in the article entitled THIN FILM DEVICES. Figure 1 shows that there are two types of traps, acceptor-like and donor-like. The acceptor-like trap can capture electrons and form negative space charges. The donor-like trap can capture holes or other positively charged species, such as hydrogen protons and form positive space charges. These trapped charges affect device operation in two ways. First, they change the potential distribution in a device and shift the device parameters, such as the threshold voltage. Second, they cause additional scattering of charge carriers in the nearby silicon, which in turn reduces carrier mobility. The closer a trap to silicon, the larger its effect.

Two important quantities for characterizing traps are capture cross section, σ, and density, N. The capture cross section is the effective physical size of a trap. Traps of different origins normally have different capture cross sections. For traps initially in a neutral state, also called neutral traps, the typical capture cross sections are 10^{-14} to 10^{-15} cm^2 for donor-like and 10^{-15} to 10^{-18} cm^2 for acceptor-like traps, respectively. Once traps are charged, they can be neutralized by capturing charge carriers of opposite sign. This process has much higher capture cross sections, on the order of $10^{-12} \sim 10^{-13}$ cm^2, due to the Coulomb attractive force. A charged trap, either acceptor-like or donor-like, is also called a Coulomb attractive trap. For the trap density, it is more convenient to use the number of traps per unit area, rather than per unit volume. For a metal-oxide-semiconductor field-effect-transistor (MOSFET), the trapped charge density in the gate oxide has to be above 10^9 cm^{-2} to have an observable effect. When the trapped charge reaches a level of 10^{13} cm^{-2}, the gate oxide will normally be broken down.

ORIGIN OF TRAPS

Impurity Traps

Atoms other than silicon and oxygen are here defined as impurities in SiO_2. There are three classes of impurities: hydrogen/water, implants, and sodium.

Hydrogen/Water-Related Traps

Acceptor-Like Traps. Hydrogen/water-related species can be introduced into the silicon dioxide during device fabrication. They act as acceptor-like traps with a capture cross section on the order of 10^{-18} cm^2 (1). Their distribution in the oxide is uniform. Water-related species can also diffuse into the oxide after fabrication, if the device is not properly encapsulated. These water centers capture electrons by releasing atomic hydrogen (2). The capture cross section is around 10^{-17} cm^2.

Donor-Like Traps. Hydrogen/water-related species can also form donor-like traps (3). These traps are located within a few nanometers from the SiO_2/Si interface. Their electrical status can be changed by the bias applied to the gate. Figure 2 shows that electrons can tunnel from silicon to the trapped charges and neutralize them under a positive gate bias. If a negative gate bias is applied, electrons can be returned to silicon and the traps become positive again. The time for this charging/discharging process generally spreads from less

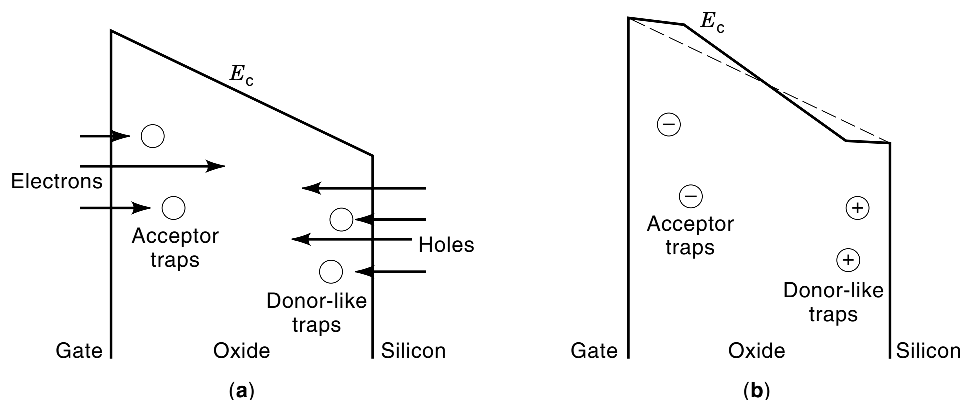

Figure 1. Charge trapping by the acceptor-like and donor-like traps in silicon dioxide. (a) Before charge trapping. (b) After charge trapping. The acceptor-like traps capture electrons and form negative space charges, while the donor-like traps capture holes and become positive. E_c is the bottom edge of the oxide conduction band. The negative space charge moves E_c upward and the positive space charge moves E_c downward.

J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*. Copyright © 1999 John Wiley & Sons, Inc.

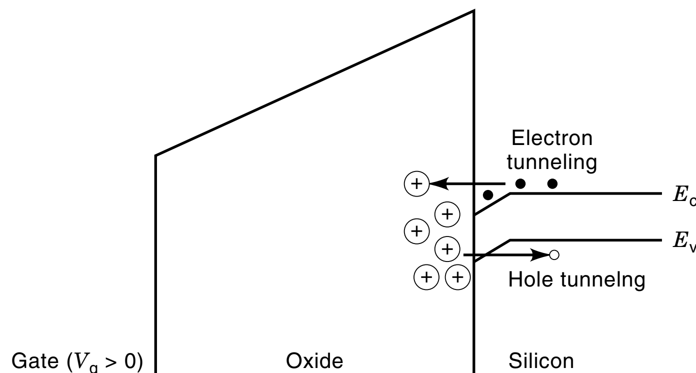

Figure 2. Detrapping of donor-like traps under a positive gate bias ($V_g > 0$). Since the donor-like traps are located closer to the oxide/Si interface, detrapping is dominated by carrier tunneling between traps and the substrate, rather than the gate.

than a millisecond to many hours. This is much longer than the time required for charging a trap at the SiO_2/Si interface, which is on the order of nanoseconds. For this reason, these donor-like traps are sometimes called *slow states.* Other names for them include *anomalous positive charges* and *border traps.*

The hydrogen/water induced acceptor-like and donor-like traps are important for silicon dioxides prepared at low temperature (<650°C) (4) by techniques such as chemical vapor deposition (CVD) and plasma oxidation. Their number can also be significant in silicon nitrides or nitrided oxides (often known as *oxynitrides*), if the nitridation gas contains hydrogen, such as NH_3 (5). For the silicon oxide grown on silicon at relatively high temperature (>900°C), the number of these traps can still be considerable (e.g., 10^{12} cm^{-2}) if a metal, such as aluminum, is used as the gate. When the ion-implanted polycrystalline silicon is used as the gate, it is necessary to anneal the device at a high temperature (e.g., 1000°C) to remove the damage induced by the implantation. This high-temperature process effectively drives the hydrogen/water species out of the device. After the annealing, the traps described will not be important.

Implantation Atom Related Traps. For MOSFETs, ion implantation is a standard technique for doping the polycrystalline Si gate, source, and drain. If the ion energy is not properly controlled, some atoms will be left in the gate dielectric. The implantation atoms can also diffuse into the dielectric during the postimplantation high-temperature annealing.

The most commonly used elements for implantation are arsenic (As) and phosphorus (P) as donors and boron (B) as acceptors. Boron in SiO_2 does not form traps itself, although it may assist in the retention of hydrogen/water-related species. As and P can act as both acceptor-like and donor-like traps. The dominant acceptor-like trap induced by As has a capture cross section in the range of 10^{-15} to 10^{-16} cm^2, which is independent of implantation energy and oxide thickness (6). The density of these electron traps is 0.7 to 1 times the ion density in the oxide. The P-induced acceptor-like trap behaves similarly to the As-related trap, except that the dominant capture cross section is on the order of 10^{-17} cm^2. The trap distribution of both acceptor-like and donor-like traps agrees well with the ion distribution. An increase of implantation energy moves the trap centroid away from the gate. Apart from As and P, the implanted fluorine (F) (7) can also trap electrons, with a capture cross section on the order of 10^{-18} cm^2.

Sodium-Related Traps. Sodium ions (Na^+) used to be one of the main sources for device instability. They can form two types of electron traps in SiO_2. The first is located 2.4 eV below the bottom of the conduction band of SiO_2. Because it is positively charged, its capture cross section can be as large as 10^{-12} cm^2. The second can only capture electrons effectively at low temperature (e.g., 77 K) and has a capture cross section in the order of 10^{-19} to 10^{-20} cm^2. The trapped electrons are located near the SiO_2/Si interface and will not be detrapped when the sample is warmed up to room temperature. In the modern semiconductor industry, the use of ultra-clean technology reduces the sodium contamination to a negligible level.

Defect and Generated Traps

Defect traps are the traps which cannot be attributed to a known impurity source. It is likely that only silicon and oxygen atoms are involved. These traps, together with interface traps, are the main sources for the degradation of transistors fabricated by modern semiconductor processes.

Donor-Like Traps. These traps can capture holes and sometimes are referred to as hole traps. They are located close to the SiO_2/Si interface, with a centroid typically a few nanometers from the interface. They have a dominant capture cross section on the order of 10^{-14} cm^2, although smaller capture cross sections were also reported. Their density is typically between 10^{12} and 10^{13} cm^{-2} (8). These traps exist in an as-grown sample and there is no clear evidence that they can be created by irradiation or electrical stress.

The defect structures proposed for hole traps include oxygen vacancies (9) and strained Si–O bonds (10). The oxygen vacancies can be formed because the number of Si atoms near the SiO_2/Si interface is more than the number of Si which can be incorporated into the normal SiO_2 network. Figure 3 shows the hole trapping process. The strained Si–O bond is caused by lattice mismatching between SiO_2 and Si. The density of both defects should reduce with distance from the SiO_2/Si interface, which agrees with the experimental observation.

Acceptor-Like Traps. For a gate oxide which has not been stressed by irradiation or a high electrical field, there are little acceptor-like traps. The capture cross section detected at low field (<6 MV/cm) is generally less than 10^{-19} cm^2 and is not

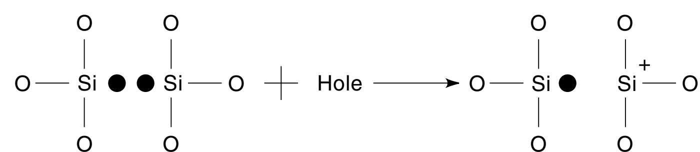

Figure 3. The microscopic structure of a hole trap, oxygen vacancy, and the trapping process. The symbol ● represents an electron. Note that the hole breaks the weak Si–Si bond and results in positive space charge.

well defined. As the number of electrons injected into the oxide for filling these traps increases, the trap density also increases and no clear saturation has been observed. It is most likely that these traps are actually created by the electron injection process.

Exposure of oxides to irradiation or a high electrical field (e.g., >6 MV/cm) can generate acceptor-like electron traps. Mobile holes and hydrogen species may be responsible for the damage. The generated traps have a capture cross section on the order of 10^{-16} to 10^{-17} cm^2, which is insensitive to the stress and device fabrication conditions (11). The trap density increases with stress time until the oxide breaks down. The created acceptor-like traps are uniformly distributed in the oxide. The structure of these traps is still not known.

TRAPPING KINETICS

First-Order Trapping Model

In this model, the trapping rate is assumed to be proportional to the number of empty traps, the number of mobile charge carriers available for trapping, and the capture cross section σ,

$$\frac{dN}{dt} = (N_s - N) \times nv \times \sigma \tag{1}$$

where N is the density of the number of filled traps, N_s is the density of total traps available, t is the time, n is the volume density of mobile charge carriers, and v is the velocity of charge carriers. The number of mobile charge carriers passing through a unit area in unit time, nv, can be related to the injection current density, J_{inj}, by

$$nv = \frac{J_{\text{inj}}}{q} \tag{2}$$

where q is one electron charge. Substituting Eq. (2) into (1) and integrating against time, we have

$$N = N_s(1 - e^{-\sigma N_{\text{inj}}}) \tag{3}$$

where N_{inj} is the number of charge carriers injected into the oxide per unit area,

$$N_{\text{inj}} = \frac{1}{q}\int_0^t J_{\text{inj}}\, dt \tag{4}$$

The number of trapped charges is an exponential function of N_{inj} and will therefore saturate at N_s.

If traps have more than one capture cross section, the total trapped carriers are the sum of the carriers captured by each cross section, and Eq. (3) can be replaced by

$$N = \sum_{i=1}^{m} N_{\text{si}}(1 - e^{-\sigma_i N_{\text{inj}}}) \tag{5}$$

where m is the number of capture cross sections, and N_{si} is the density of traps with a cross section of σ_{i}.

Applicability

This model has not taken trap generation and the detrapping of trapped carriers into account. When the oxide electrical field is sufficiently high (e.g., >6 MV/cm), trap creation and detrapping can be important and this model does not apply.

At relatively low fields, this model has been widely used for hole trapping with a typical capture cross section on the order of 10^{-14} cm^2. For the impurity-related acceptor-like traps, this model generally describes the trapping well. However, it is less certain if this model can be applied to the defect-related acceptor-like trap with a small capture cross section ($<10^{-19}$ cm^2). For these traps, the saturation behavior predicted by this model was not clearly observed. The most likely explanation for this nonsaturating behavior is that the trap has to be first created by electron injection, before it can capture electrons. The trapping rate can be dominated by trap creation. As the electron injection increases, more traps are created, which are responsible for the nonsaturation of electron trapping.

Difficulties have also been experienced when two capture cross sections are sufficiently close. The saturation behavior of traps with the larger capture cross section may not be observed due to the continuing trapping by the smaller capture cross section. This can lead to errors when capture cross sections and trap densities are estimated. In practice, two capture cross sections with a ratio less than five cannot be reliably determined by using this model (11).

DETRAPPING

The trapped charge can be detrapped optically, thermally, and electrically. The typical photo-detrapping energy is several electron-volts (>2 eV), and devices are rarely exposed to intensive light during practical operation. Readers interested in optical detrapping can find more information in Ref. 1. The thermally and electrically activated detrapping occurs concurrently and will be addressed here. We focus on the defect-related traps, since they are the most important for a device-grade gate oxide.

Detrapping Under Moderate Electrical Field

When a trap is located sufficiently close to an electrode, charge carriers can tunnel between them. The tunneling dominates the detrapping for an electrical field below 6 MV/cm. In comparison with the charge in acceptor-like traps, the charge in donor-like traps is generally less stable and the detrapping strongly depends on the polarity of gate bias. This is mainly so because the donor-like trap is located closer to the SiO_2/Si interface. Under positive gate bias, it is most likely that electrons from the silicon conduction band tunnel to the trapped positive charge and neutralize it, as is shown in Fig. 2, although hole tunneling to the valence band of Si cannot be ruled out. The tunneling time increases exponentially with the distance from the SiO_2/Si interface, which leads to a linear relation between the amount of charges detrapped and the logarithmic detrapping time. The thermal effect is weak at room temperature.

If the gate bias is negative, the charge carrier tunneling between Si and donor-like traps is suppressed, and so is the detrapping. For thin oxide (e.g., <20 nm), detrapping can take place by tunneling to the gate. Since the tunneling distance between the trap and the gate is longer than that between the trap and the substrate, the detrapping rate is significantly less.

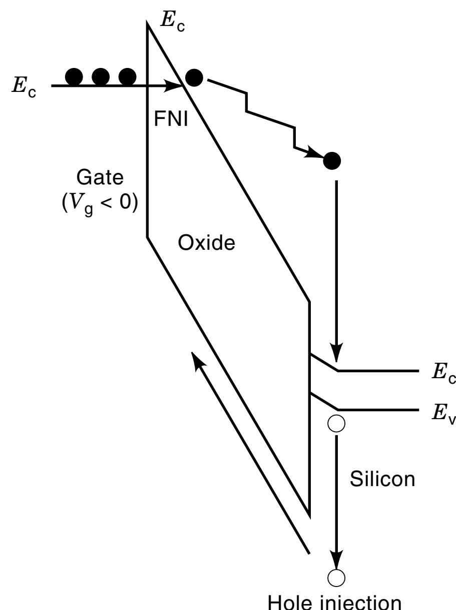

Figure 4. High field (>6 MV/cm) Fowler–Nordheim injection (FNI) under a negative gate bias. The high field reduces the width of potential barrier and allows electrons to penetrate it by tunneling. The electrons gain energy as they travel through the oxide. This energy can be partially transferred to holes and cause hole injection, when the electrons enter the anode.

When the temperature is increased to above 150°C, thermally activated detrapping becomes more important, especially when the gate bias is not positive. The trapped charge can be excited to a higher energy level and then tunnel away.

The acceptor-like traps are more difficult to detrap, since they are uniformly distributed. It is believed that the trapped electrons tunnel to the substrate or gate and the detrapping kinetics is qualitatively similar to that of donor-like traps.

Detrapping Under High-Field Fowler–Nordheim Injection

Figure 4 shows that when the electrical field across the oxide is above 6 MV/cm to 7 MV/cm the physical distance between the conduction band of SiO_2 and that of the gate becomes so thin that electrons can penetrate it. This is called *Fowler–Nordheim* tunneling. The electrons gain kinetic energy in the oxide and can create electron-hole pairs by impact ionization. When electrons enter the anode, the energy released can be transferred to holes and causes hole injection.

The Fowler–Nordheim injection (FNI) triggers additional detrapping processes, especially for the acceptor-like traps (12). The trapped negative charges can be detrapped by recombination with holes. As a result, the trap occupancy is typically low (e.g., <20%) and decreases with increasing electrical field. The relative importance of recombination for detrapping depends on oxide thickness. For thick oxides (>20 nm), recombination dominates detrapping. As the oxide becomes thinner, electrons gain less energy through the oxide and the probability for hole generation is reduced. As a result, the field-assisted tunneling will make a larger contribution. The detrapping of donor-like traps is again more efficient under positive gate bias. When the gate bias is negative, Fig. 4 shows that electrons are highly energetic when they pass through the SiO_2/Si interfacial region, where positive charges are trapped. This reduces the recombination probability.

EFFECTS OF TRAPS AND TRAPPED CHARGES ON DEVICE PERFORMANCE

Trapping Under Irradiation

The energy bandgap of SiO_2 is about 9 eV. When devices operate in an irradiation environment, such as a spacecraft, particles with energy higher than 9 eV can create electron-hole pairs in the bulk of the oxide. Although both electrons and holes are available for trapping, the trapping efficiency of electrons is generally much lower than that of holes, mainly because the capture cross section of hole traps is several orders of magnitude larger. The hole trapping efficiency strongly depends on the gate bias polarity. Under positive gate bias, Fig. 5 shows that the created holes are pushed toward the SiO_2/Si interface, where hole traps are located. As a result, trapping efficiency is high. Under a negative gate bias, holes are pulled away from the trap and the trapping efficiency is drastically reduced.

For MOSFETs operating in an irradiation environment, the main instability phenomenon is a negative shift of the threshold voltage, because of the trapped hole. This increases the leakage current of an *n*-channel MOSFET in its off-mode and reduces the driving current of a *p*-channel transistor in its on-mode.

High Field Induced Trapping and Traps

During the initial stage of the Fowler–Nordheim injection, hole trapping often has a stronger effect on devices, mainly because of its larger capture cross section. The hole trapping is stronger under negative gate bias, since a positive gate bias causes efficient detrapping. As the injection continues, more acceptor-like traps will be created and the effect of electron

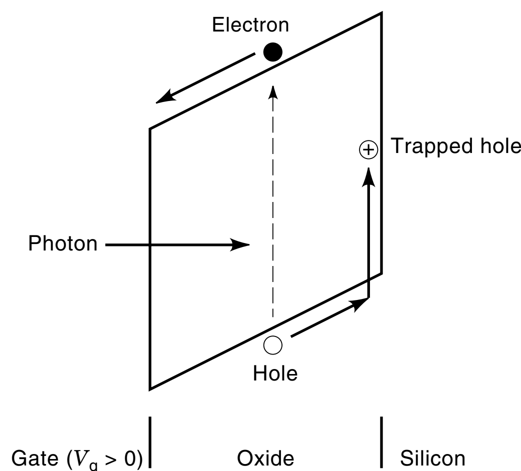

Figure 5. Electron–hole pair generation and hole trapping under irradiation with a positive gate bias. Since electron mobility is 10^5 times higher than hole mobility in the oxide, electrons are swept out from the gate. Holes are driven toward the oxide/Si interface, where hole traps are located. This leads to a net positive charge in the oxide.

trapping becomes more important. As was mentioned earlier, the trapped positive and negative charges shift the threshold voltage and reduce carrier mobility.

The high field injection can create new acceptor-like traps (11). Most of them are not filled after high field stress, because of high detrapping efficiency. These empty traps can also affect device operation by acting as “stepping-stones” for electron tunneling between gate and substrate at relatively low field (<6 MV/cm). As the oxide thickness is reduced, this stress-induced gate leakage current is increasingly important. When the number of electron traps reaches the order of 10^{13} cm^{-2}, they can form a conduction path and cause the breakdown of oxide (13).

Trapping Under Hot Carrier Stress

Hot carrier stress causes device degradation by creating interface traps and charge trapping in the oxide. The relative importance of charge trapping depends on the types of devices and the ratio between the stress gate voltage, V_g, and the drain voltage, V_d. For *n*MOSFETs, hole trapping is important when $V_g < V_d/4$, since the gate is negatively biased against the drain, which promotes hole injection. As V_g/V_d increases, the contribution of electron injection increases. For pMOSFETs of relatively larger size (>0.25 μm), electron trapping dominates the degradation for $V_g/V_d < 1$, since the gate is biased positively against the drain, which is in favor of electron injection. The effect of interface trap creation becomes stronger for *p*MOSFETs of shorter channel length. Readers can find more information on this topic in the article entitled HOT CARRIER EFFECTS of this encyclopedia and in Ref. 14.

MEASUREMENT TECHNIQUES

To characterize the traps in oxides, charge carriers have to be injected into the oxide. Ideally, only one type of charge carriers (electrons or holes) should be injected uniformly at one time and injection itself should not create new traps. This requirement makes irradiation and Fowler–Nordheim injection unsuitable for measuring traps. Two techniques have been developed for injecting charge carriers into the oxide at a relatively low electrical field, avalanche injection and substrate hot carrier injection. After traps are filled by the injected carriers, they will be measured by using charge sensing techniques. For avalanche injection, the capacitance–voltage (*C–V*) technique is used as the sensing technique. For substrate hot carrier injection, the subthreshold transfer characteristic is often used for charge sensing.

Avalanche Hot Carrier Injection

Injection of Charge Carriers. This technique uses a MOS capacitor as the testing device. For electron injection, the gate voltage often has a square waveform and *p*-type Si is used as substrate (2). When the gate voltage is switched from negative to positive, the *p*-type substrate will be driven from accumulation into deep depletion, before electrons can be thermally created. This creates a transient electrical field in the space charge region, which can be high enough to cause avalanche breakdown. The created electrons are accelerated toward the SiO_2/Si interface and some of them will have enough energy to be injected into the oxide, while others will be neutralized by recombining with holes when the gate bias returns to negative.

On the basis of the same principle, hot holes can be injected into the oxide if the substrate is *n*-type (10). However, since the energy barrier at the SiO_2/Si interface for holes (~4.6 eV) is higher than that for electrons (~3.2 eV), hole injection is more difficult. Care has to be taken to suppress the simultaneous electron injection from the gate. It has been proposed that a sawtooth waveform can suppress electron injection better than a square waveform (10).

Monitoring the Trapped Charges. The injection is periodically interrupted and the capacitance–voltage (*C–V*) characteristic is monitored to measure the trapped charges. The voltage shift at a constant capacitance, ΔV_g, is related to the trapped charges by

$$\Delta V_g = -\frac{1}{C_0}\int_0^{x_0}\left(1-\frac{x}{x_0}\right)\rho\,dx \tag{6}$$

where C_0 is the oxide capacitance per unit area, x_0 is the oxide thickness, and ρ is the volume density of trapped charges. The SiO_2/Si interface is the origin of the x coordinate taken positive toward the SiO_2/gate interface. If we define the centroid of the trapped charge, x_c, as

$$x_c = \int_0^{x_0}\rho x\,dx \Big/ \int_0^{x_0}\rho\,dx$$

and the trapped charge per unit area, Q, as,

$$Q = qN = \int_0^{x_0}\rho\,dx$$

then Eq. (6) can be written as

$$N = -\frac{C_0\Delta V_g}{q}\frac{x_0}{x_0 - x_c} \tag{7}$$

Apart from the charges trapped in the oxide, the interface traps created during avalanche injection can also contribute to ΔV_g. The accuracy of the measurement depends on the ratio of these two contributions. The effect of the generated interface traps depends on the potential at the SiO_2/Si interface. It has been proposed that interface traps remain neutral when this potential is at the middle of Si energy bandgap. As a result, ΔV_g is normally measured at the midgap voltage to minimize the contribution of interface traps.

By using Eqs. (4) and (7), the number of charge carriers injected and trapped in the oxide can be experimentally determined, respectively, if the charge centroid is known. These data can then be fitted into Eq. (5), based on the least-squares criteria, to extract the capture cross section and trap density.

Disadvantages. Two disadvantages of this technique are that the electrical field across the oxide is transient during the injection and the injection current cannot be independently controlled from the electrical field. This makes it unsuitable for studying the dependence of trapping on the elec-

trical field. The typical average electrical field strength cross the oxide is estimated to be 3 MV/cm to 4 MV/cm. This is high enough to cause the anomalous positive charge formation during electron injection if the gate is aluminum, which reduces the accuracy for extracting the capture cross section and trapped charge density (3).

Substrate Hot Carrier Injection

Carrier Injection Mechanism. This technique uses MOSFETs operating in strongly inversion. Here, we use hole injection as an example to illustrate the principle (15). Figure 6 shows that the source and drain are grounded and the oxide field is determined by the negative gate bias. The electrical field in the space charge region is controlled by applying a positive bias to the *n*-type silicon layer. There are two methods for introducing holes into the space charge region. One of them is optically generating electron-hole pairs. The other is electrically injecting holes into the *n*-region by forward biasing the *p*–*n* junction beneath the conduction channel, as is shown in Fig. 6. Under a constant oxide field, the injection current can be independently varied by either increasing the hole supply or the bias applied to the *n*-region. On the basis of the same principle, electrons can be injected into the oxide by using *n*MOSFETs.

There are two factors which can affect the injection uniformity. The first one is the potential drop due to the lateral current flowing from the middle of the channel toward the source and drain. For a channel length over 100 μm, this potential drop may not be negligible. However, for transistors with a channel length of several tens of micrometer or less, this potential drop is generally less than 0.1 V under normal experimental conditions. The second factor is that the strong inversion at the interface may not be maintained, as the buildup of trapped charges in the oxide increasingly screens the substrate from the gate. Without a strong inversion layer at the interface, the potential can vary in the lateral direction.

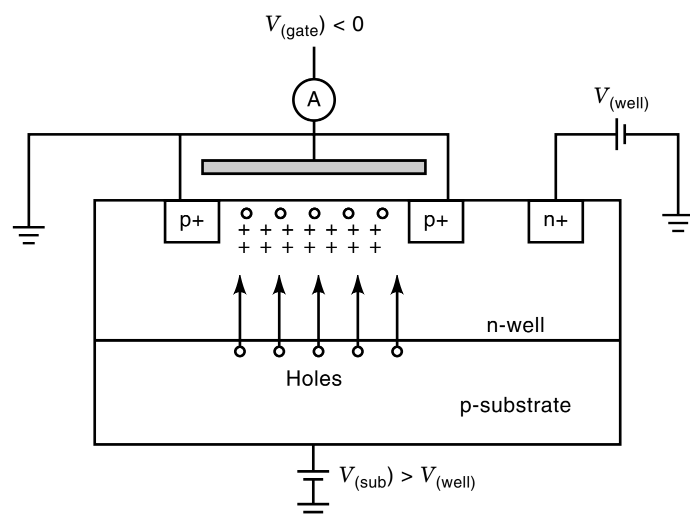

Figure 6. The set-up for substrate hot hole injection. Holes are supplied by forward biasing the *p*-substrate/*n*-well junction. They are then accelerated by the high field in the space charge region. Some of the hottest holes are injected into the oxide, while others are collected from the source and drain.

Density of Injected Charge Carriers. To determine the number of injected charge carriers from Eq. (4), the injection current density, J_{inj}, must be known. The J_{inj} generally does not equal the current density measured either from the gate or from the substrate. This is because of charge trapping and the associated displacement current, as is demonstrated by the following example.

Here, holes are injected from the substrate into the oxide and the current is measured from the gate. The current continuity equation can be written as,

$$q\frac{\partial p}{\partial t} = -\frac{\partial J_{\text{inj}}}{\partial x}$$

where p is the volume density of trapped holes. Integrating from $x = 0$ to $x = x_0$, we have,

$$J_{\text{inj}}(0) - J_{\text{inj}}(x_0) = \int_0^{x_0} q\frac{\partial p}{\partial t}\,dx \tag{8}$$

This expression shows that the charge trapping reduces the hole flux coming out of the gate. The positive charge in the oxide can also attract more electrons to both gate/SiO_2 interface and substrate/SiO_2 interface. The generated gate displacement current can be expressed as

$$J_{\text{gd}} = \int_0^{x_0} q\,\frac{x}{x_0}\frac{\partial p}{\partial t}\,dx \tag{9}$$

The total gate current is,

$$J_{\text{g}} = J_{\text{gd}} + J_{\text{inj}}(x_0) \tag{10}$$

Substituting Eqs. (8) and (9) into (10), we have

$$J_{\text{g}} = J_{\text{inj}}(0) - \frac{\partial}{\partial t}\int_0^{x_0}\left(1 - \frac{x}{x_0}\right) qp dx \tag{11}$$

An evaluation of the integration gives

$$\int_0^{x_0}\left(1 - \frac{x}{x_0}\right) qp dx = C_0\Delta V_{\text{g}} \tag{12}$$

Substituting Eq. (12) into (11) and integrating with respect to time, we have

$$N_{\text{inj}} = \frac{1}{q}\int_0^t J_{\text{inj}}(0)\,dt = \frac{1}{q}\int_0^t J_{\text{g}}\,dt - C_0\Delta V_{\text{g}} \tag{13}$$

where J_g can be measured experimentally.

For hole trapping, the second term in Eq. (13) is important and must be taken into account. However, for electron trapping in a device-grade gate oxide, its contribution to the total current is generally negligible.

Detection of the Trapped Charges. The trapped charges were monitored by periodically interrupting the injection and measuring the shift in the gate voltage corresponding to a con-

stant drain current. The current level has to be in the subthreshold region, so that the effect of trapped charges on carrier mobility is negligible. To minimize the contribution of interface traps to ΔV_g, the current level should be as low as it can be measured reliably. After taking these factors into consideration, the ΔV_g will be proportional to the trapped charges and Eq. (7) is also applicable here.

Distribution of Trapped Charges

Although the above techniques fill up the traps, they cannot determine the trap distribution in the oxide. The centroid of trapped charges can be determined by using the photo-IV technique, where electrons are alternately injected into the oxide from the two electrodes by internal photoemission (1). If the trapped charges are located closer to the SiO_2/Si interface, they will cause a larger ΔV_g when the injection is from the Si ($V_g > 0$), compared with the injection from the gate ($V_g < 0$). The centroid of trapped charges is determined by

$$x_c = \frac{|\Delta V_g(V_g < 0)|}{|\Delta V_g(V_g < 0)| + |\Delta V_g(V_g > 0)|} x_0$$

The main difficulty in this technique is that the gate is required to be transparent, while the polycrystalline Si gate is normally not. Other techniques include using samples of different oxide thickness and injecting from both interfaces under Fowler–Nordheim condition. The former requires preparing samples of different oxide thickness and is rarely used. The latter is based on the same principle as photo-IV, but uses a relatively high electrical field (>6 MV/cm), which can disturb the trapped charge during the measurement. In practice, most researchers simply assume that all traps are located at the SiO_2/Si interface and extract an effective density of the trapped charge.

BIBLIOGRAPHY

1. D. J. DiMaria, The properties of electron and hole traps in thermal silicon dioxide layers grown on silicon, in S. T. Pantelides (ed.), *The Physics of SiO_2 and Its Interfaces,* New York: Pergamon, 1978, pp. 160–178.
2. E. H. Nicollian, C. N. Berglund, P. F. Schmidt, and J. M. Andrews, *J. Appl. Phys.,* **42** (13): 5654–5664, 1971.
3. D. R. Young, E. A. Irene, D. J. DiMaria, R. F. De Keersmaecker, and H. Z. Massoud, Electron trapping in SiO_2 at 295 and 77 K, *J. Appl. Phys.,* **50** (10): 6366–6372, 1979.
4. J. F. Zhang, S. Taylor, and W. Eccleston, A comparative study of the electron trapping and thermal detrapping in SiO_2 prepared by plasma and thermal oxidation, *J. Appl. Phys.,* **72** (4): 1429–1435, 1992.
5. D. J. DeMaria and J. H. Stathis, Trapping and trap creation studies on nitrided and reoxidized-nitrided silicon dioxide films on silicon, *J. Appl. Phys.,* **70** (3): 1500–1509, 1991.
6. R. F. De Keersmaecker and D. J. DiMaria, Electron trapping and detrapping characteristics of arsenic-implanted SiO_2 layers, *J. Appl. Phys.,* **51** (2): 1085–1101, 1980.
7. L. Vishnubhotla and T. P. Ma, *Appl. Phys. Lett.,* **59** (27): 3595–3597, 1991.
8. G. Van den bosch, G. Groeseneken, H. E. Maes, R. B. Klein, and N. S. Saks, Oxide and interface degradation resulting from substrate hot-hole injection in metal-oxide-semiconductor field-effect transistors at 295 and 77 K, *J. Appl. Phys.,* **75** (4): 2073–2080, 1994.
9. H. S. Witham and P. M. Lenahan, Nature of the E' deep hole trap in metal-oxide-semiconductor oxides, *Appl. Phys. Lett.,* **51** (13): 1007–1009, 1987.
10. S. K. Lai, Interface trap generation in silicon dioxide when electrons are captured by trapped holes, *J. Appl. Phys.,* **54** (5): 2540–2546, 1983.
11. J. F. Zhang, S. Taylor, and W. Eccleston, Electron trap generation in thermally grown SiO_2 under Fowler–Nordheim stress, *J. Appl. Phys.,* **71** (2): 725–734, 1992.
12. J. F. Zhang, S. Taylor, and W. Eccleston, A quantitative investigation of electron detrapping in SiO_2 under Fowler–Nordheim stress, *J. Appl. Phys.,* **71** (12): 5989–5996, 1992.
13. R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides, *Proc. Int. Electr. Dev. Meet.* 863–866, 1995.
14. C. T. Wang (ed.), *Hot Carrier Design Considerations for MOS Devices and Circuits,* New York: Van Nostrand Reinhold, 1992.
15. G. Van den bosch, G. Groeseneken, and H. E. Maes, Critical analysis of the substrate hot-hole injection technique, *Solid-State Electron.,* **37** (3): 393–399, 1994.

JIAN FU ZHANG
Liverpool John Moores University

TRAPS, INTERFACE. See SURFACE STATES.

TRAUMA FROM ELECTRIC SHOCK. See ELECTRIC SHOCKS.