MAGNETIC LOGIC

A *logic gate* is an arrangement, or cell, of electronic devices that performs a specific logic operation. Boolean functions are processed in the form of binary signals (LOW and HIGH, or 0 and 1) applied to two inputs A and B of the specified logic gate. The binary output (LOW and HIGH, or 0 and 1) of a particular Boolean function (AND, OR, XOR, etc.) is determined by the particular arrangement of elements that comprise the cell; see BOOLEAN FUNCTIONS. For example, a particular arrangement of four CMOS FETs (both p-channel and n-channel) may form an AND gate (1), while another arrangement may comprise an OR gate; see FIELD EFFECT TRANSISTOR MEMORY CIRCUITS. These-low level logic gates are arranged together to perform higher-level functions, such as binary addition or multiplication; see LOGIC DESIGN. Most logic gates are nonlatching, and therefore the result (output) from a logic operation is usually passed to a separate memory cell to await further processing at some later clock cycle.

Speed, power, and packing density are important parameters in the design of digital information processing, all of which depend on the complexity of the elements that comprise the logic cell. Continuing the example above, each FET and interconnect has an associated delay time and power dis-

sipation and occupies some area. Alternatives to CMOS (and, more generally, semiconductor) logic are sought in an effort to increase speed and packing density and to decrease power consumption. One approach uses superconductors. Magnetic logic provides another approach, with several advantages: (1) The number of elements and interconnects per logic cell is smaller, thereby increasing both speed and packing density while decreasing power consumption. (2) The result can be latched, which in some applications can be used to combine the functionality of logic cell and memory cell. (3) A single fabricated logic cell can be "reprogrammed" to perform more than a single (Boolean) logic operation; see PROGRAMMABLE LOGIC DEVICES. Magnetic logic is presently at the research stage, and many issues remain for engineering and development. Progress will be aided by the numerous industrial research and development programs centered on integrated, nonvolatile random access memory.

CONCEPT

An intrinsic property of ferromagnetic materials has a fundamentally binary nature: The saturation magnetization $\boldsymbol{M}_s$, when measured along a chosen axis $\hat{r}$, has two values $\pm M_s$ depending on the bistable orientation ($\pm\hat{r}$) with respect to that axis. Because of this, devices and media that incorporate magnetic materials can be applied to digital applications such as storage—see MAGNETIC RECORDING HEADS; MAGNETIC STORAGE MEDIA; MAGNETIC BUBBLE MEMORY—and logic.

Bistable Ferromagnetic Films

Figure 1 illustrates the bistability of a thin ferromagnetic film with an anisotropy axis induced along an arbitrary axis, for example, the $\hat{x}$ axis, by plotting the magnetization M as a function of externally applied magnetic field H. For positive fields H much larger than the coercivity H_c, the magnetization is saturated with value M_s and has orientation $+M\hat{x}$. Equivalently stated, the magnetization of the thin film is a single domain oriented along $+\hat{x}$. As H is reduced to zero (dashed trace), the induced anisotropy preserves the orientation along $+\hat{x}$, as seen by the high remanence in the top part of the loop, $M(H = 0) \equiv M_r = M_s$. When the magnitude of H is increased along $-\hat{x}$ to a value larger than the coercivity, $H < -|H_c|$, the magnetization reorients, now having a saturation value and an orientation along $-\hat{x}$. Now the thin film magnetization is a single domain with orientation along $-\hat{x}$. The same process occurs in reverse order for fields increasing along $+\hat{x}$ (solid trace). The hysteresis loop of Fig. 1 is an example of a bistable ferromagnetic film: In zero field, the remanent magnetization has two stable values, $\pm M_s$. Any not entirely square hysteresis loops are also characterized by a switching field H_s, the field magnitude required to switch completely to a saturated state. Thin ferromagnetic films with M–H loops comparable with that of Fig. 1 can be fabricated by using a variety of techniques (2), for thicknesses of order 10 nm to 100 nm; see MAGNETIC MATERIALS.

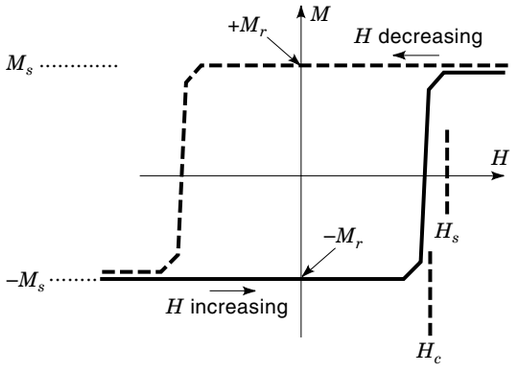

Figure 1. A thin ferromagnetic film with uniaxial anisotropy along $\hat{x}$ has a square hysteresis loop. The magnetization can be oriented along $\pm\hat{x}$, with a magnitude equal to the saturation value, M_s. The remanent magnetization, $M(H = 0) \equiv M_r$, is equal to M_s.

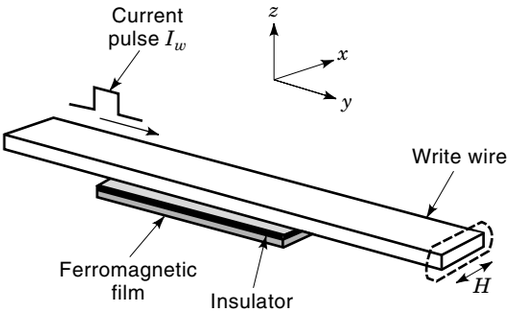

Figure 2. A "write wire" is a thin film microfabricated wire electrically isolated from, but inductively coupled to, a ferromagnetic film that is a component of a magnetoelectronic device. A positive write current transmitted along $\pm\hat{y}$ generates a local magnetic field H along $\pm\hat{x}$ in the vicinity of the ferromagnetic film, thereby controlling the magnetization orientation.

Binary Device Output

The binary capability of magnetic materials is adapted to digital applications by incorporating a ferromagnetic film as a portion of a magnetoelectronic device. The output state of such a device has one of two bistable values depending on the orientation of the ferromagnetic film, with the relatively low and high output values equated with logical LOW and HIGH, 0 and 1. The device is typically biased with a small "read" current I_r and the output is a voltage, V. A number of magnetoelectronic devices are reviewed below. Some of them, including spin transistors and hybrid hall effect devices, have bipolar output states $\pm V'$. Appropriate offset resistances can be added so that the output states corresponding to LOW and HIGH are $V = 0$ and $V = 2V' = V_0$. Other magnetoelectronic devices are based on magnetoresistance, such as "magnetoresistive magnetic multilayers" and "magnetic tunnel junctions," and have output states of V and $V + \delta V$ corresponding to the two stable resistance values R and $R + \delta R$. Such a device is paired with a reference resistor R so that difference voltages $V = 0$ and $V = \delta V$ correspond to the binary LOW and HIGH states.

Binary Device Input

The binary states of ferromagnetic thin films are addressed by inductively coupling them to digital electric currents carried by integrated "write wires." Figure 2 is a sketch of a microfabricated, thin film write wire and a ferromagnetic film. When the wire carries a positive current I_w, a magnetic fringe

field H surrounds the wire with a clockwise orientation. Beneath the wire, the field is parallel to the film plane and has magnitude that is directly proportional to the amplitude of current and is weakly dependent on distance z from the wire's center, $H_x(z) \approx \alpha I_w$, where α is an inductive coupling parameter that depends on geometry and configuration.

The HIGH and LOW input values are determined by the requirement that the field H_x must be greater than the switching field H_s of the the ferromagnetic element, as shown in Fig. 3(a). For example, when the write current amplitude is set to the value $I_w = I'$, the magnetization orientation is set along $+\hat{x}$ and, similarly, a write current of $I_w = -I'$ sets the orientation to be along $-\hat{x}$. Thus the LOW and HIGH input states correspond to $-I'$ and $+I'$, respectively. The field H_x must be applied for a duration equal to the magnetization reversal time. This can be achieved using current pulses with duration the order of ps to ns, with current amplitudes that are the order of mA (3). The switching field of typical magnetoelectric devices is 10 Oe to 100 Oe, and a current I_w = 1 mA in a 1 μm wide write wire generates a field of about 10 Oe.

Since the interaction between magnetization and electric charge is inductive, digital magnetic logic is described with the use of electric currents. Whereas semiconductor logic (e.g., CMOS) is based on voltage pulses of discrete levels, magnetic logic uses pulses of current and may require circuit elements to convert voltages to currents. Depending on the particular application, the conversion can be achieved with an appropriate resistor, or may also involve an inverting (or noninverting) buffer amplifier.

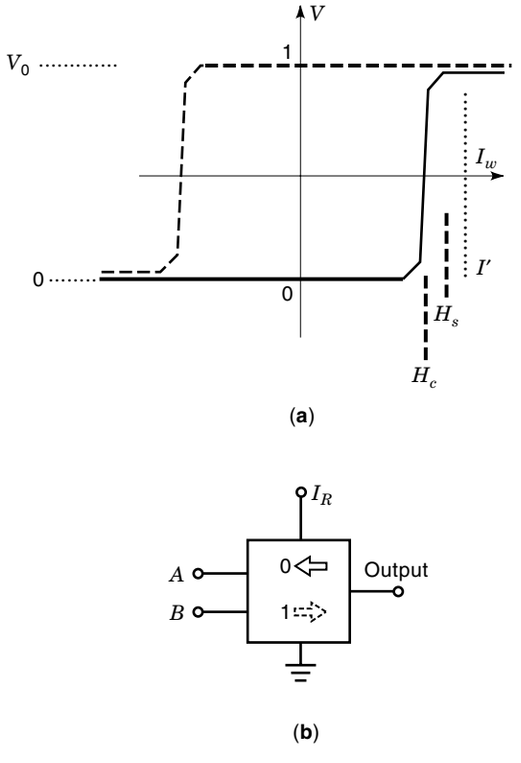

Figure 3. (a) The inductance of the write wire and the voltage characteristic of the magnetoelectronic device are used to convert the M–H loop of the ferromagnetic film of Fig. 1 to a V–I loop of a magnetic logic cell. (b) A schematic representation of a magnetic logic cell. The bistable state of the device is associated with the magnetization orientation of a ferromagnetic component. Physical embodiments of the cell can be composed of all-metal spin transistors, hybrid hall effect devices, or magnetoresistors.

LOGIC GATES

Figure 3(a) combines the binary input and output definitions developed above to present the M–H loop of a ferromagnetic thin film as a V–I characteristic of the generic magnetoelectronic device depicted in Fig. 3(b). The arrows inside the diagram of Fig. 3(b) are a graphic representation of the bistable nature of the device: the magnetization can be oriented along $-\hat{x}$ (LOW, or 0) or along $+\hat{x}$ (HIGH, 1), states which are denoted in Fig. 3(a) by 0 and 1. Examples of specific magnetoelectronic device embodiments of the schematic cell of Fig. 3(b) are discussed below. The principle of magnetic logic can be explained with the loop of Fig. 3(a), where it is understood that input terminals A and B are separate terminals to a write wire that is integrated with the ferromagnetic element of an appropriate magnetoelectronic device. Whereas semiconducting logic is steady state biased at a supply voltage (V_{DD}) and operates at a fixed clock frequency, magnetic logic is automatically latching: input pulses at A and B must be coincident but the *output* is achieved at any later time by biasing the device with a single read pulse I_R.

Simple Boolean Functions

The schematic device of Fig. 3(b), with characteristics described by the V–I loop of Fig. 3(a), performs basic Boolean logic operations using two clock steps. The first step initializes the device and the second step sets the device state according to the values of input current pulses. The latched result is "read" some time later by applying a readout bias current pulse I_R and sensing a LOW or HIGH voltage pulse. The normalized value of the write current is effected by using an appropriate conversion circuit element, which may be constant or variable.

Table 1 summarizes logic operation for the four Boolean processes OR, NOR, AND, and NAND. As seen with the aid of Fig. 3(a), when the write current is normalized to a value I' and the initialization step sets the state of the device to be 0 (magnetization $-M\hat{x}$), the device functions as an OR gate. Input write pulses of amplitude I' applied to A or B are sufficient to reset the device state to 1 (reorient the magnetization to $+M\hat{x}$), and a read bias pulse applied at some later time will result in a relatively HIGH voltage (V_0, 1) sensed at the *output.* Similarly, when the normalized write current has opposite polarity and the initialization step sets the state of the device to 1 the function of the device is inverted: It is now a NOR gate. When the write current is normalized to a value $(I')/2$ and the initialization step sets the state to be 0, the device operates as an AND gate. Now input current pulses of amplitude $(I')/2$ must be simultaneously applied to both A and B in order to reset the device state. Opposite polarity write current provides the NAND gate function. XOR and XNOR functions can be achieved in a similar way.

Programmable Gates

Table 1 demonstrates one of the unique features of magnetic logic: a single device can perform any of four Boolean opera-

Table 1. Values of Write Current Amplitude and Initialization Pulse for Boolean Operations, and the Equivalent Truth Table

	Normalized Amplitude	Initialization	A	B	Output
OR	I'	$-I'$	0	0	0
	I'	$-I'$	0	1	1
	I'	$-I'$	1	0	1
	I'	$-I'$	1	1	1
NOR	$-I'$	I'	0	0	1
	$-I'$	I'	0	1	0
	$-I'$	I'	1	0	0
	$-I'$	I'	1	1	0
AND	$(I')/2$	$-I'$	0	0	0
	$(I')/2$	$-I'$	0	1	0
	$(I')/2$	$-I'$	1	0	0
	$(I')/2$	$-I'$	1	1	0
NAND	$-(I')/2$	I'	0	0	1
	$-(I')/2$	I'	0	1	1
	$-(I')/2$	I'	1	0	1
	$-(I')/2$	I'	1	1	1

tions. Because of the fundamental properties of the device, it is intrinsically a *programmable* or *configurable* logic cell. Simple circuit elements on a chip can be used to determine the normalized write amplitude for cell input, and the function of the cell can then be determined programatically. For example, the same physical device could perform different functions at different clock cycles. This is a unique approach to *reprogrammable logic,* also called *field programmable* or *configurable logic;* see PROGRAMMABLE LOGIC ARRAYS; PROGRAMMABLE LOGIC DEVICES. Advantages include the ability to program low level logical functions rapidly.

Higher Functions

Basic, low level magnetic logic cells such as represented by Fig. 3(b) can be combined into larger cells to perform higher-level functions such as binary addition, subtraction, and multiplication. Whereas most techniques used for configurable logic involve high-level blocks of cells and many techniques are irreversible, magnetic logic offers the possibility of reprogramming basic functional blocks such as a full bit adder or a shift register.

GAIN AND FANOUT

When connecting cells together to perform higher-level operations, the necessity of using the ouput of a device at one stage to drive the input of one or more devices at the next stage is called *fanout.* Fanout requires that the gain of the device cell must be one or greater. Equivalently stated, the output voltage (or current) must be equal to, or greater than, the input voltage (or current). For example, the design of the fully restored CMOS logic family uses n-channel and p-channel FETs at the output stage to set the output LOW and HIGH voltage levels to V_{SS} and V_{DD}, respectively, thereby meeting the required input levels for the next stage.

Magnetoelectronic devices are passive and have low gain. Two methods can be used to achieve fanout. In the first, the read bias current can be adjusted to a value much larger than the required write current. For example, a prototype hybrid hall device (4), a magnetoelectronic device discussed below, has demonstrated a gain of 0.25 with a read bias current of 4 mA. With 25% of the bias current available as output (levels 0 and 1 mA), it could drive a single OR gate (or several in series) with a write amplitude $I' = 1$ mA ($H_x = 10$ Oe). Fanout of this kind is therefore plausible, but a circuit with linked devices has not yet been fabricated. However, for write currents of order mA and voltage supplies of 1 V to 5 V, the required range of bias currents can be achieved. The second approach is essentially the same as used in CMOS cells: Two FETs are used to set the output to standard CMOS levels.

Magnetoelectronic Devices

One category of magnetoelectronic devices is characterized by intrinsically bipolar output. The all-metal spin transistor (5) and the hybrid hall effect device (4) are examples of this group. The former are low impedance devices (0.1 Ω to 10 Ω), and the impedance of the latter can be tuned over the range of tens of ohms to tens of kiloohms. They have bipolar output states $\pm V'$ which are conveniently converted (with or without amplification) to the bipolar input write currents of a succeeding stage. Alternatively, appropriate offset resistances can be incorporated as a portion of the device so that the output states corresponding to LOW and HIGH are $V = 0$ and $V = 2V' = V_o$. Fabricated with transition metal ferromagnetic films with switching fields of about 30 Oe, these devices have demonstrated intrinsic (current) gains ranging from ±1% to ±12% (25% for unipolar output). In principle, they can achieve a gain of 1.

In the second category of magnetoelectronic structures, magnetoresistive devices (6) can be based on the magnetoresistance of (1) anisotropic current flow in a single ferromagnetic film, (2) a trilayer or multilayer stack of magnetic and nonmagnetic metal layers, (3) a perovskite oxide ferromagnet, or (4) a magnetic tunnel junction (7). The impedance of these devices ranges from the order of ohms to hundreds of ohms for those composed only of metals (1 and 2) to the order of

$M\Omega$ for tunnel devices. The output states are characterized by LOW and HIGH values of R and $R + \delta R$, and matched reference resistors (R) are typically used in a cell so that the LOW and HIGH output states are the difference values, 0 and δR. These devices are intrinsically dissipative and can never achieve substantial current gain. However, a number of cell designs have been implemented using amplification at the output stage (8).

A third category of magnetoelectronic devices, represented by the spin injected field effect transistor (9), combines spin-dependent resistivity with a gated semiconductor structure. Although still in basic research, this category enjoys the added benefit of good device isolation.

NONLATCHING GATES

The hysteresis loops of Figs. 1 and 3(a) are typical of the microfabricated ferromagnetic films used in magnetoelectronic devices. A variety of magnetic bias techniques can be used to shift the loop so that it is no longer centered about $H = 0$ (equivalently, $I = 0$). When shifted in a positive sense by an amount approximately equal to H_s, a device with such a ferromagnetic component operates in a nonlatching mode. For example, the initial device state is automatically LOW (0), and input write pulses with net amplitude corresponding to $2H_s$ will set the state of the device to HIGH (1) for the duration of the pulses. When the current in the write wire reverts to zero, the ferromagnetic film reverts to its initial LOW state.

Multilayer magnetoelectronic devices can have multiple, stable hysteresis loops. In a structure with two ferromagnetic layers, for example, one layer may be fabricated with a relatively large coercivity (a *hard* layer) and a magnetic bias, and the second layer may be fabricated with a small coercivity (*soft* layer) and no magnetic bias. Such a device has two stable hysteresis loops for a field range somewhat larger than the coercivity of the soft layer, and the device can be set to the state characterized by each loop by using fields somewhat larger than the coercivity of the hard layer. A programmable logic architecture uses magnetoresistive cells of this kind to switch the functions of a cell between one Boolean function (e.g., OR) and its inverse (NOR) (8).

UNIQUE ATTRIBUTES OF MAGNETIC LOGIC

Existing prototypes of magnetoelectronic devices have been fabricated with submicron dimensions and areas of order one square micron. Future device generations will be fabricated with nanometer dimensions and may achieve gains sufficiently large that fanout is possible, and magnetic logic would then have numerous benefits. A single magnetoelectronic device can act as a Boolean logic gate. Compared to four FETs typically required for the same CMOS Boolean gate, packing densities would be significantly greater and signal processing times would be much faster. Not only would each logic cell have fewer elements, it would have fewer interconnects. The parasitic resistance and capacitance of interconnects is a major contributor to dissipation and delay time, and diminishing the number of interconnects is an important concern. If very small size scales are achieved, magnetic logic becomes a candidate system for *quantum computing*. A ferromagnetic element with dimensions 10 nm, at sufficiently low temperature, meets many requirements of a quantum information bit.

With present, low-gain devices, magnetic logic can be integrated with CMOS and this kind of implementation offers related advantages. A fully restored Boolean logic cell can be fabricated with a single magnetoelectronic device, which occupies minimal space in the cell, and two FETs. This is half the number of FETs of the same CMOS logic cell and therefore offers higher packing densities and faster signal processing speed. Since the result of the operation of each stage can be latched, there may be greater savings in space by eliminating the need for a separate storage cell. Finally each single, fabricated logic cell can be "reprogrammed" to perform more than a single (Boolean) logic operation. This property makes magnetic logic ideally suited to applications where configurable (or field programmable) logic is needed.

BIBLIOGRAPHY

1. N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design,* 2nd ed., Reading, MA: Addison-Wesley, 1994.
2. R. F. Soohoo, *Magnetic Thin Films,* New York: Harper & Row, 1965.
3. A. V. Pohm et al., The design of a one Mbit nonvolatile MR memory chip, *IEEE Trans. Magn.,* **24**: 3117–3119, 1988.
4. M. Johnson et al., Hybrid hall device, *Appl. Phys. Lett.,* **71**: 974–976, 1997.
5. M. Johnson, The All-metal Spin Transistor, *IEEE Spectr. Mag.,* **31** (5): 47–52, 1994.
6. G. A. Prinz, Spin-Polarized Transport, *Phys. Today,* **48** (4): 58–63, 1995.
7. J. S. Moodera et al., Large magnetoresistance at room temperature in ferromagnetic thin film tunnel junctions, *Phys. Rev. Lett.,* **74**: 3273–3276, 1995.
8. M. M. Hassoun et al., Field programmable logic gates using GMR devices, *IEEE Trans. Magn.,* **33**: 3307–3309, 1997.
9. S. Datta and B. Das, *Appl. Phys. Lett.* **56**: 665, 1990.

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MAGNETIC LOSSES. See MAGNETIC NOISE, BARKHAUSEN EFFECT.

MAGNETIC MATERIAL. See EDDY CURRENT LOSSES; MAGNETIC REFRIGERATION.