MONOLITHIC MICROWAVE INTEGRATED CIRCUITS

Over the past ten years, microwave technology has gone through a significant evolution to meet necessary requirements for lower-cost solutions, circuit miniaturization, higher levels of integration, improved reliability, lower power consumption, low-voltage operation, and high-volume applications. Component size and weight are prime factors in the design of electronic systems for satellite communications, phased-array radar (PAR), electronic warfare, and other airborne applications, whereas high volume and low cost drive the PAR and consumer electronics market. Monolithic microwave integrated circuits (MMICs) are the key to meeting these requirements. MMICs will play a significant role in consumer electronics dealing with information transfer, communications, automotive, and entertainment and successful de-

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ployment of the PAR systems for both commercial and military applications.

The first MMIC results for transmit/receive (T/R) modules using low-frequency silicon technology were reported in 1964. The results were not promising because the low resistivity of the silicon substrate produced insufficient isolation between the individual devices in the monolithic circuit. In 1976, the first monolithic X-band amplifier, based on the GaAs Metal Semiconductor Field Effect Transistor (MESFET), was developed. By 1980, many MMIC results using MESFETs for various circuits had been reported. Since that time, tremendous progress has been made both in MMIC developments and in system applications. The outstanding progress in MMIC technology is attributed to the following:

1. Rapid development of GaAs material technology, including semi-insulating wafers, epitaxial growth, and ion implantation.
2. Advanced photo- or E-beam lithography technology developed for Si ICs and directly applicable to GaAs ICs.
3. Excellent microwave properties of semi-insulating GaAs substrates, which permit easy isolation of devices for high-level integration (high dielectric constant, $\epsilon_r = 12.9$, and low loss $\tan \delta = 0.0005$).
4. The development of low-noise MESFETs and power MESFETs operating at up to ~60 GHz have provided MMIC designers with versatile active circuit components.
5. Virtually any microwave solid-state circuit. They were realized using combinations of MESFETs, dual-gate MESFETs, Schottky-barrier diodes, and switching MESFETs, each of which can be fabricated simultaneously using the same or similar process. HEMT MMICs provide enhanced performance in terms of noise figure, bandwidth, and frequency range. Using HEMT monolithic technology the frequency range was extended to 150 GHz.
6. High Electron Mobility Transistors (HEMTs) and Heterojunction Bipolar Transistors (HBTs), which are, in addition to MESFETs, the other most common active devices used in MMICs.
7. The development of good models for characterizing active devices and passive components.
8. The availability of commercial CAD tools for accurate simulation and optimization of microwave circuits.
9. The availability of on-wafer high-frequency test probes that permit both low-cost MMIC screening and the collection of a large amount of statistically significant data without the cost and variability of packaging.
10. Government funding for technology development and maturation.
11. Expanding military and commercial applications.

The MESFET, commonly referred to simply as FET, is the most mature active device and is widely used in production applications. With MMIC technology, a typical microwave subsystem can be produced on a single chip for less than \$100 while simpler single-function chips cost less than \$10. Some very simple MMIC chips are now produced in plastic packages for less than \$1.

Whereas most MMICs currently in production operate in the 0.5 GHz to 30 GHz microwave range, applications covering the millimeter wave (mmW) spectrum from 30 GHz to 300 GHz are increasing. Monolithic technology is particularly suited for millimeter wave applications through the elimination of the parasitic effects of bond wires which connect discrete components in conventional hybrid microwave integrated circuits (HMICs). In MMIC-based mmW subsystems, the cost can be lowered by a factor of ten or more as compared to hybrid solutions.

Advantages of MMICs include low cost, small size, light weight, circuit design flexibility, broadband performance, elimination of circuit tweaking, high-volume manufacturing capability, package simplification, improved reproducibility, radiation hardness, improved reliability, and multifunction performance on a single chip. Indeed, the concept of implementing a "subsystem on a chip" became a reality through monolithic microwave technology.

IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, published from 1982 to 1996, *IEEE RFIC Symposium Digest,* published since 1997 and *IEEE GaAs IC Symposium Digest,* published since 1980 include comprehensive information on the design, fabrication, and performance of monolithic microwave and millimeter-wave integrated circuits as well as their applications. Several other books listed (1–17) deal with this subject either partially or exclusively.

MMIC FABRICATION

In fabricating MMICs, all active and passive circuit elements and interconnections are formed together on the surface of a semi-insulating substrate (usually gallium arsenide). Typically MMICs use microstrip and metal-insulator-metal (MIM) capacitors for the matching networks, whereas at low microwave frequencies, lumped inductors and MIM capacitors are commonly used. Via holes, metal-filled holes from the bottom of the substrate (ground plane) to the top surface of MMICs, provide low-loss and low-inductance ground connections. Figure 1 shows a three-dimensional view of an MMIC.

There are many ways to fabricate MMICs. MMICs using MESFET and HEMT are most commonly fabricated by a recessed gate process, but the self-aligned gate (SAG) process is gaining popularity because it permits the efficient fabrication of devices optimized for different functions (e.g., micro-

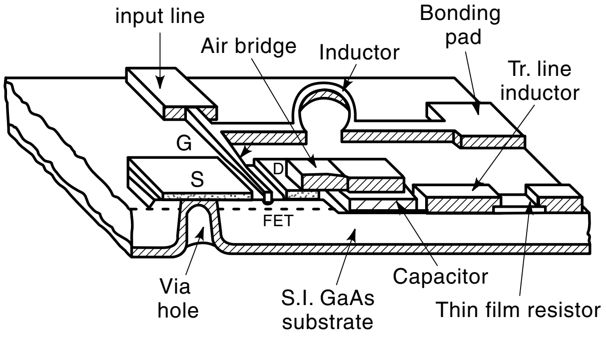


Figure 1. An MMIC three-dimensional view showing MESFET, inductor, capacitor, resistor, air bridge, via-hole, and a microstrip section.

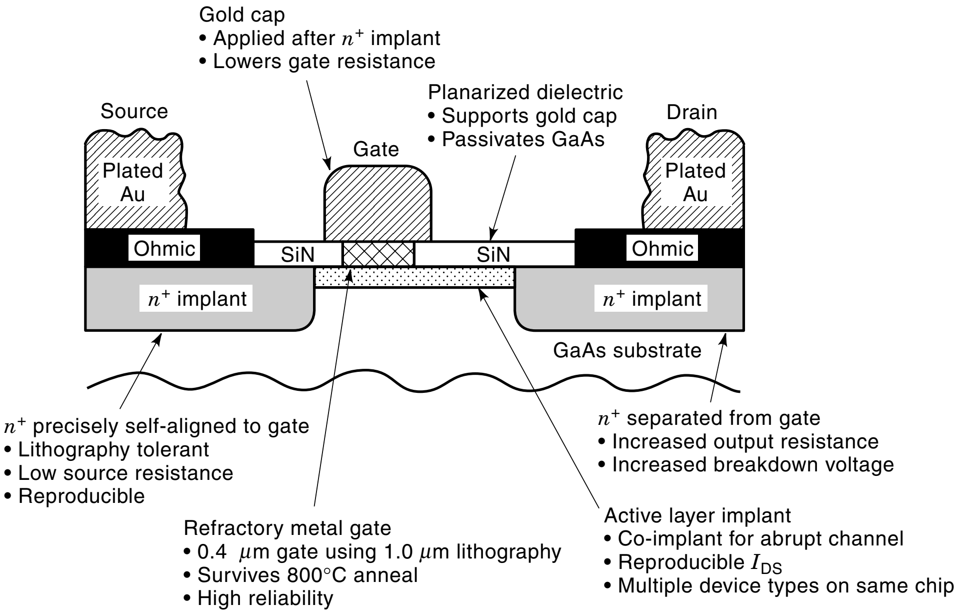


Figure 2. SAG FET cross section showing features to improve manufacturability.

wave small signal, microwave power, and digital) on the same wafer at the same time. The self-aligned gate process has demonstrated superior performance uniformity in a manufacturing environment.

Figure 2 shows a SAG MESFET cross section along with salient features.

In order to give the reader an understanding of the relative complexity of GaAs MMIC manufacturing, a process flow chart for the SAG process is given in Fig. 3. The process for recessed gate MMICs has many similarities. The process includes the fabrication of active devices, resistors, capacitors, inductors, distributed matching networks, air bridges, and via holes for ground connections through the substrate. Basic process steps are similar for any MMIC technology.

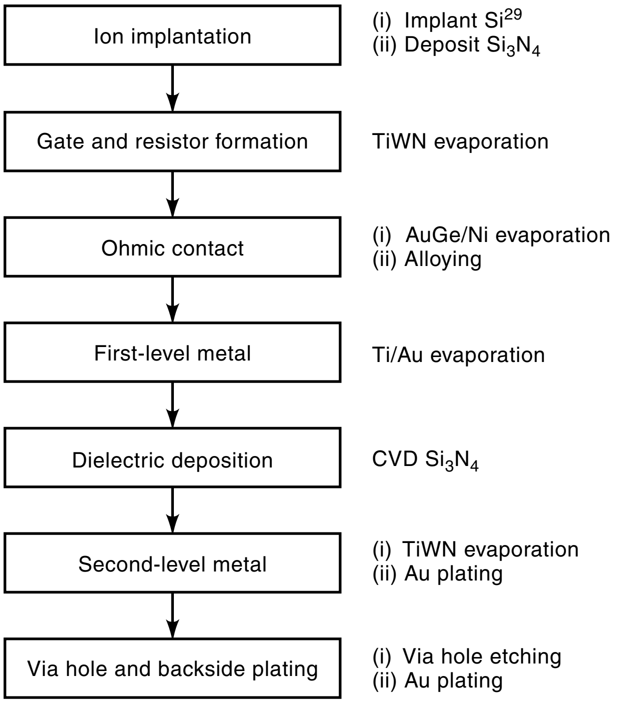


Figure 3. MMIC process flow chart for self-aligned gate process.

It should be noted that GaAs MMIC processing is less complex than silicon processing for devices operating at the low end of the microwave spectrum. Because silicon has inherently lower frequency capability and poorer isolation properties for integration purposes, more exotic processing is required to compete in the frequency region of overlap with GaAs applicability (~1 GHz to 2 GHz). For example, a silicon bipolar-complementary metal-oxide semiconductor (BiCMOS) process for such IC applications may require two to three times as many mask layers, adding significantly to the cost.

Active Layers

The MMIC process starts with the formation of an active layer on or into semi-insulating GaAs substrate. There are basically two methods of forming an *n*-type active layer: ion implantation and epitaxy. In the ion implantation technique, the dopant Si ions bombard the GaAs substrate in an area specified by a photolithographic photoresist pattern or mask. A suitable combination of energy and dose is used for the particular FET characteristics desired. During ion implantation, the crystal lattice of GaAs is damaged, and the implanted atoms come to rest at random locations with the material. A high temperature (850° to 900°C) annealing step is performed to heal the lattice damage and allow the implanted atoms to move onto lattice sites. With this technique, different active device types (with different active layer properties) can be readily fabricated on the same wafer through respective selective implants defined by photoresist masks. This technique is well suited to high volume production since the methods and equipment are nearly identical to those used in the silicon industry.

As discussed earlier, epitaxial devices are sometimes required for particular high performance applications. In the epitaxial technique, additional GaAs (or other III–V compound) material layer(s) are grown on the surface of the GaAs substrate in a manner that preserves the crystal structure. There are four basic types of epitaxy that have been used for GaAs: liquid-phase epitaxy (LPE), vapor phase epitaxy (VPE), molecular-beam epitaxy (MBE), and metal-organic chemical vapor deposition (MOCVD). LPE is the oldest technique used to grow epitaxial layers on GaAs crystals, but it is not suitable for MMIC fabrication because of inherent surface roughness. VPE is typically used for GaAs power FETs. MBE is the most recent and powerful technique. Its advantage is that it can produce almost any epitaxial layer (III–V compound) composition, layer thickness, and doping with the highest possible accuracy and uniformity across a wafer. MOCVD has similar flexibility with the added advantage of being better suited to low-cost manufacturing; however, the material's electrical quality is not yet as good as that for MBE. The specified active areas are isolated either by mesa etching or by bombarding with ions, which increase resistivity by creating damage to the crystal lattice. A disadvantage of these techniques, relative to ion implantation, is that different device types generally require different epitaxial layers requiring not only multiple expensive growth runs but also relatively costly processing to isolate the different device types.

Schottky or Gate Formation

The quality and placement of the gate metal is critical to FET performance in both low-noise and power FETs. The choice of the gate metal is generally based on good adhesion to GaAs, electrical conductivity, and thermal stability. Recessed gate FETs utilize evaporated materials such as TiPdAu or TiPtAu. SAG FETs (15) use a TiWN material, which forms a thermally stable, refractory Schottky gate in order to withstand the high temperature annealing step, which is performed after the gate is in place. It is deposited by reactive sputtering.

Gate formation can be accomplished using optical lithography techniques for critical dimensions down to about 0.5 μm. Below 0.5 μm, the direct write electron beam lithography (EBL) method is often used. Although quite expensive because of the high cost of the equipment and relatively slow throughput, EBL provides a high degree of precision making dimensions as small as 0.1 μm practical. The SAG technique uses lower-cost 1.0 μm optical lithography, along with a plasma underetch, to achieve 0.4 μm or smaller gate dimensions. Gate metalization is also used for thin film resistors. Typical resistance values are about 10 Ω/square.

Ohmic Contact

Device ohmic contacts are made next. The purpose of an ohmic contact on a semiconductor material is to provide a good contact between the interconnect metal and the active channel at the semiconductor surface. The most common approach in industry to fabricate ohmic contacts on GaAs is by alloying gold and germanium (88% Au and 12% Ge by weight, with a melting point of 360°C). A thin layer of AuGe alloy, followed by a thin layer of Ni, is deposited by evaporation. The total layer thickness is about 2000 Å. The ohmic contact pads are defined by a photoresist mask and chemical lift off of metal on the photoresist regions. The step is followed by alloying at 400°C in a hydrogen ambient.

First-Level Metal

Next a thick (about 0.5 μm) Ti/Au metal is overlayed on the gate by evaporation and liftoff. The metal reduces the gate resistance and also serves as a first-level metalization for MMIC fabrication (e.g., as a capacitor bottom plate or the interconnect metal under air bridges or crossovers).

Dielectric Deposition

Dielectric films are used in GaAs MMICs for passivation of active areas of FETs, diodes, and resistors; for MIM capacitors; and for crossover isolation. Silicon nitride (Si_3N_4) is commonly used as dielectric material, which is easily deposited either by plasma-assisted chemical vapor deposition or sputtering. The thickness of the dielectric film determines the capacitance per unit area of the MMIC capacitor. The thickness is usually between 1000 Å and 3000 Å, and is optimized to have minimum pin holes, high breakdown voltage, and maximum possible capacitance. The capacitance value ranges from 240 pF/mm^2 to 1200 pF/mm^2 with breakdown voltages from 16 V to greater than 60 V. Typical values for capacitance and breakdown voltage are 300 pF/mm^2 and 60 V, respectively.

Second-Level Metal

Interconnection of components, air bridges, and the top plate of MIM capacitors is formed with the second-level layer TiWN/Au metal system. In order to achieve low-resistance connections, gold plating (4.5 μm thick) is added to provide maximum current capability of about 10 mA/μm of line width and a sheet resistance of less than 10 mΩ/square. Typical line widths for microstrip line interconnects vary from 10 μm to 200 μm.

Backside Processing

Backside processing consisting of thinning by grinding or lapping, via hole source ground contact finalization and plating, is an important and cost-sensitive part of processing. In a production environment, a significant investment has been made in the wafer by the time the frontside processing is completed and the backside processing started. Also, several of the backside operations critically affect the circuit function and the yield as a whole. Typical functional yield for frontside processed MMICs is 90 to 95%, whereas for frontside and backside processed MMICs, yield numbers are 80 to 85%. After the frontside process, the wafer is thinned by a lapping technique from ~600 μm to the required thickness, typically 100 to 125 μm for small signal MMICs and 50 to 75 μm for power MMICs (to maximize heat dissipation). MMIC wafers may also be thinned down to 50 to 75 μm for frequencies greater than 50 GHz to minimize ground return parasitics. High-performance MMICs require low inductance ground connections to the FET source and good thermal dissipation paths from the FET to its ground. In via-hole technology, holes are etched through GaAs substrate under each FET source connection as well as under other pads where ground connections are needed. Then the backside and the via-hole sidewalls are metallized. This provides a good connection from the frontside devices and components to the backside ground plane. This also eliminates the need for separate wire bonds to ground for each FET and other RF ground connections. The first check for a good circuit is automatic testing on wafer with micro-

Table 1. Comparison of Monolithic Integrated-Circuit Substrates[a]

Property	Silicon	SiC	GaAs	InP	GaN
Semi-insulating	No	Yes	Yes	Yes	Yes
Resistivity (Ω-cm)	10^3–10^5	$>10^{10}$	10^7–10^9	$\sim 10^7$	$>10^{10}$
Dielectric constant	11.7	9.7	12.9	14	8.9
Electron mobility (cm^2/V-s)	1450	500	8500	4000	800
Saturation electrical velocity (cm/s)	9×10^6	2×10^7	1.3×10^7	1.9×10^7	2.3×10^7
Radiation hardness	Poor	Excellent	Very good	Good	Excellent
Density (g/cm^3)	2.3	3.1	5.3	4.8	—
Thermal conductivity (W/cm-°C)	1.45	4.3	0.46	0.68	1.3
Operating temperature (°C)	250	>500	350	300	>500
Energy gap (eV)	1.12	2.86	1.42	1.34	3.39
Breakdown field (kV/cm)	≈300	≥2000	400	500	≥5000

[a] Pure materials at room temperature.

wave probes. After identifying RF good ICs, the wafer is diced into chips.

MMIC SUBSTRATES

Any assessment of MMIC technology options available to the microwave designer will generally be in terms of chip size, weight, reliability, reproducibility, cost, maximum frequency of operation, and availability of a wide range of active devices for design flexibility. Various substrate materials used for MMICs are bulk silicon, silicon carbide, GaAs, InP and GaN. Their electrical and physical properties are compared in Table 1. The semi-insulating property of the base material is crucial to providing higher device isolation and lower dielectric loss for MMICs. For example, even though bipolar silicon devices are capable of operating up to about 10 GHz, the relatively low resistivity of bulk silicon precludes monolithic integration for frequencies above the S band (2 GHz to 4 GHz).

The GaAs FET as a single discrete transistor has been widely used in hybrid amplifiers (low-noise, broadband, medium-power, high-power, high-efficiency), mixers, multipliers, switching circuits, and gain control circuits. This wide use of GaAs FETs can be attributed to their high frequency of operation and versatility. All these benefits are automatically realized in MMICs as well. GaAs semi-insulating substrates provide isolation up to about 100 GHz. This, combined with much higher electron mobility (5 to 6 times that of silicon), enables GaAs MMICs to be produced for operation at up to 60 GHz. Additionally, MMICs at 94 GHz have been demonstrated using highly specialized HEMT devices epitaxially grown on semi-insulating GaAs. Hence, GaAs has been the technology of choice for most MMIC applications. At the lower end of the microwave spectrum for new emerging wireless applications, GaAs power FETs are more suitable, compared with biopolar transistors, because of their high-gain, low-noise figure; high power with good efficiency, and low-battery voltage (3 V to 6 V) operation.

InP has been used for millimeter-wave monolithic integrated circuits using HEMTs, but very little work has been done on InP MMICs using MESFETs. The low Schottky-barrier height of metals on *n*-type InP is a chronic impediment to the development of an InP MESFET technology of equivalent performance to that of GaAs. Pseudomorphic HEMTs fabricated on InP substrate, exhibit much higher performance in terms of gain, noise figure, and power than a GaAs-based HEMT of similar geometry. In this case, the InP substrate supports higher two-dimensional electron gas densities resulting in high current and transconductance values. The high values of transconductance in InP HEMTs is responsible for ultra-low-noise figure, high gain, and high frequency of operation.

Table 1 compares the properties of several semiconductor materials suitable for MMIC applications. Except Si, all other substrate materials shown in Table 1 are called compound semiconductors. Silicon dominates the marketplace. GaAs is a distant second with less mature technologies such as InP, SiC, and GaN only now emerging. For high-power and high-temperature applications, wide band gap materials with relatively high thermal conductivity, such as SiC and GaN, play a significant role. Recent advancements in the epitaxial techniques have made it possible to develop good active devices on these substrates, which is a prime requirement for any semiconductor material to be used as a substrate for MMICs.

TRANSMISSION LINES

The microstrip line and coplanar waveguide (CPW) are the two commonly used transmission media in MMICs. The microstrip is more popular due to its quasi-TEM nature and excellent layout flexibility. Cross-sectional views of these lines with physical parameters are shown in Fig. 4. Sections of mi-

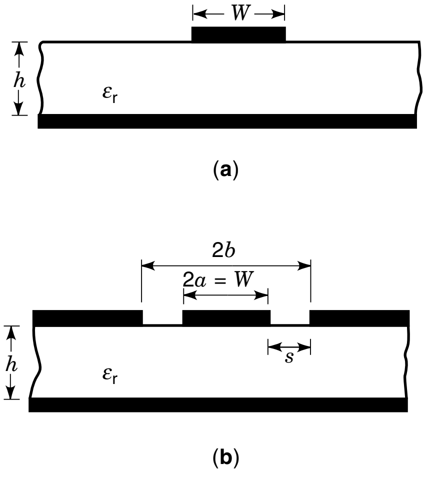


Figure 4. Transmission lines for MMICs: (a) microstrip; and (b) coplanar waveguide.

crostrip lines and coplanar waveguides constitute the basic passive component building blocks of monolithic microwave integrated circuits. When the size of the microstrip section is reduced to dimensions much smaller than the wavelength, it can be used as a lumped element. Examples of lumped microstrip elements are spiral inductors, thin film resistors, and interdigital capacitors. Microstrip sections in lumped and distributed form are commonly used in passive and active monolithic microwave integrated circuits.

The important parameters for designing these transmission lines are the characteristic impedance Z_0, effective dielectric constant ϵ_{re}, attenuation constant α, discontinuity reactances, frequency dispersion, surface wave excitation and radiation. Several methods to determine these parameters are summarized in Ref. 18. Basic properties such as Z_0, ϵ_{re}, α, and maximum frequency of operation are briefly described here.

Microstrip

The microstrip propagation properties are controlled by conductor width W and substrate height h for a given dielectric constant value ($\epsilon_r = 12.9$ for GaAs). Figure 5 shows the variations of Z_0, ϵ_{re}, and α. As an example, for a 50 Ω line on a GaAs substrate, the value of W/h is about 0.7.

The characteristic impedance value decreases when the strip width-to-height ratio W/h of the line increased. Wavelength in microstrip λ is related to ϵ_{re} by

$$\lambda = \lambda_0/\sqrt{\epsilon_{re}} \tag{1}$$

where λ_0 is the free space wavelength.

The maximum frequency of operation of a microstrip transmission line is limited as a result of several factors including excitation of spurious modes, higher losses, pronounced discontinuity effects, low Q caused by radiation from discontinuities, effect of dispersion on pulse distortion, tight fabrication tolerances, handling fragility and, of course, technological processes. The frequency at which significant coupling occurs between the dominant quasi-TEM mode and the lowest-order surface wave spurious mode is given by (18),

$$f_T = \frac{150}{\pi h}\sqrt{\frac{2}{\epsilon_r - 1}}\tan^{-1}(\epsilon_r) \tag{2}$$

where f_T is in gigahertz and h is in millimeters. Thus the maximum thickness of the GaAs substrate for microstrip circuits designed at 100 GHz is less than 0.3 mm.

The excitation of higher order modes in a microstrip can be avoided by operating it below the cut-off frequency of the first higher-order mode, which is given approximately by (18)

$$f_c = \frac{300}{\sqrt{\epsilon_r}(2W + 0.8h)} \tag{3}$$

where f_c is in gigahertz, and W and h are in millimeters. This limitation is mostly applicable for low-impedence lines that have wide microstrip conductors.

CPW

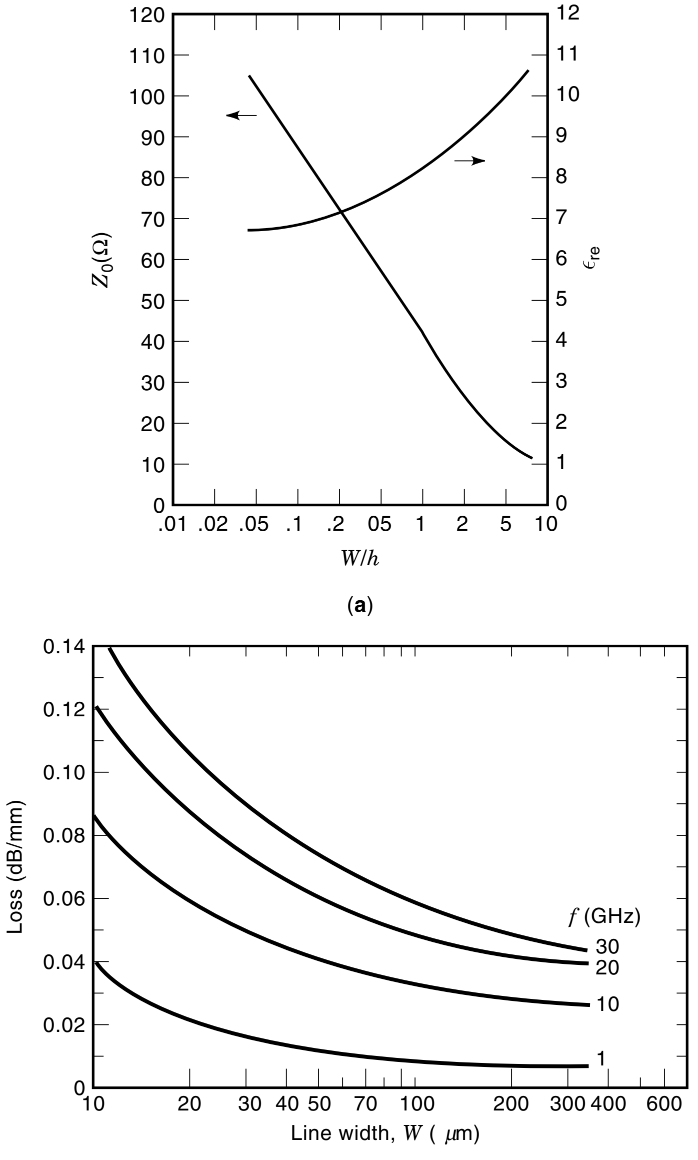


Figure 5. GaAs Microstrip parameters: (a) characteristic impedence and effective dielectric constant; and (b) attenuation constant measured as 1 GHz, 10 GHz, 20 GHz, and 30 GHz; substrate thickness of GaAs: 100 μm.

CPW properties are controlled by the center conductor width W and the spacing between the strip and the ground plane conductor denoted by s in Fig. 4(b). In a CPW, the substrate thickness generally used is large so that if the substrate has a conductor backing to improve the mechanical strength, it does not affect CPW's electrical characteristics. Figure 6 shows the variation of Z_0, ϵ_{re}, and α as functions of the conductor width to gap separation ratio.

In addition to dielectric and ohmic losses, coupling of power to surface waves and radiation from unwanted (parasitic) modes contribute to the total loss of the coplanar lines. The parasitic mode in a coplanar waveguide is the odd-mode with antiphase voltages in the two slots. This mode can be excited at discontinuities, and radiation may occur. Radiation from this mode can be minimized by maintaining symmetry of the circuits and thus avoiding its excitation or by using air bridges at regular intervals to short it out. In a conductor-

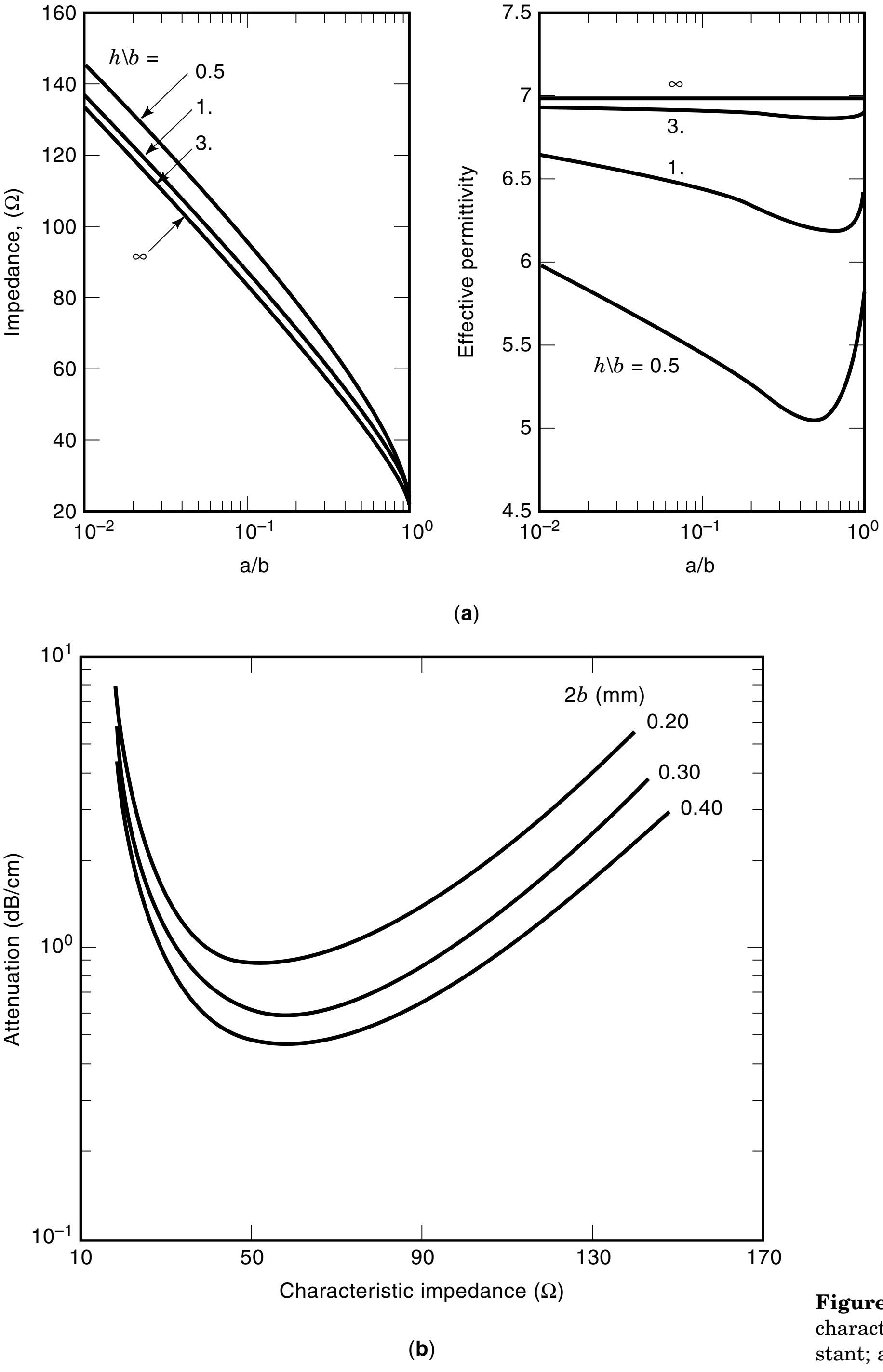


Figure 6. GaAs coplanar waveguide parameters: (a) characteristic impedance and effective dielectric constant; and (b) attenuation constant.

backed coplanar waveguide, the parallel plate waveguide modes are other parasitic modes. Surface waves or the substrate modes are the TM and TE modes supported by the substrate. Excitation of these modes can be avoided if a thin substrate is used such that the cutoff frequency of the surface modes is pushed above the operating frequency. This is achieved if the substrate thickness h is chosen such that

$$h \leq 0.12\lambda_0/\sqrt{\epsilon_r} \tag{4}$$

where λ_0 and ϵ_r are respectively the free space wavelength and dielectric constant of the substrate.

CPW MMICs, compared with microstrip-based MMICs, can have lower loss at millimeter wave frequencies by properly designing matching networks, they require no via hole technology for RF ground connections, and they are more suitable for flip-chip mounting.

MMIC ACTIVE DEVICES

Since the first reported GaAs MMIC, the MESFET and the Schottky diode have been the workhorses for analog integrated circuits (ICs). MESFET technology commonly uses

0.25 μm to 1.0 μm gate lengths for microwave applications. MESFET low noise and power MMICs demonstrate excellent performance at microwave frequencies. However, increasing emphasis is being placed on new devices for better-performance and higher-frequency operation. HEMT and HBT devices offer potential advantages in microwave and millimeter-wave IC applications, arising from the use of heterojunctions to improve charge transport properties (as in HEMTs) or *p*–*n* junction injection characteristics (as in HBTs). HEMTs appear to have a niche in ultra-low-noise and high-frequency (mmW) applications. The MMICs produced using novel structures such as pseudomorphic, lattice-matched HEMTs also known as PHEMTs have significantly improved the noise performance and high-frequency (up to 150 GHz) operation. PHEMTs that use multiple epitaxial III–V compound layers have shown excellent millimeter-wave power performance from Ku- through W-bands. HBTs are vertically oriented heterostructure devices and are gaining popularity as power devices for high-efficiency and larger-bandwidth applications. They offer better linearity and lower phase noise than FETs and HEMTs. A cross-sectional view of the three basic device types (MESFET, HEMT, and HBT) is shown in Fig. 7. In a PHEMT structure there is another InGaAs active layer between the AlGaAs spacer and GaAs buffer that provides bet-

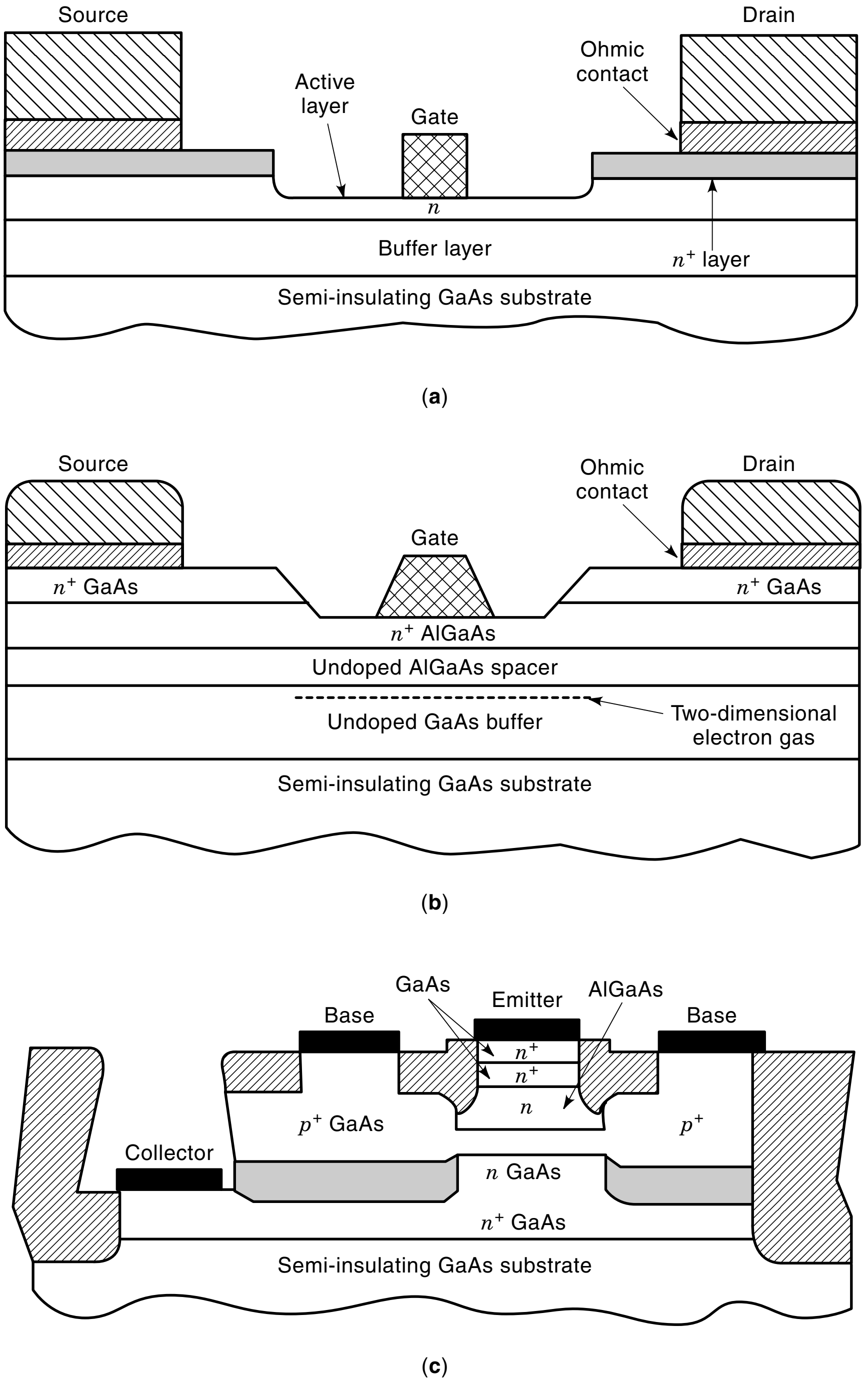


Figure 7. Schematic cross section of: (a) MESFET; (b) HEMT; and (c) HBT.

ter carrier concentration in the channel than a conventional HEMT structure.

MESFETs, HEMTs, and HBTs have been used to develop state-of-the-art circuit functions. GaAs-based MESFET, HEMT, and HBT devices are quite mature and versatile. These devices can be used for low-noise, switching, mixing, and power amplification depending on application requirements. For power circuits, where one needs much higher current, either a large number of cells are employed or larger gate periphery devices are used. Nearly all microwave circuit functions have now been realized as MMICs. Many of these functions have been demonstrated over the entire 1 GHz to 100 GHz frequency range. Furthermore, many of these functions have been combined on a single chip to form portions of a microwave system. Examples of such single and multifunction ICs are described in the section entitled “Typical Circuits and Performance.”

The upper frequency limit of MMICs is generally dictated by the active devices used. The performance of microwave transistors in MMIC technologies is improving every year. The performance of these devices (FETs, HEMTs, and HBTs) depends upon the subtrate material, process type, and channel physical dimensions. A commonly used figure of merit for devices is known as the maximum frequency of oscillation and denoted by $f_{\max}$. Generally, for amplifiers the maximum frequency of operation is about half of $f_{\max}$. For FETs on a GaAs substrate, a simplified expression for $f_{\max}$ is given by (19)

$$f_{\max} = 38.05L^{-0.953} \tag{5}$$

where L is the gate length in microns. Thus, for FETs having gate length of 0.25 μm, the $f_{\max}$ value is about 140 GHz. As reported in the literature, the $f_{\max}$ values for a 0.1 μm gate length PHEMT on an InP substrate is about 600 GHz, and for a 1 μm emitter HBT it is about 170 GHz. A three-stage amplifier fabricated using a 0.1 μm PHEMT on an InP substrate has

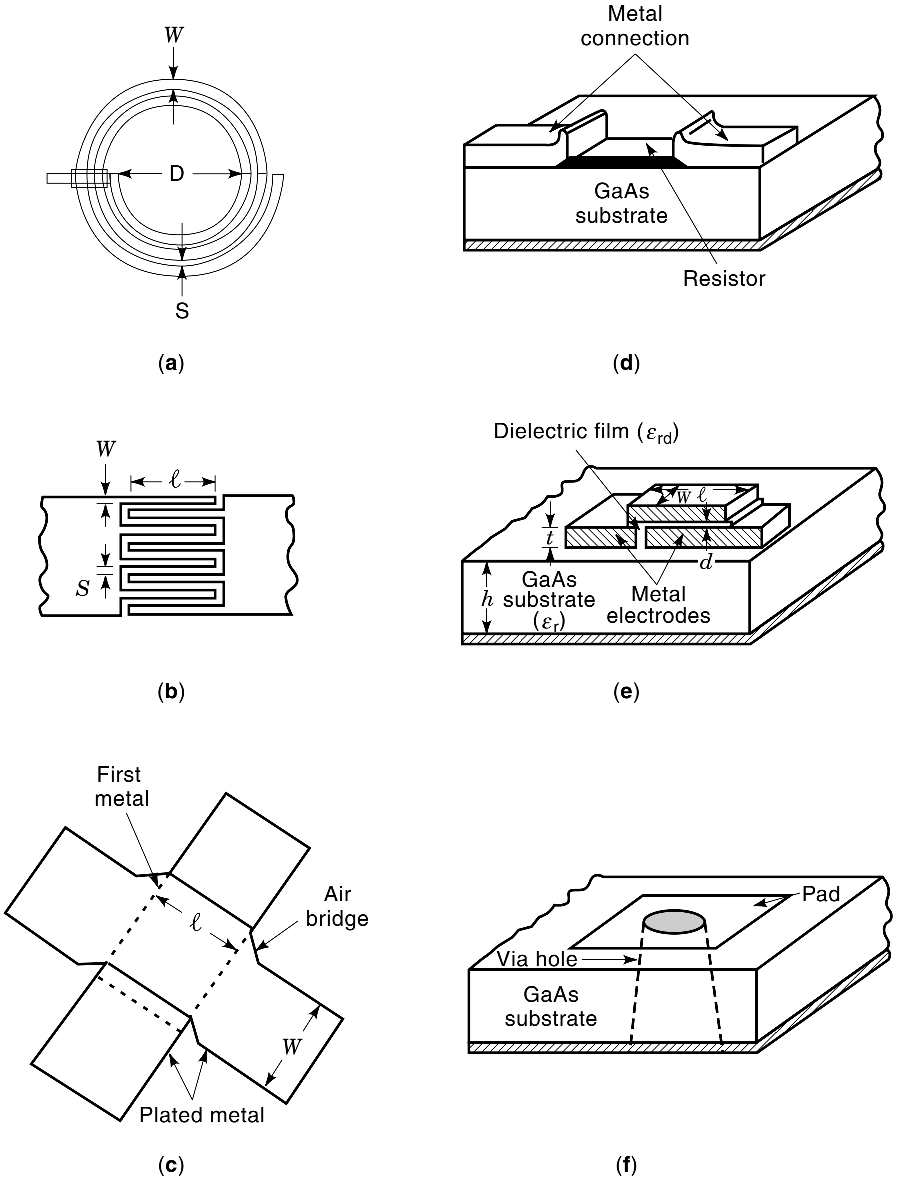


Figure 8. MMIC circuits use passive lumped elements: (a) spiral inductor; (b) interdigital capacitor; (c) air bridge crossover; (d) thin-film resistor; (e) MIM capacitor; and (f) via hole.

exhibited about 12 dB gain at 153 GHz to 155 GHz, the highest reported (20) frequency of operation for an MMIC.

COMPONENTS AND CIRCUITS

Monolithic Microwave Integrated Circuits consist of passive components and active devices fabricated simultaneously on a semi-insulating substrate. Passive components can be divided into lumped and distributed categories, where "lumped" refers to components that are small with respect to the operating wavelength and "distributed" describes elements with sizes being comparable to the wavelength. Generally, monolithic design requires both lumped and distributed elements depending upon its size, frequency of operation, types of circuit function, and cost. Examples of lumped elements, as shown in Fig. 8, are spiral inductors, thin-film resistors, interdigital capacitors, MIM capacitors, via holes, and air bridges. Distributed elements are commonly realized using sections of a microstrip transmission line or a coplanar waveguide. Lumped elements such as spiral inductors are usable in the microwave frequency range where the size and bandwidth are critical parameters. Distributed elements are preferred in applications where lower-loss and higher-power handling capability are important. However, thin-film resistors, capacitors, air bridges, and via holes are used in almost all microwave and millimeter wave monolithic integrated circuits. The lumped elements have a lower Q than the distributed elements, but they have the advantage of smaller size, ability of large impedance transformations and wideband characteristics compared with distributed elements.

MMIC passive components include filters, impedance transformers, hybrids, couplers, power dividers/combiners, delay lines and baluns. The design of such components has been thoroughly discussed in Refs. 8 and 21–25. In order to predict the performance of microstrip passive components, the effect of junction and layout discontinuities and interaction effects between circuit elements caused by close proximity is usually included in the circuit analysis, with the help of Electromagnetic (EM) field simulators. Figure 9 shows commonly used MMIC passive components.

In active MMIC components/subsystems, all interconnections are made along with active/passive devices on the semi-insulating semiconductor substrate, thereby eliminating discrete components and wire bond interconnects. MMIC active components use two types of devices: two-terminal devices referred to as diodes, such as Schottky and PIN, and three-terminal devices, such as MESFET, HEMT, and HBT. Microwave circuits that use these devices include amplifiers, oscillators, multipliers, mixers, switches, phase shifters, attenuators, modulators, limiters, and many others used for receiver or transmitter applications covering microwave and millimeter-wave frequency bands. The theory and performance of most of these circuits have been well documented (1–17,26–29). Figure 10 shows a physical layout of a broadband amplifier using FETs, microstrip lines, resistors, capacitors, via holes, and air bridges. Several examples of active circuits using various MMIC technologies are described in the section entitled "Typical Circuits and Performance."

MMIC DESIGN

The design of MMICs requires state-of-the-art Computer Aided Design (CAD) tools. The need for increased design sophistication arises from the fact that the post-fabrication tuning flexibility available in conventional hybrid microwave circuits is no longer present in the monolithically fabricated circuits. Consequently, a new design methodology is required. This includes development of accurately characterized standard library cells as well as subcircuits, accurate models for linear and nonlinear active devices, accurate passive component models, use of circuit topology and circuit elements that are more tolerant to process variations, tolerance centering of designs, proximity effect models, comprehensive simulation of complete circuits, and automatic RF testing of ICs on wafer. The latter is needed in order to obtain sufficient statistical

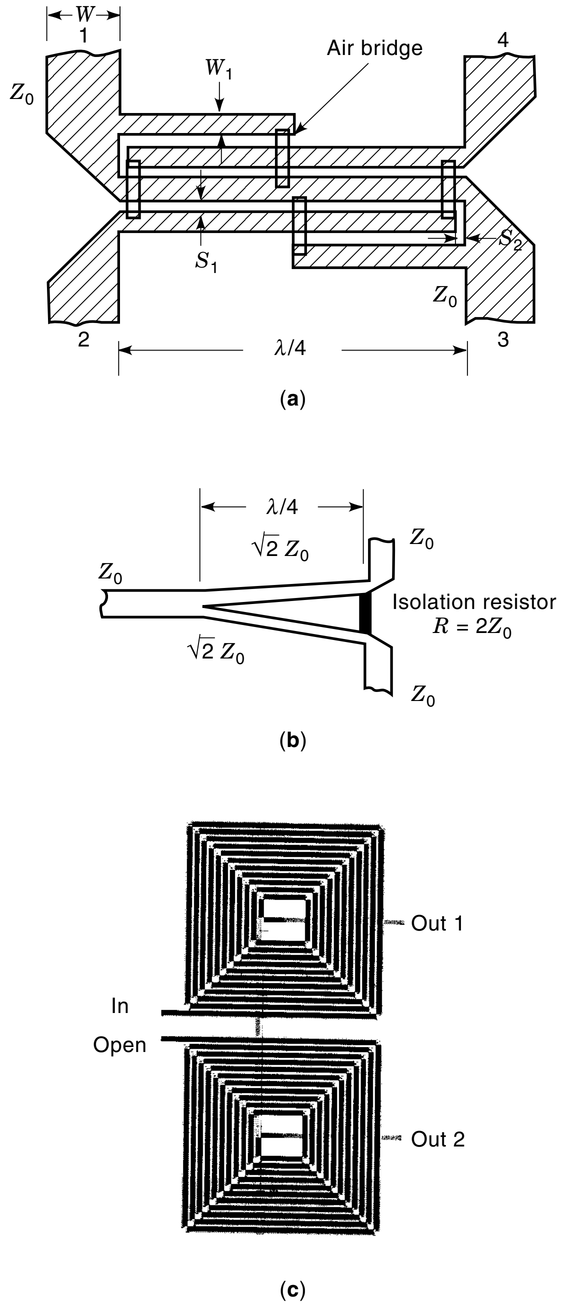


Figure 9. Typical MMIC Passive Components: (a) Lange Coupler, (b) Wilkinson divider, and (c) Spiral Marchand balun.

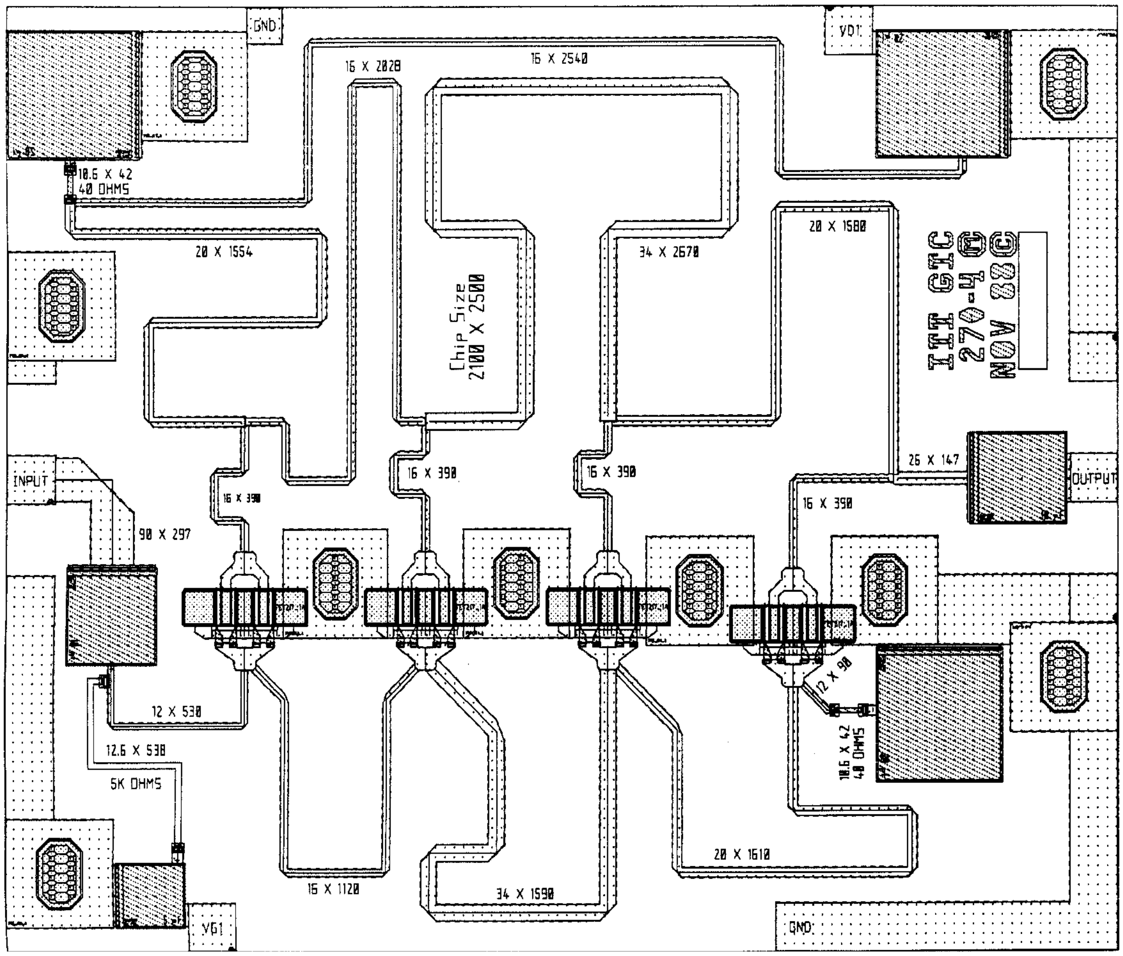


Figure 10. Physical layout of an MMIC amplifier using four FETs, capacitors, resistors, microstrip as matching elements and several vias.

characterization data without having to do expensive mounting or packaging.

Figure 11 shows (30) a comprehensive Computer Aided Engineering (CAE) tool, which consists of device, circuit, system simulators, and their accurate models (including physics-based and electromagnetic), statistical design feature, and a link between CAD, Computer Aided Test (CAT), and Computer Aided Manufacturing (CAM). A workstation-based MMIC CAD tool (31) is conceptually shown in Fig. 12. This interactive system will provide efficient coupling between the circuit simulation, the schematic captive/text editor, and the layout generator, greatly improving overall accuracy and reducing design cycle time. With such a system, first-pass-design success for simple microwave functions should be achievable.

The evolution of a typical small signal MMIC design generally follows the flow diagram depicted in Fig. 13. The design starts with the circuit specifications, which derive from the system requirements. System requirements also dictate the circuit topology along with the types of passive elements and active devices to be used (e.g., distributed or lumped passive elements, single- or dual-gate FETs, and low-noise or power FETs). Comprehensive passive element and active device models developed by foundry or by users are used to simulate circuit functions. The final design is completed by taking into account layout discontinuities, interaction between the components, stability analysis in case of amplifiers, and circuit yield analysis by considering process variations. In the case of nonlinear circuit design, (e.g., power amplifier, oscillator, or mixer) an accurate nonlinear model for each device used is essential in order to design the circuit accurately.

EM SIMULATORS

The main contribution of electromagnetic (EM) simulators to MMIC CAD tools has been in the area of accurate modeling of passive circuit elements and components. These simulators are commonly used to model circuit elements like microstrip and coplanar waveguide structures, discontinuities, and coupling between transmission line sections and discontinuities, structures using multilayer dielectric and plating, inductors, capacitors, via holes, and crossovers. Passive components, such as filters, couplers, resonators, power dividers/combiners, baluns, matching impedance transformers, and several types of interconnects and packages, are accurately simulated using EM simulators. Accurate characterization of active device-parasitics also requires EM simulation. Another key and important role of EM simulators in successful MMIC design

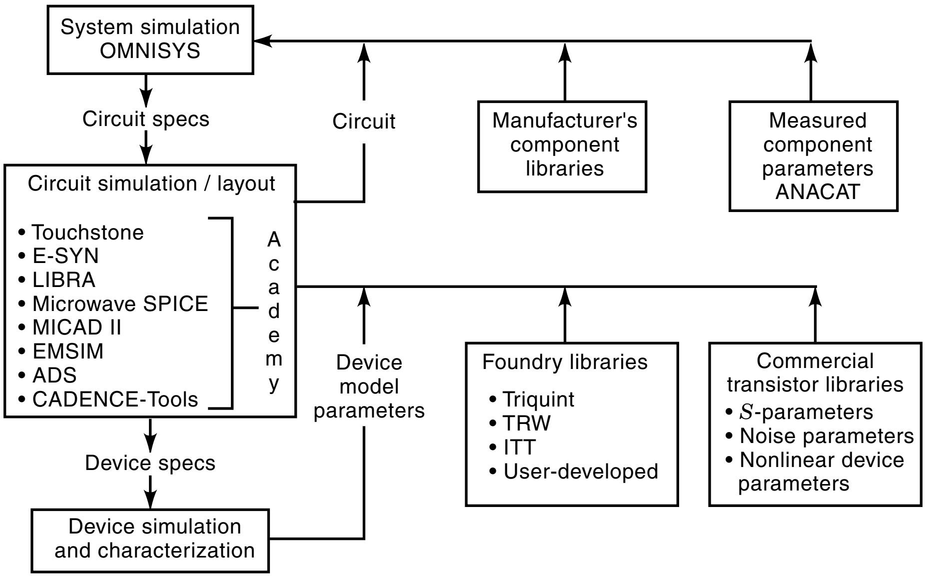


Figure 11. HP-EEsof's hierachical microwave design system.

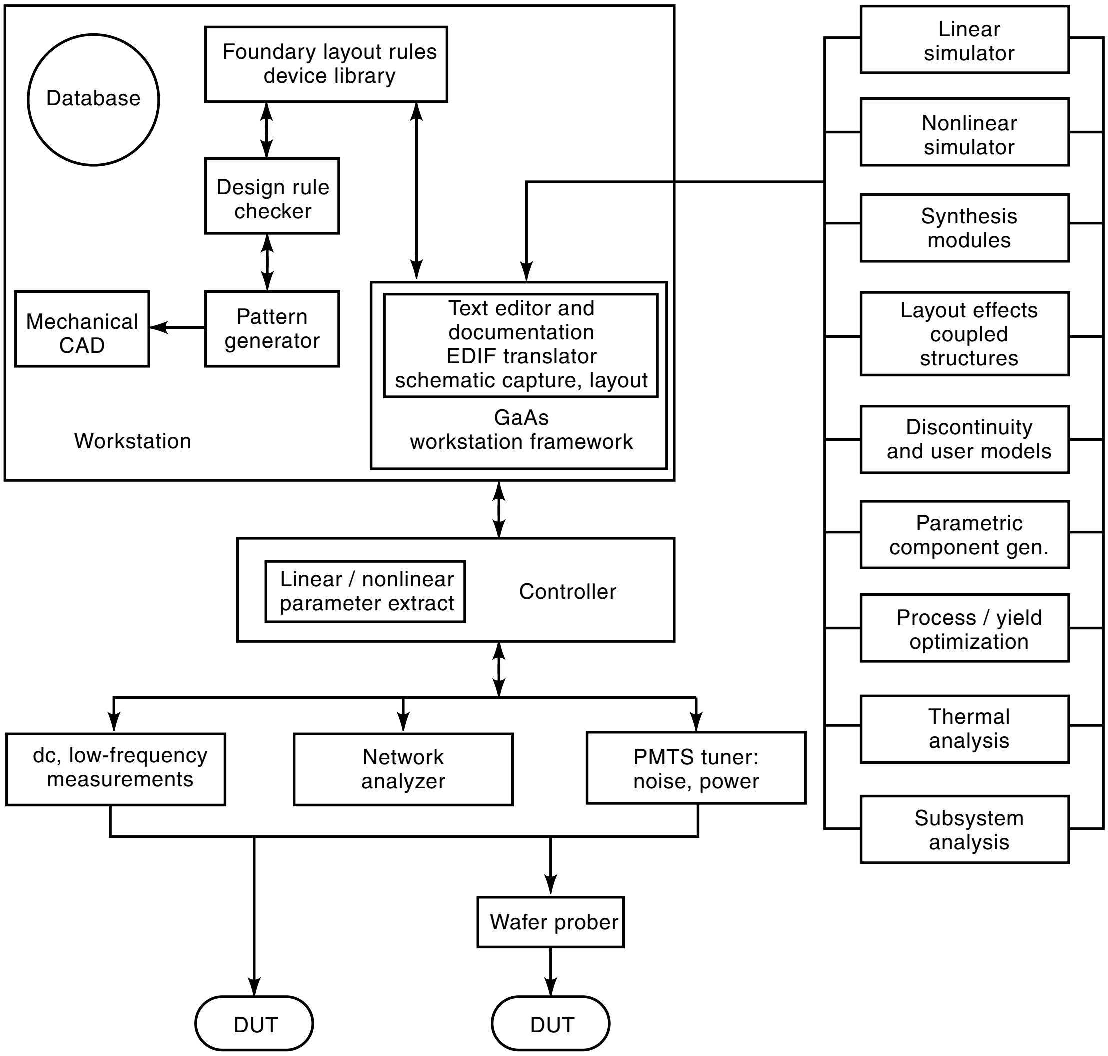


Figure 12. Next-generation MMIC workstation concept.

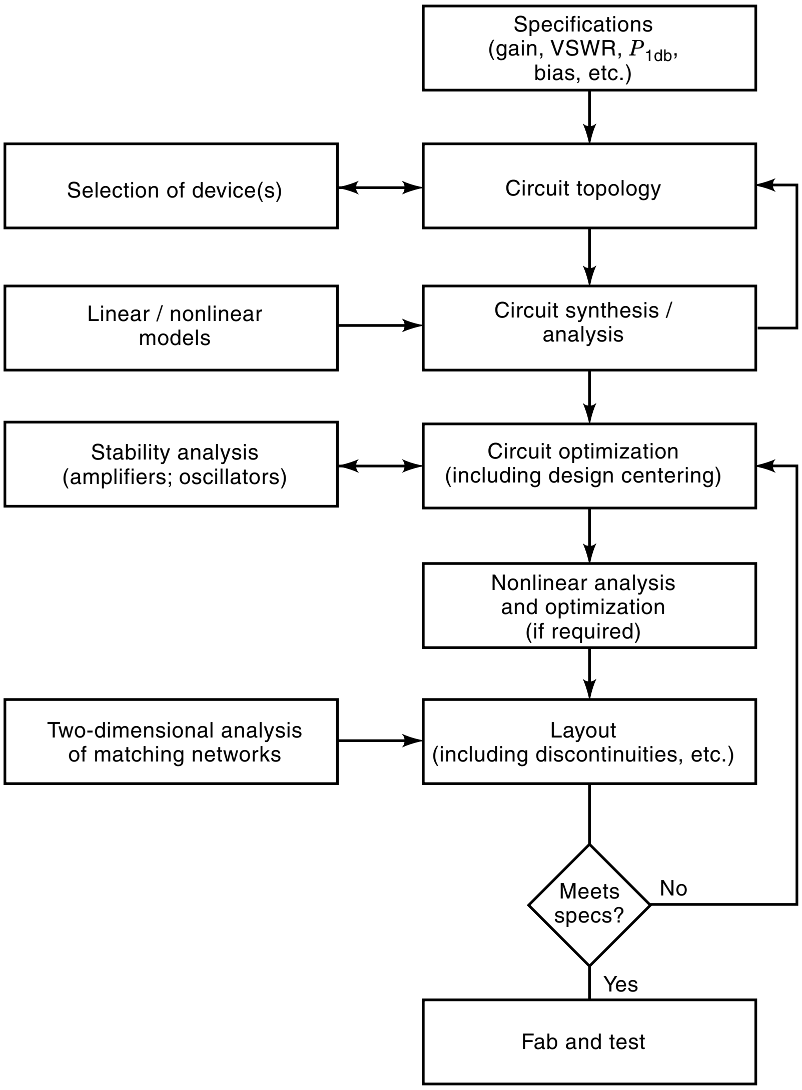


Figure 13. Typical flow chart for a MMIC design.

is the capability of incorporation of parasitic coupling effects among various parts of the circuit layout. Accurate evaluation of radiation and surface waves can be performed using EM simulators only. These effects become increasingly important as MMIC designs become more compact and are not easily incorporated using conventional network theory-based CAD tools. However, due to very large computation time, only a small portion of a circuit is analyzed using EM simulators, and the numerical results are combined with conventional CAD tools to obtain the response of the complete circuit. Most EM simulators work in the integrated simulation environment (i.e., they can be interfaced with microwave computer-aided design and engineering tools). In the past decade, outstanding progress made on personal computers and workstations lead to commercial EM simulators.

Electromagnetic Simulation Methods

Several different field simulation methods have been used and described in the literature (32,33). The most commonly used technique for planar structures is the method of moments (MoM), and for three-dimensional structures, the finite element method (FEM) is usually used. Both these techniques perform EM analysis in the frequency domain. FEM as compared to MoM, can analyze more complex structures but requires much more memory and longer computation time. There are several time-domain analysis techniques; among them the transmission-line matrix method (TLM) and finite-difference time-domain method (FDTD) are commonly used. Fast Fourier transformation is used to convert time-domain data into frequency domain results. An overview of commercially available EM simulators is given in Table 2. A more comprehensive information on these tools can be found in recent publications (34–36).

In EM simulators, Maxwell's equations are solved in terms of electric and magnetic fields or current densities, which are in the form of integral-differential equations, by applying boundary conditions. When the structure is analyzed and laid out, the input ports are excited by known sources (fields or currents), and the EM simulator solves numerically the integral-differential equations to determine unknown fields or induced current densities. The numerical method involves discretizing (meshing) the space for evaluation of unknown fields or currents. Using FEMs six field components (three electric and three magnetic) in an enclosed

Table 2. An Overview of Some Electromagnetic Simulators Being Used for MMICs

Company	Software Name	Type of Structure	Method of Analysis	Domain of Analysis
HP-EEsof	Momentum	3D Planar	FEM	Frequency
	HFSS	3D Arbitrary	FEM	Frequency
Sonnet Software	Em	3D Planar	MoM	Frequency
Jansen Microwave	Unisim	3D Planar	Spectral domain	Frequency
	SFMIC	3D Planar	MoM	Frequency
Ansoft Corporation	Maxwell-Strata	3D Planar	MoM	Frequency
	Maxwell SI Eminence	3D Arbitrary	FEM	Frequency
Compact Software	Microwave Explorer	3D Planar	MoM	Frequency
MacNeal–Schwendler Corp.	MSC/EMAS	3D Arbitrary	FEM	Frequency
Zeland Software	IE3D	3D Arbitrary	MoM	Frequency
Kimberly Communications Consultants	Micro-Stripes	3D Arbitrary	TLM	Time
Remco	XFDTD	3D Arbitrary	FDTD	Time

3-D space are determined, while MoMs results in current distribution on the surface of metallic structures.

Application to MMIC Design

All EM simulators are designed to solve arbitrarily shaped strip conductor structures and provide simulated data in single or multiport S parameters, which can be read in a circuit simulator. To perform an EM simulation, the structure to be simulated is defined in terms of dielectric and metal layers, and their thicknesses and material properties. After creating the complete circuit/structure, the ports are defined, and the layout file is saved as an input file for EM simulations. Then an EM simulation engine is used to perform electromagnetic analysis. After the simulation is complete, the field or current information is converted into S parameters and saved to be used with other CAD tools.

EM simulators, although widely used, still cannot handle complex designs. There is considerable emphasis on achieving first-pass success of single- and multi-function MMICs in order to keep the MMIC development cycle time and cost low. Thus, microwave circuits should not only perform as individual components but also work as designed in the subsystem environment (e.g., T/R chip). This mandates comprehensive simulation of the complete chain including parasitic coupling effects between the closely spaced matching networks belonging to different microwave circuits. Although the advent of EM simulators has enhanced the accuracy of individual circuit functions, they are seldom used to perform comprehensive simulation of the complex MMIC chips such as T/R chips because of their large circuit size and very large CPU time. Thus, next-generation EM simulators are required to characterize compact and multilayer MMICs, highly integrated MMICs, multichip assemblies (MCAs), for greater use of parallel computation and better integration with the circuit simulator so that they can become part of optimization. Recent advances in the numerical methods, computation speed, multiprocessor computations, and optimization techniques will set the course for EM simulators to become the microwave CAD tools of choice.

MODELING

The development of integrated CAD tools and accurate and comprehensive models for passive circuit elements and active devices have been a major activity during the 1980s and 1990s. Both play a key role in the successful development of MMICs. Passive circuit elements that have linear models (independent of bias conditions and input power) include resistors, inductors, capacitors, via holes, air bridges/crossovers, transmission lines, discontinuities, and interaction effects. Active devices consist of diodes, and transistors (single- and dual-gate FETs, HEMTs, and HBTs). Transistors are of low noise, switching, and power types. Active devices use both linear and nonlinear (bias and input power-dependant) models. Figure 14 is an attempt to summarize the current models for active devices and passive circuit elements. More comprehensive information on modeling can be found in books (11,19,21,37) and other publications (38–41).

Basically there are three types of models:

1. Physics/electromagnetic theory based models,
2. Analytical or hybrid models, and
3. Measurement-based models.

These models are briefly described next.

Physics/Electromagnetic Theory Based Models

Development of accurate physics-based models for active devices that are derived in terms of doping profile and physical geometry are essential for establishing the link between the process and RF performance and for designing MMICs. These models consist of two parts: instrinsic and extrinsic. The intrinsic part deals with the active channel of the device, whereas the extrinsic part represents device pad/electrode parasitics, which are expressed in resistances, inductances, and capacitances. The intrinsic part of the model, the heart of the device, is obtained by solving device equations using appropriate boundary and bias conditions in the device channel (e.g., under the gate between the gate, source and drain electrodes). The semiconductor device equations are derived from the Boltzmann transport equation coupled to the solution of the Poisson equation. These equations, which are of partial differential type and describe carrier transport properties of the device, are solved numerically by using such technique as finite differences or finite elements. The physical models also include device interface phenomena, quantum effects, effects of temperature and heterostructures, low noise

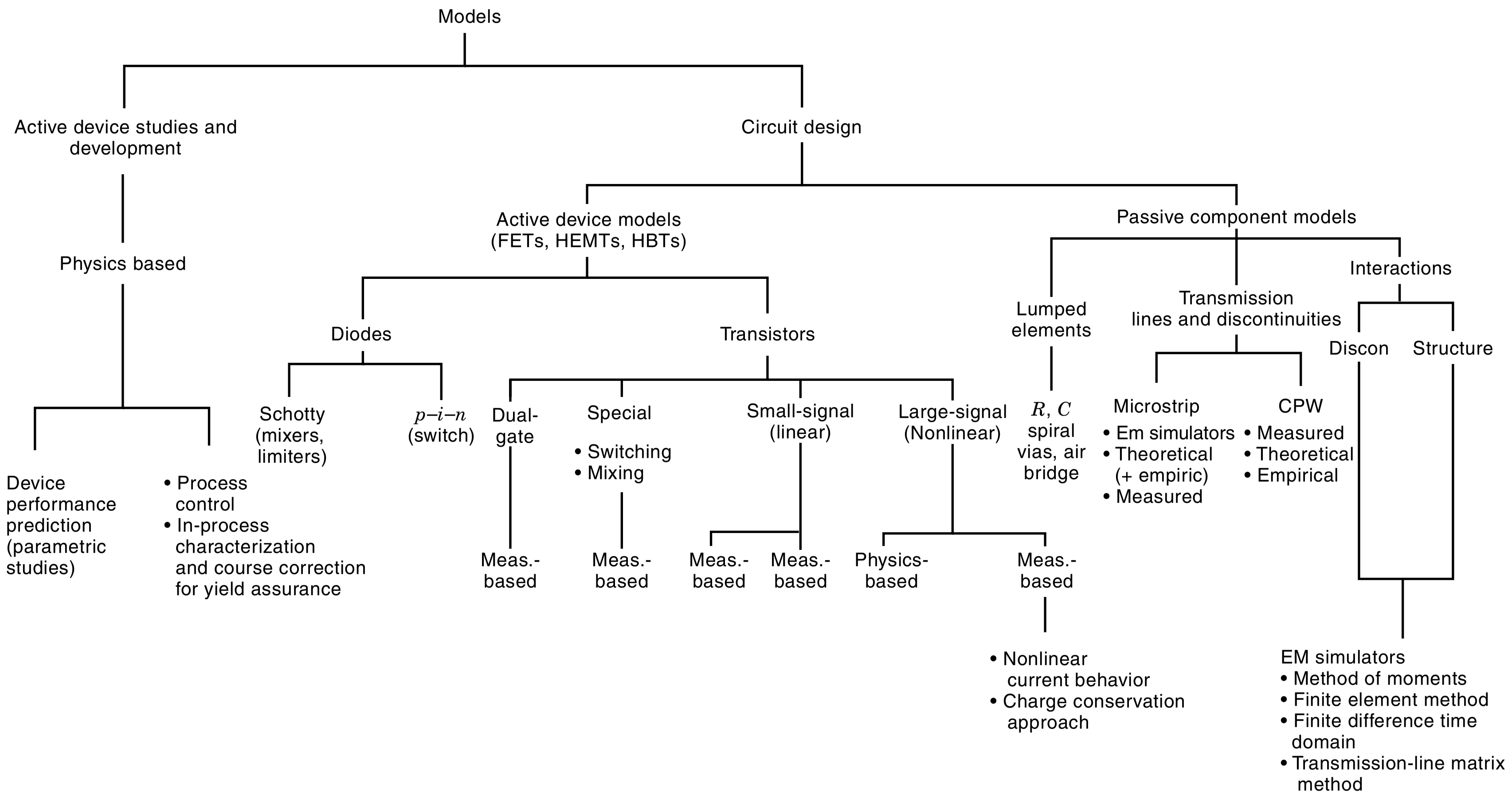


Figure 14. Spectrum of models and modeling techniques to support MMIC technologies.

and high-field phenomena, electromagnetic interaction effects between electrodes and many other effects. These models are of general nature but quite complex. They include accurate parasitics and bias temperature and frequency dependence and can be used in time and frequency domains. The physical models are very useful for investigating the physical operation of active devices, predicting device performance as a function of process, material and geometry. Thus, the device model helps in device studies, process control, and circuit yield and optimization. Any adjustment in the device can be achieved using the physics band model without costly fabrication experiments.

Because of lengthy execution times (physics-based analysis time increases rapidly with model complexity), the application of physical models is usually limited to device studies. Models are available for FETs, HEMTs and HBTs. Given sufficient computer resources, these models can become an integral part of microwave CAD tools.

Analytical or Hybrid Models

Analytical or hybrid models for passive circuit elements and active devices are based on simple equivalent circuit (EC) representation. The model parameters are formulated based on simple equations whose values are obtained from the physics of the component, or dc or RF or both measurements. The analytical models fall between physics- and measurement-based techniques. Transmission lines and their discontinuities and nonlinear devices are generally represented by analytical models.

Measurement-Based Models

The most commonly used method of developing models for passive lumped elements and active devices is by measuring their dc characteristics and S parameters. This modeling approach gives quick and accurate results, although they are generally limited to just the devices measured. The component is represented by an equivalent circuit model whose parameter values are extracted by computer correlation to the measured dc and S parameter data.

The accuracy of the measurement-based models depends upon the accuracy of the measurement systems, the calibration techniques and the calibration standards. On-wafer measurements using high-frequency probes provide accurate, quick nondestructive, and repeatable results up to millimeter wave frequencies. Various vector network analyzer calibration techniques are being used to determine a two-port error model that de-embeds the device S parameters. The conventional Short, Open, Load, and Through (SOLT) calibration technique has proven unsatisfactory because the open and short reference planes cannot be precisely defined. Unfortunately, the recently introduced calibration technique, Through-Short-Delay (TSD) also relies on either a short or open standard. The reference plane uncertainties for “perfect” short limit the accuracy of these techniques. The Line-Reflect-Match (LRM) calibration technique requires a perfect match on each port. The Thru-Reflect-Line (TRL) calibration method is based on the transmission line calibration standards, which include nonzero length thru and a reflect (open or short) and delay line standards (one or more dictated by the frequency range over which the calibration is performed). The advantage of TRL calibration lies in simple standards that can be placed on the same substrate as the components ensuring a common transmission medium. This calibration technique accurately locates the reference planes and minimizes radiative crosstalk effects between the two probes because they are sufficiently far apart during the calibration procedure.

Measurement-based models fall into two groups: linear (passive circuit elements and active devices for linear operation) and nonlinear (active devices for nonlinear operation such as mixing, power amplification, multiplication, and oscillation). In current measurement-based linear modeling, the components are electrically characterized by measuring dc and RF parameters. A lumped element equivalent circuit model for each component that describes its frequency-dependent electrical characteristics is chosen. The lumped-element model parameter values are extracted by computer optimization to replicate the measured S parameters. Noise characterization of active devices is obtained by measuring “on-wafer” S parameters and noise parameters. The switching devices are modeled by two lumped element equivalent circuit models: one for when the device is on (low-impedance state) and the second one for when the device is off (high-impedance state). The model parameter extraction is generally based on statistical data with average and standard deviation values that will help in centering designs for high yield.

As an example, an equivalent circuit (EC) model for an inductor along with its physical layout is shown in Fig. 15. This figure also includes model parameter values for three different inductors. An EC model for a MESFET is shown in Fig. 16(a), and its parameter values are shown in Fig. 16(b). This model describes basic linear operation of an FET, and the model reproduces the small-signal RF terminal characteristics of the device with good accuracy. The model is widely used to extrapolate S parameters to frequencies for which experimental data are not available and can be scaled to different sizes of the same device. The main disadvantages of the equivalent circuit model are difficulty in scaling to different physical structures, frequency independence of circuit elements, no time dependence feature, and the inherent limitation to linear circuits.

Many nonlinear equivalent circuit models have been reported in the literature. All these models have the same basic configuration as shown in Fig. 16(a) and generate similar common-source dc or pulsed I–V curves that are in qualitative agreement with experimental data. Significant differences occur, however, in the quantitative behavior of the models, both in comparison to each other and in comparison with experimental data. The differences in the various models are the expressions used to characterize the drain current generator and gate-source and the gate-drain capacitances. Some of the most commonly referred models are Curtice, Curtice-Ettenberg, Stratz, Materka, and TOM (42–44).

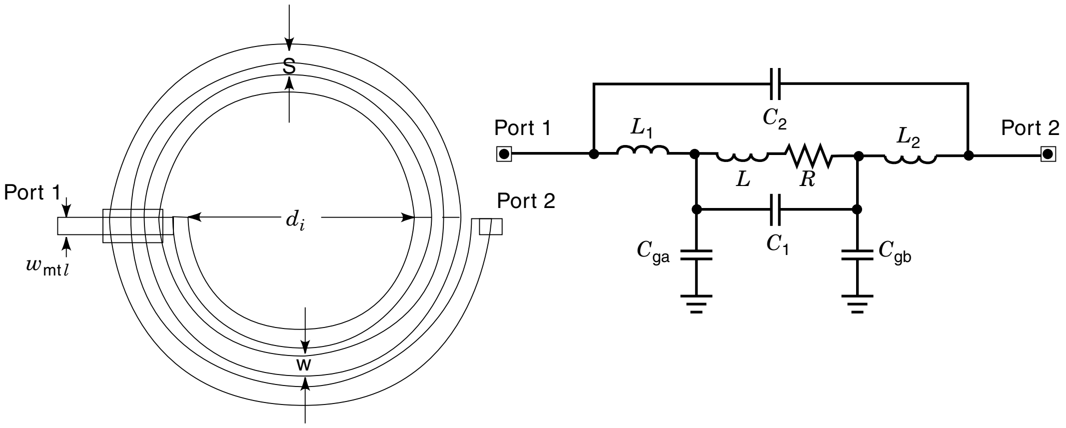
The measurement-based models need to include terminal voltage dependent equivalent circuit elements such as I_{ds} (g_m, R_{ds}), C_{gs} and C_{gd} as shown in Fig. 16 to accurately predict the nonlinear behavior of the active device.

Commonly used representation of the nonlinear MESFET model is given by

$$I_{ds} = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3)\tanh(\alpha V_{ds}) \tag{6}$$

where

$$V_1 = V_{gs}[1 + \beta(V_{ds0} - V_{ds})] \tag{7a}$$



Parameters	Units	1-511	2-511	3-511
Total inductance	nH	0.545	1.405	2.742
L	nH	0.249	0.985	2.138
L_1	nH	0.148	0.180	0.283
L_2	nH	0.148	0.240	0.321
C_1	pF	0.017	0.014	0.010
C_2	pF	0.008	0.009	0.0094
C_{ga}	pF	0.024	0.031	0.041
C_{gb}	pF	0.024	0.042	0.052
R_{dc}	Ω	0.370	0.600	1.100
Freq range	GHz	0–18	0–18	0–18

Dimensions		Units			
n_{turns}	(number of turns)		1.5	2.5	3.5
d_i	(inductor inside diameter)	μm	108	108	108
w	(conductor width)	μm	20	16	12
s	(conductor space)	μm	8	10	14
$w_{\text{mt}l}$	(width of metal 1)	μm	18	18	18

Calculations internal to Libra model:
Data taken from wafers 295-7-1 and 295-7-6
Substrate thickness = 125 μm

$R = R_{dc}\,[\,1 + 0.125\,\sqrt{f\,(\text{GHz})}\,]\ \Omega$
Valid frequency range = 0–18 GHz
Maximum current capacity = 35 mA

Figure 15. Physical layout and the equivalent circuit model and its values of spiral inductors (1.5, 2.5 and 3.5 turns).

and

$$C_{gs} = C_{gs0} \cdot f(V_{gs}, V_{gd}) \tag{7b}$$

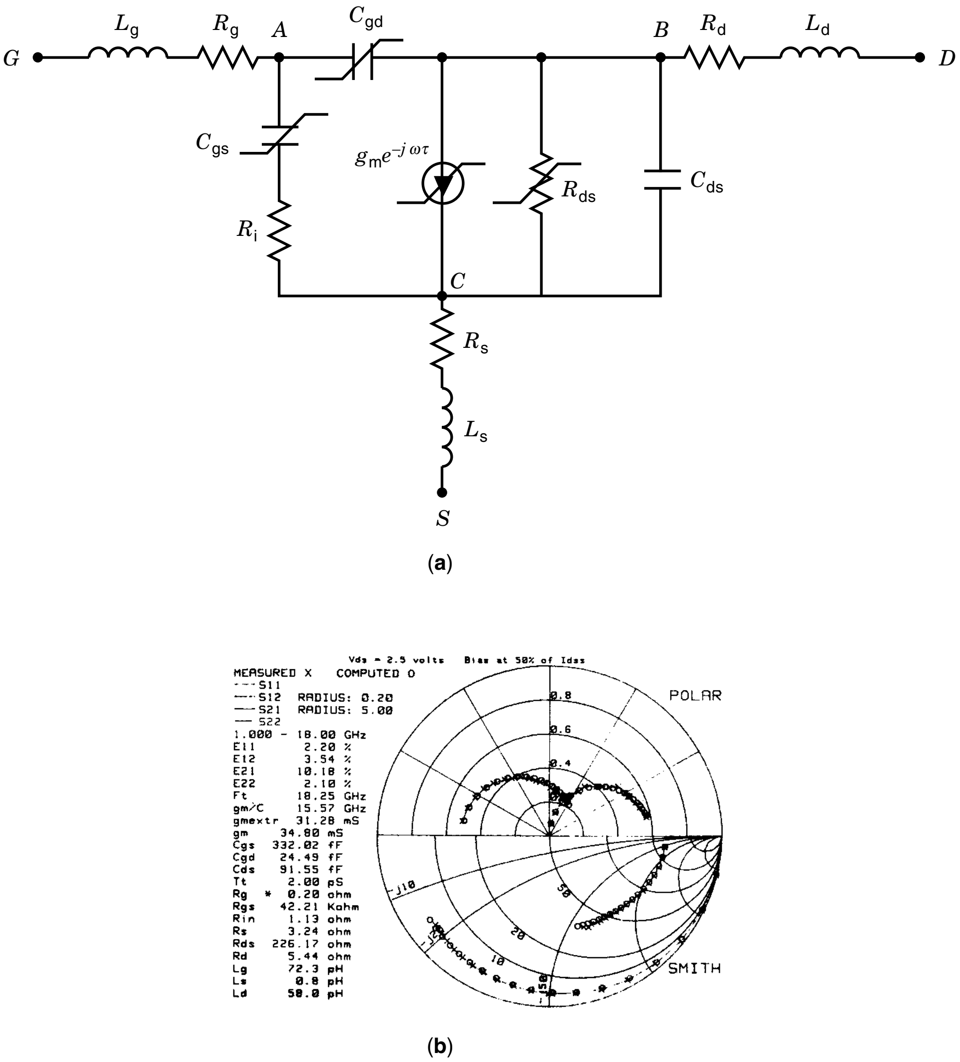
$$C_{gd} = C_{gd0} \cdot g(V_{gs}, V_{gd}) \tag{7c}$$

Here V_{gs}, V_{gd}, and V_{ds} are the terminal voltages between gate-source, gate-drain, and drain-source of the device, respectively. The source of the FET is normally grounded. The A_i coefficients and constants α, β, and V_{ds0} are evaluated using measured dc or pulsed I–V data. The quantities C_{gs0} and C_{gd0} are extracted from the measured S parameter at the operating dc bias conditions, whereas f and g, which are functions of both V_{gs} and V_{gd}, are determined from measured S parameters over a large range of dc bias conditions to cover the full range of device operation.

Basically there are three steps in the development of nonlinear equivalent circuit models.

- Extract coefficients for I_{ds} to match with measured I–V data. Important data are near the knee of the curves and break down near pinch-off.
- Measure S parameters, extract small-signal model values, and derive coefficients for gate-source and gate-drain capacitances to describe its dependence on gate and drain voltages.
- Validate model by comparing measured and simulated data with 50 Ω input and output for P_{1dB} compression point and power levels for other harmonics. Simulations are generally carried out using harmonic balance analysis.

The main advantage of the equivalent circuit models is the ease with which they can be integrated into radio frequency (RF) circuit simulators. For linear operation (i.e., small-signal) the interface is direct because the entire device and cir-



```
                Vds = 2.5 volts   Bias at 50% of Idss
MEASURED X   COMPUTED O
---S11
---S12  RADIUS: 0.20
---S21  RADIUS: 5.00
--- S22
1.000 - 18.00 GHz
E11        2.20 %
E12        3.54 %
E21       10.18 %
E22        2.10 %
Ft        18.25 GHz
gm/C      15.57 GHz
gmextr   31.28 mS
gm     34.80 mS
Cgs   332.02 fF
Cgd    24.49 fF
Cds    91.55 fF
Tt      2.00 pS
Rg  *   0.20 ohm
Rgs    42.21 Kohm
Rin     1.13 ohm
Rs      3.24 ohm
Rds   226.17 ohm
Rd      5.44 ohm
Lg      72.3 pH
Ls       0.8 pH
Ld      58.0 pH
```

Figure 16. FET's small signal equivalent circuit model and typical model values for a 300 μm power FET biased at $V_{ds} = 2.5$ V, $I_{ds} = 50\%$ I_{dss}. Variable elements: C_{gs}, C_{gd}, g_m and R_{ds} are strong functions of bias conditions.

cuit model are simulated in the frequency domain. For nonlinear applications, the device models are formulated in the time domain and are interfaced with the frequency domain linear circuit simulators by means of the Harmonic Balance Method. The RF performance obtained from these simulators can be satisfactory to good for a well-defined circuit, especially for mildly nonlinear applications such as a class A power amplifier not operating in hard saturation. The large-signal equivalent circuit models generally do not scale well with varying operational conditions such as frequency or bias. As the circuit becomes increasingly nonlinear, simulator performance degrades.

The main disadvantage of the equivalent circuit models is inherent inaccuracy resulting from simplifications in the model formulation, such as neglect of domain capacitance and the interdependencies of the nonlinear elements. In an actual device, all nonlinear elements are interdependent. For example, in a MESFET, it is not possible to change the device transconductance without also changing elements such as the gate-source capacitance. Perhaps the most significant limitation of the equivalent circuit models, however, is the need to experimentally characterize the devices that are to be used. The devices must be designed, fabricated, and characterized before the CAD models can be defined. A change in any design parameter (such as gate width or channel impurity concentration) requires an almost complete recharacterization because scaling techniques are difficult to apply. This limits the designer's flexibility in obtaining optimum performance integrated circuits where tailoring the device design for special applications would be desirable.

TYPICAL CIRCUITS AND PERFORMANCE

In the last 16 years, tremendous progress has been made in amplifiers, including low noise, power, transimpedance, logarithmic, and limiting and variable gain. In addition to these amplifiers, control circuits, mixers, oscillators, and multifunction integrated circuits (MFICs) also have advanced the state of the art in microwave technology. Because this technology is growing rapidly, new examples of its application are constantly appearing. No attempt to include an exhaustive sampling is made; instead, a selection of circuits that have been developed for various applications will be described so that the diversity of the MMIC technology may be illustrated. Circuits chosen for exposition include low-noise and power

Table 3. Best Reported InP HEMT MMIC LNA Results

Frequency (GHz)	Number of Stages	Minimum NF (dB)	Gain (dB)	NF over Band (dB)	Year Reported
2.3–2.5	3	0.4	35	0.5 max	1993
7–11	2	1.0	21	1.2 max	1993
19–22	3	1.1	38	1.2 max	1995
43–46	2	—	25	2.3 ave	1993
43–46	3	1.9	22	2.0 ave	1995
50	2	2.8	9	—	1994
63	2	3.0	18	—	1990
56–60	2	3.2	15	4.2 ave	1992
56–64	3	2.7	25	3.0 ave	1993
58–62	2	2.2	16	2.3 ave	1995
75–110	3	3.3	11	5.0 max	1993
75–110	4	6.0	23	—	1993
92–96	3	3.3	20	4.4 max	1995
120–124	2	—	11	—	1994
142	2	—	9	—	1995

amplifiers, oscillator, mixer, and integrated multifunction circuits.

Low-Noise Amplifiers

A low-noise amplifier (LNA) at a receiver front end sets the system noise figure. Narrowband and broadband LNAs are required depending upon the system application. Table 3 compares the state of the art in narrowband MMIC multistage LNAs developed using PHEMTs (45). Noise figures of about 1 dB and 3.3 dB have been achieved at 10 GHz and 94 GHz, respectively. The photograph of a three-stage 75 GHz to 110 GHz MMIC amplifier is shown in Fig. 17. For this chip, the best noise figure measured was 3.3 dB at the W band.

Power Amplifiers

In comparison with power tubes, microwave power solid-state amplifiers are compact in size, lightweight, low cost, more reproducible, more efficient and reliable, and they operate at lower supply voltages. These amplifiers are used in transmitters and require much shorter warm-up time. Furthermore, no adjustment in the bias is required over long periods of operation. The performance of MESFET, PHEMT, and HBT amplifiers is constantly improving in terms of output power, power-added efficiency, linearity, and frequency. Microwave power amplifiers using monolithic technology look attractive for realizing tens of watts of power; these chips can be combined further using standard hybrid MIC techniques to obtain much higher power levels. High-efficiency operation of these circuits is becoming one of the most important factors for enhancing battery operating life in commercial communication applications and for reducing prime power and cooling requirements for advanced microwave and millimeter wave systems. These characteristics are particularly useful for space and military applications where weight, size, and power-added efficiency requirements can impose severe limitations on the choice of components and systems. Figure 18 depicts (46) power performance for single-chip MMIC amplifiers at microwave and millimeter wave frequencies, and a photograph of a 15 W amplifier chip using MESFET technology is shown in Fig. 19. This C-band amplifier achieved over 60% power-added efficiency (47).

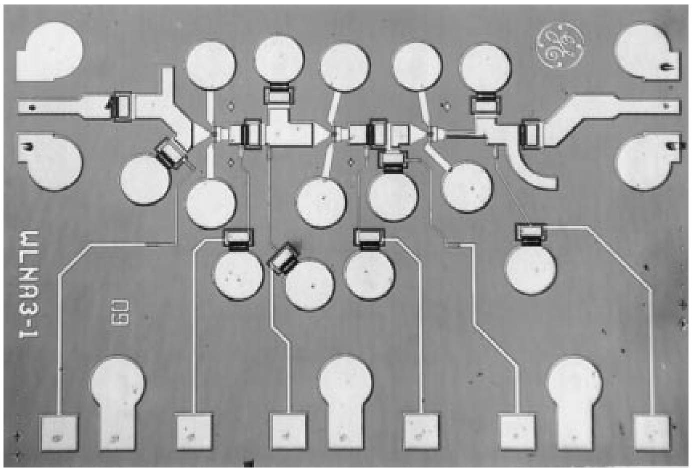


Figure 17. A three-stage 75 GHz to 110 GHz PHEMT MMIC low-noise amplifier. Chip size is 5 mm^2. (Reprinted with permission from P. M. Smith, and IEEE © 1996.)

Voltage Controlled Oscillators and Mixers

Voltage-controlled oscillators (VCOs) and mixers are integral parts of receivers. Figure 20 shows the photograph of a 28 GHz VCO developed using HBT technology (48). Output power up to -5 dBm and tuning range up to 20% were achieved for this chip. Figure 21 shows the photograph of a VCO-mixer, which works as an upconverter developed using GaAs HEMT-HBT IC technology (49). The compact MMIC's area is only 1 mm^2. The VCO uses HBT and provided 0 dBm output power over 28.5 GHz to 29.3 GHz, whereas the active mixer used HEMT and achieved 6 dB to 9 dB conversion loss over a 31 GHz to 39 GHz output frequency range.

Multifunctional MMICs

Up until now, we have described single-function monolithic circuits. The next four examples represent highly integrated MMICs. A high level of integration at the MMIC chip level reduces the number of chips and results in low test and assembly costs, which in turn reduces the subsystem cost. The

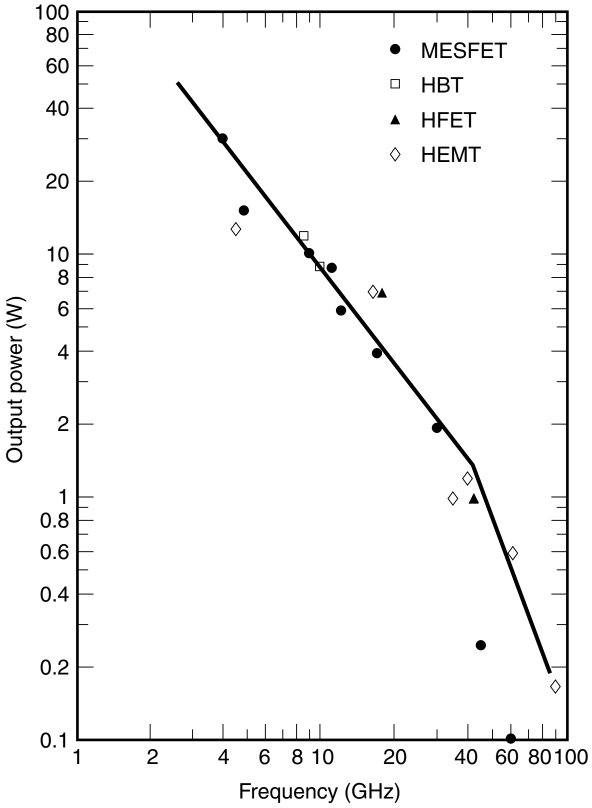


Figure 18. Performance status of single-chip power MMIC amplifiers using MESFET, HFET, HEMT, and HBT technologies. HFET: heterojunction FET.

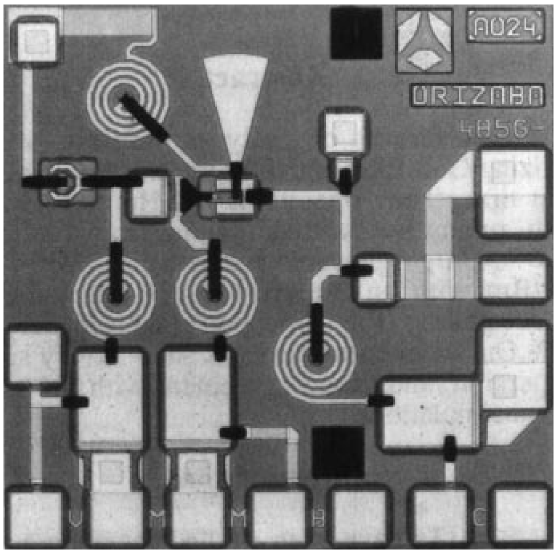


Figure 20. A 28 GHz HBT MMIC voltage control oscillator. Chip size is 1 mm^2. (Reprinted with permission from H. Blanck, and IEEE © 1994.)

downside of high integration is higher nonrecurring engineering costs, and greater difficulty in optimizing each subcircuit's performance.

In active-phased array antennas, each antenna element consisting of a transmitter, a receiver, a radiator, and control circuitry is called a transmit/receive module. Thus, reducing the cost of GaAs IC-based transmit/receive modules is essential to the deployment of low-cost active-phased array radars. A complete C-band multifunction monolithic transceiver, containing 16 microwave circuits, has been developed (50) on a GaAs substrate measuring 10.8 × 15.7 mm (170 mm^2). The chip includes a class-B 4 W power amplifier with 40% power-added efficiency, a high-power T/R switch, several SPDT switches, buffer amplifiers, a 6-bit programmable phase shifter, digital and analog attenuators, and an LNA with 4.5 dB. Figure 22 shows the photograph of the chip. The IC used 58 separate FETs, 87 via holes, 83 MIM capacitors, 153 resistors, 6 spiral inductors and 65 airbridges. A single 2 to 20 GHz T/R chip on GaAs has also been developed (51). A photograph of the chip is shown in Fig. 23. The chip, which measures 17.6 mm^2, consists of T/R switches, driver amplifer, power amplifier, and LNA. A basic traveling wave design approach was used for amplifiers. The measured performance includes a maximum noise figure of 10 dB with associated gain of 18 dB and minimum power output of 200 mW with associated gain of 12 dB. This chip uses 44 FETs, 60 via holes, 44 MIM capacitors, 69 resistors, and 60 spiral inductors. Typical yield for a circuit of this complexity exceeds 50%. A highly integrated multifunction macro synthesizer chip has also been reported by Mondal et al. (52). It has more than 30 RF building blocks and some individual blocks operate through 40 GHz. This MMIC represents the highest level of integration on a single GaAs chip.

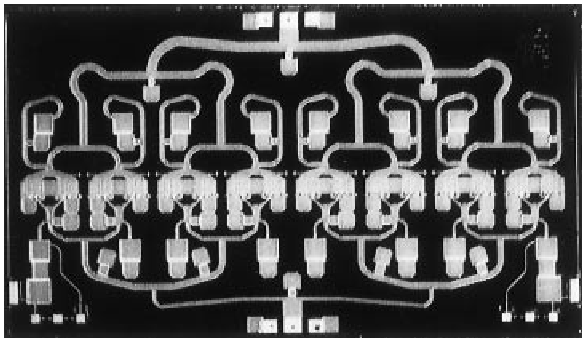


Figure 19. A C-band MESFET 15 W power MMIC amplifier. Chip size is 24 mm^2. (Photograph courtesy of ITT Industries.)

Microwave and millimeter wave components, subsystems, and systems have been experiencing ever-increasing pressure to reduce costs to support the emergence of wireless and mobile communications applications and widespread use of phased-array radars. There is a need for new technologies to meet the challenge in size, performance, and cost requirements. Recently, GaAs monolithic 3-D technology has made tremendous progress in achieving both performance and cost requirement goals. 3-D technologies provide another dimension in the integration and compaction of MMICs, where the matching networks, interconnects, and passive circuits are realized in a multilayer 3-D volume. As an example, Fig. 24 shows a complete receiver (53), using low-noise amplifier, local oscillator amplifier, couplers and voltage gain amplifier, and occupies only a 4 mm^2 chip area on GaAs when fabricated using 3-D MMIC technology.

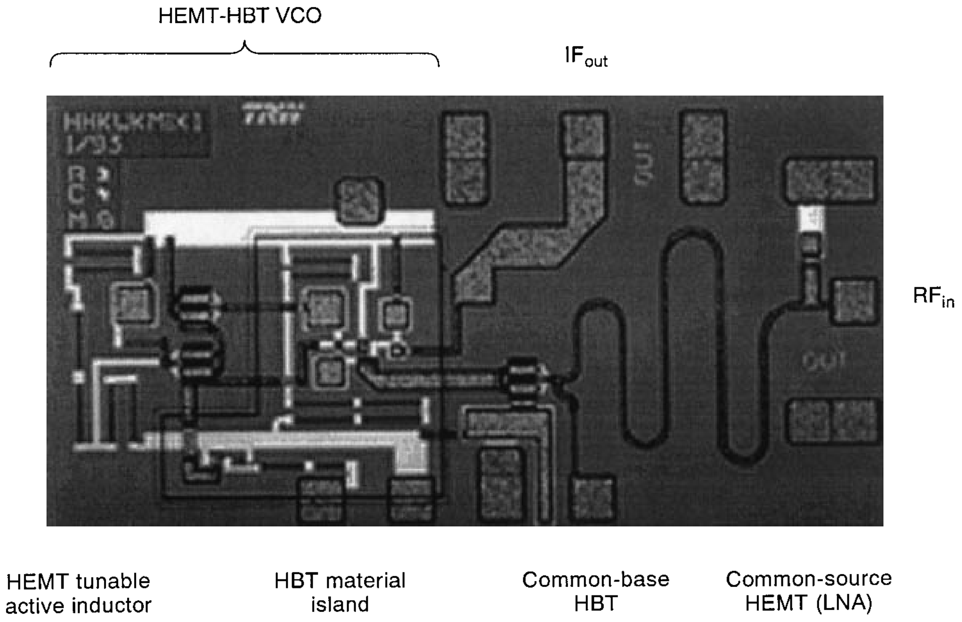


Figure 21. The HEMT-HBT VCO-mixer. The Compact MMIC is only 1.1 mm^2 in size. (Reprinted with permission from K. W. Kobayashi, and IEEE © 1997.)

MMIC PACKAGING

Microwave packages and assembly techniques play a very important role in the performance, cost, and reliability of MMICs. Because MMICs represent state-of-the-art technology in terms of size, weight, performance, reliability, and cost, MMIC performance must not be compromised by packaging. The affordability requirement on packages mandates that their complexity be minimized. Minimizing both the number of dielectric layers and the overall size, dramatically improves electrical performance, production yields, and lower costs. However, a trade-off exists between simplicity and the number of functional features in terms of costs. Some high-volume applications demand package costs as low as five or ten cents, whereas high-performance, low-volume applications can tolerate package costs (in the $5 to $25 range).

Many of the packaging considerations for MMICs are similar to those for hybrid MICs. Most ceramic/metal packages should meet the environmental requirements of MIL-S-19500 and test requirements of MIL-STD-750/883. The package must pass rigorous tests of hermetic properties, thermal and mechanical shock, moisture resistance, resistance to salt atmosphere, vibration and acceleration, and solderability. In order to minimize the effect of the package on MMIC performance, electrical, mechanical and thermal modeling of packages must be performed.

The most important electrical characteristics of microwave packages are low insertion loss, high return loss and isolation, and no cavity or feedthru reasonance over the operating frequency range. When a chip or chip set is placed in the cavity of a microwave package, there should be minimum degradation in the chip's performance. Generally this cannot be ac-

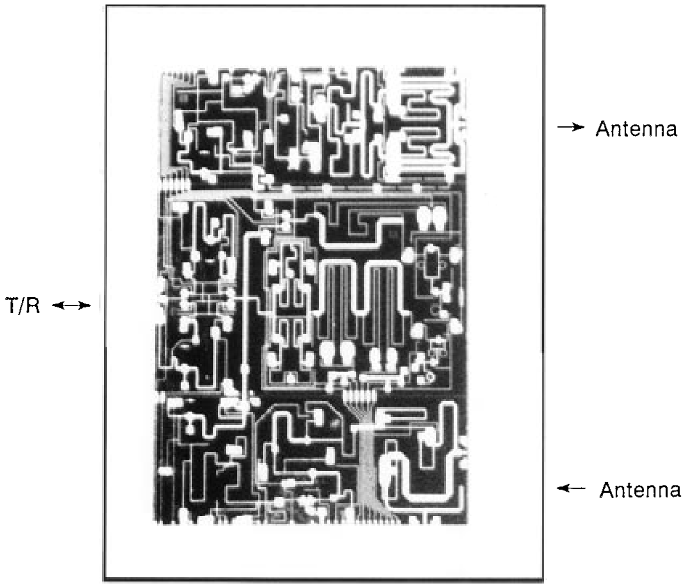


Figure 22. The 16-microwave function C-band T/R chip. Chip size = 170 mm^2. (Photograph courtesy of ITT Industries.)

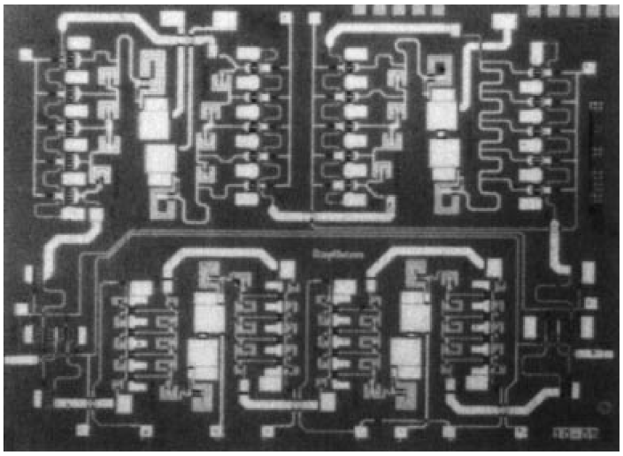


Figure 23. The broadband (2 GHz to 20 GHz) T/R chip. (Reprinted with permission from M.J. Schindler, and IEEE © 1990.)

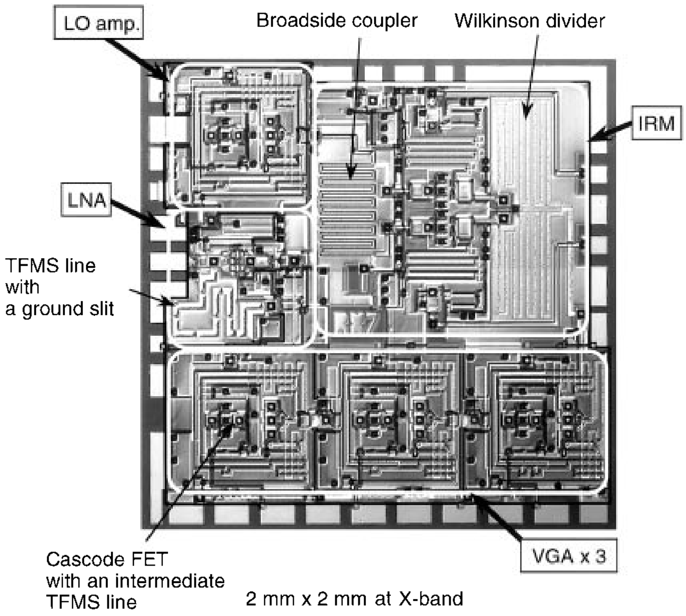


Figure 24. The 3-D MMIC single-chip receiver. Chip size is 4 mm^2. (Reprinted with permission from I. Toyoda, and IEEE © 1996.)

complished without accurate electrical and electromagnetic modeling of the critical package elements. Microwave design must be applied to three parts of the package: RF feedthru, cavity and dc bias lines. Of the three, the design of the RF feedthru is the most critical in determining the performance of packaged MMIC chips.

MMIC packaging can be performed at three levels as shown (15) in Fig. 25. ICs can be mounted in individual packages; ICs can be packaged with support circuitry in a housing; or the ICs can be packaged at the subsystem level. The packaging requirements depend upon the application at hand. For example, in wireless communications applications below 2 GHz, GaAs MMICs are being mounted into plastic packages in order to achieve low cost goals. Because of relatively low power operation, thermally they are acceptable. For high-frequency, high-performance, and high-power applications, we require metal base ceramic packages, which have low thermal resistance, good hermetic properties, high power capability, and good reliability characteristics.

Ceramic Packages

The selection of the substrate material and thickness for ceramic packages depends on the electrical performance requirements, cost, and frequency range of interest. The substrate thickness is selected to match its height with MMIC thickness; otherwise, a pedestal for mounting MMIC chips is required because MMIC chips are about 4 mil thick. Microwave packages generally use 10 mil to 20 mil thick alumina substrate, whereas millimeter-wave packages use 4 mil to 5 mil thick quartz. A low dielectric constant is generally preferred because it makes the package interconnects electrically insensitive and tolerant to microstrip dimensions and broadband frequency ranges and results in a high yield. The microstrip width and thickness determines the characteristic impedance and the dc resistance, whereas the spacing between the two conductors on the same plane controls the crosstalk because of coupling. Generally, sufficient space between the MMIC, the package walls, and the lid is provided in order to prevent any interactions. The effect of the package lid on the MMIC characteristics is kept to a minimum by keeping the lid above the MMIC surface about five times the package substrate thickness. Lids with absorbing materials are also used.

Several ceramic (alumina, Al_2O_3), beryllium-oxide (BeO) and aluminum nitride (AlN) packages with metal base (Kovar, copper, copper-tungston, or copper mollybdum) are now available. Their cost depends upon package size, frequency of operation, and volume. Some of these packages can be used up to 40 GHz, and others can be obtained for less than \$3 in large volume. In small quantities, they cost between \$20 and \$50. Typically, the measured dissipative loss per RF feed is less then 0.5 dB at 20 GHz. These packages provide much higher frequency of operation, low leadframe inductance, very

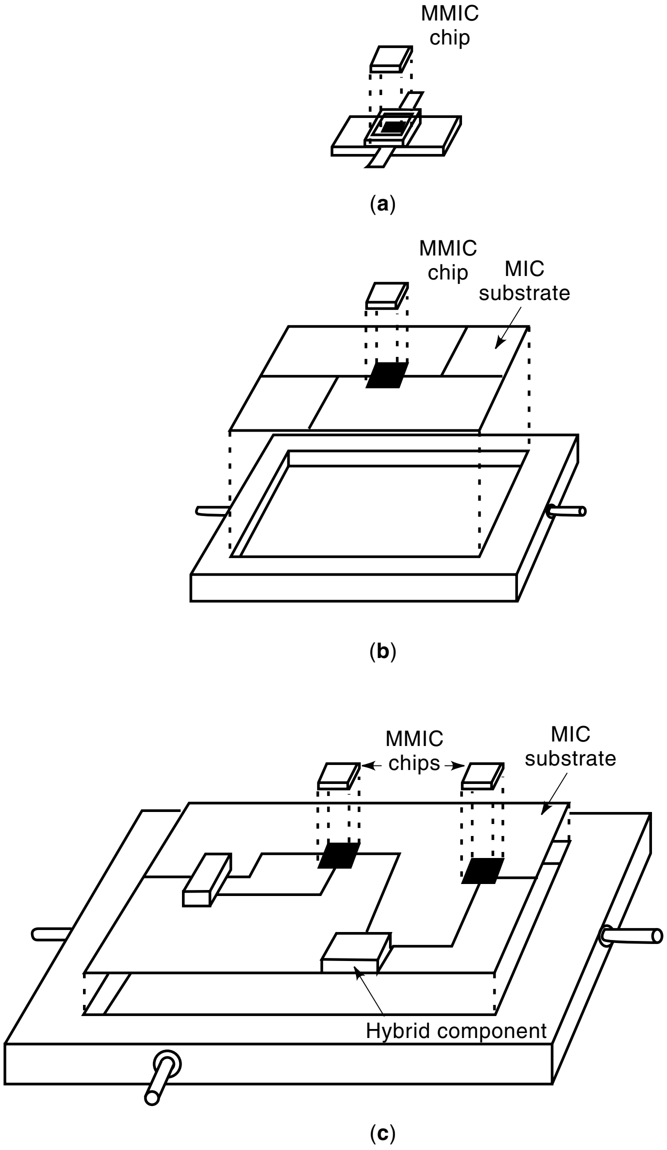


Figure 25. Three packaging level details: (a) MMIC in package; (b) MMIC with support circuitry; and (c) MMICs with hybrid and support circuitry.

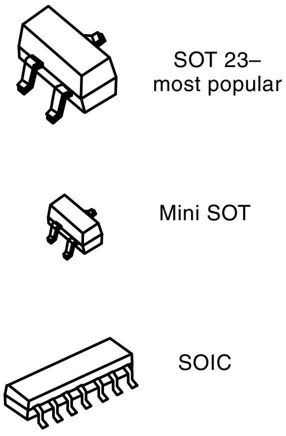


Figure 26. Plastic packages for RF and microwave applications.

low ground connection inductance, and much lower thermal resistance than the plastic packages. Ceramic-type packages are well suited for high-frequency small signal and high-power MMICs, whereas the plastic packages are commonly used for low-cost solutions at the lower end of the microwave frequency band.

Plastic Packages

Small outline transistor (SOT) and small outline integrated circuit (SOIC) plastic packages are commonly used. These packages are shown in Fig. 26. SOIC packages have 8 to 16 pins, and they work reasonably well up to 2 GHz. The measured dissipative loss in a SOIC 8 lead package is on the order of 0.2 dB at 2 GHz. In order to improve the RF performance and power dissipation for power ICs, customer-fused lead frames with low-signal lead parasitics and reduced-ground bond inductance are being used in custom plastic packages. Plastic-molded IC packages are described in two packaging handbooks (54,55). The dielectric constant and loss tangent values of the organic molding compound are about 3.7 and 0.01, respectively. The lead frame, which is the central support structure for ICs, is the backbone of a molded plastic package. Several different types of lead frame materials such as nickel-iron and copper-based alloys are being used. Their selection for a particular application depends on factors such as cost, performance, and ease of fabrication. The ICs are packaged using surface-mounting techniques. SOIC packages are manufactured in quantities of over 10 billion per year, the material and packaging labor cost together are less than $0.25 per package.

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