DC–DC POWER CONVERTERS

CHOPPERS

SWITCHING POWER SUPPLIES

INTRODUCTION

Direct current–direct current (dc–dc) power converters are employed in a variety of applications, including power supplies for personal computers, office equipment, spacecraft power systems, laptop computers, and telecommunications equipment, as well as dc motor drives. The input to a dc–dc converter is an unregulated dc voltage V_g. The converter produces a regulated output voltage V, having a magnitude (and possibly polarity) that differs from V_g. For example, in a computer off-line power supply, the 120 V or 240 V ac utility voltage is rectified, producing a dc voltage of approximately 170 V or 340 V, respectively. One or more dc-dc converters then reduce the voltage to the regulated several volts required by the processor integrated circuits (ICs).

High efficiency is invariably required because cooling of inefficient power converters is difficult and expensive. The ideal dc–dc converter exhibits 100% efficiency; in practice, efficiencies of 70% to 95% are typically obtained. This is achieved using *switched-mode,* or *chopper,* circuits whose elements dissipate negligible power. *Pulse-width modulation* (PWM) allows control and regulation of the total output voltage. This approach is also employed in applications involving alternating current, including high-efficiency dc–ac power converters (inverters and power amplifiers), ac–ac power converters, and some ac–dc power converters (low-harmonic rectifiers).

Power Stage Operation

A basic dc–dc converter circuit known as the *buck converter* is illustrated in Fig. 1 ((1–5)) A single-pole double-throw (SPDT) switch is connected to the dc input voltage V_g as shown. The switch output voltage $v_s(t)$ is equal to V_g when the switch is in position 1 and is equal to zero when the switch is in position 2. The switch position varies periodically, such that $v_s(t)$ is a rectangular waveform having period T_s and duty cycle D. The duty cycle is equal to the fraction of time that the switch is connected in position 1, and hence, $0 \le D \le 1$. The *switching frequency* f_s is equal to $1/T_s$. In practice, the SPDT switch is realized using semiconductor devices such as diodes, power metal-oxide-semiconductor field-effect transistors (MOSFETs), insulated-gate bipolar transistors (IGBTs), bipolar junction transistors (BJTs), or thyristors. Typical switching frequencies lie in the range 1 kHz to 1 MHz, depending on the speed of the semiconductor devices.

The switch network changes the dc component of the voltage. By Fourier analysis, the dc component of a waveform is given by its average value. The average value of

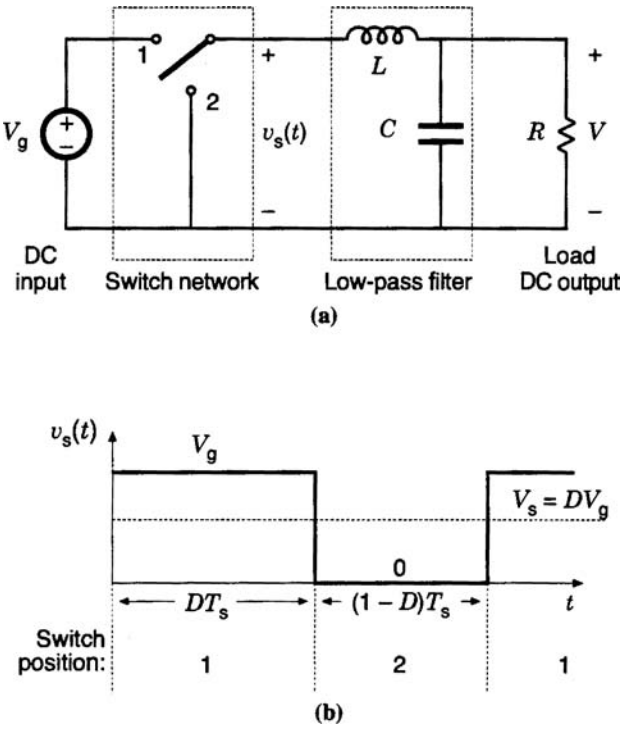


Figure 1. The buck converter consists of a switch network that reduces the dc component of voltage and a low-pass filter that remove the high-frequency switching harmonics: (a) schematic and (b) switch voltage waveform.

$v_s(t)$ is given by

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)dt = DV_g \tag{1}$$

The integral is equal to the area under the waveform or the height V_g multiplied by the time DT_s. It can be observed that the switch network reduces the dc component of the voltage by a factor equal to the duty cycle D. As $0 \le D \le 1$, the dc component of V_s is less than or equal to V_g.

The power dissipated by the switch network is ideally equal to zero. When the switch contacts are closed, then the voltage across the contacts is equal to zero and hence the power dissipation is zero. When the switch contacts are open, then there is zero current and the power dissipation is again equal to zero. Therefore, the ideal switch network can change the dc component of voltage without dissipation of power.

In addition to the desired dc voltage component V_s, the switch waveform $v_s(t)$ also contains undesired harmonics of the switching frequency. In most applications, these harmonics must be removed, such that the converter output voltage $v(t)$ is essentially equal to the dc component $V = V_s$. A low-pass filter is employed for this purpose. The converter of Fig. 1 contains a single-section L-C low-pass filter. The filter has corner frequency f_0 given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

The corner frequency f_0 is chosen to be sufficiently less than the switching frequency f_s, so that the filter essentially

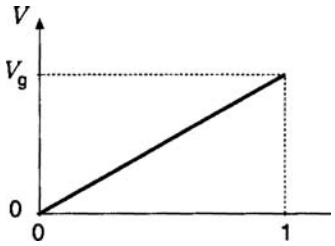


Figure 2. Buck converter dc output voltage V vs. duty cycle D.

passes only the dc component of $v_s(t)$. To the extent that the inductor and capacitor are ideal, the filter removes the switching harmonics without dissipation of power. Thus, the converter produces a dc output voltage whose magnitude is controllable via the duty cycle D, using circuit elements that (ideally) do not dissipate power.

The *conversion ratio M(D)* is defined as the ratio of the dc output voltage V to the dc input voltage V_g under steady-state conditions:

$$M(D) = \frac{V}{V_g} \tag{3}$$

For the buck converter, *M(D)* is given by,

$$M(D) = D \tag{4}$$

This equation is plotted in Fig. 2. It can be observed that the dc output voltage V is controllable between 0 and V_g, by adjustment of the duty cycle D.

Figure 3 illustrates one way to realize the switch network in the buck converter, using a power MOSFET and diode. A gate drive circuit switches the MOSFET between the conducting (on) and blocking (off) states, as commanded by a logic signal $\delta(t)$. When $\delta(t)$ is high (for $0 < t < DT_s$), then MOSFET Q_1 conducts with negligible drain-to-source voltage. Hence, $v_s(t)$ is approximately equal to V_g, and the diode is reverse-biased. The positive inductor current $i_L(t)$ flows through the MOSFET. At time $t = DT_s$, $\delta(t)$ becomes low, commanding MOSFET Q_1 to turn off. The inductor current must continue to flow; hence, $i_L(t)$ forward-biases diode D_1 and $v_s(t)$ is now approximately equal to zero. Provided that the inductor current $i_L(t)$ remains positive, then diode D_1 conducts for the remainder of the switching period. Diodes that operate in the manner are called *freewheeling diodes*.

PWM Control System

As the converter output voltage $v(t)$ is a function of the switch duty cycle D, a control system can be constructed that varies the duty cycle to cause the output voltage to follow a given reference v_r. Figure 3 illustrates the block diagram of a simple converter feedback system. The output voltage is sensed using a voltage divider and is compared with an accurate dc reference voltage v_r. The resulting error signal is passed through an op-amp compensation network. The analog voltage $v_c(t)$ is next fed into a PWM. The modulator produces a switched voltage waveform that controls the gate of the power MOSFET Q_1. The duty cycle D of this waveform is proportional to the control voltage $v_c(t)$.

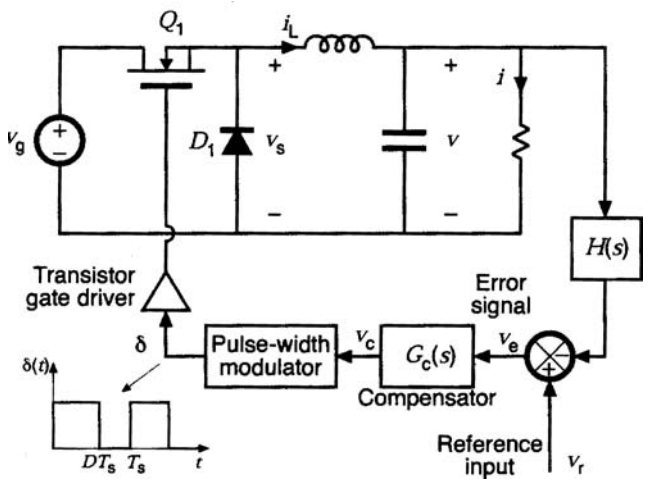


Figure 3. Realization of the ideal SPDT switch using a transistor and freewheeling diode. In addition, a feedback loop is added for regulation of the output voltage.

This approach is sometimes called *voltage-mode control*.

If this control system is well designed, then the duty cycle is automatically adjusted such that the converter output voltage v follows the reference voltage v_r and is essentially independent of variations in v_g or the load current. Because the PWM samples $v_c(t)$ at a rate equal to the switching frequency f_s the feedback system generally is designed such that its bandwidth is substantially slower than the switching frequency.

CONVERTER CIRCUIT TOPOLOGIES

A large number of dc–dc converter circuits is known that can increase or decrease the magnitude of the dc voltage and/or invert its polarity (1–5). Figure 4 illustrates several commonly used dc–dc converter circuits, along with their respective conversion ratios. In each example, the switch is realized using a power MOSFET and diode; however, other semiconductor switches such as IGBTs, BJTs, or thyristors can be substituted if desired.

The first converter is the buck converter, which reduces the dc voltage and has conversion ratio $M(D) = D$. In a similar topology known as the boost converter, the positions of the switch and inductor are interchanged. This converter produces an output voltage V that is greater in magnitude than the input voltage V_g. Its conversion ratio is $M(D) = 1/(1 - D)$.

In the buck-boost converter, the switch alternately connects the inductor across the power input and output voltages. This converter inverts the polarity of the voltage and can either increase or decrease the voltage magnitude. The conversion ratio is $M(D) = -D/(1 - D)$.

The Cuk converter contains inductors in series with the converter input, and output ports. The switch network alternately connects a capacitor to the input and output inductors. The conversion ratio *M(D)* is identical to that of the buck-boost converter. Hence, this converter also inverts the voltage polarity, while either increasing or decreasing the voltage magnitude.

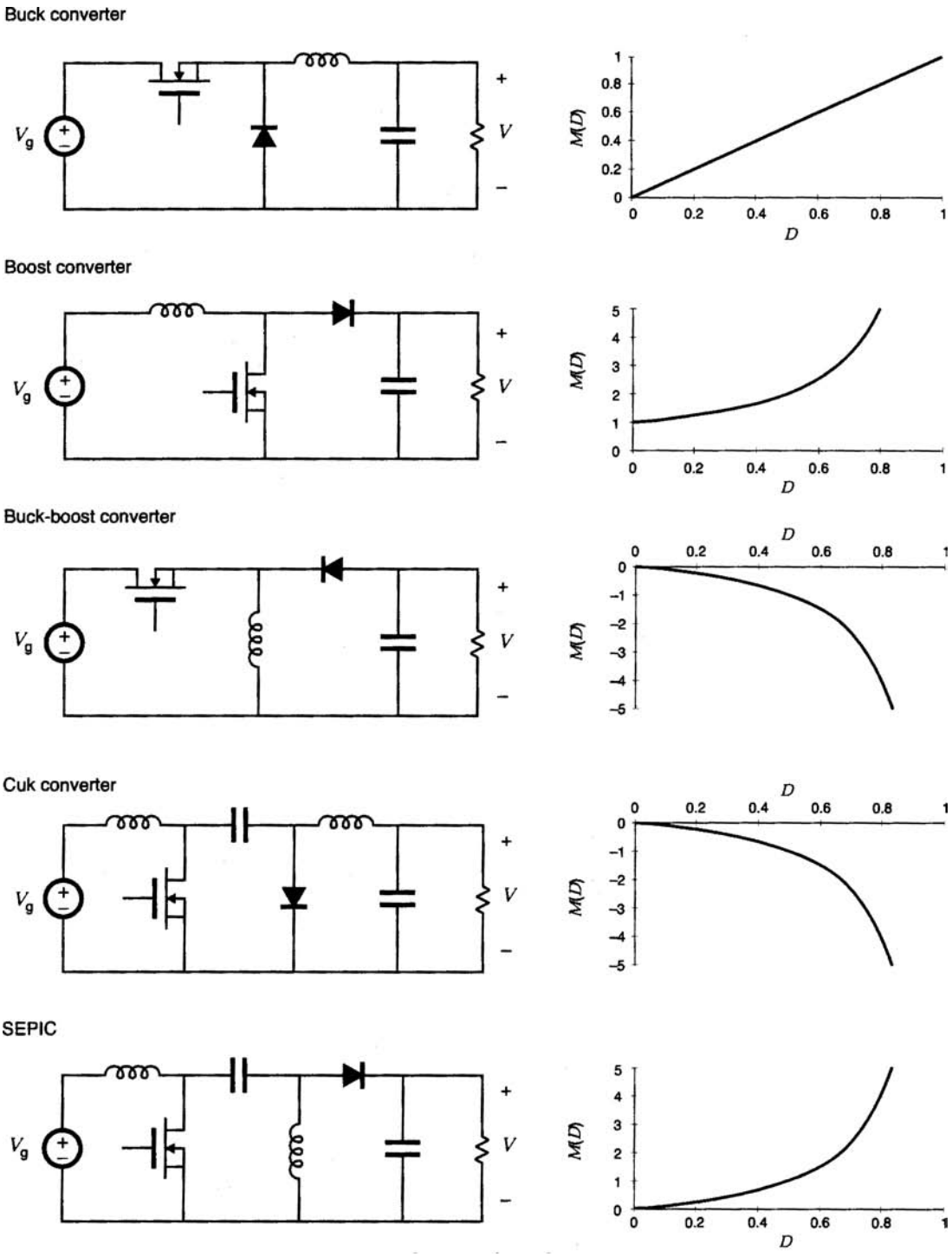


Figure 4. Several basic dc–dc converters and their dc conversion ratios $M(D) = V/V_g$.

The single-ended primary inductance converter (SEPIC) can also either increase or decrease the voltage magnitude. However, it does not invert the polarity. The conversion ratio is $M(D) = D/(1 - D)$.

ANALYSIS OF CONVERTER WAVEFORMS

Under steady-state conditions, the voltage and current waveforms of a dc–dc converter can be found by use of two basic circuit analysis principles. The principle of *inductor volt-second balance* states that the average value, or dc component, of voltage applied across an ideal inductor winding must be zero. This principle also applies to

each winding of a transformer or other multiple winding magnetic devices. Its dual, the principle of *capacitor amp-second* or *charge balance*, states that the average current that flows through an ideal capacitor must be zero. Hence, to determine the voltages and currents of dc–dc converters operating in periodic steady state, one averages the inductor current and capacitor voltage waveforms over one switching period and equates the results to zero.

The equations are greatly simplified by use of a third artifice, the *small ripple approximation*. The inductor currents and capacitor voltages contain dc components, plus *switching ripple* at the switching frequency and its harmonics. In most wel-designed converters, the switching ripple is small in magnitude compared with the dc components. For inductor currents, a typical value of switching ripple at maximum load is 10% to 20% of the dc component of current. For an output capacitor voltage, the switching ripple is typically required to be much less than 1% of the dc output voltage. In both cases, the ripple magnitude is small compared with the dc component and can be ignored.

As an example, consider the boost converter of Fig. 5(a). A resistor R_L is included in series with the inductor, to model the resistance of the inductor winding. It is desired to determine simple expressions for the output voltage V, inductor current I_L, and efficiency η. Typical inductor voltage and capacitor current waveforms are sketched in Fig. 5(b).

With the switch in position 1, the inductor voltage is equal to $v_L(t) = V_g - i_L(t)R_L$. By use of the small ripple approximation, we can replace $i_L(t)$ with its dc component I_L and hence obtain $v_L(t) \approx V_g - I_L R_L$. Likewise, the capacitor current is equal to $i_C(t) = -v(t)/R$, which can be approximated as $i_C(t) \approx -V/R$.

When the switch is in position 2, the inductor is connected between the input and the output voltages. The inductor voltage can now be written $v_L(t) = V_g - i_L(t)R_L - v(t) \approx V_g - I_L R_L - V$. The capacitor current can be expressed as $i_C(t) = i_L(t) - v(t)/R \approx I_L - V/R$.

When the converter operates in steady state, the average value, or dc component, of the inductor voltage waveform $v_L(t)$ must be equal to zero. Upon equating the average value of the $v_L(t)$ waveform of Fig. 5(b) to zero, we obtain

$$0 = D(V_g - I_L R_L) + (1 - D)(V_g - I_L R_L - V) \tag{5}$$

Likewise, application of the principle of capacitor charge balance to the capacitor current waveform of Fig. 5(b) leads to

$$0 = D(-\frac{V}{R}) + (1 - D)(I - \frac{V}{R}) \tag{6}$$

Equations 5 and 6 can now be solved for the unknowns V and I_L. The result is

$$\frac{V}{V_g} = \frac{1}{(1 - D)} \frac{1}{(1 + \frac{R_L}{(1-D)^2 R})} \tag{7}$$

$$I_L = \frac{V_g}{(1 - D)^2 R} \frac{1}{(1 + \frac{R_L}{(1-D)^2 R})} \tag{8}$$

Equation 7 is plotted in Fig. 6 for several values of R_L/R. In the ideal case, when $R_L = 0$, the voltage conversion ratio *M(D)* is equal to one at $D = 0$ and tends to infinity as D approaches one. In the practical case where some small inductor resistance R_L is present, the output voltage tends to zero at $D = 1$. In addition, it can be observed that the inductor winding resistance R_L (and other loss elements as well) limits the maximum output voltage that the converter can produce. Obtaining a given large value of V/V_g requires that the winding resistance R_L be sufficiently small.

The converter efficiency can also be determined. For this boost converter example, the efficiency is equal to

$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V^2/R)}{(V_g I_L)} \tag{9}$$

Substitution of equation 7 and 8 into equation 9 leads to

$$\eta = \frac{1}{(1 + \frac{R_L}{(1-D)^2 R})} \tag{10}$$

This expression is plotted in Fig. 7, again for several values of R_L/R. It can be observed that to obtain high efficiency, the inductor winding resistance R_L should be much smaller than $(1 - D)^2 R$. This is much easier to accomplish at low duty cycles, where $(1 - D)$ is close to unity, that at high duty cycles where $(1 - D)$ approaches zero. Consequently, the efficiency is high at low duty cycles but decreases rapidly to zero near $1 = D$. This behavior is typical of converters having boost or buck-boost characteristics.

Semiconductor *conduction losses*, caused by the *on-resistances* or forward voltage drops of the semiconductor switching elements, can be modeled in a similar manner. Semiconductor *switching losses* arise during the switching transitions when the SPDT switch changes from position 1 to position 2 or vice versa and are described in more detail below.

TRANSFORMER ISOLATION

In many applications, it is desired to incorporate a transformer into the switching converter, to obtain dc isolation between the converter input and output. For example, in off-line power supply applications, isolation is usually required by regulatory agencies. This isolation could be obtained by simply connecting a 50 Hz or 60 Hz transformer at the power supply ac input terminals. However, as transformer size and weight vary inversely with frequency, incorporation of the transformer into the converter can make significant improvements: the transformer then operates at the converter switching frequency of tens or hundreds of kilohertz. The size of modern ferrite power transformers is minimized at operating frequencies ranging from several hundred kilohertz to roughly one Megahertz. These high frequencies lead to dramatic reductions in transformer size.

When a large step-up or step-down conversion ratio is required, the use of a transformer can allow better converter optimization. By proper choice of the transformer turns ratio, the voltage or current stresses imposed on the transistors and diodes can be minimized, which leads to improved efficiency and lower cost.

Multiple dc outputs can also be obtained in an inexpensive manner, by adding multiple secondary windings and converter secondary-side circuits. The secondary turns ra-

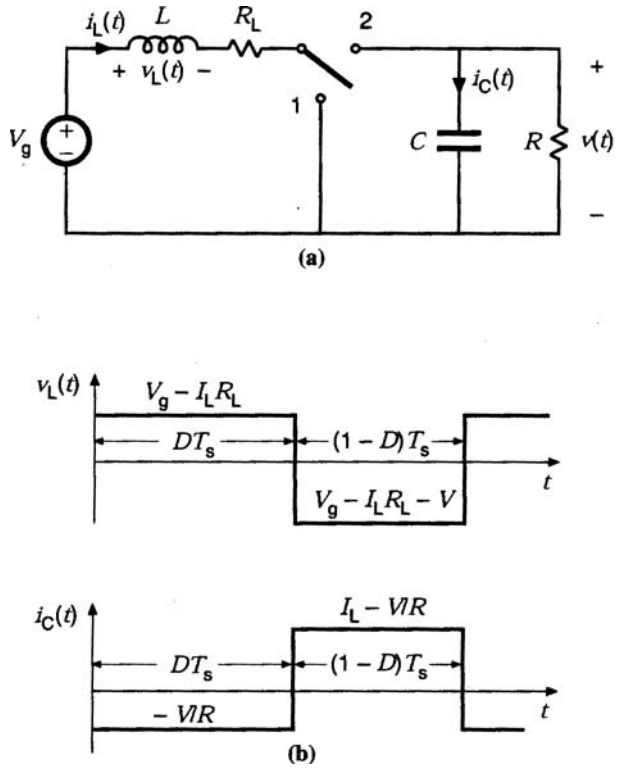


Figure 5. A nonideal boost converter: (a) schematic and (b) inductor voltage and capacitor current waveforms.

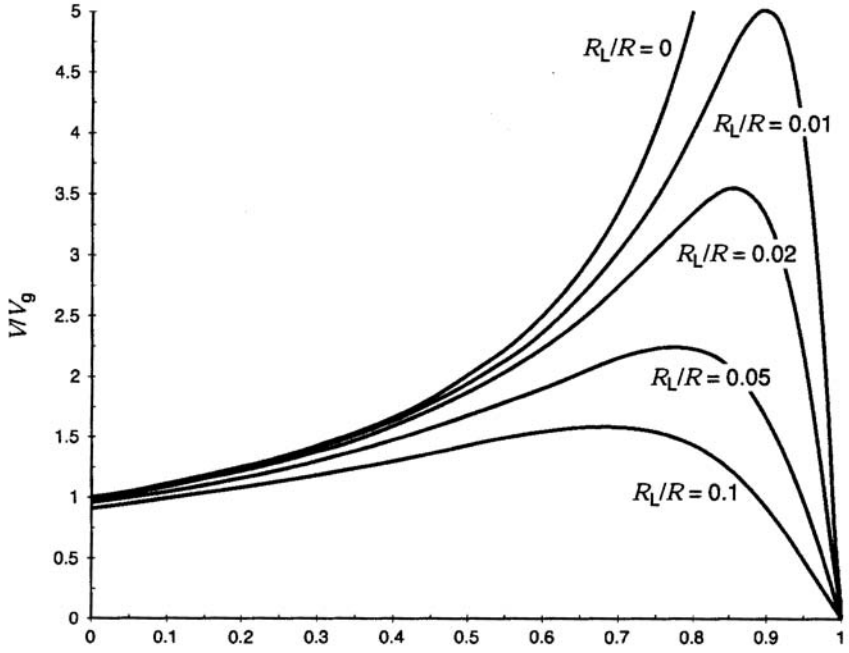


Figure 6. Output voltage vs. duty cycle, for the nonideal boost converter of Fig. 5.

tios are chosen to obtain the desired output voltages. Usually, only one output voltage can be regulated, via control of the converter duty cycle, so wider tolerances must be allowed for the auxiliary output voltages. *Cross regulation* is a measure of the variation in an auxiliary output voltage, given that the main output voltage is regulated perfectly.

The basic operation of transformers in most power converters can be understood by replacing the transformer

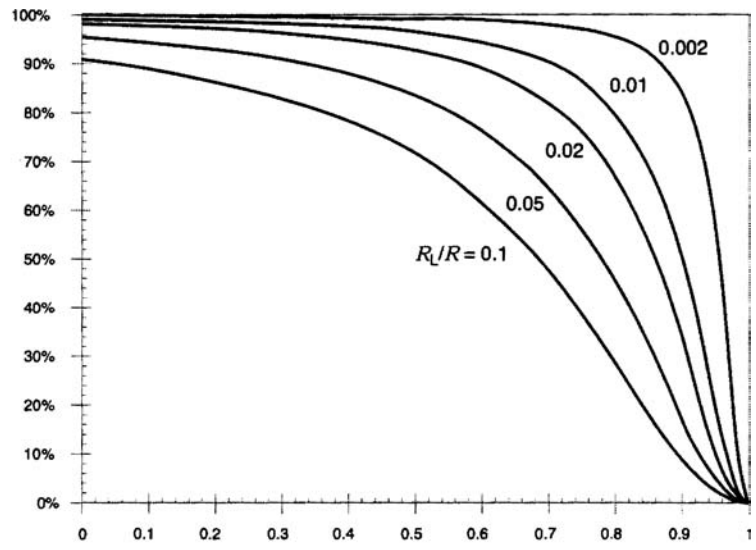
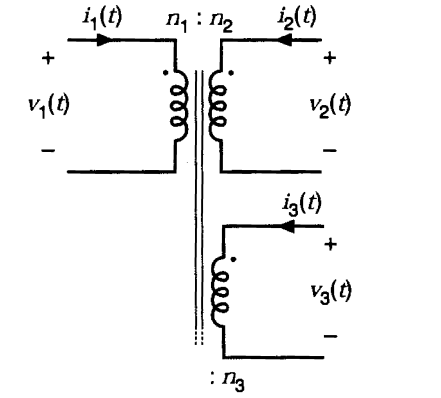
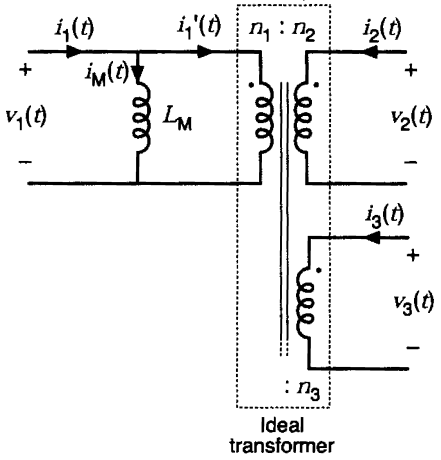


Figure 7. Efficiency vs. duty cycle, for the nonideal boost converter of Fig. 5.



(a)



(b)

Figure 8. Modeling a physical transformer such that its basic operation within an isolated dc–dc converter can be understood: (a) transformer schematic symbol and (b) equivalent circuit model that includes magnetizing inductance L_M and an ideal transformer.

with the simplified model illustrated in Fig. 8(b). The model neglects losses and imperfect coupling between windings; such phenomena are usually considered to be converter nonidealities. The model consists of an ideal transformer plus a shunt inductor known as the magnetizing inductance L_M. This inductor models the magnetization of the physical transformer core, and hence, it must obey all of the usual rules for inductors. In particular, volt-second balance must be maintained on the magnetizing inductance. Furthermore, as the voltages of all windings of the ideal transformer are proportional, volt-second balance must be maintained for each winding. Failure to achieve volt-second balance leads to transformer saturation and, usually, destruction of the converter. The means by which transformer volt-second balance is achieved is known as the *transformer reset* mechanism.

There are several ways of incorporating transformer isolation into any dc–dc converter. The full-bridge, half-bridge, forward, and push-pull converters are commonly used isolated versions of the buck converter. Similar isolated variants of the boost converter are known. The flyback converter is an isolated version of the buck-boost converter. Isolated variants of the SEPIC and Cuk converter are also known. The full-bridge, forward, and flyback converters are briefly described in this section.

Full-Bridge Buck-Derived Converter

The full-bridge transformer-isolated buck converter is sketched in Fig. 9. Typical waveforms are illustrated in Fig. 10.

The transformer primary winding is driven symmetrically, such that the net volt-seconds applied over two switching periods is equal to zero. During the first switching period, transistors Q_1, and Q_4 conduct for time DT_s. The volt-seconds applied to the primary winding during this switching period are equal to $V_g DT_s$. During the following switching period, transistors Q_2 and Q_3 conduct for time DT_s, thereby applying $-V_g DT_s$ volt-seconds to the transformer primary winding. Over two switching periods, the net applied volt-seconds is equal to zero.

In practice, small imbalances exist such as the small differences in the transistor forward voltage drops or transistor switching times, so that the average primary winding voltage is small but nonzero. This nonzero dc voltage can lead to transformer saturation and destruction of the converter. Transformer saturation under steady state conditions can be avoided by placing a capacitor in series with the transformer primary. Imbalances then induce a dc voltage component across the capacitor, rather than across the transformer primary. Another solution is the use of current-mode control; the series capacitor is then omitted.

By application of the principle of volt-second balance to the output filter inductor voltage, the dc load voltage can be shown to be

$$V = nDV_g \tag{11}$$

So, as in the buck converter, the output voltage can be controlled by adjustment of the transistor duty cycle D. An additional increase or decrease of the voltage V can be obtained via the physical transformer turns ratio n.

The full bridge configuration is typically used in switching power supplies at power levels of several hundred watts or greater. At lower power levels, approaches such as the forward converter are preferred because of their lower parts count. Four transistors and their associated drive circuits are required. The utilization of the transformer is good, which leads to small transformer size. The transformer operating frequency is one half of the transistor switching frequency.

Forward Converter

The forward converter is illustrated in Fig. 11. This transformer-isolated converter is also based on the buck converter. It requires a single transistor and therefore finds application at power levels lower than those encountered in the full bridge circuit. The maximum transistor duty cycle is limited in value; for the common choice $n_1 = n_2$, the duty cycle is limited to the range $D < 0.5$.

The transformer is reset while transistor Q_1 is in the off state. When the transistor conducts, the input voltage V_g is applied across the transformer primary winding, which causes the transformer magnetizing current to increase. When transistor Q_1, turns off, the transformer magnetizing current forward-biases diode D_1 and hence, voltage $-V_g$ is applied to the second winding. This negative voltage causes the magnetizing current to decrease. When the magnetizing current reaches zero, diode D_{1x} turns off. Volt-second balance is maintained on the transformer windings provided that the magnetizing current reaches zero before the end of the switching period. It can be shown that this occurs when

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}} \tag{12}$$

For the common choice $n_2 = n_1$ this expression reduces to

$$D \leq \frac{1}{2} \tag{13}$$

Hence, the maximum duty cycle is limited. If this limit is violated, then the transistor off time is insufficient to reset the transformer. There will then be a net increase in the transformer magnetizing current over each switching period, and the transformer will eventually saturate.

The converter output voltage can be found by application of the principle of inductor volt-second balance to the output filter inductor L. The result is

$$V = \frac{n_3}{n_1} DV_g \tag{14}$$

This expression is subject to the constraint given in equation 12.

A two-transistor version of the forward converter is illustrated in Fig. 12. Transistors Q_1 and Q_2 are controlled by the same gate drive signal, such that they conduct simultaneously. After the transistors turn off, the transformer magnetizing current forward-biases diodes D_1 and D_2. This applies voltage $-V_g$ across the primary winding, thereby resetting the transformer. The duty cycle is again limited to $D < 0.5$ This converter has the advantage that the transistor peak blocking voltage is limited to V_g and is clamped

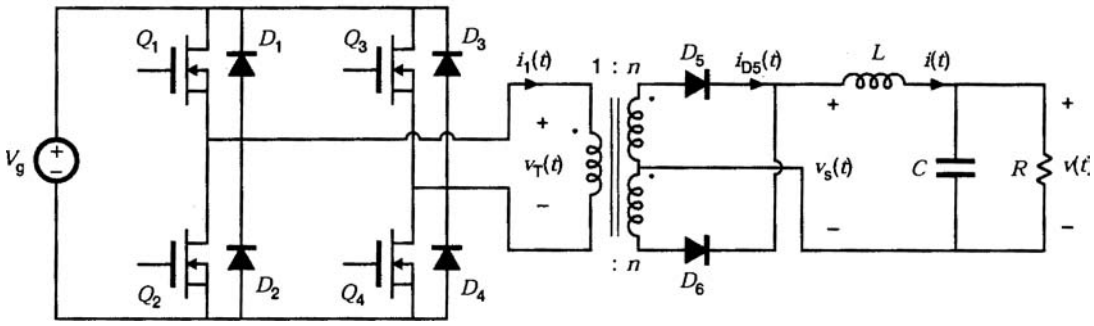


Figure 9. The full bridge transformer-isolated buck converter.

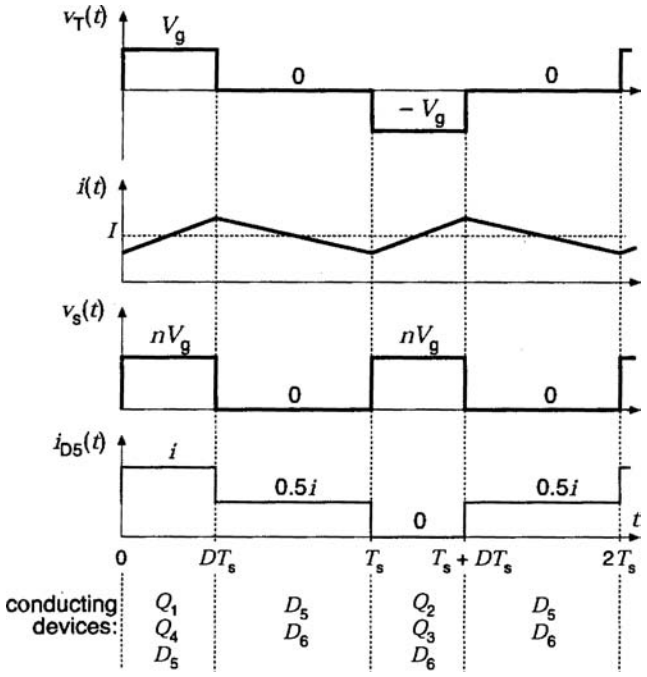


Figure 10. Waveforms of the full bridge circuit of Fig. 9.

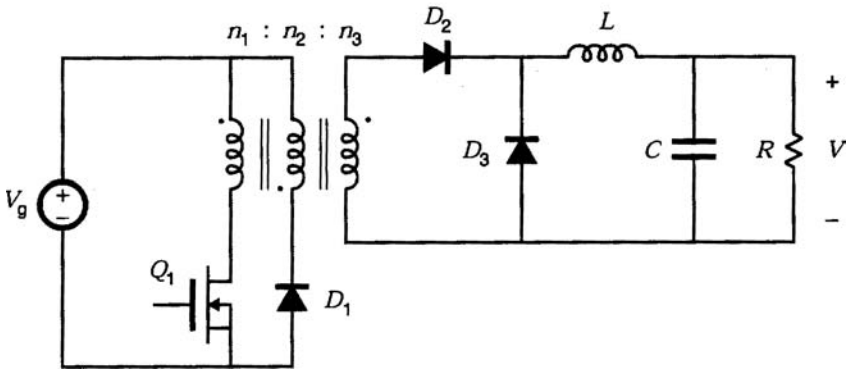


Figure 11. The forward converter, a single-transistor isolated buck converter.

by diodes D_1 and D_2. This circuit is quite popular in power supplies having 240 Vac inputs.

Flyback Converter

The flyback converter of Fig. 13 is based on the buck-boost converter. Although the two-winding magnetic device is represented using the same symbol as the transformer, a more descriptive name is "two-winding inductor." This de-

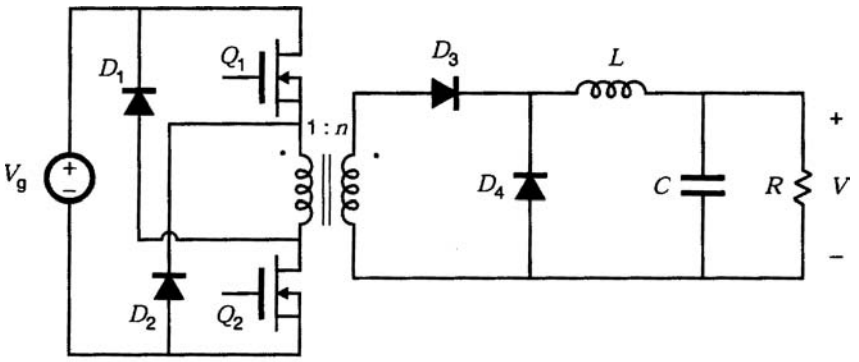


Figure 12. A two-transistor version of the forward converter.

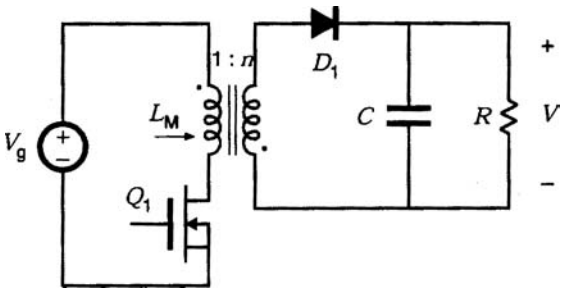


Figure 13. The flyback converter, a single-transistor isolated buck-boost converter.

vice is sometimes also called a "flyback transformer." Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer. Rather, the flyback transformer magnetizing inductance assumes the role of the inductor of the buck-boost converter. The magnetizing current is switched between the primary and the secondary windings.

When transistor Q_1 conducts, diode D_1 is reverse-biased. The primary winding then functions as an inductor, connected to the input source V_g. Energy is stored in the magnetic field of the flyback transformer. When transistor Q_1 turns off, the current ceases to flow in the primary winding. The magnetizing current, referred to the secondary winding, now forward-biases diode D_1. Energy stored in the magnetic field of the flyback transformer is then transferred to the dc load.

Application of the principle of inductor volt-second balance to the transformer primary winding leads to the following solution for the conversion ratio of the flyback converter:

$$M(D) = \frac{V}{V_g} = n\frac{D}{(1-D)} \tag{15}$$

Thus, the conversion ratio of the flyback converter is similar to that of the buck-boost converter but with an added factor of n.

The flyback converter has traditionally been used in the high-voltage power supplies of televisions and computer monitors. It also finds widespread application in switching power supplies with power levels of tens of watts. This converter has the advantage of a very low parts count. Multiple outputs can be obtained using a minimum number of added elements: Each auxiliary output requires only an additional winding, diode, and capacitor. However, in comparison with buck-derived transformer-isolated converters such as the full bridge and forward circuits, the flyback converter has the disadvantage of poor cross regulation.

SWITCH IMPLEMENTATION

The switch network realization of Fig. 3 employs *single-quadrant* switches. Each semiconductor element can conduct current of only one polarity in the on state and block voltage of one polarity in the off state, which implies that, for proper functioning of the switch network, the source voltage, load voltage, and inductor current must all be positive. Consequently, the switch network allows the instantaneous power to flow in one direction only: from the source V_g toward the load.

Bidirectional (regenerative) power flow can be obtained with a current-bidirectional *two-quadrant* realization of the switch network. An example is illustrated in Fig. 14, in which a dc–dc converter interfaces batteries to the main dc power bus of a spacecraft. The anti-parallel-connected transistors and diodes form current-bidirectional switches. Transistor Q_2 is driven with the complement of the Q_1 drive signal, such that Q_2 is off when Q_1 is on, and vice versa. To charge the battery, the inductor current $i_L(t)$ is positive and flows through transistor Q_1 and diode D_2. To discharge the battery, the current $i_L(t)$ reverses polarity and flows through transistor Q_2 and diode D_1. In both cases, the battery voltage is less than the main dc bus voltage. The magnitude and polarity of the battery current can be controlled via adjustment of the duty cycle D.

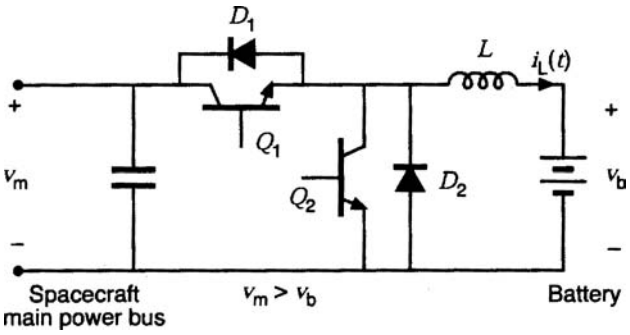


Figure 14. A buck converter with two-quadrant switches and bidirectional power flow. Spacecraft battery charger/discharger example.

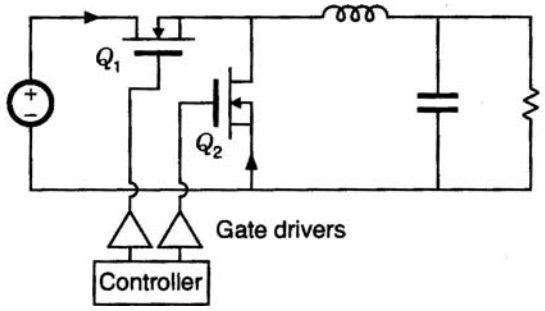


Figure 15. Buck converter employing synchronous rectifier Q_2.

Synchronous rectifiers are commonly employed in dc–dc converters that supply a low voltage such as the one or two volts required by computer processors. In such applications, the approximately fixed diode forward voltage drop leads to considerable loss. The efficiency can be improved by replacing the diode with a MOSFET Q_2 having low on-resistance, as illustrated in Fig. 15. The forward voltage drop can then be made as small as desired if a large MOSFET having sufficiently small on resistance is employed. The synchronous rectifier exploits the ability of the power MOSFET to conduct reverse current; the gate of transistor Q_2 should be driven so that Q_2 turns on when the diode would have turned on.

Switching loss imposes an upper limit on the switching frequencies of practical converters. During the switching transitions, the transistor voltage and current are simultaneously large. In consequence, the transistor experiences high instantaneous power loss, which can lead to significant average power loss, even though the switching transitions are short in duration. Switching loss causes the converter efficiency to decrease as the switching frequency is increased.

Several mechanisms lead to switching loss. Significant energy can be lost during the slow switching times of minority-carrier semiconductor devices such as BJTs, IGBTs, and thyristors. The *p-n* diode reverse recovery process induces substantial additional energy loss in the transistor during the transistor turn-on transition. The energy stored in the semiconductor output capacitances is dissipated during the transistor turn-on transition. Energy stored in transformer leakage inductances and other stray inductances is usually dissipated by the transistor during the turn-off transition. The total switching loss is equal to the sum of the energy losses that arise via these mechanisms, multiplied by the switching frequency. Switching loss can be partially mitigated through the use of a *resonant* or *soft-switching* converter.

DISCONTINUOUS CONDUCTION MODE

When the switching ripple in an inductor current or capacitor voltage is large enough to cause the polarity of the applied switch voltage or current to reverse, then converters that employ single-quadrant switches enter the *discontinuous conduction mode* (DCM), which typically occurs at light load (small load current) in dc–dc converters that employ diodes rather than synchronous rectifiers. In some cases, dc–dc converters are purposely designed to operate in DCM at all load currents.

The properties of dc–dc converters change radically when DCM is entered. The conversion ratio *M(D)* becomes load-dependent. The output voltage is increased, and the small-signal converter dynamics are altered substantially. Control of the output voltage may be lost when the load is removed; indeed, the output voltages of boost and buck-boost converters tend to very large values when the load is disconnected.

Figure 16 illustrates operation of a buck converter in DCM. The inductor current ripple Δi_L is greater than the dc component I, and hence, the diode becomes reverse-biased at time $t = (D_1 + D_2)T_s$. The remainder of the switching period constitutes a third subinterval in which both the transistor and the diode are off. It can be shown that the condition for operation in DCM can be expressed as

$$K < K_{crit}(D) \tag{16}$$

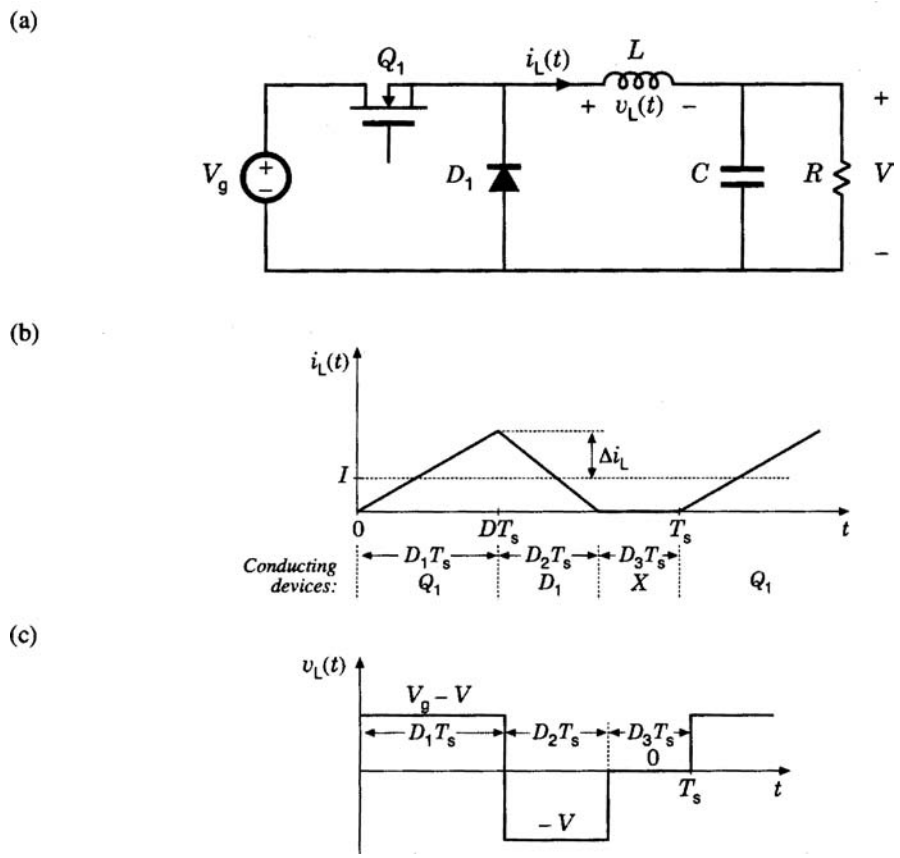


Figure 16. Operation of the buck converter in the discontinuous conduction mode: (a) schematic, (b) inductor current waveform, and (c) inductor voltage waveform.

where $K = 2L/RT_s$ and $K_{crit}(D) = (1 - D)$ for the buck converter. In general, the DCM boundary can be expressed with an equation in this form; the expressions for $K_{crit}(D)$ for basic converters are listed in Table 1. When equation 16 is not satisfied, then the converter operates in the *continuous conduction mode* (CCM) as described by Fig. 1 and equation 4.

The dc output voltages of converters operating in DCM can be found by application of inductor volt-second balance and capacitor charge balance, as described previously, taking care to account for the large inductor current ripple. In steady state, the dc component of inductor voltage must be zero. For the buck converter waveform $v_L(t)$ of Fig. 16(c), this leads to

$$0 = D_1(V_g - V) + D_2(-V) + D_3(0) \tag{17}$$

In addition, the dc component of capacitor current must be zero in steady state; for the buck converter, this implies that the dc load current is equal to the dc component of the inductor current:

$$\frac{V}{R} = \frac{D_1T_s}{2L}(D_1 + D_2)(V_g - V) \tag{18}$$

Equations 17 and 18 contain two unknowns: V and D_2. Elimination of D_2 and solution for the conversion ratio yields

$$M(D) = \frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + 4\frac{K}{D_1^2}}} \tag{19}$$

with $D = D_1$. Table 1 summarizes the steady-state characteristics for the converters of Fig. 4. Note that, for the Cuk and SEPIC topologies, the parameter K depends on the parallel combination of the two inductor values $L_1||L_2 = L_1L_2/(L_1 + L_2)$.

CURRENT-MODE CONTROL

In the voltage-mode control approach of Fig. 3, the pulse-width modulator drives the transistor at a duty cycle that is a direct function of the control signal. A popular alternative approach is *current-mode control*, in which a mixed-signal control circuit that causes the switch current to follow a control signal replaces the pulse-width modulator (6–9). Both peak-current and average-current controllers are available commercially.

The principal advantage of current-mode control is its simpler dynamics. Effectively, the controller employs current feedback information; this significantly reduces the influence of inductor dynamics on the converter small-signal transfer functions and transient response. Although current-mode control requires sensing of the switch or in-

Table 1. Continuous and discontinuous conduction mode results for several basic converters

Converter	CCM *M(D)*	DCM *M(D)*	K	$K_{crit}(D)$
Buck	D	$\frac{2}{1+\sqrt{1+4K/D^2}}$	$\frac{2L}{RT_s}$	$1-D$
Boost	$\frac{1}{(1-D)}$	$\frac{1+\sqrt{1+4D^2/K}}{2}$	$\frac{2L}{RT_s}$	$D(1-D)^2$
Buck-boost	$-\frac{D}{(1-D)}$	$-\frac{D}{\sqrt{K}}$	$\frac{2L}{RT_s}$	$(1-D)^2$
Cuk	$-\frac{D}{(1-D)}$	$-\frac{D}{\sqrt{K}}$	$\frac{2L_1 \| L_2}{RT_s}$	$(1-D)^2$
SEPIC	$\frac{D}{(1-D)}$	$\frac{D}{\sqrt{K}}$	$\frac{2L_1 \| L_2}{RT_s}$	$(1-D)^2$

Table 2. Canonical model parameters for several basic converts

Converter	*M(D)*	L_e	*e(s)*	*j(s)*
Buck	D	L	$\frac{V}{D^2}$	$\frac{V}{R}$
Boost	$\frac{1}{(1-D)}$	$\frac{L}{(1-D)^2}$	$V\left(1-\frac{sL}{(1-D)^2R}\right)$	$\frac{V}{(1-D)^2R}$
Buck-Boost	$-\frac{D}{(1-D)}$	$\frac{L}{(1-D)^2}$	$-\frac{V}{D^2}\left(1-\frac{sDL}{(1-D)^2R}\right)$	$-\frac{V}{(1-D)^2R}$

Table 3. Small-signal transfer function parameters for basic dc–dc converters

Converter	G_{g0}	G_{d0}	ω_0	Q	ω_z
Buck	D	$\frac{V}{D}$	$\frac{1}{\sqrt{LC}}$	$R\sqrt{\frac{C}{L}}$	∞
Boost	$\frac{1}{(1-D)}$	$\frac{V}{(1-D)}$	$\frac{(1-D)}{\sqrt{LC}}$	$(1-D)R\sqrt{\frac{C}{L}}$	$\frac{(1-D)^2R}{L}$
Buck-Boost	$-\frac{D}{(1-D)}$	$\frac{V}{D(1-D)^2}$	$\frac{(1-D)}{\sqrt{LC}}$	$(1-D)R\sqrt{\frac{C}{L}}$	$\frac{(1-D)^2R}{DL}$

ductor current, such current sensing is normally present anyway, in conjunction with overcurrent protection circuitry. Current-mode control can also reduce or eliminate transformer saturation problems in isolated dc–dc converters such as the full bridge or push–pull topologies.

Figure 17 illustrates elements of a current-mode controlled buck converter. A latch is set by a clock signal at the beginning of each switching period, turning on transistor Q_1. This applies positive voltage across the inductor, which causes the inductor current and the transistor current to increase. A sensor circuit produces a signal $i_s(t)R_f$ that is proportional to the switch current $i_s(t)$. When this signal is equal to a control signal $v_c(t)$, the latch is reset and the current-mode controller turns off the transistor switch. In consequence, the peak transistor current, and the peak inductor current, follow the control signal $v_c(t)$. The control signal $v_c(t)$ is typically generated by an output voltage controller as illustrated in Fig. 17. Additionally, an "artificial ramp" may be required for stabilization of the current-mode controller, particularly at operating points that require a duty cycle greater than 0.5.

DC-DC CONVERTER MODELING

To design the control system of a converter, it is necessary to model the converter dynamic behavior. In particular, it is of interest to determine how variations in the power input voltage $v_g(t)$, the load current, and the duty cycle *d(t)* affect the output voltage. Unfortunately, understanding of converter dynamic behavior is hampered by the nonlinear time-varying nature of the switching and pulse-width modulation process. These difficulties can be overcome through the use of waveform averaging and small-signal modeling techniques (10–15). A well-known converter modeling technique known as *state-space averaging* is briefly described here. An equivalent approach known as *averaged switch modeling* is also described; this approach is well suited to computer simulation. Results for several basic converters are listed in tabular form.

State-Space-Averaging

The state-space averaging technique generates the low-frequency small-signal ac equations of PWM dc–dc con-

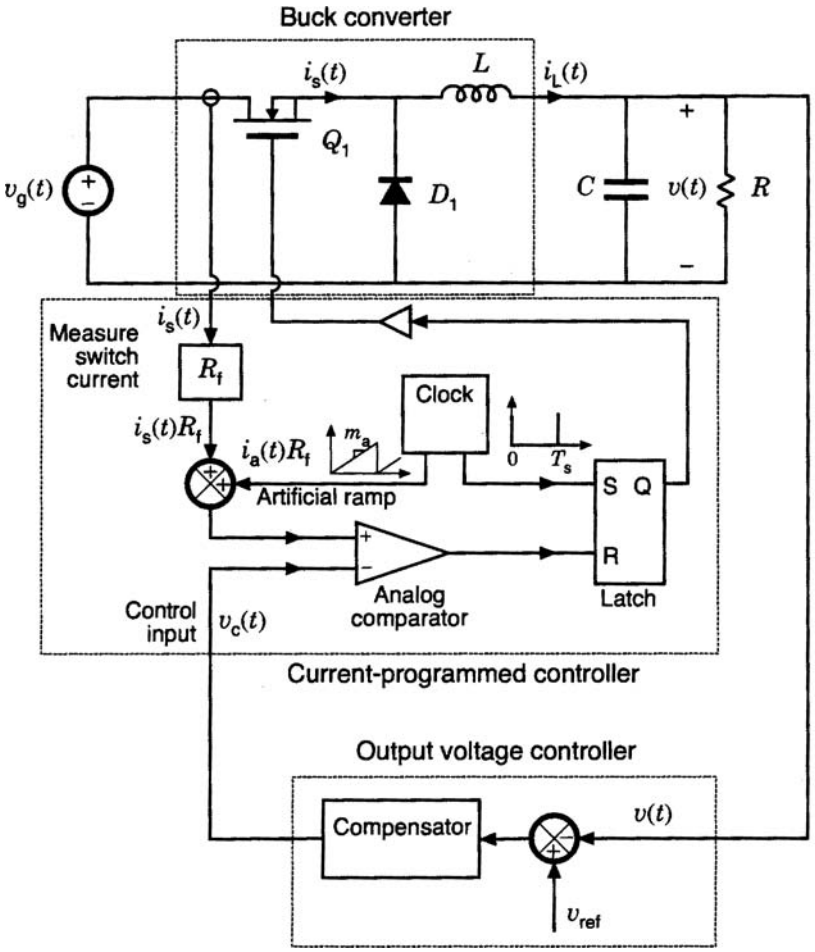


Figure 17. Elements of a current-mode controlled buck converter.

verters. Converter transfer functions and equivalent circuit models can be obtained.

The converter contains independent state variables such as inductor currents and capacitor voltages, which form the state vector $\mathbf{x}(t)$, and the converter is driven by independent sources that form the input vector $\mathbf{u}(t)$. The output vector $\mathbf{y}(t)$ contains dependent signals of interest. During the first subinterval, when the switches are in position 1 for time dT_s, the converter reduces to a linear circuit whose equations can be written in the following state-space form:

$$\begin{aligned} \frac{d\mathbf{x}(t)}{dt} &= \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}_1\mathbf{x}(t) + \mathbf{E}_1\mathbf{u}(t) \end{aligned} \tag{20}$$

The matrices $\mathbf{A}_1$, $\mathbf{B}_1$, $\mathbf{C}_1$, and $\mathbf{E}_1$, describe the network connections during the first subinterval. The duty cycle $d(t)$ may now be a time-varying quantity. During the second subinterval, the converter reduces to another linear circuit, whose state space equations are

$$\begin{aligned} \frac{d\mathbf{x}(t)}{dt} &= \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}_2\mathbf{x}(t) + \mathbf{E}_2\mathbf{u}(t) \end{aligned} \tag{21}$$

The matrices $\mathbf{A}_2$, $\mathbf{B}_2$, $\mathbf{C}_2$, and $\mathbf{E}_2$ describe the network connections during the second subinterval, of length $(1 - d)T_s$.

It is assumed that the natural frequencies of the converter network are much smaller than the switching frequency. This assumption coincides with the small ripple approximation and is usually satisfied in well-designed converters. It allows the high-frequency switching harmonics to be removed by an averaging process. In addition, the waveforms are linearized about a dc quiescent operating point. The converter waveforms are expressed as quiescent values plus small ac variations, as follows:

$$\begin{aligned} \mathbf{x}(t) &= \mathbf{X} + \hat{\mathbf{x}}(t) \\ \mathbf{u}(t) &= \mathbf{U} + \hat{\mathbf{u}}(t) \\ \mathbf{y}(t) &= \mathbf{Y} + \hat{\mathbf{y}}(t) \\ d(t) &= D + \hat{d}(t) \end{aligned} \tag{22}$$

This small-signal linearization is justified provided that

$$\begin{aligned} \|\mathbf{X}\| &\gg \|\hat{\mathbf{x}}(t)\| \\ \|\mathbf{U}\| &\gg \|\hat{\mathbf{u}}(t)\| \\ \|\mathbf{Y}\| &\gg \|\hat{\mathbf{y}}(t)\| \\ D &\gg |\hat{d}(t)| \end{aligned} \tag{23}$$

where $\|\mathbf{x}\|$ represents the norm of vector $\mathbf{x}$.

The state-space averaged model that describes the quiescent converter waveforms is

$$\begin{aligned} 0 &= \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} &= \mathbf{CX} + \mathbf{EU} \end{aligned} \tag{24}$$

where the averaged state matrices are

$$\begin{aligned} \mathbf{A} &= D\mathbf{A}_1 + (1-D)\mathbf{A}_2 \\ \mathbf{B} &= D\mathbf{B}_1 + (1-D)\mathbf{B}_2 \\ \mathbf{C} &= D\mathbf{C}_1 + (1-D)\mathbf{C}_2 \\ \mathbf{E} &= D\mathbf{E}_1 + (1-D)\mathbf{E}_2 \end{aligned} \tag{25}$$

The steady-state solution of the converter is

$$\begin{aligned} \mathbf{X} &= -\mathbf{A}^{-1}\mathbf{B}\mathbf{U} \\ \mathbf{Y} &= (-\mathbf{C}\mathbf{A}^{-1}\mathbf{B} + \mathbf{E})\mathbf{U} \end{aligned} \tag{26}$$

The state equations of the small-signal ac model are

$$\begin{aligned} \frac{d\hat{\mathbf{x}}(t)}{dt} &= \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\hat{d}(t) \\ \hat{\mathbf{y}}(t) &= \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{E}_1 - \mathbf{E}_2)\mathbf{U}]\hat{d}(t) \end{aligned} \tag{27}$$

These equations describe how small ac variations in the input vector and duty cycle excite variations in the state and output vectors.

Simulation via Averaged Switch Modeling

In the averaged switch modeling approach, a switch network is defined that contains all switching elements of the converter. The low-frequency components of the terminal waveforms of the switch network are found, with the high-frequency switching harmonics discarded via a process known as *averaging*. The result is a time-invariant network that models the dc and low-frequency ac components of the converter waveforms. The converter small-signal transfer functions can be found using this model. In addition, the model allows efficient simulation of the converter dynamics using a conventional program such as SPICE (3, 16–18).

Consider the buck-boost converter of Fig. 18. The transistor and diode switching elements are grouped into a two-port switch network, and the remainder of the converter circuit is linear and time-invariant. For this example, the terminal waveforms of the switch network are taken to be the MOSFET drain-to-source voltage $v_1(t)$, the MOSFET drain current $i_1(t)$, the diode anode-to-cathode voltage $v_2(t)$, and the diode cathode current $i_2(t)$. These terminal waveforms are sketched in Fig. 19, for operation in the continuous conduction mode.

Next, we assume that the natural time constants of the converter circuit are much longer than the switching period T_s, so that the converter effectively low-pass filters the switching harmonics. When this assumption is satisfied, then one may average the waveforms over a period that is short compared with the system natural time constants without significantly altering the system response (12). In particular, averaging over the switching period T_s removes the switching harmonics while preserving the underlying low-frequency components of the converter waveforms. This step removes the small but mathematically complex switching harmonics, which leads to a relatively simple and tractable dc and ac converter model. In practice, we need only average the waveforms of the switch network, because switching harmonics are not generated in the remainder of the converter.

An appropriate definition of the average $\langle v(t)\rangle$ of a waveform $v(t)$ is

$$\langle v(t)\rangle = \frac{1}{T_s}\int_t^{t+T_s} v(\tau)d\tau \tag{28}$$

For the buck-boost waveforms of Fig. 19, the averages are given approximately by

$$\begin{aligned} \langle v_1(t)\rangle &= (1-d(t))(\langle v_g(t)\rangle + \langle v(t)\rangle) \\ \langle v_2(t)\rangle &= d(t)(\langle v_g(t)\rangle + \langle v(t)\rangle) \\ \langle i_1(t)\rangle &= d(t)\langle i_L(t)\rangle \\ \langle i_2(t)\rangle &= (1-d(t))\langle i_L(t)\rangle \end{aligned} \tag{29}$$

Division of these equations leads to

$$\begin{aligned} \langle v_1(t)\rangle &= \frac{1-d(t)}{d(t)}\langle v_2(t)\rangle \\ \langle i_2(t)\rangle &= \frac{1-d(t)}{d(t)}\langle i_1(t)\rangle \end{aligned} \tag{30}$$

This constitutes the basic set of equations that relates the low-frequency components of the terminal waveforms of the switch network.

Equation 30 suggests that the switch network could be modeled by one of the equivalent circuits of Fig. 20. Figure 20(b) illustrates replacement of the transistor and diode with dependent voltage and current sources according to equation 30; this model is useful for SPICE simulation. Equivalently, an ideal *dc transformer*, denoted by a transformer symbol having a solid horizontal line, can replace the dependent sources as illustrated in Fig. 20(c). The dc transformer model has an effective turns ratio equal to $(1-d)/d$. It obeys all of the usual properties of transformers, except that it can pass dc voltages and currents. Although conventional magnetic-core transformers cannot pass dc voltages, we are nonetheless free to define an ideal dc transformer symbol; use of this symbol in modeling dc–dc converter properties is justified because it correctly predicts how the switch network converts dc and low-frequency ac voltages and currents, ideally with 100% efficiency.

The transformer model of Fig. 20(c) is a time-varying element because its effective turns ratio depends on the control input *d(t)*. For analysis of converter transfer functions, it is necessary to linearize this element in a manner similar to that employed in equations 22 and 23. The result is the small-signal switch model of Fig. 20(d). In any of the basic converters, such as those of Fig. 4, the transistor and diode can be replaced by the model of Fig. 20(d), which results in a small-signal equivalent circuit that predicts the small-signal transfer functions of the converter.

The averaged switch model of Fig. 20(b) provides a simple and very efficient means for converter simulation in conventional computer programs such as SPICE. Analyses of the dc operating points, transients, and frequency responses can be easily performed while avoiding the need to calculate the details of the switching transitions. In addition, the model of Fig. 20(b) can be generalized to account for operation in DCM by manipulation of the *M(D)* expressions listed in Table 1, into the form of equation 30. The

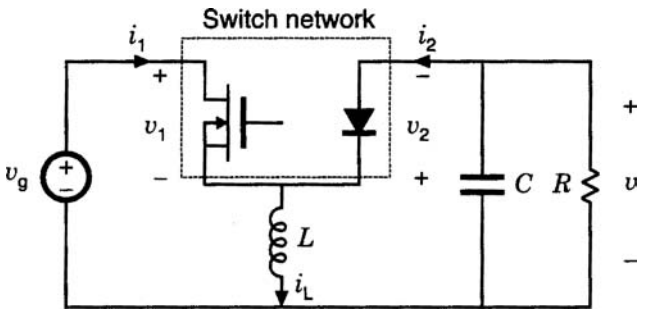


Figure 18. Averaged switch modeling of a buck-boost converter

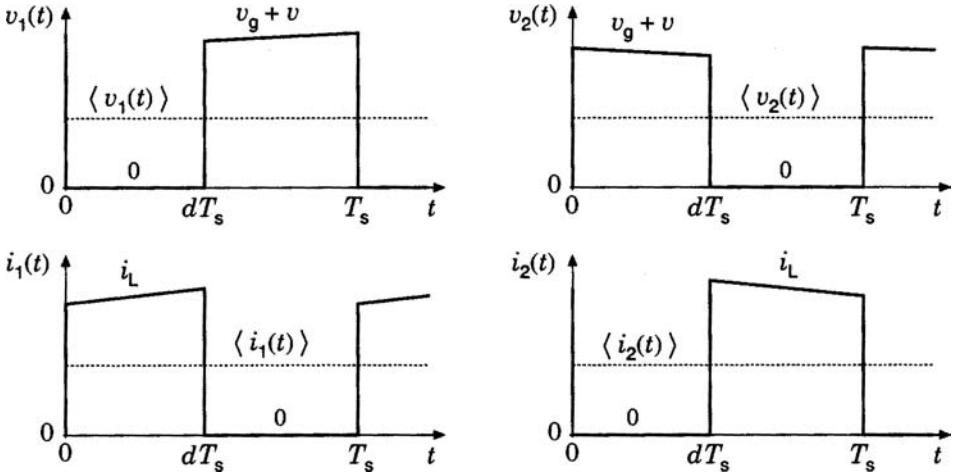


Figure 19. Waveforms of the switch network of Fig. 18.

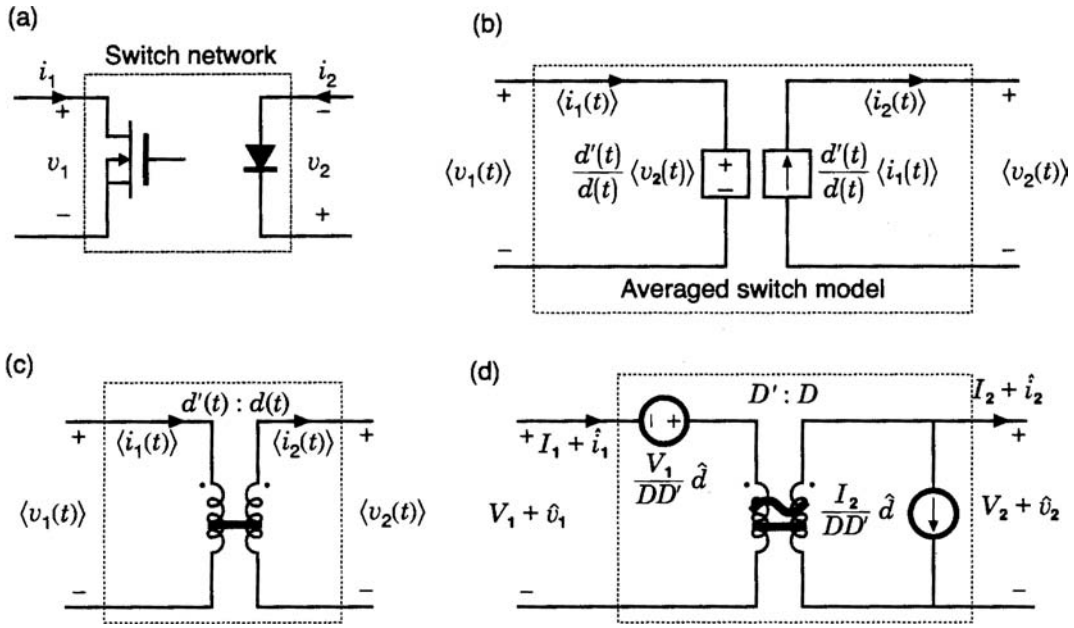


Figure 20. Evolution of the averaged switch model in CCM: (a) original switch network, (b) averaging the waveforms, (c) large-signal transformer model, and (d) small-signal ac model.

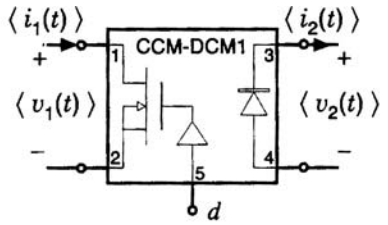
result is

$$\begin{aligned} \langle v_1(t) \rangle &= \frac{1-u(t)}{u(t)} \langle v_2(t) \rangle \\ \langle i_2(t) \rangle &= \frac{1-u(t)}{u(t)} \langle i_1(t) \rangle \end{aligned} \tag{31}$$

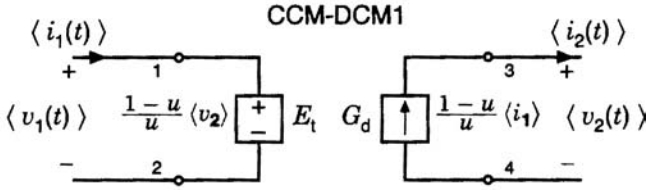
where u is the effective switch duty cycle given by

$$u = \left\{ \begin{array}{ll} d, & \text{CCM} \\ \dfrac{d^2}{d^2 + 2L\, f_s \dfrac{\langle i_1 \rangle}{\langle v_2 \rangle}}, & \text{DCM} \end{array} \right\} \tag{32}$$

(a)



(b)



(c)

```
*****************************************************************
* MODEL: CCM-DCM1
*****************************************************************
* Pararmeters:
*   L = inductor value
*   fs = switching frequency
*****************************************************************
* Nodes:
*   1-transistor positive terminal (Drain for n-ch MOSFET)
*   2-transistor negative terminal (Source for n-ch MOSFET)
*   3-diode cathode
*   4-diode anode
*   5-duty cycle control input
*****************************************************************
.subckt CCM-DCM1 1 2 3 4 5  params: L=100u fs=1E5
Et 1 2 value={(1-v(u))*v(3,4)/v(u)}
Gd 4 3 value={(1-v(u))*i(Et)/v(u)}
Ga 0 a value={MAX(i(Et),0)}
Va a b
Ra b 0 1k
Eu u 0 table {MAX(v(5),
+ v(5)*v(5)/(v(5)*v(5)+2*L*fs*i(Va)/v(3,4)))} (0 0) (1 1)
.ends
*****************************************************************
```

Figure 21. Averaged switch model for converter simulation: (a) schematic entry symbol, (b) electrical circuit, and (c) PSPICE code.

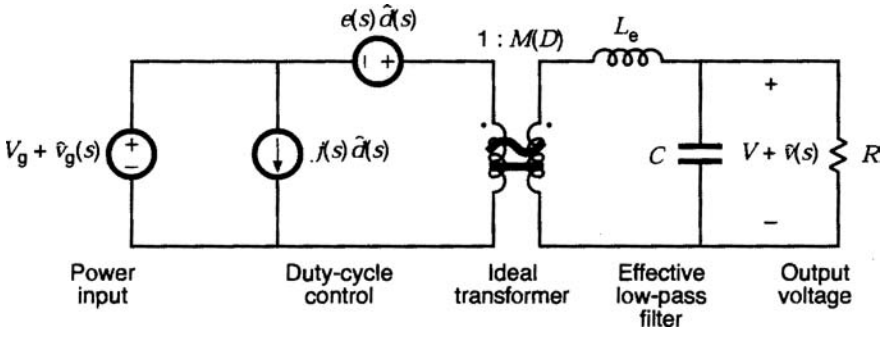


Figure 22. The canonical model: a small-signal equivalent circuit that models dc–dc converter dynamics and transfer functions.

The equations for $u(d)$ intersect at the CCM–DCM mode boundary, and operation in DCM causes the output voltage to rise. Hence, we can simply select the larger of the two expressions for u in equation (32).

An averaged switch model that implements the above equations in PSPICE is illustrated in Fig. 21. The model terminals 1-2 and 3-4 replace the transistor and diode, respectively. Terminal 5 is the duty cycle input; the duty cycle d is represented by a voltage in the range [0,1]. The model automatically switches between CCM and DCM, and can be applied to dc, ac, or transient simulation of single-transistor PWM converters.

Canonical Model

Equivalent circuit models of dc–dc converters can be constructed using the state-space averaged equations 24 and 27 or by manipulation or the averaged switch models above, As all PWM dc–dc converters perform similar basic functions, one finds that the equivalent circuit models have the same form. Consequently, the *canonical circuit model* of Fig. 22 can represent the physical properties of PWM dc–dc converters (10).

The primary function of a dc–dc converter is the transformation of dc voltage and current levels, ideally with 100% efficiency. As in the averaged switch model described above, this function is represented in the model by an ideal dc transformer, denoted by a transformer symbol having a solid horizontal line. The dc transformer model has an effective turns ratio equal to the converter quiescent conversion ratio $M(D)$.

Small ac variations in the source voltage $v_g(t)$ are also transformed by the conversion ratio *M(D)*. Hence, a sinusoidal line is added to the dc transformer symbol, to denote that it also correctly represents how small-signal ac variations pass through the converter.

Small ac variations in the duty cycle *d(t)* excite ac variations in the converter voltages and currents. This is modeled by the $e(s)\hat{d}$ and $j(s)\hat{d}$ generators of Fig. 22. In general, both a current source and a voltage source are required.

The converter inductors and capacitors, necessary to low-pass filter the switching harmonics, also low-pass filter ac variations. The canonical model therefore contains an effective low-pass filter. Figure 22 illustrates the two-pole low-pass filter of the buck, boost, and buck-boost converters; complex converters having additional inductors and capacitors, such as the Cuk and SEPIC, contain correspondingly complex effective low-pass filters. The element values in the effective low-pass filter do not necessarily coincide with the physical element values in the converter. In general, the element values, transfer function, and terminal impedances of the effective low-pass filter can vary with quiescent operating point.

Canonical model parameters for the ideal buck, boost, and buck-boost converters are listed in Table 2. Transformer-isolated versions of the buck, boost, and buck-boost converters, such as the full bridge, forward, and flyback converters, can also be modeled using the equivalent circuit of Fig. 22 and the parameters of Table 2; one must then correctly account for the transformer turns ratio by referring all quantities to the transformer secondary.

Small-Signal Transfer Functions of the Buck, Boost, and Buck-boost Converters

The canonical circuit model of Fig. 22 can be solved using conventional linear circuit analysis techniques, to find quantities of interest such as the small-signal control-to-output and line-to-output transfer functions. The control-to-output transfer function $G_d(s)$ is the transfer function from *d(s)* to *v(s)*, with $v_g(s)$ set to zero. The line-to-output transfer function $G_g(s)$ is the transfer function from $v_g(s)$ to $v(s)$, with *d(s)* set to zero. For the buck, boost, and buck-boost converters, these transfer functions can be written in the following forms:

$$G_d(s) = G_{d0}\frac{(1-\frac{s}{\omega_z})}{1+\frac{s}{Q\omega_0}+(\frac{s}{\omega_0})^2} \tag{33}$$

$$G_g(s) = G_{g0}\frac{1}{1+\frac{s}{Q\omega_0}+(\frac{s}{\omega_0})^2} \tag{34}$$

Expressions for the parameters of equations 33 and 34 are listed in Table 3. The boost and buck-boost converters exhibit control-to-output transfer functions containing two poles and one right half-plane (nonminimum phase) zero. The buck converter $G_d(s)$ exhibits two poles but no zero. The line-to-output transfer functions of all three converters contain two poles and no zeroes.

The results of Table 3 can be applied to transformer-isolated versions of the buck, boost, and buck-boost converters, by referring all element values to the transformer secondary side. Equation 34 must also be multiplied by the transformer turns ratio.

The control systems of boost and buck-boost converters tend to be destabilized by the presence of the right-half plane (RHP) zero in the control-to-output transfer function. This occurs because, during a transient, the phase lag of the RHP zero causes the output to initially change in the wrong direction. When a RHP zero is present, it is difficult to obtain an adequate phase margin in conventional single-loop feedback systems having wide bandwidth. Prediction of the RHP zero, and the consequent explanation of why the feedback loops controlling continuous conduction mode boost and buck-boost converters tend to oscillate, was one of the early successes of averaged converter modeling and state-space averaging.

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