DIODES FOR POWER ELECTRONICS

The decades since the 1950s have seen a tremendous development in semiconductor processing and device performance. At the end of the twentieth century, high-power devices are now available for blocking voltages more than 12 kV and with current capabilities up to several kiloamperes. Modern high-power diodes are almost exclusively fabricated from silicon and doped by diffusion processes. For discrete diodes, the active silicon utilized is a single slice of the area up to that of the grown crystal. As part of power modules, diodes typically consist of a parallel arrangement of smaller individual chips, connected by the common module packaging techniques.

With the development of modern high-power turn-off devices in the early 1980s, it was recognized that the available diode performance was no longer sufficient. Substantial growth in diode design and process activities thus resulted with the aim of further optimizing diodes, for example, to reduce power losses or to improve fast turn-off capability. Some of these concepts will be discussed in the section on advanced designs.

DEVICE DESIGN AND APPLICATIONS

Diode Design

Housing Design for Discrete Diodes. Discrete high-power diodes are manufactured from silicon slices that may be almost as large in area as the cross section of state-of-the-art crystal size allows. Today, common diameters of silicon usable for high-power devices are 4 in., 5 in., and 6 in. The crystals are grown as round rods. It is common to design the diode housings essentially cylindrical in shape. Owing to the high rated blocking voltages, a minimum flashover distance of some tens of millimeters is required, and minimum creepage path lengths (distances along the surface between locations of high difference in potential) consistent with common environmental conditions need to be respected. This leads to anode and cathode contacts lying on the two flat sides of the cylinder.

Two different housing designs are commonly available on the high-power market. For the lower current range, stud-type designs [Fig. 1(a)] are typically used, where the device is screwed onto one single cooling surface. This surface is simultaneously one of the two electrodes (anode or cathode). On the opposite side, the other electrode can be contacted by a thick, flexible cable. If higher current ratings are needed and therefore higher power loss is produced in the diode, double-sided cooling with heat sinks on both sides of the diode is preferable. Then, the so-called hockey-puck or press-pack type housing is utilized [Fig. 1(b)]. In this case, diode and heat sinks are pressed together in a stack with a mounting pressure of typically 1.5 kN/cm^2 of contact area.

Layer Structure. For high blocking voltages, the silicon slice that is able to insulate the rated voltage is about 0.3 mm to 1 mm thick. To reach the required insulation distance across the housing, the residual thickness has to be filled up with a metal that conducts well, that is, normally with two copper "pole pieces." Now, the silicon slice can handle high power

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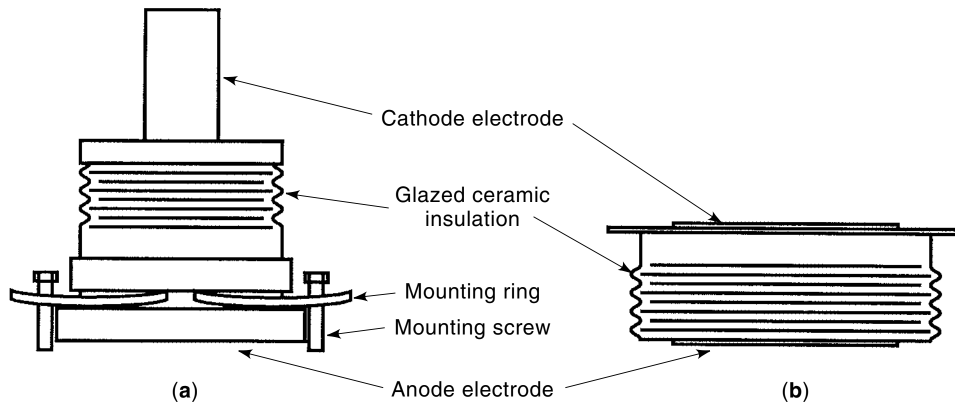

Figure 1. Housing outlines for high-power diodes. (a) Stud design, (b) hockey-puck design. Typical dimensions: up to 35 mm thickness (hockey puck), contact diameter up to 100 mm.

dissipation, and it is therefore allowed to be heated up to typically 125°C or even 175°C. At these temperatures, the copper pole pieces thermally expand much more than the silicon slice, and they would break the brittle silicon easily. For this reason, a strain buffer plate, typically a molybdenum disk of less than 1 mm to 3 mm thickness, is placed on both sides between the silicon slice and the copper pole piece.

To ensure a good electrical and thermal contact between the different layers inside a housing, the layers are compressed with the high mounting force applied on the outside of a housing in case of a hockey-puck design. In a stud housing, the mounting force is produced by a spring, or the layers are soldered together for lower power ratings. For nonsoldered solutions, two variations in technology are known (Fig. 2). In the *alloyed* technology [Fig. 2(a)], the silicon slice is alloyed onto the anode-side molybdenum disk. This allows for very efficient cooling of the silicon, even at the periphery of the slice, and therefore for high maximum operation temperatures (above 160°C). The more advanced *free-floating silicon* technology [Fig. 2(b)] uses dry pressure contacts on both sides of the silicon. This gives the device designer substantially increased flexibility to optimize the diode slice, and the power dissipation may thus be lowered so that an operation temperature of more than 160°C is no longer needed. Lower operating temperatures are advantageous in long-term reliability, that is, load cycling capability of the design.

Silicon Doping. The silicon slice, in principle, consists of a plane p^+–n^-–n^+ structure according to Fig. 3. The + and − superscripts indicate high and low doping concentrations, respectively. In high-power diodes, such a doping structure is usually accomplished by starting with a very homogeneously phosphorous-doped (n^-) silicon slice [doped by converting a small quantity of the silicon atoms to phosphorus in a nuclear reactor, using the so-called neutron transmutation doping (NTD) process] and diffusing aluminum and boron (p/p^+) or phosphorous (n^+) atoms at high temperature into the slice. At the end of the diffusion processes, metallization layers are deposited for good electrical and thermal contact with the adjacent molybdenum disks.

The heavily doped cathode emitter layer is able to inject electrons, while the anode emitter can inject holes into the lightly doped n-base region, and thus the diode will become highly conductive in the forward direction. On the other hand, the lightly doped and wide n base is needed to allow for high blocking capability in the reverse direction. It thus becomes immediately evident that high blocking capability is connected to high conduction loss when two otherwise equivalent designs are compared. A thorough discussion on the principles of operation of the p^+–n^-–n^+ structure will be given later in the section on device theory.

For low blocking voltages (<200 V) and extremely low forward-voltage drop, Schottky-barrier diodes (SBD) can be

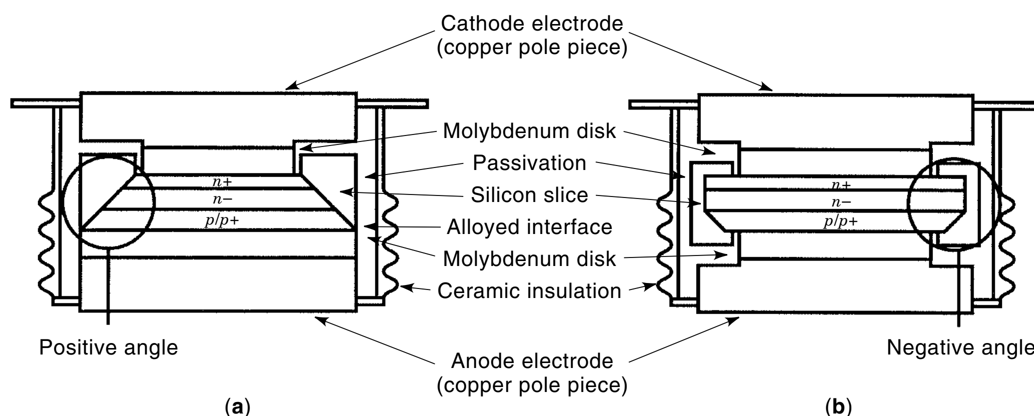

Figure 2. Typical cross section of the layer sequence inside a hockey-puck diode. (a) Alloyed technology with positive angle (the p/p^+ region has a *larger* area then the n^- region). (b) Free-floating silicon technology with negative angle (the p/p^+ region has a *smaller* area than the n^- region).

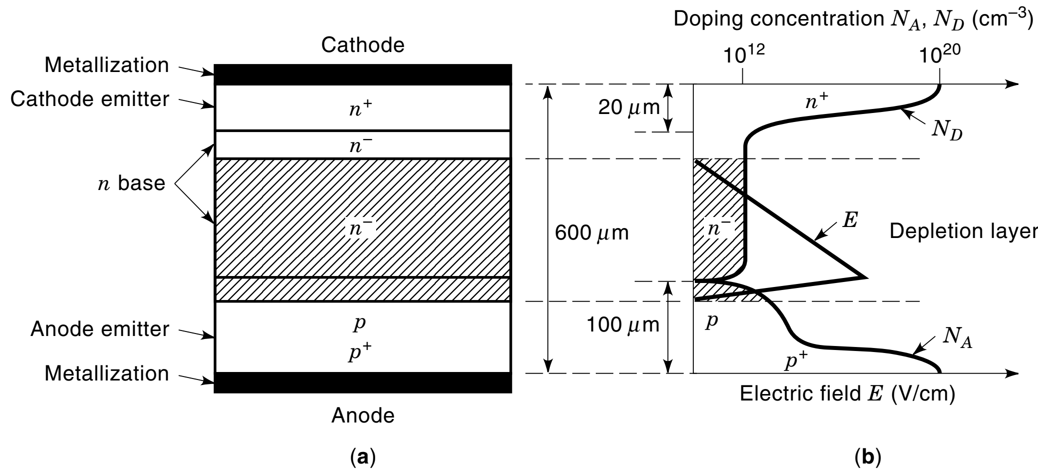

Figure 3. (a) Simplified cross-sectional display and (b) concentrations of n-type (N_D) and p-type (N_A) dopant atoms in a silicon diode of 4.5 kV blocking capability as a function of axial dimension of the slice. p^+ means high p-type concentration N_A; n^- low and n^+ high n concentration N_D. The extent of the depletion layer shown is reached when high reverse voltage is applied to the diode.

manufactured, using a metal-to-silicon junction instead of a p–n junction for blocking (1).

Carrier Lifetime. Besides diffusing fully ionized impurities into the slice in order to create n- and p-type doping regions, it is, particularly for fast switching diodes, approporiate to reduce the charge-carrier lifetime (the average time a particular electron or hole participates in the conduction process) to a value lower than what is is directly after the diffusion processes. This ensures a low production spread in many relevant electrical parameters and is indispensable for fast switching diodes. Today it is mostly usual to apply electron irradiation for this purpose. This technique results in a very accurate control of the electrical parameters of the diode. If a sufficently high electron energy (>2 MeV) is utilized, the resulting carrier lifetime is the same all over the lightly doped portion of the silicon. Alternative techniques will be mentioned later in this article.

Junction Termination and Passivation. Because of the asymmetry of the depletion layer around its metallurgical p–n junction and because of the high dielectric constant of silicon, the electric field at the surface of the silicon (the *junction termination*) has to be controlled by a specific silicon geometry. Bevels with so-called positive and negative angles can be utilized for this purpose, as shown in Fig. 2. Whereas a positive-angle structure is easier to design and is the only one compatible with alloyed technology, the negative-angle structure has significant advantages in long-term reliability and production yield.

To render a properly beveled junction termination stable over extended periods of time, it has to be protected against impurities that might be deposited at the end of the production steps or over long times even inside a sealed housing. For this purpose, one or several insulating organic (or inorganic) passivation layers are deposited on the junction termination. The traditional solution for this purpose is the use of a thick layer of silicone rubber, which also increases the creepage distance on the silicon and mechanically protects the slice during production. In some cases, a thin polyimide layer is also placed between silicon and silicone rubber.

Diode Application Ranges

There are two main design variations in power diodes: slow and fast recovery. The difference is given by the carrier lifetime as pointed out before. A slow-recovery diode is optimized to exhibit very low forward voltage drop in conduction, but there is normally no critical requirement on fast turn-off. Such *rectifier diodes* are often utilized in one- or three-phase bridges for power supplies for electrolysis, for substations, or for power supplies for welding equipment. Very often they are operated at frequencies of 60 Hz or 50 Hz, and therefore the switching losses are almost negligible in comparison with the conduction losses. Such rectifier diodes have an extremely high surge-current capability, which is an important requirement to cover specific short-circuit fault cases.

In combination with modern voltage-source or current-source converters, *fast-recovery diodes* (FRD) are very important devices. Figure 4 displays a simple turn-off switch circuit

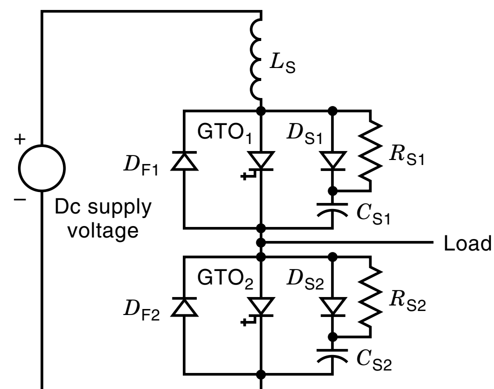

Figure 4. Simple phase leg containing two switching functions 1 and 2, consisting of GTO, free-wheeling diode D_F, snubber inductor L_S limiting *di*/*dt* at switching, snubber capacitor C_S, snubber diode D_S, and snubber resistor R_S to protect GTO and diode against excessive overvoltages upon switching.

configuration in which fast switching diodes are utilized. Used as *free-wheeling diodes,* they contribute to regular phase current conduction during some time intervals when the associated gate turn-off thyristor (GTO) or insulated-gate bipolar transistor (IGBT) is in the off state. It is worth mentioning that the free-wheeling diode of GTO_1 shown in Fig. 4 is D_{F2} and vice versa. With today's typical switching frequencies of 200 Hz and up for GTOs and 1 kHz and up for IGBTs, switching losses become dominant factors. It is therefore advantageous to design diodes with low carrier lifetime, thus exhibiting low switching losses at increased forward voltage drop and thus increased conduction loss.

Moreover, the *snubber diode* displayed in Fig. 4 is a fast-recovery diode as well. It serves to short-circuit the snubber resistor when the GTO or the free-wheeling diode turn off, so that the snubber capacitor can very efficiently limit dv/dt when the blocking voltage builds up across the GTO and free-wheeling diode.

Limiting Parameters

In general, voltage and current handling capabilities as well as maximum temperature are the main limiting parameters. When these limits are violated, an excessive temperature and subsequent melting of silicon or metal will lead to device failure.

The nonrepetitive and repetitive *peak blocking voltages* are important limiting parameters. Ratings up to 6.5 kV for single-chip diodes or more than 12 kV for multichip diodes and high currents are available on the market. Fast-recovery diodes in particular may additionally have strong requirements on high *continuous ac voltage* withstanding capability, because a switch similar to those drawn in Fig. 4 may be exposed to more than 50% of its peak voltage rating during half of its life. It has been found in the early 1990s, after Undeland and McMurray snubbering schemes had emerged, that special design measures needed to be taken (2–4) to adjust the diode capability to the requirements.

The *current-handling capability* of a diode is merely a matter of maximum junction temperature. Diode suppliers generally specify a maximum average current for given current waveform and housing temperature, leading to a certain power dissipation and thus a temperature drop between the silicon junction and housing contact surface. A typical maximum average current value might be 3.3 kA for a 3.3 kV rectifier diode of 120 mm housing diameter at a half-sinusoidal current and 90°C housing temperature. It is important to note that for product comparisons the maximum average current value can only be compared if the underlying current waveform and housing temperatures are specified and identical. Another limit is given by the *rate of change of forward current* (di_F/dt) at diode turn-on and turn-off. Different semiconductor mechanisms can lead to current filamentation and thus to diode destruction if these limits are violated. In many fault cases, a diode has to survive substantial overcurrents for a short time. For such cases, the *surge-current handling capability* is another limiting parameter. The previously mentioned rectifier diode can withstand a half-sinusoidal surge-current pulse of as much as 50 kA peak amplitude at 10 ms duration, if no reverse voltage is applied right after the current pulse. If, on the other hand, reverse voltage follows, the surge-current limit is reduced to 40 kA, typically.

The main temperature limit is the *maximum junction temperature* allowed when the diode is required to block full reverse voltage. This temperature typically lies in the range of 125°C to 160°C. To avoid violating this limit, the circuit designer has to analyze the current and voltage waveforms applied to the diode and the resulting conduction, turn-on and turn-off switching losses carefully. Typically, a total power loss of more than 3 kW can be handled by a double-sided water-cooled 120 mm diode. By use of the thermal resistance or impedance of the device, together with the corresponding data of the heat sink and cooling system, and relation to ambient temperature, the actual junction temperature can then be calculated and can be compared to the specified junction temperature limit.

A *minumum junction temperature* limit normally has to be respected as well. Here, the reverse blocking capability may be at its minimum, and the turn-on process becomes particularly slow.

A further limit relating to temperature is the *load-cycling capability* of a diode. As a consequence of repeated temperature increases and decreases, which are of particular relevance in traction applications, the dry interfaces inside and outside a diode housing suffer many expansions and contractions during their life and therefore underlie a wear-out process. Traction applications may require up to a few million cycles of 50°C to 80°C temperature difference, for example. In cases of very high requirements, such a criterion may make it necessary to utilize more powerful diodes than needed otherwise or to use a parallel connection of several diodes in order to ensure the required mean time to failure (MTTF) for the diode.

DIODE THEORY

In this section we focus on physical effects of structures that constitute a practical semiconductor power diode fabricated in silicon. The following treatment of this subject assumes that the reader is familiar with basic semiconductor physics (doping by impurities, recombination through traps and Auger processes, carrier lifetime, conduction, etc). We will refer in the text to some basic semiconductor formulas that are given in the Appendix for the reader's convenience. This Appendix also shows important constants for semiconductor calculation. Examples of textbooks in this field are given in the Reading List. The article DIODES, also deals with basic semiconductor physics.

With the emphasis on physical effects valid for ordinary power diodes, we first concentrate on the *p–n* junction in low injection. (Low injection implies that the concentration of injected carriers is lower than that of the doping impurities.) Then we discuss high-injection effects as well as properties of a power diode in practical operation under steady-state and dynamic conditions. Finally we briefly comment on modeling the behavior of the diode in different simulation environments.

The *p–n* Junction in Low Injection

The rectifying properties of a semiconductor power diode are due to different Fermi energy levels in *p*- and *n*-type

silicon. Forming two regions of opposite conduction type in the same silicon crystal will make the interface constitute a p–n junction. In thermal equilibrium, that is, when no external terminal voltage is applied, the Fermi level of such a structure is constant. The energy levels of the valence and conduction bands must then bend correspondingly. This forms a potential barrier between the p- and n-type regions, named the diffusion voltage or built-in voltage V_d, where the value of V_d is of the order of 0.5 V to 1 V. A depletion layer (space-charge region) of width w will then support the junction voltage. Adding a suitable metal contact to each region makes the previously mentioned structure a simple diode. The contact on the p side is the anode of the diode and the other one the cathode. By selecting the metals to avoid Schottky barriers, the contacts will be practically ohmic.

Supplying an external terminal voltage V_a to the diode will change the conditions at the p–n junction (the subscript a indicates applied voltage). In the forward-bias case, that is, if the anode potential is positive with respect to the cathode (V_a is positive), the barrier height will decrease. Conversely, in reverse bias the height will increase. Let us assume that all the terminal voltage drop will be caused by the p-n junction, that is, there is no voltage drop across the metal contacts or in the bulk material. The resulting junction voltage V_j will then equate the built-in voltage minus the terminal voltage; thus $V_j = V_d - V_a$. If the applied voltage V_a is positive, it cannot be larger than V_d for fundamental reasons. On the other hand, in the reverse direction V_a is negative and might assume absolute values of several kilovolts for high-power diodes.

Depletion-Layer Properties. For given impurity doping concentrations and spatial profiles, the junction voltage V_j determines several properties of the p–n junction: (1) the width w of the depletion layer, (2) the electric field $E(x)$ within that layer, and (3) the charge Q of the ionized impurities (acceptors or donors). Figure 5 shows schematically how these quantities will depend on junction voltage for an abrupt p–n junction, that is, a junction in which the type of doping changes abruptly. By Eq. (A13) (see Appendix), the gradient of the electric field is proportional to the charge concentration. Therefore, independent of voltage, the electric field increases linearly from zero at the borders of the depletion layer up to its (absolute) maximum value E_{max} at the junction. The electric field diagram constitutes a triangle that increases with voltage. The area of this triangle equates the junction voltage; thus $V_j = \frac{1}{2}E_{max}w$. Furthermore, the space charge within the depletion layer causes a differential junction capacitance C_d that is largely dependent on voltage in contrast to the case of a usual capacitor. E_{max} and w increase with voltage in reverse bias, while C_d decreases. Furthermore, E_{max} increases with impurity concentration, while w instead decreases. E_{max}, however, must not reach the value at which avalanche effects could occur. Therefore, since $V_j = \frac{1}{2}E_{max}w$, a high reverse voltage capability of the diode requires at least one side of the p–n structure being both lightly doped and wide as well.

Minority-Carrier Concentration in the Quasineutral Regions. Outside the depletion layer, in the so-called quasineutral regions, the semiconductor is electrically neutral, since free holes of concentration p and electrons of concentration n compensate the charge of the fixed acceptor and donor ions [Eq. (A1)]. The concentration of majority carriers approximately equates the concentration of impurities [Eqs. (A3) to (A4)]. Then the minority-carrier concentrations p_{n0} and n_{p0} in thermal equilibrium (indicated by the subscript 0) in these quasineutral regions follow from Eq. (A2): $p_{n0} = n_i^2/N_D$ and $n_{p0} = n_i^2/N_A$, where n_i is the intrinsic electron concentration. This thermal equilibrium case is further illustrated in Fig. 6(a). Under forward bias, carrier diffusion exceeds drift, thus resulting in the injection of minority carriers [Fig. 6(b)]. We can derive the minority-carrier concentrations at the depletion-

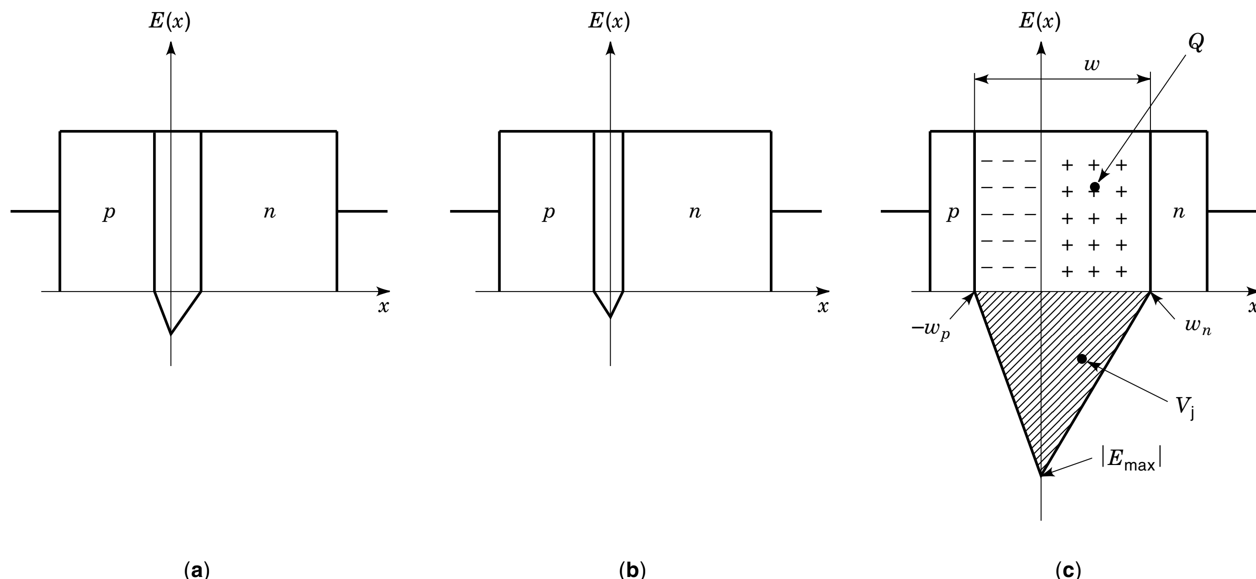

Figure 5. Schematic illustration of depletion-layer width w, electric field $E(x)$, and charge Q for an abrupt p–n junction in (a) thermal equilibrium, (b) forward bias, and (c) reverse bias. The junction voltage V_j is also indicated as the screened triangular area.

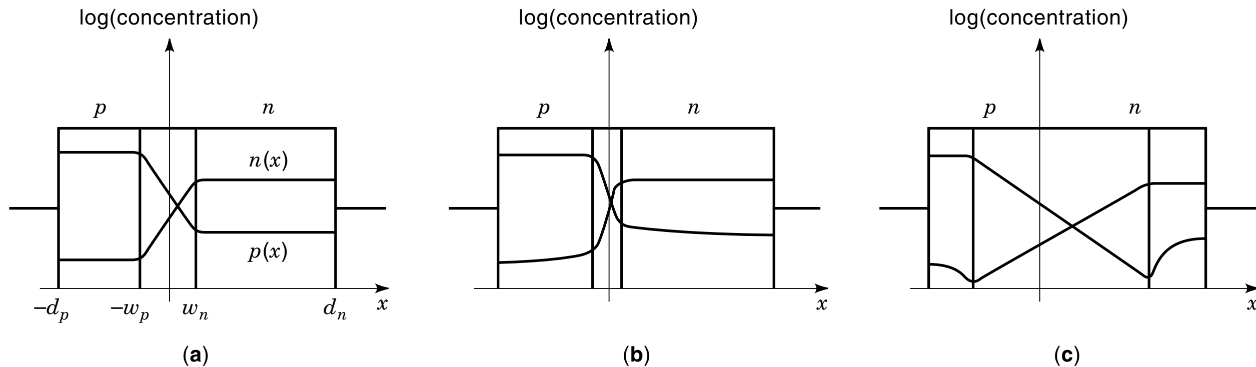

Figure 6. Schematic illustration of the hole concentration $p(x)$ and the electron concentration $n(x)$ for an abrupt p–n junction in (a) thermal equilibrium, (b) forward bias, and (c) reverse bias. The anode and cathode contacts are located at $-d_p$ and d_n, respectively. The depletion layer extends from $-w_p$ to w_n.

layer boundaries w_n and $-w_p$ from Eqs. (A3) to (A6), (A23), (A27), and (A28):

$$p_n(w_n) = p_{n0}e^{qV_a/kT} \tag{1}$$

$$n_p(-w_p) = n_{p0}e^{qV_a/kT} \tag{2}$$

where k is the Boltzmann constant, q the electron charge, and T the absolute temperature. Equations (1) and (2) approximately hold in reverse bias, too. Since $kT/q \approx 0.026$ V (room temperature), the boundary concentrations $p_n(w_n)$ and $n_p(-w_p)$ will be practically zero already at low reverse voltages [Fig. 6(c)].

We can assume that the minority-carrier concentration at the contacted end of the quasineutral region equates the thermal equilibrium value. Then, using the boundary condition Eqs. (1) and (2), the diffusion Eqs. (A18) and (A19) will have the following solutions:

$$p_n(x) = p_{n0} + p_{n0}(e^{qV_a/kT} - 1)\frac{\sinh\left(\dfrac{d_n - x}{L_p}\right)}{\sinh\left(\dfrac{d_n - w_n}{L_p}\right)} \tag{3}$$

$$n_p(x) = n_{p0} + n_{p0}(e^{qV_a/kT} - 1)\frac{\sinh\left(\dfrac{d_p + x}{L_n}\right)}{\sinh\left(\dfrac{d_p - w_p}{L_n}\right)} \tag{4}$$

where d_n and $-d_p$ are the locations of the metal contacts at the n and p side. L_p and L_n are the diffusion lengths of holes in the n region and electrons in the p region, and they relate to the minority-carrier lifetimes τ_p and τ_n for holes and electrons through Eqs. (A16) and (A17). For thick regions, that is, where the thickness of the quasineutral part is much larger than the diffusion length, Eqs. (3) and (4) simplify to

$$p_n(x) = p_{n0} + p_{n0}(e^{qVa/kT} - 1)e^{-(x-w_n)/L_p} \tag{5}$$

$$n_p(x) = n_{p0} + n_{p0}(e^{qVa/kT} - 1)e^{(x+w_p)/L_n} \tag{6}$$

Diffusion Currents and the Diode Formula. Deviations from thermal equilibrium will cause diffusion and drift of carriers within the quasineutral regions. In the low-injection case, which we are considering here, the concentration of minority carriers is so low that their drift contribution is negligible. Thus, from Eqs. (A9) and (A10) the hole current I_p in the n region and the electron current I_n in the p region is determined by diffusion only:

$$I_p(x) = -qAD_p\frac{dp_n}{dx} \tag{7}$$

$$I_n(x) = qAD_n\frac{dn_p}{dx} \tag{8}$$

where A is the area of the diode and D_p and D_n the diffusion constants for holes and electrons, respectively. The origin of the diode current is the nonuniform minority-carrier concentrations in the quasineutral regions [Figs. 6(b) and 6(c)]. In forward bias, the gradient of the hole concentration is negative, resulting in a positive hole current. Vice versa, in reverse bias the gradient is positive, leading to a negative current. Assuming no net carrier recombination or generation in the depletion layer, the total current I will be [Fig. 7(a)]

$$I = I_p(w_n) + I_n(-w_p) \tag{9}$$

Finally, for the above diode with thick quasineutral regions we obtain the so-called diode formula [Fig. 7(b)] from Eqs. (5) to (9):

$$I = I_s(e^{qV_a/kT} - 1) \tag{10}$$

where the prefactor $I_s = A[(qD_p/L_p)p_{n0} + (qD_n/L_n)n_{p0}]$ is constant (the subscript s stands for saturation). In reverse bias, the exponential term in Eq. (10) approaches zero already at very low negative voltages; thus $I = -I_s$ is basically independent of terminal voltage. The absolute value of I_s is therefore named the saturation current of the diode. According to the above description, the saturation current emanates from diffusion only. It is determined by (1) the carrier lifetimes τ_p and τ_n, leading to the diffusion lengths L_p and L_n, and (2) by the doping levels through p_{n0} and n_{p0}.

Generation Current and Carrier Multiplication in Reverse Bias. At sufficiently high reverse voltage, however, thermal generation of carriers within the depletion layer will significantly contribute to the reverse current. Let us assume that

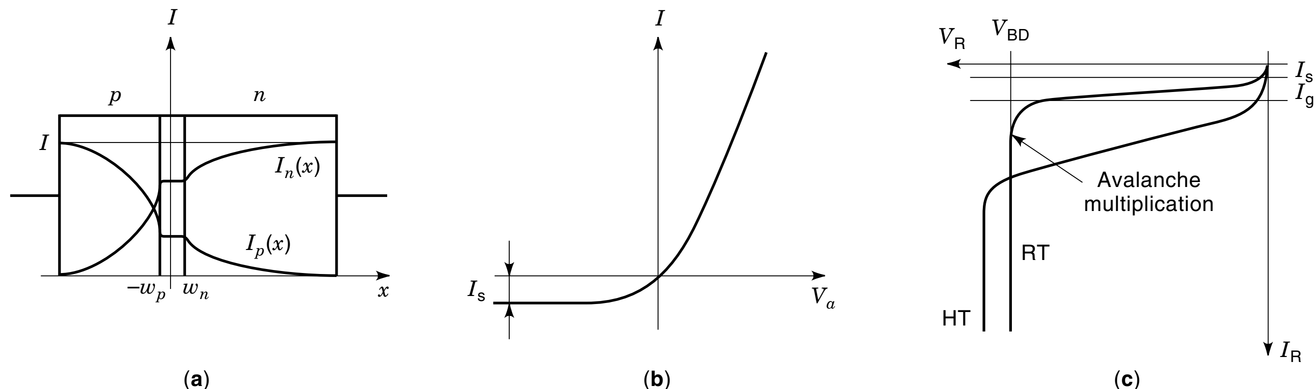

Figure 7. The diode in forward and reverse bias. (a) Schematic representation of hole current $I_p(x)$ and electron current $I_n(x)$ for an abrupt p–n junction in forward bias. (b) Illustration of the ideal diode characteristic. The reverse-bias saturation current I_s is indicated in the figure. (c) Realistic diode characteristic in reverse bias. Generation current I_g and avalanche multiplication effects are included in the reverse current I_R. At high temperature (HT), voltage breakdown V_{BD} occurs at higher reverse voltage V_R than at room temperature (RT).

the strong electric field will sweep out all the generated carriers from this layer (holes towards the anode and electrons towards the cathode) before any recombination takes place. The generation current I_g will then be proportional to the generation rate $G = -n_i/\tau_{sc}$, where τ_{sc} is the space-charge generation lifetime, and the depletion-layer width w. Then

$$I_g = -A\frac{qn_iw}{\tau_{sc}} \tag{11}$$

We can neglect the built-in voltage V_d at sufficiently high reverse voltage V_R. (By definition, V_R is positive in negative direction.) Then, since $V_a = -V_R$, Eq. (A25) shows that the generation current is approximately proportional to $\sqrt{V_R}$. The total reverse leakage current I_R (positive in the negative direction) is

$$I_R = -(I_s + I_g) \approx c_1 + c_2\sqrt{V_R} \tag{12}$$

where c_1 and c_2 are constants that can be derived from Eqs. (A25), (10), and (11).

At very high V_R, however, the electric field within the depletion region may accelerate passing carriers to such an extent that they create new electron–hole pairs by impact ionization. The incident particle flow will then be amplified by the multiplication factor M:

$$M = \frac{1}{1 - \int_{-w_p}^{w_n} \alpha_{eff}\,dx} \tag{13}$$

The effective impact ionization coefficient α_{eff} in the ionization integral in Eq. (13) is strongly dependent on the electric field:

$$\alpha_{eff} = ae^{-b/E} \tag{14}$$

where a and b are empirically determined constants. In case α_{eff} is high enough, that is, when V_R and thus E is sufficiently high (about 2×10^5 V/cm), the ionization integral approaches unity and the multiplication factor increases towards infinity. The leakage current I_R, in turn, also increases towards infinity, thus setting a physical-based limit on the voltage capability of the p–n junction: the so-called breakdown voltage V_{BD} caused by avalanche multiplication. As indicated by Eq. (A24), the breakdown voltage is determined by the doping conditions. For a p–n junction with 1 kV capability, the impurity concentration in the n material should not be higher than about 2×10^{14} cm^{-3}.

***I–V* Characteristics in Reverse Bias.** To sum up reverse conditions, the leakage current consists of a diffusion component I_s from the quasineutral regions and a generation component I_g from the depletion layer. Furthermore, at high reverse voltage avalanche multiplication becomes significant. I_s is basically independent of the reverse voltage, V_R, while I_g increases approximately with the square root of V_R. Furthermore, both of these current components increase drastically with temperature since n_i, and thus p_{n0} and n_{p0}, increases very steeply with temperature [Eqs. (10) and (11)]. The limiting junction breakdown voltage, too, increases with temperature. This is because the mean free path of the carriers in the depletion layer decreases at high temperatures due to enhanced lattice vibrations. The coefficients a and b in Eq. (14) will then be temperature dependent in such a way that a higher electric field, and hence a higher reverse voltage, will be needed to gain sufficient kinetic energy of the carriers for impact ionization. Typically, I_R increases by a factor of 1000 from 25° to 125°C, while V_{BD} increases with about 0.1%/°C. Figure 7(c) illustrates reverse I–V characteristics of a diode at different temperatures when taking all the previously noted reverse current and voltage effects into consideration.

The schematic reverse-bias characteristics in Fig. 7(c), however, implies that we can disregard self-heating effects; that is, the voltage pulses must be sufficiently short and of low repetition rate. Otherwise thermal runaway due to currents in bulk or edge-region imperfections may damage the diode. Furthermore, catastrophic failures due to cosmic-ray-induced local avalanche in the depletion region may be significant in long-term dc reverse-voltage applications. Thus, a 100 FIT reliability requirement (1 FIT = 1 failure per 10^9

hours of operation time) at high dc reverse voltage will require appropriate design, resulting in slightly higher losses than for a low-dc device.

Additional Comments. In the preceding treatment of reverse-bias formulas, we did not consider possible deteriorating effects due to edge conditions. We can disregard such effects, however, for instance, when using an edge contour according to Fig. 2(a). We did also presuppose a diode structure with abrupt *p–n* junctions. In practical power diodes, however, *p–n* junctions are formed by diffusion processes, thus resulting in slowly decreasing diffusion profiles. Deeply diffused junctions may be considered linearly graded at low voltages, but at higher voltages the abrupt junction is the preferred approximation.

In forward-biased power diodes, the diode formula given before [Eq. (10)] is not valid at practical current levels. Instead, we need to consider high-injection conditions for diodes in forward conduction, as we will do in detail in the next section on power diodes.

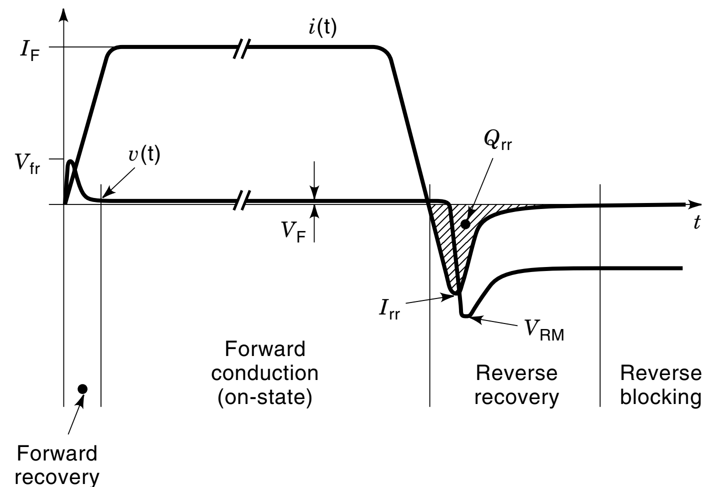

Figure 9. Diode current and voltage in different operating states. Forward conditions are indicated by the subscipt f or F and reverse conditions by r or R. The reverse-recovery charge Q_{rr} equals the screened area. The reverse-recovery time t_{rr} is also indicated.

THE POWER DIODE IN HIGH INJECTION

As we have seen in the previous section, a high reverse-voltage capability of a power diode requires that at least one of the bulk regions is lightly doped to avoid voltage breakdown. Furthermore, this region must be sufficiently wide to accommodate the depletion layer. This implies that the current capability would be very low if the comparatively small number of free minority carriers (in the lightly doped side) were to carry the current alone. Therefore, a practical power diode constitutes a p^+–p–n–n^+ structure, as is shown in Figs. 3(b) and 8. Thin but heavily doped emitter layers next to the metal contacts provide injection of both holes and electrons into the bulk. The injected-carrier plasma will then accomplish high conductance in forward bias. The *n*-type bulk region, the so-called *n* base, accomodates the major part of the depletion layer in reverse bias. The *p–n* junction lies rather deep in the bulk to prevent the *p*-sided depletion layer from touching possible crystal imperfections close to the surface. Figure 3(b) indicates examples of diffusion depths and impurity concentrations for a high-voltage (some kilovolts) diode. However, to minimize the silicon thickness, and hence the forward voltage, the diode may be designed as a punch-through structure; see Fig. 17(b). The rectangular shape of the electric field distribution, achieved by very light *n*-base doping in combination with a field-stopping *n* buffer layer, will then maintain the voltage capability of the device.

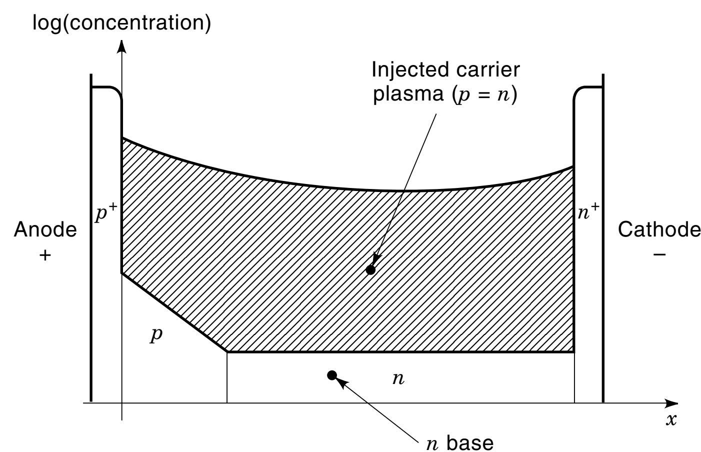

Figure 8. Elementary diagram of a conducting p^+–p–n–n^+ power diode in steady state. The plasma of injected holes and electrons floods the deep *p* region and the *n* base completely.

The diode can adopt different states in operation; see the schematic operation sequence in Fig. 9. We can distinguish two states: the reverse blocking and the forward conducting. When switching from blocking to conducting, the buildup of carriers will need some time resulting in the forward recovery process (diode turn-on). When switching in the other direction, the diode will not stop conducting until the middle region is free from remaining carriers, that is, when the reverse-recovery process (diode turn-off) is completed. The structural design of the diode and the action of the external circuits determine the detailed behavior of these transient processes, resulting in, for instance, the reverse-recovery current I_{rr} and the peak reverse voltage V_{RM}. For line-commutated high-voltage diodes, the (steady-state) forward voltage V_F is in the range of 0.7 V to 2 V, and the forward-recovery effect is negligible. In reverse recovery, however, we must take the reverse-recovery charge Q_{rr} into account although I_{rr} will be much lower than the forward current I_F. At very fast switching, on the other hand, the peak forward-recovery voltage V_{fr} at turn-on may amount to 100 V or more and I_{rr} may be even larger than I_F. We dealt with the low-injection physics of the reverse-blocking state in the previous section. Diode switching and conduction, however, are high-injection phenomena that we now will study in this section on the power diode.

High-injection conditions prevail when the concentration of carriers is higher than that of the impurities. This can be accomplished by injection from the emitters or by optical carrier generation. Furthermore, at pronounced high-injection levels the impurity concentration is negligible in comparison with the carrier concentration. Therefore, we can omit the *p* and *n* subscripts we have used in low injection since the im-

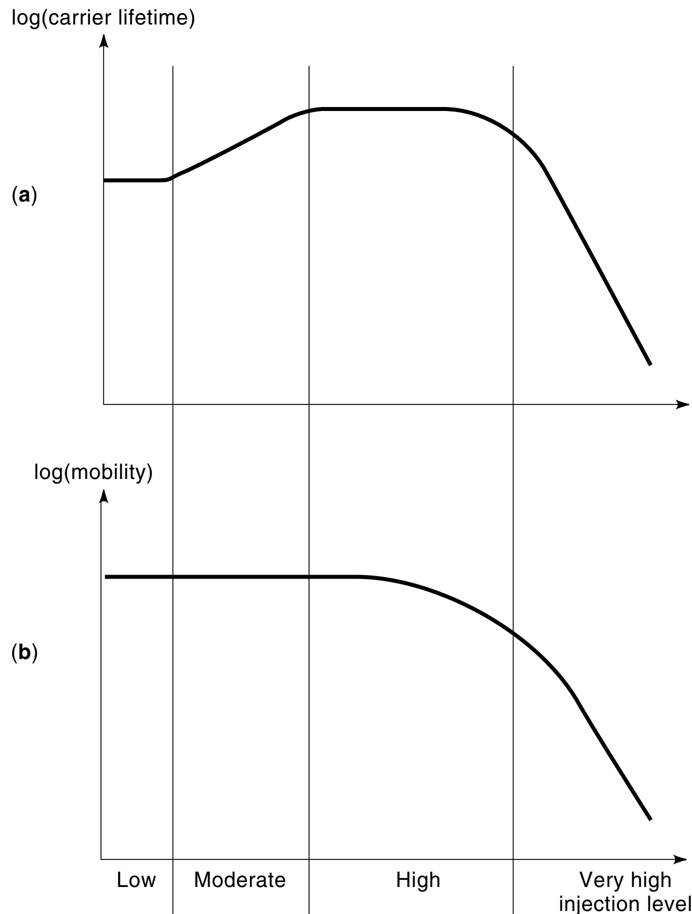

Figure 10. Schematic illustration of the injection-level dependence of (a) carrier lifetime and (b) carrier mobility. At high-injection levels, Auger recombination will substantially reduce the carrier lifetime. The mobility is reduced by carrier–carrier scattering.

purity concentration is practically not visible. In high injection, charge neutrality requires that the concentrations of holes and electrons are approximately equal. The concentrations $\Delta p = p - p_0$ and $\Delta n = n - n_0$ of the injected carriers themselves, however, will be exactly equal. Thus

$$p \approx n \tag{15}$$

where $p,n \gg$ net concentration of ionized impurities and

$$\Delta p = \Delta n \tag{16}$$

Impact of High-Level Injection on Physical Properties. In high injection, the increased amount of carriers affects the behavior of physical properties such as carrier lifetime and mobility. Figure 10 sketches how these properties depend on injection level. Recombination by traps (deep centers) becomes less likely at high injection levels, and the carrier lifetime increases to a constant high-injection carrier lifetime $\tau_h = \tau_p + \tau_n$, where τ_p and τ_n are the minority-carrier lifetimes in n- and p-type silicon, respectively. The detailed properties of the dominating recombination center will determine the relationship between τ_p and τ_n; for electron-irradiated silicon τ_n is about $3\tau_p$, leading to $\tau_h \approx 4\tau_p$. At very high injection levels ($p \geq 10^{17}$ cm^{-3}) the carrier lifetime decreases again due to the dominating influence of Auger recombination. The hole and electron mobilities μ_p and μ_n, in turn, decrease rapidly above injection levels of about 10^{15} cm^{-3} because of the enhanced carrier–carrier scattering effect. Analytical expressions for the dependence of carrier lifetime and mobility on injection level in the high-injection regime are available as well as the temperature dependence of these properties (5–7).

Emitter Recombination. Consider the forward-biased one-sided abrupt p^+–n junction in Fig. 11. (The designation p^+–n implies that $N_A \gg N_D$. We omit the deeply diffused p region for the sake of simplicity.) This junction represents the anode emitter of a diode. The emitter injects holes into the n base, and the electron concentration in the same region increases correspondingly by injection from the cathode emitter. This, in turn, results in a net flow of electrons leaving the n base and entering into the p^+ emitter. At very low forward bias [Fig. 11(a)], low-injection conditions will prevail in the n base. The minority-carrier (electron) concentration in the p^+ emitter will then be very low and thus its gradient, too. The associated electron current I_n will therefore also be very low [Eq. (8)] and negligible compared with the hole current I_p. Neglecting recombination in the depletion layer, the injection efficiency γ, that is, the fraction of current carried by holes injected from the p^+ emitter, is

$$\gamma = \frac{I_p}{I} = 1 - \frac{I_n(w_n)}{I} \approx 1 - \frac{I_n(-w_p)}{I} \tag{17}$$

Hence, in low injection, γ will be close to unity.

Let us now consider a higher forward bias that leads to high-injection conditions in the n base [Figs. 11(b) and 11(c)], and let us calculate the electron current through the depletion layer in this case. First, we again assume that we can neglect any carrier recombination within the depletion layer, thus $I_n(w_n) \approx I_n(-w_p)$. Then, since low injection still prevails in the emitter, $I_n(-w_p)$ can be calculated using low-injection formulas. From Eqs. (A27) and (A28) we obtain (approximately) $p_p(-w_p)n_p(-w_p) = p(w_n)n(w_n) = n(w_n)^2$. Thus

$$n_p(-w_p) = \frac{n(w_n)^2}{N_A} \tag{18}$$

Using Eqs. (2) and (4) we obtain the electron distribution in the p^+ emitter:

$$n_p(x) = n_{p0} + \left(\frac{n(w_n)^2}{N_A} - n_{p0}\right) \frac{\sinh\left(\dfrac{d_p + x}{L_n}\right)}{\sinh\left(\dfrac{d_p - w_p}{L_n}\right)} \tag{19}$$

Since the emitter is heavily p-doped, we can neglect n_{p0} as compared with the term $n(w_n)^2/N_A$. After differentiation of Eq. (19) and insertion of the electron concentration $dn_p(-w_p)/dx$ close to the depletion layer into Eq. (8), we finally obtain $I_n(w_n)$, the so-called emitter recombination current:

$$I_n(w_n) = qAhn(w_n)^2 \tag{20}$$

In this formula, we have replaced the part that contains physical and structural properties of the emitter by a design-dependent quantity h, the so-called h parameter. For practical

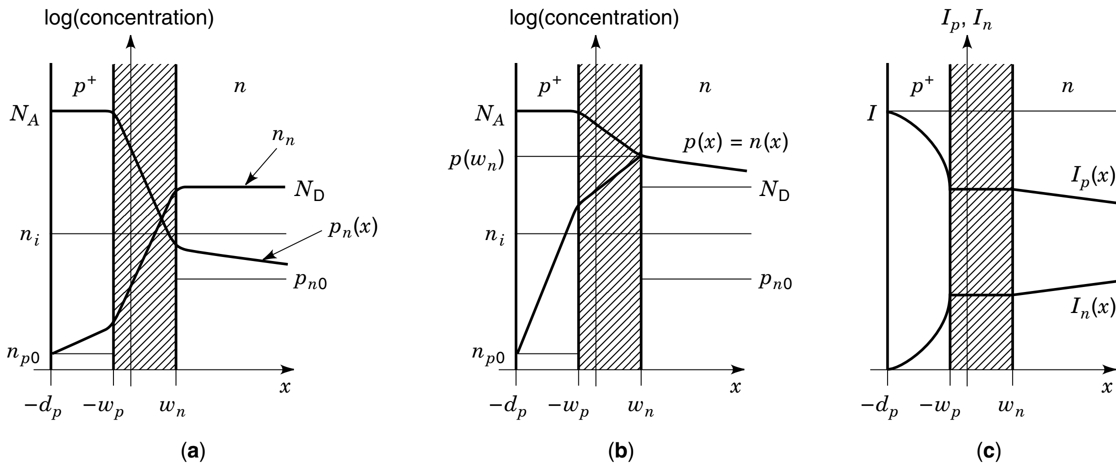

Figure 11. One-sided abrupt p^+–n junction in forward bias. Distribution of hole concentration p and electron concentration n in (a) low-injection and (b) high-injection conditions at the n side. (c) Hole current I_p and electron current I_n in high-injection conditions.

high-power diodes h amounts to 1×10^{-14} cm^4/s to 2×10^{-14} cm^4/s (8). The quadratic expression for the emitter recombination current can also be described in terms of the saturation current for the p^+–n junction (9). Notice that the minority-carrier diffusion length in the emitter is very short since both the carrier lifetime and the mobility are very small due to the high impurity concentration.

At high-injection conditions in the bulk of the diode, the emitter-recombination current represents a substantial part of the total diode current. The emitter efficiency may then decrease considerably as we see in the following example. Let us assume that the current density is 100 A/cm^2 and the concentration of carriers in the bulk, close to the emitter, amounts to the reasonable value of 10^{17} cm^{-3}. Then, with $h = 2 \times 10^{-14}$ cm^4/s, Eqs. (17) and (18) give $\gamma = 0.68$. Hence, as much as 32% of the hole current emerging at the metal contact will disappear by recombination in the emitter; the remaining 68% only will contribute to the charge buildup in the bulk of the diode. Furthermore, the emitter-recombination current increases by the square of the carrier concentration at the boundary W_n. Thus the emitter recombination, together with the previously mentioned Auger recombination and carrier–carrier scattering, will strongly counteract the enhancement of carrier concentration at very high currents. The carrier concentration will therefore hardly exceed 10^{18} cm^{-3} even in surge-current conditions (10).

Forward-Biased Emitter Junctions in High Injection. Consider the foward-biased diode structure in Fig. 8. As illustrated in the figure, injected carriers will completely flood the middle region, that is, the region between the two emitters. Therefore, all three junctions are forward-biased. Let as assume that the impurity concentration in the deep p region is considerably lower than the injection level. Then, detailed calculations show that we can approximate such a structure by a p^+–n–n^+ diode [or even by an imaginary p^+–i–n^+ diode, where i stands for an intrinsic (undoped) semiconductor] from the on-state voltage point of view (11). Figure 12 shows an elementary diagram of a simplified diode structure with impurity concentrations N_A^+ and N_D^+ in the emitter regions and N_D in the middle region of width W. The locations 0^- and 0^+ represent the depletion-layer boundaries at the anode side and W^- and W^+ the boundaries at the cathode side. We can now from Eqs. (A23) and (A27) calculate the externally applied voltage V_{a0} required to maintain the carrier concentration in the middle region, close to the anode, at the level $p(0^+)$. [Notice that Eqs. (A27) and (A28) are valid in high injection, too.] Since $p_p(0^-) \approx N_A^+$, we get

$$V_{a0} = \frac{kT}{q} \ln \frac{p(0^+)N_D}{n_i^2} \tag{21}$$

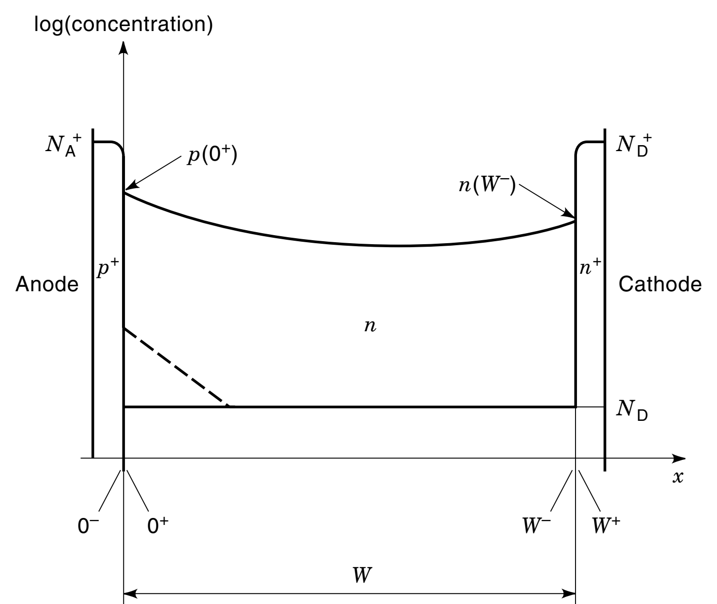

Figure 12. Elementary diagram of a p^+–n–n^+ diode in high-injection conditions. The dashed line indicates the deep p region. The concentration of injected carriers is $p(0^+)$ at the anode side and $n(W^-)$ at the cathode side. The superscripts + and − indicate the left-hand and the right-hand border, respectively, of the junction depletion layer.

A similar consideration for the n–n^+ junction yields the externally applied voltage V_{aW} required to maintain the injection close to the cathode at the level $p(W^-)$:

$$V_{aW} = \frac{kT}{q} \ln \frac{n(W^-)}{N_D} \tag{22}$$

Above, we focus on the concentration of injected holes from the anode [Eq. (21)] and injected electrons from the cathode [Eq. (22)]. These equations show that we must apply the external voltages V_{a0} and V_{aW} across the emitter junctions to increase these concentrations from their thermal equilibrium values $p_{n0} = n_i^2/N_D$ and $n_{n0} = N_D$ to their high-injection values $p(0^+)$ and $n(W^-)$. Let us in conclusion compare numerically the externally applied junction voltages at room temperature in pure low injection with a high-injection case using Eqs. (1), (21), and (22). Assume (1) $p_n(0^+) = 10^{12}$ cm^{-3} and $p_n(W^-) = p_{n0} = n_i^2/N_D$ (thermal equilibrium) in low injection, and (2) $p(0^+) = 10^{17}$ cm^{-3} and $n(W^-) = 7 \times 10^{16}$ cm^{-3} in high injection. For $N_D = 10^{19}$ cm^{-3}, we get the applied voltages $V_{a0} = 0.280$ V and $V_{aW} = 0$ V in low injection, and $V_{a0} = 0.579$ V and $V_{aW} = 0.230$ V in high injection. Thus, as expected, high-injection conditions lead to considerably higher applied voltages than in low injection. We can also see that the sum of the externally applied junction voltages is about 0.8 V in high injection. This sum will not change substantially with injection level due to the logarithmic nature of the voltage formulas; in fact, when changing the injection level by an order of magnitude, the voltage sum will not change more than 60 mV. From Eqs. (21) and (22) we can also see that the voltage sum is independent of the impurity concentration level in the middle region:

$$V_{a0} + V_{aW} = \frac{kT}{q} \ln \frac{p(0^+)n(W^-)}{n_i^2} \tag{23}$$

This formula is exactly the same as what can be obtained for a p^+–i–n^+ structure (12).

The Ambipolar Diffusion Equation. The diffusion equations (A18) and (A19) are very instrumental for calculation of minority-carrier distributions under low injection [Eqs. (3) and (4)]. Let us therefore derive a similar expression valid under high injection. The carrier concentrations are in this case such high that we cannot neglect the drift components of the transport equations. Furthermore, both types of carriers contribute to the diffusion process at the same location. The hole and electron equations, however, relate to each other through the electric field E. From charge neutrality, that is, $p + N_D = n$, we get $p \approx n$ and $dp/dx = dn/dx$. We assume, for the sake of simplicity, that p exactly equates n. By adding the transport equations (A7) and (A8) for the hole current density j_p and the electron current density j_n, respectively, the total current density $j = j_p + j_n$ will be

$$j = q(\mu_n + \mu_p)pE + q(D_n - D_p)\frac{dp}{dx} \tag{24}$$

The electric field E can be eliminated from Eq. (24) by using the transport equation (A7). Then, by use of Einstein's relationships (A14) and (A15), we obtain

$$j = \frac{D_n + D_p}{D_p} j_p + 2qD_n \frac{dp}{dx} \tag{25}$$

For elimination of the hole current j_p, we use the continuity equation for holes, Eq. (A11), in steady state (we neglect the thermal equilibrium value p_0 in this high-injection case):

$$\frac{dj_p}{dx} = -\frac{q}{\tau_h} p \tag{26}$$

where τ_h is the previously defined high-injection carrier lifetime. We can get the left term in this expression from Eq. (25) after differentiation, considering $dj/dx = 0$. Then, by introducing the ambipolar diffusion constant D_a and the ambipolar diffusion length L_a in high injection:

$$D_a = \frac{2D_nD_p}{D_n + D_p} \tag{27}$$

$$L_a = \sqrt{D_a \tau_h} \tag{28}$$

we finally obtain the ambipolar diffusion equation in a very simple form:

$$\frac{d^2p}{dx^2} = \frac{p}{L_a^2} \tag{29}$$

Forward Steady-State Operation

The term *steady state,* or *quasi–steady state,* implies that the time constant for changes in the terminal conditions is much longer than the carrier lifetime. Such a situation applies, for instance, for a forward-conducting power diode in line-frequency operation. In this section, we will study current and terminal voltage conditions for a forward-conducting diode in steady state.

Injection in the Middle Region. Figure 12 illustrates the hyperbolic shape of the curve that represents the injected carrier concentration. Assuming that D_a and L_a are constant throughout the middle region, Eq. (29) can easily be solved:

$$p(x) = p_0 \cosh \frac{x - x_0}{L_a} \tag{30}$$

where (p_0, x_0) is the location of the minimum concentration. We can see that $p(x)$ is symmetrical around x_0 and that it increases monotonously for $x \neq x_0$. The values of p_0 and x_0 are determined by the injection levels at the emitters, and these conditions, in turn, are determined by the total current and the emitter recombination as well.

The stored charge Q_m of holes in the middle region is

$$Q_m = qA \int_0^W p(x)\,dx \tag{31}$$

According to the charge control equation (A20), Q_m is proportional to hole current flowing into the middle region minus the hole current that flows out at the same time. With the

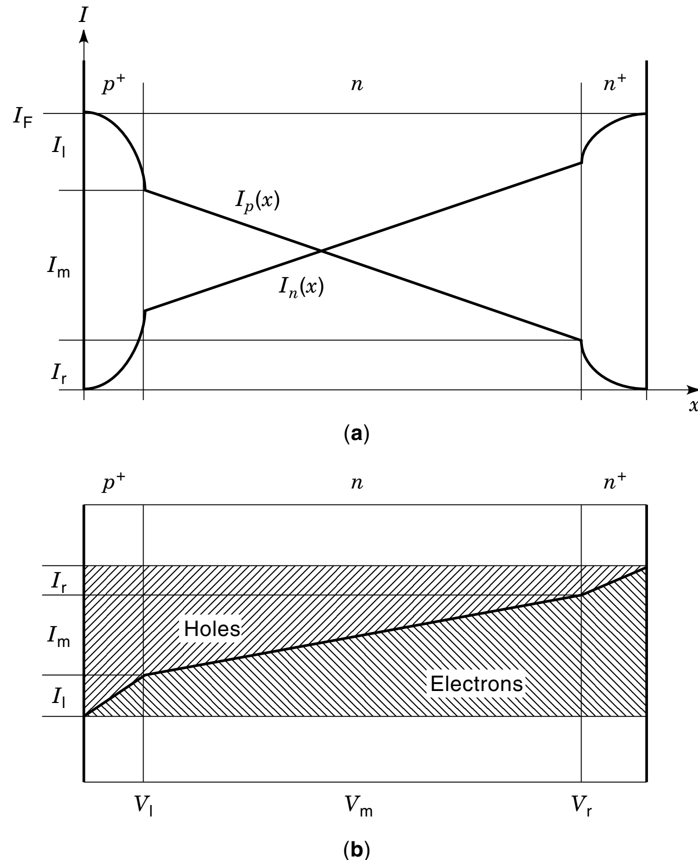

Figure 13. Schematic illustration of the recombination contributions to the diode current I_F. The components I_l and I_r recombine in the anode and cathode emitters, respectively, while I_m recombines in the middle region. (a) Hole current $I_p(x)$ and electron current $I_n(x)$ throughout the structure. (b) The diode current, starting as a hole current at the anode contact, gradually changes into an electron current on the course towards the cathode. The voltage drop components V_l, V_m, and V_r are also indicated in the figure.

commonly accepted designation rules used in Fig. 13, in which the subscript l denotes conditions at $x = 0^+$ and r at $x = W^-$, the total diode current I_F can be divided into three parallel branches:

$$I_F = I_l + I_m + I_r \tag{32}$$

where I_l is the current that recombines in the anode emitter, I_m in the middle region, and I_r in the cathode emitter. (In general, the subscripts l and r indicate the left and right side emitters, respectively.) This recombination behavior is further illustrated in Fig. 13(b). Equation (A20) gives

$$I_m = \frac{Q_m}{\tau_h} \tag{33}$$

Thus, in high injection, the stored charge is proportional to the current component I_m that recombines in the middle region rather than to the total diode current I_F. From Eq. (20), the other current contributions become

$$I_l = qAh_l p_l^2 \tag{34}$$

$$I_r = qAh_r p_r^2 \tag{35}$$

where h_l and h_r are the h parameters at the anode and cathode emitter, respectively. [Equation (35) can be derived analogously to Eq. (34).]

We can see from Eqs. (30) and (31) that p_l and p_r would change proportionally to Q_m. I_l and I_r will therefore increase much faster with the total current I_F than I_m will do, and thus the emitter recombination will be predominant at higher currents. Let us illustrate this fact by a numerical example, assuming that $h_l = h_r = h$. We can derive the relationship between I_m and I_F by solving Eqs. (30) to (35). After some (rather cumbersome) elimination procedures we obtain

$$I_F = I_m + \frac{h\tau_h^2}{2qAL_a^2} \left[\coth^2\left(\frac{W}{2L_a}\right) + \left(\frac{b-1}{b+1}\right)^2 \frac{I_F^2}{[I_m + (h\tau_h^2/qAL_a^2)I_m^2]^2} \tanh^2\left(\frac{W}{2L_a}\right)\right] I_m^2 \tag{36}$$

where

$$b = \frac{\mu_n}{\mu_p} = \frac{D_n}{D_p} \tag{37}$$

Equation (36) might look complicated, but it contains many quantities that can be considered constant for each specific calculation. Using the following realistic values for a high-voltage power diode, $h = 2 \times 10^{-14}$ cm^4/s, $\tau_h = 50\ \mu$s, $b = 2.8$, $L_a = 250\ \mu$m, and $W = 500\ \mu$m, we can find (1) $I_l + I_r = 0.62 I_F$ at 10 A/cm^2 and (2) $I_l + I_r = 0.86 I_F$ at 100 A/cm^2. Thus this result supports the previous statement that the emitter recombination will be predominant at high current levels.

Forward Characteristics. As previously mentioned, we can approximate a practical power diode by a p^+–n–n^+ diode (Fig. 12) when we calculate the forward voltage V_F. In Fig. 13(b) we can see that V_F comprises (1) the externally applied voltage V_l across the p^+–n junction, (2) the voltage drop V_m across the middle region, and, finally, (3) the externally applied voltage V_r across the n–n^+ junction. To calculate the respective voltage contributions, we need to know the detailed shape of the carrier distribution in the middle region. Equation (30) cannot be easily used for this purpose since we do not know the minimum point (p_0, x_0). Instead, we can solve the ambipolar diffusion equation (29) differently using the boundary conditions $p(0^+) = p_l$ and $p(W^-) = p_r$. The carrier concentration function will then be

$$p(x) = \left(p_l \sinh\frac{W-x}{L_a} + p_r \sinh\frac{x}{L_a}\right) \bigg/ \sinh\frac{W}{L_a} \tag{38}$$

Evidently, p_l and p_r depend on current. We will now use the emitter recombination formulas (34) and (35) to solve p_l and p_r as functions of the diode current I_F. Then we need to know how I_l and I_r depend on I_F. First, with $j_p = I_F/A$ and $D_n = (b + 1)D_a/2$Eq. (25) reads

$$I_F = (1+b)I_p + q(b+1)AD_a\frac{dp}{dx} \tag{39}$$

Then, derivation of Eq. (38), insertion in Eq. (39), and use of $I_p(0^+) = I_F - I_l$ result in

$$I_l = \frac{b}{b+1} I_F + \frac{qAD_a}{L_a}\left(-p_l \coth\frac{W}{L_a} + \frac{p_r}{\sinh\frac{W}{L_a}}\right) \quad (40)$$

Analogously, for the recombination current I_r we obtain

$$I_r = \frac{1}{b+1} I_F + \frac{qAD_a}{L_a}\left(\frac{p_l}{\sinh\frac{W}{L_a}} - p_r \coth\frac{W}{L_a}\right) \quad (41)$$

Finally, from Eqs. (34), (35), (40), and (41) we can find the relationships between p_l, p_r, and I_F:

$$p_l = \frac{D_a}{2hL_a}\left(-\coth\frac{W}{L_a} + \sqrt{\coth^2\frac{W}{L_a} + \frac{4b}{b+1}\frac{h\tau_h}{qAD_a}I_F + \frac{4hL_a}{D_a}\frac{p_r}{\sinh\frac{W}{L_a}}}\right) \quad (42)$$

$$p_r = \frac{D_a}{2hL_a}\left(-\coth\frac{W}{L_a} + \sqrt{\coth^2\frac{W}{L_a} + \frac{4}{b+1}\frac{h\tau_h}{qAD_a}I_F + \frac{4hL_a}{D_a}\frac{p_l}{\sinh\frac{W}{L_a}}}\right) \quad (43)$$

As in Eq. (36), most terms and factors in Eqs. (42) and (43) are constants. We can therefore easily calculate p_l and p_r for each I_F, for instance, by numerical methods (12).

As mentioned before and indicated in Fig. 13(b), three terms contribute to the forward voltage:

$$V_F = V_l + V_r + V_m \quad (44)$$

We can obtain the first two terms, and the sum of them, from Eqs. (21) to (23):

$$V_l = \frac{kT}{q}\ln\frac{p_l N_D}{n_i^2} \quad (45)$$

$$V_r = \frac{kT}{q}\ln\frac{p_r}{N_D} \quad (46)$$

$$V_l + V_r = \frac{kT}{q}\ln\frac{p_l p_r}{n_i^2} \quad (47)$$

Thus, as already pointed out before, the sum of the externally applied voltages across the junctions is independent of the impurity concentration as long as high-injection conditions apply.

The third term in Eq. (44) follows from integration of the electrical field $E(x)$:

$$V_m = \int_0^W E(x)\,dx \quad (48)$$

We can express $E(x)$ in terms of forward current and hole concentration using Eq. (24) and, for simplification of the second term, Eqs. (A14), (A15), and (37):

$$E(x) = \frac{1}{qA(\mu_n + \mu_p)p} I_F - \frac{kT}{q}\frac{b-1}{(b+1)p}\frac{dp}{dx} \quad (49)$$

Thus we realize that V_m comprises two parts: (1) an ohmic term V_{res} that is based on the resistivity, Eq. (A22), of the middle region in high injection,

$$V_{res} = \frac{I_F}{A}\int_0^W \frac{1}{q(\mu_n + \mu_p)p}\,dx \quad (50)$$

and (2) a second term, the so-called Dember voltage V_{DB}, that is independent of current,

$$V_{DB} = -\frac{kT}{q}\int_0^W \frac{b-1}{(b+1)p}\frac{dp}{dx}\,dx = \frac{kT}{q}\frac{b-1}{b+1}\ln\frac{p_l}{p_r} \quad (51)$$

where, as an approximation, we have assumed that the ratio $(b-1)/(b+1)$ is constant throughout the whole middle region. Since b always is larger than unity in silicon, the Dember voltage is positive when p_l, as usually is the case, is larger than p_r. The Dember effect will therefore normally increase the forward voltage. For ordinary diodes, however, this contribution is small (<10 mV). In contrast, by purposely reducing the anode emitter efficiency the Dember effect can be used to reduce the forward voltage for very thin diodes.

From Eqs. (47), (50) and (51), the final forward voltage formula will be

$$V_F = \frac{kT}{q}\ln\frac{p_l p_r}{n_i^2} + \frac{I_F}{A}\int_0^W \frac{1}{q(\mu_p + \mu_n)p}\,dx + \frac{kT}{q}\frac{b-1}{b+1}\ln\frac{p_l}{p_r} \quad (52)$$

From above, in normal high-injection conditions the first term is rather constant (≈0.8 V) and the last term is negligible. Then the current dependence of V_F mainly emanates from the middle term. This contribution, however, is not directly proportional to the current I_F since both the injection level p and the mobilities μ_n and μ_p depend on current.

Knowing the design parameters of a power diode and taking into account the injection-level dependence of mobilities and carrier lifetime, we can calculate the forward characteristic using Eqs. (38), (42), (43) and (52). Furthermore, we can also calculate the forward characteristics for different temperatures. While the h parameter can be considered independent of temperature (13), the carrier lifetime increases with temperature and the mobilities decrease. Either temperature effect will dominate depending on the current level, which explains why the characteristics may cross each other as illustrated in Fig. 14. The temperature coefficient of the forward voltage will then be positive (V_F increases with temperature) at current levels above the crossover point (the so-called inversion point). This behavior is particularly desirable to obtain good current sharing when paralleling diodes.

Dynamic Conditions

We briefly covered switching between reverse-blocking and forward-conducting states of a diode in the description of the

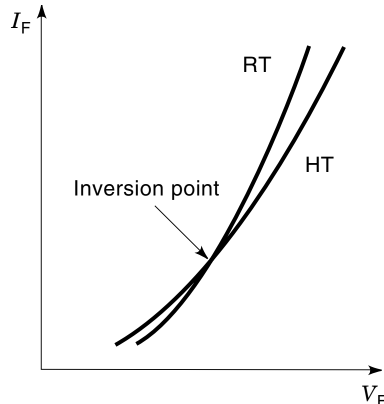

Figure 14. Realistic forward characteristics of a power diode at room temperature (RT) and high temperature (HT). I_F is the current and V_F the voltage. The curves cross at the inversion point.

operation sequence shown in Fig. 9. In the following we will explain principles of the transient behavior of the terminal current and voltage by physical processes inside the diode. The current–voltage relationship for practical devices, however, cannot be derived analytically as was done in the steady-state case. We will therefore return to this issue in the modeling section.

Forward Recovery. The emitters will, in forward recovery, increasingly inject carriers until steady-state conditions are reached. In this process, the diode current at first conducts mainly through majority carriers, thus exhibiting a substantial terminal voltage if the forward current rate of rise di_F/dt is high; see Fig. 15(a). After some time, high injection gradually develops starting from the anode side (time t_1). The electric field in the low-injection region, however, may remain considerably high. The minority-carrier current in that region will therefore be due to both diffusion and drift in this time regime (14). In the very beginning, the forward voltage rises steeply with current. Then the voltage increase will slow down since the conductance of the device increases by injection. Therefore, the voltage exhibits a peak V_{fr} at the time t_2; then it gradually decreases (time t_3) until it reaches the steady-state level at time t_4.

The time-dependent distribution of injected carriers, as well as the shape of the forward current pulse, determines the forward voltage transient. We can arrive at a relationship between hole current density and carrier distribution by using the same method as when deriving Eq. (25), but keeping $p + N_D = n$:

$$j_p = \frac{p}{bN_D + (b+1)p}\, j - \frac{b(N_D + 2p)}{bN_D + (b+1)p}\, qD_p \frac{dp}{dx} \qquad (53)$$

This general equation is valid under all injection conditions, even at medium injection. In low injection and in high injection, as well, it simplifies to the usual transport equations for holes:

$$j_p = -qD_p \frac{dp}{dx} \qquad \text{(low injection)} \qquad (A9)$$

$$j_p = \frac{1}{b+1}\, j - qD_a \frac{dp}{dx} \qquad \text{(high injection)} \qquad (54)$$

Notice that Eq. (54) follows from Eq. (39). In principle, we can treat Eq. (54) in a similar way as we used for Eq. (25) in steady state, but the diffusion equation will now include a time-dependent term. This will complicate solving the resulting diffusion equation, even if we neglect the recombination term in this fast turn-on transient. Another way is to approximate the carrier distribution by simple functions and then make use of the charge control Eqs. (A20) and (A21). However, independently of how we obtain the time-dependent distributions of the carrier concentration and the electric field, the forward voltage can be calculated by integrating the electric field and adding the applied junction voltages.

Reverse Recovery. In Fig. 9, we assume that the conducting period ends by commutation, that is, by forcing the current down towards zero through switching it to another current path in the circuit. In normal cases, the current decreases so fast that we cannot assume (quasi-) steady-state conditions, and the charge Q_m in the middle region will not vanish in pace with the declining current; see Fig. 15(b). Instead, the remaining charge at the current zero-crossing point ($t = t_1$) will constitute a substantial part of the steady-state value. The shape of the carrier distribution at this moment largely determines the turn-off transients in the following reverse-recovery process. This carrier distribution, in turn, depends

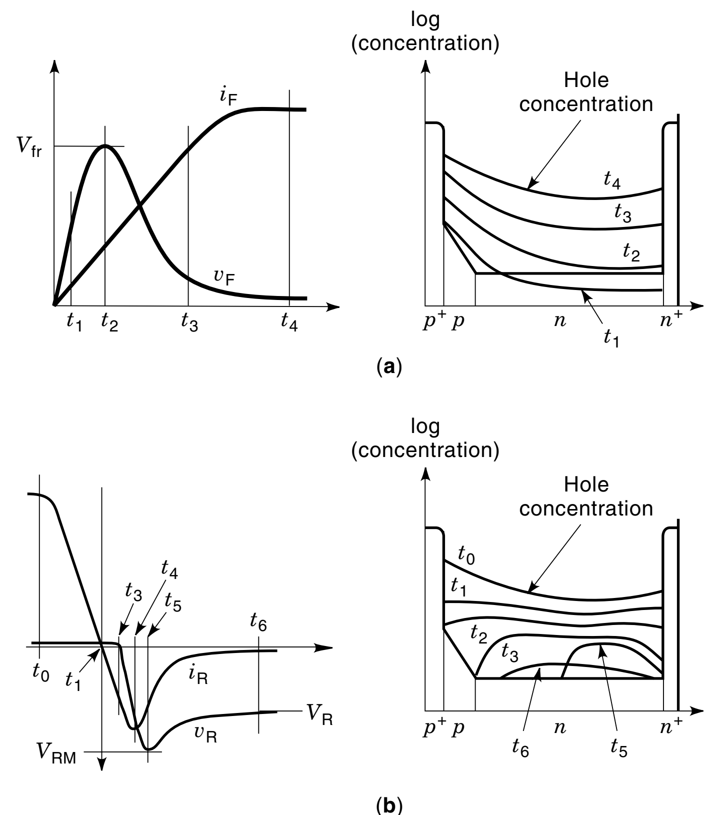

Figure 15. Elementary diagram of a power diode in dynamic conditions. Current and voltage transients and the corresponding hole distribution in (a) forward recovery and (b) reverse recovery. Forward current and voltage are i_F and v_F, respectively, while the corresponding reverse quantities are i_R and v_R (positive in the reverse direction). In (b), t_2 is omitted in the left figure and t_4 in the right figure for clarity.

on the preceding steady-state conditions and on the current ramp between the time points t_0 and t_1. Therefore we must consider what is going on inside the diode already from the very onset of the current commutation. Before the current zero crossing, the emitters are still injecting, but then, since the current reverses its direction, the reverse current i_R makes holes flow to the anode and electrons to the cathode. Thus this reverse current extracts carriers from the borders of the excess charge region. Additionally, the ongoing carrier recombination simultaneously reduces Q_m all over the highly injected region. Hence both extraction and recombination will accomplish removal of charges throughout the whole reverse-recovery phase. The extraction part equates the charge that passes the terminals, while the recombination part is not observable from outside. Hence the recovery charge Q_{rr} equates the stored excess charge at current zero crossing minus the recombination part.

We can assume approximately high-injection conditions within the whole region of remaining charge; hence, the gradient of the carrier distribution follows from Eq. (54):

$$\frac{dp}{dx} = \frac{1}{qD_a}\left(\frac{1}{b+1}\,j - j_p\right) \tag{55}$$

Let us consider the sign of the gradient at the p-side border $x = x_l$ of the remaining charge: (1) At positive current, the sum within the large parentheses is negative; thus the gradient will be negative. (2) At current zero crossing, the gradient will be zero, provided we can neglect emitter recombination. (Otherwise, $j_p = -j_n = -qhp_l^2$.) (3) Finally, when the diode current is negative (i_R is positive), all current to the left of the border consists of hole current since no electrons are available there, thus $j_p = j = -i_R/A$ and the gradient will be positive.

Analogously, the gradient at the right border $x = x_r$ is positive before $t = t_1$ and, when neglecting emitter recombination ($j_p = 0$), negative afterwards. Thus, Eq. (54) gives, from current zero crossing and further on, the gradients of the carrier concentration curve at the borders:

$$\left.\frac{dp}{dx}\right|_{x=x_l} = \frac{1}{qAD_a}\,\frac{b}{b+1}\,i_R, \qquad t \ge t_1 \tag{56}$$

$$\left.\frac{dp}{dx}\right|_{x=x_r} = -\frac{1}{qAD_a}\,\frac{1}{b+1}\,i_R, \qquad t \ge t_1 \tag{57}$$

We can observe from Eqs. (56) and (57) that the concentration curve is a factor of b steeper at the anode side due to the difference in hole and electron mobilities. The anode emitter junction, even in the simplified structure in Fig. 12, will therefore be cleared before the cathode emitter in the reverse-recovery process.

After clearing the p^+–p junction at $t = t_2$, the point x_l moves inwards and the concentration gradients becomes steeper since i_R increases monotonously. The diode voltage, however, remains positive since the p^+–p and n–n^+ junctions still are forward-biased. At time t_3, the combined carrier extraction and recombination have cleared the deep p–n junction of excess carriers, and the diode can start blocking. The continuing removal of charge develops a depletion layer at the junction that will support an increasing reverse voltage v_R. Strictly speaking, in the case of diffused p–n junctions the voltage will go negative slightly before the reverse current clears the junction (15). As i_R continues to grow, the concentration curve becomes still steeper. Formulas like the charge control Eqs. (A20) and (A21) and Eqs. (55) and (A25) will control the detailed internal relationships among (1) charge extraction and carrier recombination, (2) shape of the remaining excess charge, and (3) reverse voltage of the depletion layer. At high reverse currents, however, the holes flowing through the depletion layer will provide an appreciable positive charge that adds to that of the impurity ions [Eq. (A13)]. This, in turn, may substantially reduce the width of the depletion layer. Consequently, the electric field increases, thus imposing the risk of carrier multiplication and a subsequent dynamic avalanche (16). In the case of clearing the n–n^+ junction, too, we must also consider the ohmic voltage drop in the quasineutral region close to the cathode emitter. The internal relationships described before, together with the external circuit conditions, will then determine the resulting current–voltage transients. In the case of the inductive load shown in Fig. 9, the rate of rise of the reverse current decreases when the diode takes over voltage from the series inductor. At $t = t_4$, v_R equates the circuit voltage, thus $di_R/dt = 0$. Then, during the subsequent voltage overshoot, the reverse current decreases rapidly accompanied by a corresponding decrease of the gradient of the carrier distribution. The reverse voltage reaches its maximum V_{RM} at $t = t_5$, and then it decays to the steady-state value V_R (time t_6) while the depletion layer shrinks correspondingly.

From the preceding description we can conclude the following: (1) The carrier lifetime affects the reverse recovery in two respects, namely, in determining the excess charge at current zero crossing as well as the carrier recombination throughout the following recovery process. A high carrier lifetime is favorable for conduction, but the recovery charge Q_{rr} and, consequently, the turn-off loss will be high. On the other hand, the lower lifetime that is required for a fast switching diode leads to high conduction losses. The trade-off between V_F and for instance Q_{rr} can be improved by special techniques as localized lifetime reduction or optimized emitter design (see the section entitled "Advanced Designs" later). (2) The doping of the n-type middle region is essential for the diode behavior in reverse recovery. For an ideal punch-through structure, the reverse voltage would not increase noticeably until the depletion layer reaches the n^+ buffer at the cathode side. This, in turn, would not happen until the whole middle region is cleared of excess charge, which may result in a very sharp (snappy) turn-off. Therefore, unless sophisticated design techniques are utilized, a so-called soft reverse recovery without sharp voltage transients requires a sufficiently heavy doping of the n region.

Diode Modeling

Modeling of different passive and active components is an essential part in development of modern electric and electronic equipment. The power diode can be modeled in several ways with different degree of complexity depending on purpose: (1) We can use finite-element methods (FEM) based on the generic semiconductor equations and accounting for most of the relevant physical effects. This technique is accurate, but it is comparatively elaborate and time-consuming and it can hardly go together with complicated external circuits. FEM simulation is therefore more adapted to detailed investigation of the diode itself than to circuit design. (2) For investigation of the physics involved in the interaction between diode and

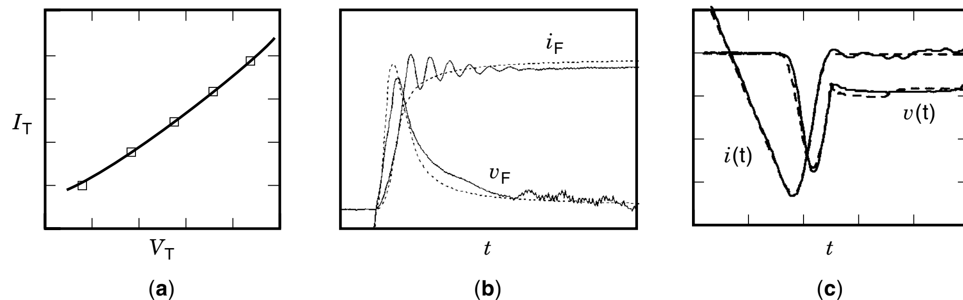

Figure 16. Comparison of measured and simulated results of (a) forward characteristics of a power thyristor (a thyristor can be considered a diode in high injection) at room temperature, (b) forward recovery of a fast diode at room temperature (from Ref. 20), and (c) reverse recovery of a fast diode at high temperature (from Ref. 21). Measurements are boxes or solid lines, while simulations are dashed lines.

external circuit, a circuit simulator that is programmable with analytical expressions as the equations above can be very useful. Then, depending on purpose or requested accuracy, we can implement diode models of different complexity. Models for line-commutated diodes with high carrier lifetime may approximate the excess charge in the whole middle region by simple geometrical curves (17). In models for fast-recovery diodes, however, it may be necessary to divide the charged region into a fixed number of sections that adjust themselves and move in pace with the entire region (18). Using this simulation technique, the the so-called rubber-band method, we can, for instance, study how changes in design of the diode will affect its terminal behavior in a specific external circuit (3). Finally, we can use a circuit simulator that has built-in facilities for modeling the terminal behavior of a diode (19). Such tools can be library models for existing diodes or more generic models that need parameter inputs. These parameters are generally not obtainable from common physical expressions; instead they must be extracted separately from data sheets or special characterization measurements. Once we have introduced the necessary inputs (part number or parameter data), the calculations are fast and can easily be used for studying circuit design, provided the model and its parameters are valid in all of the investigated regime.

To illustrate the feasibility of using the formulas described above, Fig. 16 shows comparisons between simulated and measured results for the following cases as examples. (1) Forward characteristics of a thyristor at room temperature (a thyristor can be considered a diode in this high-level injection case): The middle region is treated as a whole as described in the preceding section on forward characteristics. The injection-level dependence of the mobility has been taken into account at the integration in Eq. (52). We do not need any circuit simulator in this case. (2) Forward recovery of a fast diode at room temperature (20): The circuit simulator includes diode modeling by the rubber-band method. The excess charge is piecewise approximated by polynomials of second degree. (3) Reverse recovery of a fast diode at high temperature (21): The temperature dependence of carrier lifetime and mobilities are included in this example. The modeling technique here is the same as in the forward-recovery case. From the examples in Fig. 16 we can conclude that approximate modeling using high-injection formulas may serve as a useful tool in circuit simulations.

ADVANCED DESIGNS

Trade-Offs between Parameters of Electrical Capability

Punch-Through Design. As can be recognized in the previous sections, there is a strong correlation between blocking capability and power loss for a given silicon area. The reason for this is the thickness of the depletion layer, which increases with increased blocking capability. Traditional designs use a triangular shape of the electric field versus axial dimension, as was shown in Fig. 4. With improved process and design capabilities it has become possible to convert the triangle of the electric field to nearly a rectangle of same area, that is, the same blocking capability (Fig. 17), which allows to reduce the silicon thickness significantly. Thus, a strongly reduced conduction loss can be achieved. Further optimization of the trade-off between conduction and switching loss leads to an additional improvement of the total power loss in the diode.

Axial Carrier Lifetime Profiling. As mentioned earlier, most modern power diodes are irradiated with electrons for accurate carrier lifetime control. Due to the high electron energies commonly utilized (10 MeV to 16 MeV), the resulting carrier lifetime is essentially constant along the thickness dimension of the silicon slice. This leads to fixed trade-off relationships between forward voltage drop and turn-off speed and thus between conduction and switching losses. Several ways to improve these relationships have been proposed. One of them is axial lifetime profiling, that is, nonconstant lifetime along the symmetry axis of the slice. Axial lifetime profiling additionally allows to eliminate snappy turn-off (i.e., to induce soft recovery) in thin diodes when they are switched at high di/dt. Snappy turn-off is an unwanted behavior at which the reverse-recovery current suddenly jumps to zero when all remaining carriers have disappeared, and thus a sudden increase in reverse overvoltage results, which often gives rise to ringing and high-frequency disturbances in the circuit.

For many years, such techniques have been used in fast switching diodes with fast diffusing impurities such as *gold* and *platinum* as recombination centers. The concentration of these recombination centers depends on the emitter doping and is therefore nonconstant in the silicon. It can be controlled to some degree by the process parameters, but it is not very well reproducible.

The availability of commercial sources for *high-energy ion irradiation* (protons, He^{2+} ions) as well as powerful computer simulation has made it possible to design power diodes with improved loss relationships and soft recovery behavior (22–24). In contrast to electron irradiation, high-energy ion irradiations can use the ion acceleration energy as an additional degree of freedom to control the depth of local lifetime reduction. This opens a wide range of optimization opportunities, even by combining several irradiations with different dosages and energies. An interesting discussion of the effect of varying the location of low lifetime is shown for thyristors in (25).

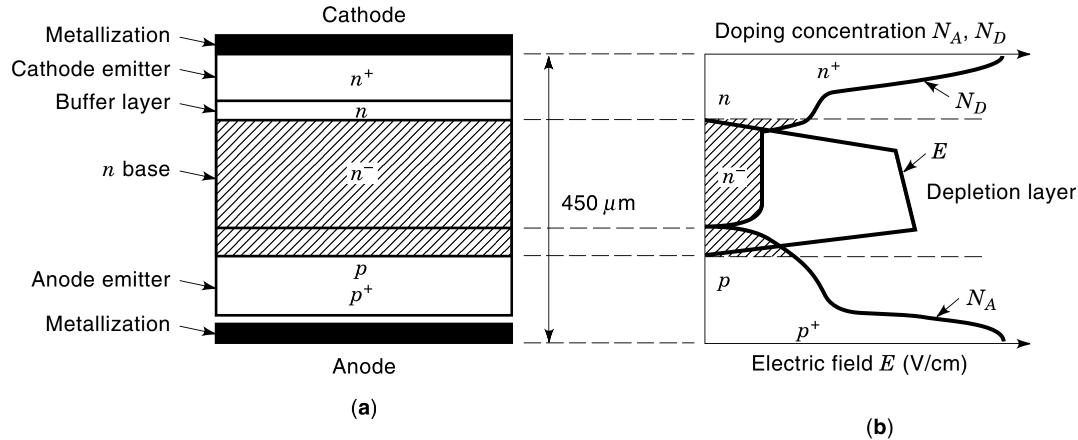

Figure 17. Typical design of a punch-through diode, where the depletion layer "punches through" to the n "buffer layer" profile, (a) as a cross section and (b) with the dopant profiles. If the area under the electric field, which is the applied external voltage, is the same as in a non-punch-through diode, the silicon can be made thinner (compare 600 μm in Fig. 19 and 450 μm shown here), thus leading to smaller losses.

Low-Efficiency Emitters. Another concept to tailor loss trade-off and switching softness is the optimization of emitter efficiency. Whereas traditional emitters are very heavily doped and therefore very efficient, the emitter efficiency can be reduced by laterally interrupting this heavy doping on part of the surface area or by reducing the depth and doping concentration of the emitter zone. Figure 18 gives a simple picture of these ideas. Many different approaches have been published in this field. The main idea is to reduce the amount of charge injected in the conducting state of the diode, thus improving turn-off capability at somewhat deteriorated forward conduction. The self-adjusting p-emitter efficiency diode (SPEED) concept (26) utilizes this idea by tuning the p-emitter doping such that the reduced doping of most of the area is just sufficient for good stationary conduction but that the heavily doped regions enable good surge-current capability nevertheless. Comparisons and references on other low-efficiency emitter concepts are given in Refs. 27 and 28. The idea of lightly doped and thin emitter profiles ("transparent emitters") is another alternative, but today it is more often used in IGBTs and GTOs than in diodes (29,30).

High-Voltage Junction Termination

Planar Junction Termination. In contrast to the beveled junction termination techniques presented in the first part of this article, planar terminations rely on metallurgical junctions terminating in one of the large surfaces of the silicon slice. To avoid a large loss of blocking capability in comparison with the bulk, the electric field distribution has to be widened at the surface. Several concepts have been used for this purpose. The *field-plate* approach (31) uses insulated conductive layers above the junction termination to model the shape of the electric field lines. This technique is very sensitive to electric charges deposited on the surface. In the *field-ring* technique (32), ring-shaped zones of opposite doping are built into the junction termination region. This concept is sensitive to surface charge as well, and it moreover requires a very accurate

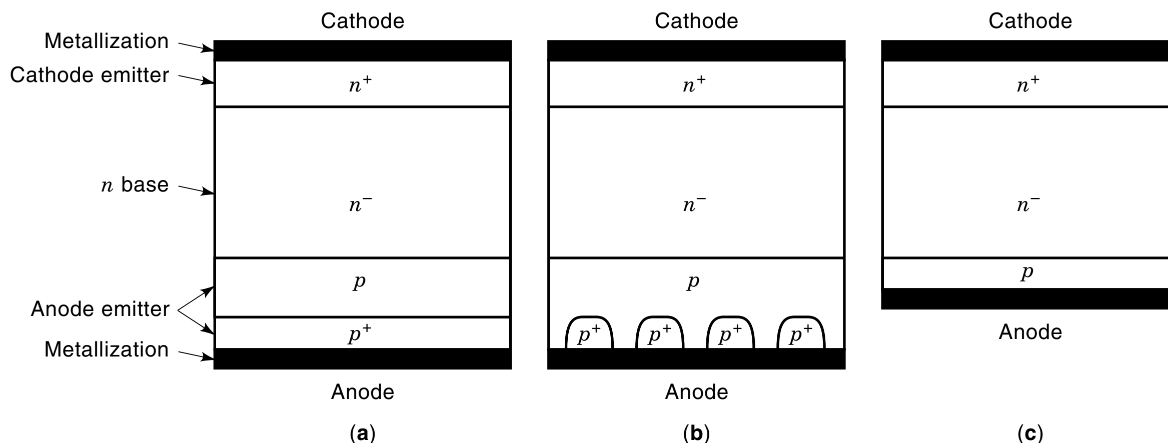

Figure 18. Cross sections of diode doping with different anode concepts. (a) Standard design, (b) low p-emitter efficiency with SPEED concept, (c) low p-emitter efficiency using a transparent p emitter.

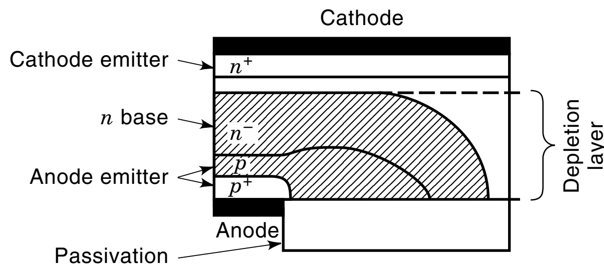

Figure 19. Planar junction termination extension by termination of the p-doped anode emitter zone in a gradual lateral doping decrease. The width of the depletion layer is thus increased along the interface to the passivation layer, and the maximum field is reduced.

control of doping concentration for the field-ring structures. It, though, can be modified by making the field rings lightly doped and overlap and by thus realizing a lateral smooth decrease in doping concentration (33) as seen in Fig. 19. If such a structure is properly designed, it is less sensitive to surface charge and doping concentration than the preceding concepts (34) and can reach breakdown voltages close to those of the bulk. Today, this technique is often referred to as *junction-termination extension.*

Semi-Insulating Passivation. The traditional organic passivation layer techniques can solve only part of the problem: they protect the junction termination on the silicon surface by providing freedom from dangerous mobile ions at the immediate silicon surface, but ions reaching the surface of the passivation layer or diffusing into it can still distort the field distribution. A semi-insulating passivation layer can remove this problem. In integrated circuits, the concept of semi-insulating polycrystalline silicon (SIPOS) has been used for a long time. Typically, such SIPOS layers are additionally covered with a layer of silicon nitride, which prevents ions from diffusing into or through the SIPOS. This makes the passivation layer system "hermetic," so that plastic housings can be utilized with excellent reliability figures. Such SIPOS–nitride systems have also been adopted for high-voltage passivation in power devices, for example, up to 3.5 kV breakdown voltage (35). They are utilized as the standard technique in modules with high-power IGBTs and diodes.

For large-area discrete diodes, on the other hand, the SIPOS–nitride process is expensive and less well compatible with the process sequence. A more appropriate technique has been introduced recently in advanced diode production, consisting of diamondlike carbon (DLC) layers on the silicon surface (36). These layers are impermeable for mobile ions and therefore do not require an additional diffusion barrier layer on top. Excellent blocking capability above 6 kV has been demonstrated.

Diodes for High-Power Modules

Antiparallel diodes integrated in high-power modules are essentially designed as described in the first part of this article. In IGBT modules, the IGBT chips cannot be manufactured with high yield on large area, and therefore a number of chips of about 1 cm^2 in area are connected in parallel. The same is done for the diode. The diode chips are then manufactured with planar junction termination and SIPOS passivation. A specific problem in this case is some derating required for current sharing between the separated parallel diode chips in comparison with a single-chip diode.

Silicon Carbide Diodes: the Solution of the Future

The never-ending search for higher blocking capability and improved power loss has led the high-power semiconductor device community to silicon carbide (SiC) as a new semiconductor material. SiC devices are able to block voltage up to much higher temperatures than silicon, and, due to the much higher avalanche breakdown field strength, high-voltage devices can be made much thinner, so that the power loss is strongly reduced. Great progress has been made in the 1990s to develop SiC wafer production and device processing technology (37). The first diode structures have been manufactured with a blocking capability of 4.5 kV (38). One of the main problems still is that it is hard to manufacture diodes with high yield because of bulk imperfections in the SiC material. Additionally, techniques have to be further developed for a reliable passivation of junction terminations at very high operating temperatures. Another problem that still needs to be solved is a packaging technology capable of withstanding the high temperatures allowable for SiC and exhibiting sufficient long-term reliablity for load-cycle operation, since the number of load cycles permitted very strongly depends on the temperature difference in a load cycle, as was shown for silicon in Ref. 39.

CONCLUSION

The mechanical design of typical high-power diodes has been discussed. Ratings up to more than 12 kV reverse blocking voltage, several kiloamperes in average current, and more than 3 kW maximum power dissipation are available on the market. Depending on the type of application, diodes can be optimized for rectifier use or for fast recovery. A discussion of the basic theory has been given, including blocking junctions, on and off states, and switching characterstics. Advanced designs include different concepts to reduce the emitter efficiency and to control the carrier lifetime locally. Planar junction termination and semi-insulating passivation are new techniques, mainly utilized for chip diodes integrated in power modules. The authors believe that silicon carbide will yield a new quantum step in high-power device performance as soon as it is ready for economical use.

APPENDIX

Semiconductor in Thermal Equilibrium

Space-charge neutrality:

$$p - n + N_\mathrm{D} - N_\mathrm{A} = 0 \tag{A1}$$

p–n product:

$$p_0 n_0 = n_i^2 \tag{A2}$$

Majority-carrier concentration:

$$p_{p0} = N_A \qquad (N_A \gg n_i, N_D) \tag{A3}$$

$$n_{n0} = N_D \qquad (N_D \gg n_i, N_A) \tag{A4}$$

Minority-carrier concentration:

$$p_{n0} = \frac{n_i^2}{N_D} \qquad (N_D \gg n_i, N_A) \tag{A5}$$

$$n_{p0} = \frac{n_i^2}{N_A} \qquad (N_A \gg n_i, N_D) \tag{A6}$$

Basic Semiconductor Formulas

Transport equations:

$$j_p = q\mu_p pE - qD_p \frac{dp}{dx} \tag{A7}$$

$$j_n = q\mu_n nE + qD_n \frac{dn}{dx} \tag{A8}$$

$$j_p = -qD_p \frac{dp}{dx} \qquad \text{(low injection)} \tag{A9}$$

$$j_n = qD_n \frac{dn}{dx} \qquad \text{(low injection)} \tag{A10}$$

Continuity equations:

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial j_p}{\partial x} - \frac{p - p_0}{\tau_p} \tag{A11}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial j_n}{\partial x} - \frac{n - n_0}{\tau_n} \tag{A12}$$

Electric field:

$$\frac{dE}{dx} = \frac{q(p - n + N_D - N_A)}{\epsilon} \tag{A13}$$

Einstein's relationships:

$$D_p = \frac{kT}{q}\mu_p \tag{A14}$$

$$D_n = \frac{kT}{q}\mu_n \tag{A15}$$

Diffusion lengths:

$$L_p = \sqrt{D_p \tau_p} \tag{A16}$$

$$L_n = \sqrt{D_n \tau_n} \tag{A17}$$

Diffusion equations in steady state:

$$\frac{d^2 p_n}{dx^2} = \frac{p_n - p_{n0}}{L_p^2} \qquad \text{(low injection)} \tag{A18}$$

$$\frac{d^2 n_p}{dx^2} = \frac{n_p - n_{p0}}{L_n^2} \qquad \text{(low injection)} \tag{A19}$$

Charge control equations:

$$\frac{dQ}{dt} + \frac{Q}{\tau_p} = -[i_p(x_2) - i_p(x_1)] \tag{A20}$$

$$\frac{dQ}{dt} + \frac{Q}{\tau_n} = i_n(x_2) - i_n(x_1) \tag{A21}$$

Resistivity:

$$\rho = \frac{1}{q(\mu_p p + \mu_n n)} \tag{A22}$$

Basic Formulas for Abrupt *p–n* Junctions

Built in voltage:

$$V_d = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2} \tag{A23}$$

Maximum electric field:

$$E_{max} = \sqrt{\frac{2q}{\epsilon}\frac{N_A N_D}{N_A + N_D}}\sqrt{(V_d - V_a)} \tag{A24}$$

Depletion-layer width:

$$w = \sqrt{\frac{2\epsilon}{q}\frac{N_A + N_D}{N_A N_D}}\sqrt{(V_d - V_a)} \tag{A25}$$

Differential capacitance:

$$C_d = \sqrt{\frac{q\epsilon}{2}\frac{N_A N_D}{N_A + N_D}}\frac{1}{\sqrt{V_d - V_a}} \tag{A26}$$

Minority-carrier concentration:

$$p_n(w_n) = p_p(-w_p)e^{-q(V_d - V_a)/kT} \qquad \text{(under bias)} \tag{A27}$$

$$n_p(-w_p) = n_n(w_n)e^{-q(V_d - V_a)/kT} \qquad \text{(under bias)} \tag{A28}$$

General Constants

Electron charge	q	1.602×10^{-19}	$A \cdot s$
Boltzmann constant	k	1.380×10^{-23}	J/K
Permittivity in vacuum	ϵ_0	8.85×10^{-12}	$A \cdot s/V \cdot m$

Some Silicon Properties in Low Injection (Room Temperature)

Intrinsic carrier concentration	n_i	1.45×10^{10}	cm^{-3}
Dielectric constant	ϵ/ϵ_0	11.7	
Electron mobility	μ_n	1350	$cm^2/V \cdot s$
Hole mobility	μ_p	480	$cm^2/V \cdot s$
Electron diffusion coefficient	D_n	35	cm^2/s
Hole diffusion constant	D_p	12	cm^2/s

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DIODES, LIGHT EMITTING. See LIGHT EMITTING DIODES.

DIODES, SCHOTTKY OXIDE RAMP. See SCHOTTKY OXIDE RAMP DIODES.

DIODES, THIN FILMS. See THIN FILM DEVICES.