THYRISTORS FOR POWER ELECTRONICS

The gate turn-off (GTO) thyristor is a very high power semiconductor switch for use in industrial applications. As a member of the thyristor family, the GTO thyristor is basically a four-layer regenerative structure characterized by the ulti-

mate in voltage blocking and current carrying capabilities. The standard thyristor considered so far can only return from the forward conducting state to the forward blocking state when the current follow is reversed by the action of the external circuit which controls the load current. GTO thyristors are designed to turn off when a negative gate current is applied to the gate electrode. As a result, they make it possible, in power conversion applications, to eliminate forward commutation circuits, thereby significantly contributing to reduction of equipment size and weight, and enhancing the power conversion efficiency.

A thyristor with turn-off capability from the gate was first discussed by van Ligten and Navon (1), and Goldly et al. (2). The theoretical analysis for the gate turn-off phenomena was extended by Wolley (3) in 1966. Four years later brought publication of a report on a high power GTO thyristor with a handling capacity of 1000 V, 50 A (4). It was followed by a higher current device of 200 A in 1973 (5). The main subject in the development of the GTO thyristors has been attaining a higher maximum anode current to be interrupted without device failure. The maximum anode current depends on an interruptable current of the unit-segment and on a local increase in the current density during the gate turn-off phase. Through numerous efforts by numerical analysis of the design criteria and by experimental studies on how design parameters influence to the interruptable current, and also in the development of process technologies to attain uniform operation throughout the whole device, the maximum current has been gradually increased as the blocking voltage has risen. In 1981, high power GTO thyristors of current-voltage ratings of 2500 V, 600 A and 3000 V, 1000 A were developed (6,7), and the ratings now stand at 6000 V, 6000 A (8). Power GTO thyristors have been principally used in the motor speed control for traction and other industrial applications, but their uses are being extended to electric conversion systems, such as static var compensator (SVC) and high voltage direct current transmission (HVDC).

BASIC STRUCTURE OF GTO THYRISTOR

The basic segment structure of a GTO thyristor is shown in Fig. 1. It is similar in structure to a standard thyristor consisting of four p-n-p-n layers. The most important differences between the GTO thyristor and the standard thyristor are that the GTO thyristor has long, narrow emitter strings surrounded by gate electrodes. In a practical device, many segments are arrayed in a GTO thyristor pellet according to the device current carrying capability.

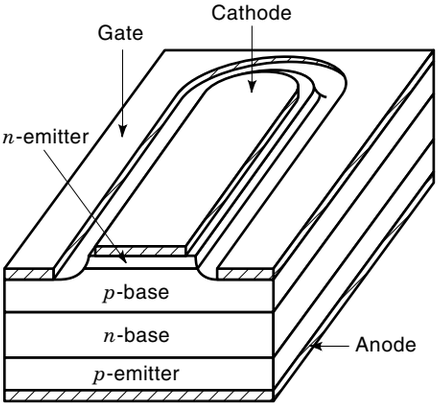

Figure 1. Schematic structure of the GTO segment. Its important difference from the standard thyristor is that the segment has long and narrow emitter strings surrounded by the gate electrode.

PRINCIPLE OF GTO THYRISTOR OPERATION

Turn-On

Refer to Fig. 2(a). The GTO thyristor's turn-on mechanism is analogous to that of a standard thyristor. A gate current is injected to the gate electrode across the cathode $n+$-emitter junction. The $n+$ layer emits electrons into the p-base layer, some of which reach the $n-$-base layer across the p-base layer. These electrons bias the anode $p+$-emitter in the forward direction, and lead to the emission of holes from the emitter into the $n-$-base layer, some of which then diffuse across the n-base layer and also reach to the p-base layer. When these holes enter the p-base layer, they have the same effect as the firstly applied gate current, that is, electrons are emitted from the $n+$-layer to the p-base layer, since the holes build up the emitter junction in deeper forward bias, and the process is reinforced. Once the current reaches the critical level of the latching current, at which the anode current flow is self-sustaining, the device can be held in conduction even if the gate current is removed.

On-State

Refer to Fig. 2(b). The on-state is maintained without any gate current in a principal manner, if the anode current is retained at a value much more than the critical level which is defined as holding current. The regenerative process usually injects a great number of electrons and holes from the emitter into the p- and n-base layers, which store these carriers. A conductivity modulation in both base layers produces the low on-state voltage for GTO thyristors.

Turn-Off

Refer to Fig. 2(c). The turn-off process in the GTO thyristor is initiated by a negative gate current. The stored holes in the p-base layer flow laterally to the negatively polarized gate electrodes until the whole $n+$-emitter junction is reverse biased. During this period, called the storage time, the anode current progressively forms filaments towards the middle of the emitter area due to the lateral resistance for the gate current. At the instance of a pinch-off of the filamentation, the anode current falls rapidly, and the p-emitter junction experiences current flow through the gate electrode with a gradual reduction, called the tail current, which corresponds to the stored carriers in the n-base layer. So the gate current must be able to sustain voltage until all the stored carriers are swept out from the base for a complete turn-off. The filamentation of current at the end of the storage period tends to increase the forward current density exponentially, hence power losses are generated in a small volume, and a snubber circuit can be used in order to manage the power losses by commutating the anode current into the snubber capacitor.

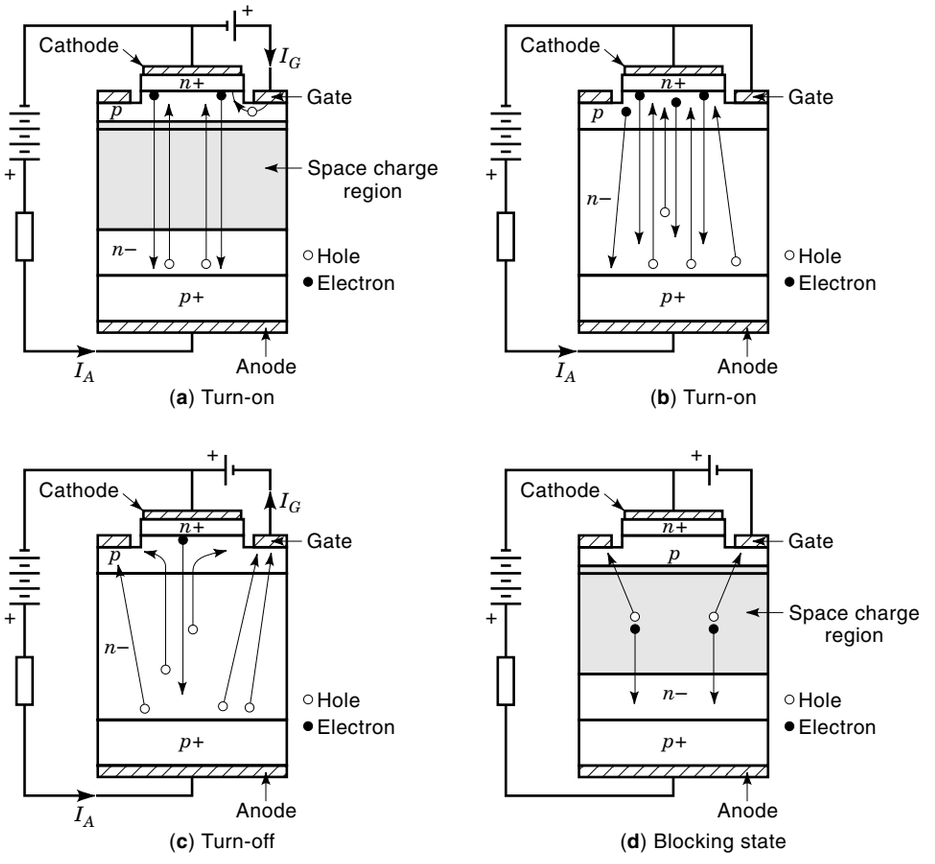

Figure 2. Switching processes and operating states in the GTO thyristor, which consists of (a) turn-on, (b) on-state, (c) turn-off, and (d) blocking state.

Blocking State

Refer to Fig. 2(d). During the blocking state, the GTO thyristor is almost free of mobile charge carriers. The externally applied blocking voltage generates a space charge region in both base layers. The space charge region extends mainly into the n-base layer and sustains the blocking voltage. During ordinary operation, a reverse bias is applied to the gate-cathode so as to maintain blocking capacity at a high temperature condition and maximize the dv/dt capability.

THEORY OF GATE TURN-OFF

A two-dimensional analytical model describing the turn-off for a GTO thyristor has been proposed by Wolley (3). The schematic for turn-off is depicted in Fig. 3(a). Initially, the device conducts the anode current I_A which is determined by the anode voltage V_A and the load resistance R_L. A negative gate voltage V_G applied to the gate by closing the switch in the gate lead will cause a negative gate current I_G to flow in a step function [Fig. 3(b)] which tends to reverse bias the cathode emitter. The anode current responses are shown in Fig. 3(c). For the duration of the storage time t_s, the anode current remains essentially constant, and the minority carrier electron-hole plasma is "squeezed" toward the center of the cathode emitter. For the duration of the fall time t_f, the plasma density is reduced by the gate current until the blocking junction becomes unsaturated and the device turns off.

The Turn-Off Velocity

In order to obtain a quantitative evaluation for the turn-off time and the maximum turn-off current, the velocity with which the plasma is squeezed laterally toward the center of the cathode should be determined. The net rate of removal of minority carriers from an elemental volume at the boundary x_b, between the "on" and "off" region is considered [Fig. 3(a)]. The removal of minority carriers at the boundary x_b is the gate current I_G minus the lateral electron diffusion current into the elemental volume, the magnitude of which is set by the slope $1/L_n$, where L_n is defined as an effective diffusion length. From the assumption of a constant gradient of the electron concentration in the "on" region, the turn-off velocity dx_b/dt is finally given by

$$\frac{dx_b}{dt} = \frac{D_n}{L_n} + \frac{x_b + L_n}{t_p(G_{\text{off}} - 1)} \tag{1}$$

where D_n is the diffusion coefficient, $t_p = W_{\text{PB}}^2/2D_n$, which is the transit time for carrier through the p-base, and G_{off} is the turn-off gain defined as I_A/I_G.

The Storage Time and Maximum Turn-Off Gain

The storage time t_s is essentially the time it takes to squeeze the electron-hole plasma from its original uniform flow through the entire unit-segment into a filament line of width L_n. Then Eq. (1) is integrated in x between emitter width X_E

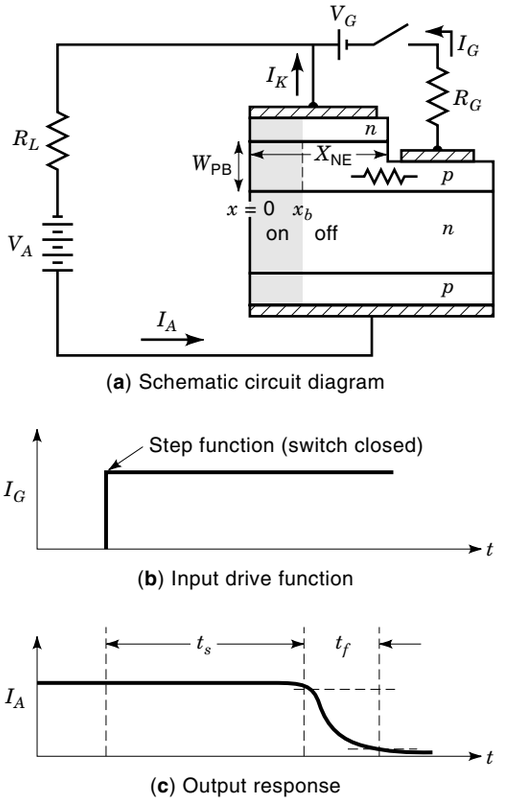

Figure 3. The schematic for turn-off of a GTO thyristor is depicted. The current conducting area is squeezed toward the center of the emitter by applying the negative gate current.

and L_n, which results in

$$t_s = t_p(G_{\text{off}} - 1)\ln\frac{(X_E L_n/W_{\text{PB}}^2) + (2L_n^2/W_{\text{PB}}^2) - G_{\text{off}} + 1}{(4L_n^2/W_{\text{PB}}^2) - G_{\text{off}} + 1} \quad (2)$$

The storage time t_s approaches infinity when the denominator of the logarithmic term in Eq. (2) goes to zero, that is, the maximum turn-off gain is given as follows:

$$G_{\text{off}}(\max) = \frac{4L_n^2}{W_{\text{PB}}^2} + 1 \quad (3)$$

Equation (3) can be used to calculate the storage time as a function of the turn-off gain. The results of such calculations are depicted in Fig. 4 using the lateral diffusion length as a parameter. The storage time is a strong function of the turn-off gain. It should be noted that this turn-off gain is set by the external gate input circuit and output circuit conditions [such as $V_G - R_G$ and $V_A - R_L$ in Fig. 3(a)] and is limited by the internal device impedance.

Maximum Turn-Off Current

The lateral gate current I_G during turn-off causes a voltage drop along the cathode emitter junction. This drop may reach the cathode-gate breakdown voltage as observed by van Ligten and Navon (1) and limit the interruptable current. For the device model of Fig. 3(a) the maximum lateral gate resistance is experienced when the "on" region is reduced to its minimum width of L_n. Thus, this lateral gate resistance beneath the width L_x of the cathode emitter is determined as

$$R_G = \rho_{\text{SPB}}(X_E - L_n) \quad (4)$$

where ρ_{SPB} is the sheet resistivity of the unmodulated, active gate region. Because of the restriction [see Fig. 3(c)]

$$I_G R_G < V_{\text{GK}} \quad (5)$$

where V_{GK} is the gate-cathode breakdown voltage, there exists an upper limit for the anode current that can be turned off. With the assumption that $X_E \gg L_n$ it then follows from Eqs. (3), (4), and (5), that

$$I_A(\max) = G_{\text{off}}\frac{V_{\text{GK}}}{\rho_{\text{SPB}} X_E} \quad (6)$$

The relation between I_A(max) and $\rho_{\text{SPB}}X_E$ in Eq. (6) has been confirmed experimentally by Azuma et al. (9) and other researchers.

CURRENT FILAMENTATION IN THE UNIT GTO THYRISTOR SEGMENT

The exact local carrier-density distribution during turn-off operation of the GTO thyristor has been investigated by Lundqvist et al. (10). Some typical results are shown in Fig. 5(b) for

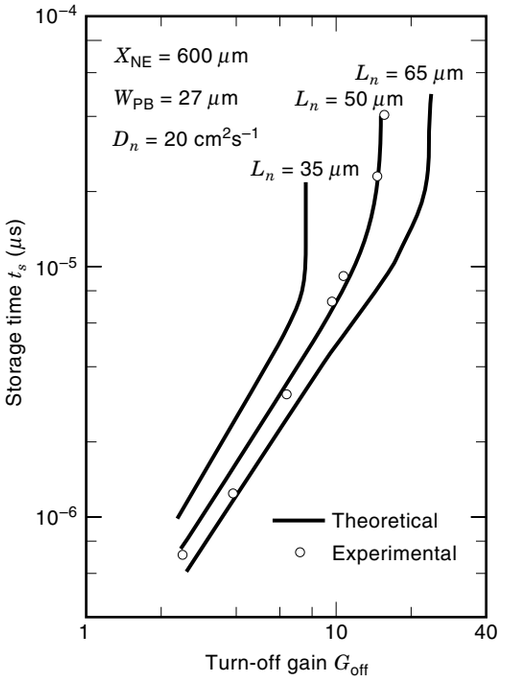

Figure 4. Storage time vs. turn-off gain (3). The storage time is a strong function of the turn-off gain.

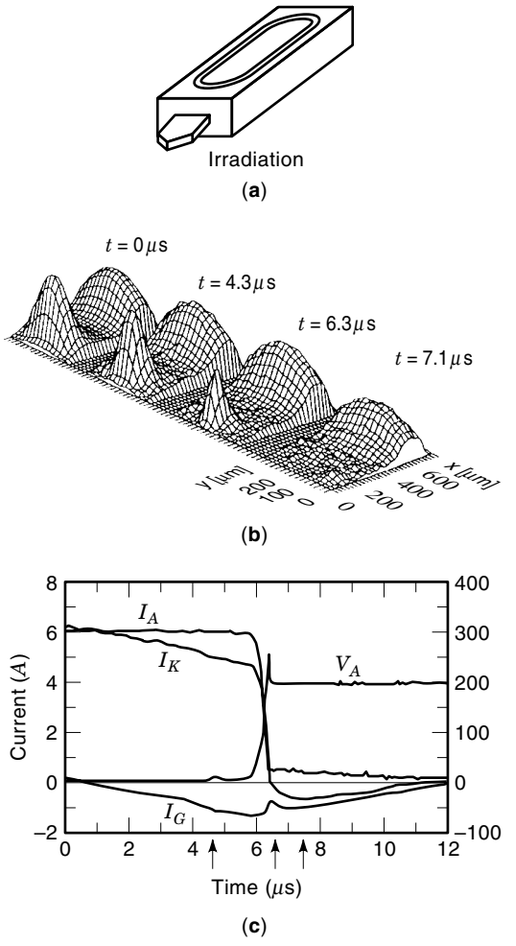

Figure 5. Carrier redistribution in turn-off operation (10). The lateral plasma squeezes along the cathode-emitter width in the storage time period of the turn-off cycle.

the sample construction under investigation [Fig. 5(a)]. The corresponding electrical characteristics are given in Fig. 5(c), where the instants of the carrier-distribution maps are marked. Figure 5(b) is measured by the detection of recombination radiation emitted from the surface defined by the cathode-width direction [XY-plane in Fig. 5(a)]. The data show tendencies of monotomic lateral plasma squeezing in the storage time period of the turn-off cycle. The conduction region squeezes along the cathode-length direction [YZ-plane in Fig. 5(a)] in the fall time period have been investigated by Azuma et al. (11) by using a similar infrared observation method of the measurement. Squeezing in both directions proceeds further, to the final stage in the turn-off process, to form a single filamentational spot approximately corresponding to the diffusion length of the minority carrier in the *p*-base. These results explain the exact turn-off phenomena, which were studied analytically by Wolley (3) with the two-dimensional model described in the previous section.

TURN-OFF FAILURE MODES OF GTO THYRISTORS

The turn-off failure mechanism in GTO thyristors has been the subject of several experimental (12–14) and simulation studies (15,16). While the understanding of the failure mechanism is still unsatisfactory, the two basic failure modes of the GTO thyristor were successfully modeled by Bakowski and Gustafsson (17) in 1995 using two-dimensional simulations. The numerical analysis includes self-heating, impact ionization, and realistic representation of the external circuits. The two basic failure modes are the thermal runaway mode (mode 1 failure) due to stress inflected by the snubber leak inductance and the local dynamic avalanche mode (mode 2 failure) due to the excessive tail current. The immediate cause of the failure in both cases is the local retriggering of the cathode emitter junction occurring in one single segment of the device.

Failure Mode 1

The failure mode 1 induced by the snubber leak inductance and the inductive V_{DSP} peak voltage is shown in Fig. 6 with both measured and simulated I and V waveforms. Figure 6 illustrates the impact ionization and temperature at point d, where the point d corresponds to the times in the simulated waveforms. The maxima of impact ionization and temperature distribution are located at the center portion of the seg-

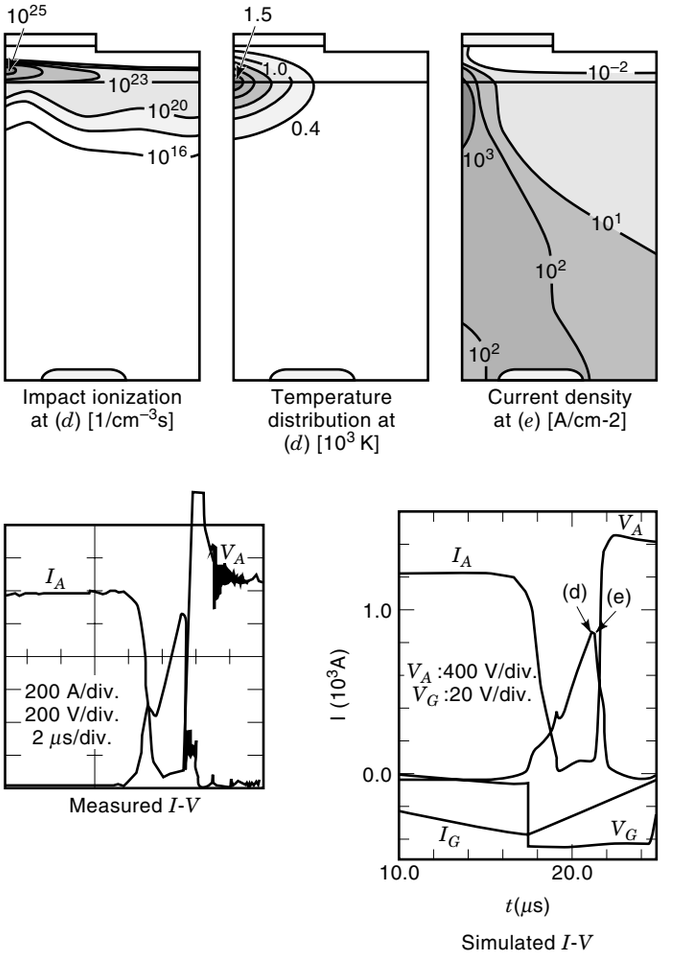

Figure 6. Failure mode 1: the thermal run-away mode (17). The maximum of impact ionization and temperature distribution are located at the center portion of the emitter. This failure is due to current filamentation during the fall period.

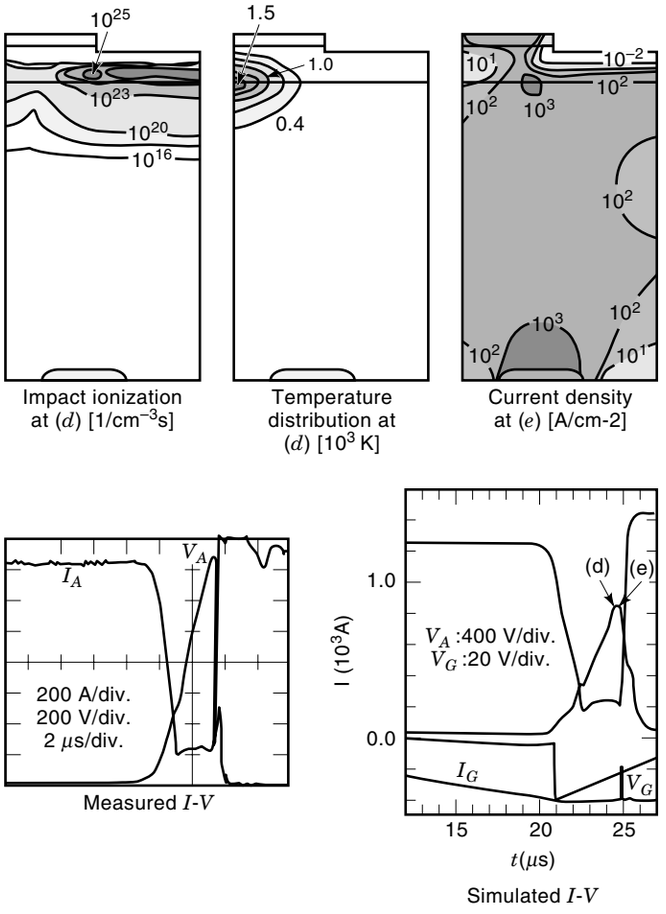

Figure 7. Failure mode 2: the local dynamic avalanche failure (17). The maximum of the impact ionization is shifted toward the emitter periphery. This failure is due to the local dynamic avalanche.

ment. Local retriggering also occurs at the center, and the thermal generation of carriers, further enhanced by the impact ionization, causes the retriggering. From these results, it can be confirmed that this failure mode is due to the excessive current in the current filament formed during the fall time period. Uncontrollable current generation is the result of the device entering the thermal runaway mode because of stress inflected by the inductive anode voltage peak V_{DSP}.

Failure Mode 2

Failure mode 2 is often observed in actual cases and is due to the excessive tail current normally caused by too high a lifetime in the device. This is demonstrated in Fig. 7 with the turn-off waveforms. The maximum of the temperature distribution is at the center of the segment. On the other hand the maximum of the impact ionization is shifted toward the periphery of the emitter junction. Local retriggering occurs off-center of the segment due to screening of the *p*-base potential by the avalanche generated charge. Consequently, the impact generation of carriers at the periphery of the emitter junction is the cause of the retriggering. From these results, it can be confirmed that mode 2 failure is due to the local dynamic avalanche taking place off-center of the segment. The electric field generated by mobile hole doping is greater in the gate region of the segment due to the absence of the compensating electrons which are still present at the center portion of the segment.

SAFE OPERATING AREA (SOA) OF GTO THYRISTOR

The safe operating area (SOA) curve of the GTO thristor segments can be depicted schematically in Fig. 8. Retriggering of the device does not occur if the current-voltage locus exist in the SOA during gate turn-off operation. This can be separated into three distinct regions: (1) the maximum permissible anode current due to thermal power dissipation limitations, (2) the sustain voltage V_C limitation, which is given essentially by the SOA of the *npn* transistor section driven by holes injected from the *p*-emitter, and (3) the dynamic avalanche limitation at the tail current region which is given by the SOA of the *pnp* transistor section. It has been found that the V_C values increase monotonically with increasing the *n*-base thickness and also with reducing the *p*-base resistivity by Azuma et al. (11), and by Bakowski and Gustafsson (17), the latter as simulation studies. Satou et al. (13) predicted that when approaching the SOA limit the current density in the cylindrical filament spot is about 30 kA/cm^2.

ANODE EMITTER SHORTING

The importance of a higher turn-off gain for a larger interruptable current I_{TQRM} has been discussed in the previous section [Eq. (6)]. The turn-off gain G_{off} is given in the following:

$$G_{\text{off}} = \frac{I_A}{I_G} = \frac{\alpha_{npn}}{\alpha_{npn} + \alpha_{pnp} - 1} \tag{7}$$

where α_{npn} and α_{pnp} are common base current gains of the *n*-*p*-*n* and *p*-*n*-*p* transistors, respectively, which makes up the GTO thyristor. It is shown here that the *p*-*n*-*p* transistor current gain α_{pnp} must be low in order to arrive at a high turn-off gain. In the GTO thyristor this low α_{pnp} can be achieved in two ways: (1) the minority carrier lifetime in the *n*-base can be reduced by introducing recombination centers using gold diffusion and/or electron irradiation technologies, and (2) the

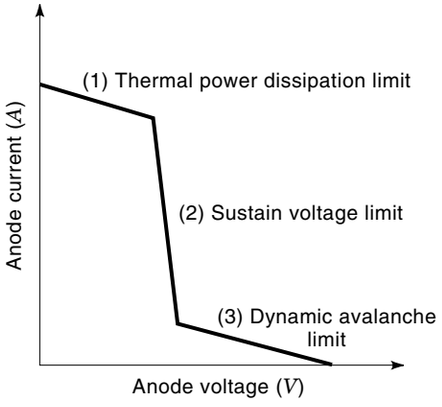

Figure 8. Safe operating area for a GTO thyristor. Retriggering does not occur if the current-voltage locus is in the SOA.

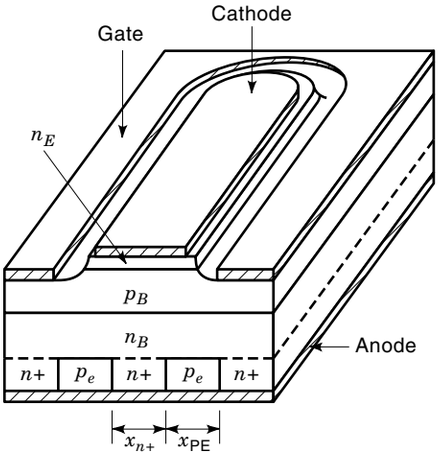

Figure 9. Schematic segment structure with anode emitter shorting. The anode shorting can reduce the carrier concentration in the n-base in the current conducting state and can sweep out carriers during the turn-off phase.

anode emitter shorting as depicted in Fig. 9. An effective gain α_{pnp} (effective) can be defined for the p-n-p transistor section as follows:

$$\alpha_{pnp}(\text{effective}) = \alpha_{pnp}\frac{I_A - I_S}{I_A} \tag{8}$$

where I_A is the anode current, I_S is the electron current flowing in the shorting area which is given as $V_{PE}R_S$ (R_S: short resistance and V_{PE}: emitter junction voltage). The anode shorting can reduce the carrier concentration in the n-base at the current conducting state, and also have an effect of sweeping out carriers during the turn-off phase, which is similar to a reduction of carrier lifetime. The advantages of anode shorting are that compared to minority carrier lifetime control it results in good tradeoff between the on-state voltage and the turn-off losses, and in good voltage blocking characteristics with a low leakage current at high temperature. Hence, the technique of anode shorting is favored for higher voltage and larger area GTO thyristors.

The relationships between turn-off characteristics, on-state voltage, and the structural parameters of emitter shorting have been investigated by using a group of small-size test samples by Yatsuo et al. (18). Figure 10 shows anode currents

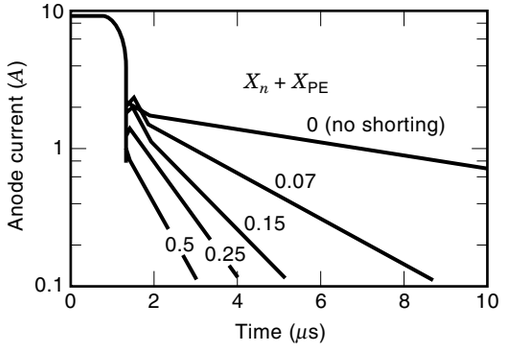

Figure 10. Anode currents as a function of time in a tail period for various emitter shorting factors (18). The anode shorting has a similar effect on reduction of carrier lifetime.

as a function of time at a late stage of the gate turn-off for various shorting structures. In the tailing part of the anode current, I_A decays linearly in the semilogarithm plots, and can be expressed as $I_A \sim \ln(-R_S t)$, where R_S represents shorting resistance which decreases with an increase in X_{n+}/X_{PE}, and X_{n+} and X_{PE} are defined as the shorting and p-emitter widths, respectively. It is understood that p-emitter shorting has a similar effect on the carrier decay in the n-base to that of a lifetime reduction by doping with a lifetime killer such as gold.

SEGMENT ARRANGEMENT IN GTO THYRISTORS

In general, large current GTO thyristors have a multiemitter structure consisting of hundreds or thousands of unit-GTO segments corresponding to their current carrying capability. However, it has been found that the maximum interruptable current rating of such GTOs does not increase in proportion to the number of segments, unless uniform operation is being realized among many unit-GTO segments during the turn-off operation. Typically, the current appears to be evenly distributed in the on-state, but during turn-off, some segments of the device will turn-off first, leaving the remaining segments with an increased proportion of the total anode current. This behavior was investigated first by New et al. (4) in 1970, and several experimental and simulation studies followed published (19–21). An important design point regarding large-current GTO thyristors is the prevention of current crowding.

Figure 11 shows a photo of several common surface arrangements of high-power GTO thyristors, in which the emit-

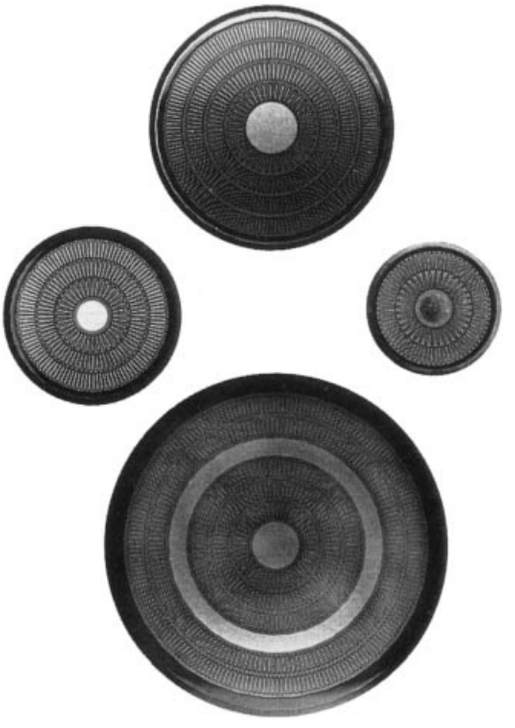

Figure 11. Typical GTO thyristor basic segment arrays (19), with a multi-emitter structure corresponding to the current carrying capability. An important design point for large current GTO thyristors is how to prevent current crowding during turn-off operation.

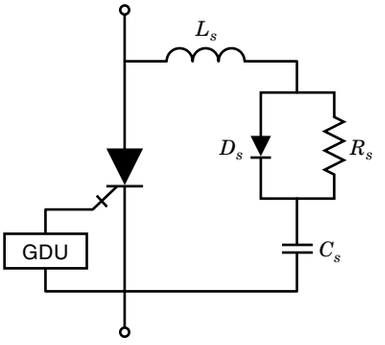

Figure 12. GTO thyristor with snubber and gate drive unit (GDU). Actual snubber circuits have stray inductance *Ls* in the wiring, which gives a high spike voltage due to the *LsdI*/*dt* effects.

ter consists of an array of individual segments arranged in concentric rings. A reliable contact system would typically be similar to that shown in Fig. 9 where the cathode emitters are raised above the gate regions and the cathode contact is made using a pressure plate. The common gate contact can be in the center of the device, or in a ring. When there is no uniformity for steady on-state currents, turn-off of a large current unit-GTO segment is slower than that for other segments in the same pellet so that current crowding occurs. Even if the steady on-state currents are uniform between whole segments in the device, gate operation for the unit-GTO segments at some distance from the gate contact is also slow due to the impedance of the gate electrode, so that their turn-off is accompanied by current crowding.

Current crowding also occurs because of the complex relationship between the steady on-state current and gate operation. Therefore it is important to optimize the gate structure for distribution of the steady on-state current. For the device with a radial segment array such as in Fig. 11, current crowding during turn-off operation has been investigated by a special measurement method of current distribution and by a computer simulation technique by Yatsuo et al. (20). According to these investigations and those of others, the ring-shaped gate structures are conventionally applied to a large diameter and large current GTO thyristors such as the maximum interruptable current of 6000 A (8).

TURN-OFF CHARACTERISTICS OF GTO THYRISTORS

In actual applications of GTO thyristors attention must be directed towards the influence of the external circuits on the GTO thyristor behavior. A GTO thyristor in a typical circuit arrangement of a gate drive unit and a snubber circuit is shown in Fig. 12. The effective functions of the snubber circuit are considered in detail in the next section on snubber circuits. In Fig. 13, typical GTO thristor anode circuit current and voltage waveforms (upper traces), and gate circuit waveforms (lower traces) are illustrated with corresponding parameter definitions. In the turn-off periods, there are three time domains to be distinguished: (1) the storage time t_S during which the stored carriers are removed from under the cathode emitters but the load current is kept up by the load inductance L; (2) the fall time t_f where the anode current drops quickly to the tail current, and the anode voltage rises rapidly with the spike voltage, V_{DSP}, which is induced in the snubber circuit due to a voltage drop in the diode D_S and capacitance C_S, and due to stray inductance L in their wiring; and (3) the tail time t_{tail} where the remaining carriers are removed through recombination across the anode emitter shorts. These are influences of the external circuits such as the snubber circuits and of the gate drive condition, as well as the device's own characteristics.

SNUBBER CIRCUITS

During turn-off the rapid fall of the anode current is accompanied by a fast rise in anode voltage. If the rising rate of the

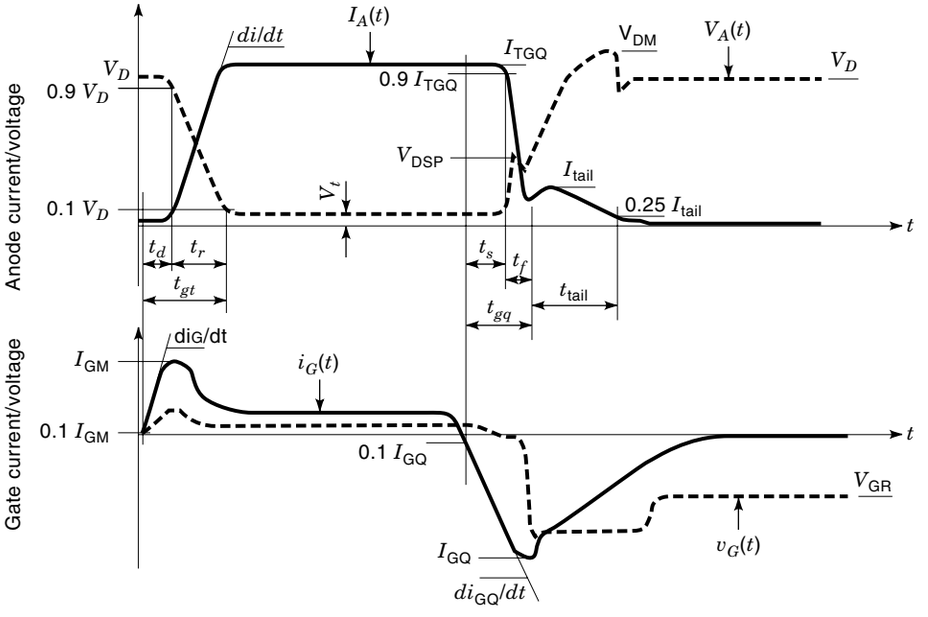

Figure 13. Current and voltage waveforms and parameter definitions for GTO thyristors.

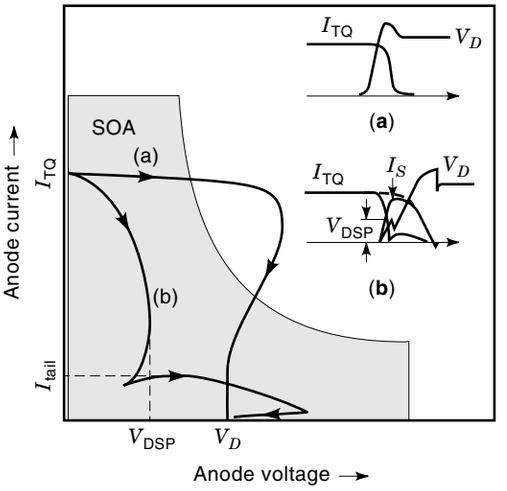

Figure 14. Turn-off locus and SOA of GTO thyristor. The current-voltage locus can be suppressed in the SOA due to the effect of the snubber circuit, unlike the case without the snubber circuit.

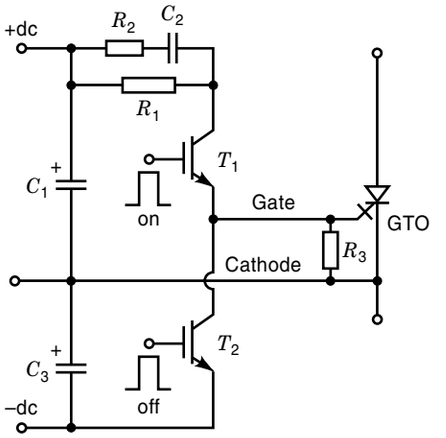

Figure 15. A typical gate drive circuit for turn-on and turn-off of the GTO thyristor.

anode voltage is too high then it can cause the GTO thyristor to retrigger, and cause possible device destruction in association with exceeding the limits of the SOA. In practical circuits the rising voltage is limited by a snubber circuit. Figure 14 illustrates the effect of the snubber circuit on the turn-off criteria of the GTO thyristor, in which each anode current-voltage locus for the cases with and without a snubber circuit are drawn, as well as the device SOA. From the current-voltage waveforms, it can be seen that during the fall period the load current is essentially diverted into the snubber as charging current for the snubber capacitance C_S (b); this prevents a rapid cut off of the load current and therefore prevents a rapid dV/dt condition. Due to this effect of the snubber circuit, its current-voltage locus (b) can be suppressed in the SOA, unlike the case without the snubber circuit (a). Real snubber circuits, however, have stray inductance L_S in their wiring and also the capacitance C_S, which gives a high spike voltage due to the $L_S dI/dt$ effect. Therefore the stray inductance in the GTO thyristor, R_S, C_S, and D_S loops must be minimized. To achieve this, C_S must have a low internal inductance and the snubber components must be mounted as close to the GTO thyristors as possible. Larger snubber capacitance's are commonly accompanied by higher snubber losses, so it is very important in the device design to increase the maximum interruptable current while keeping the snubber capacitance as small as possible.

GATE DRIVER FOR GTO THYRISTORS

The gate driver circuit provides gate pulses which turn on or turn off the GTO thyristor in response to a control signal given from the system controller. Figure 15 shows a typical gate drive circuit. In this figure, C_1, C_2, R_1, R_2, and T_1 form the positive gate current for turn-on, and C_3, R_3, and T_2 constitute the turn-off channel which provides negative gate voltage during the blocking state of the GTO thyristor. At the initiation of turn-on, high power gate pulses must be supplied to the device in order to ensure a large initial turn-on area, so as to reduce the turn-on losses and turn-on time. Continuous supply of the turn-on gate pulse is not required in principle during the on-state, because the GTO thyristor is a latch-type device, but a positive gate current should be supplied in following the initial gate pulse, so as to ensure anode current flows in the on-state. In Fig. 15, R_1 determines amplitude of the continuous gate current, whereas R_2 and C_2 shape the initial gate pulse (I_{GM} in Fig. 13). At the initiation of turn-off, high power turn-off gate pulses, which have a very short rise time and high peak value, must be given to individual devices so as to reduce the storage time and also the turn-off losses. Higher power gate pulses make the number of stored carriers drop rapidly and allow voltage blocking capability of the GTO thyristors to be recovered. Continuous supply of turn-off gate pulses is not required after a complete turn-off process in principle, however, the gates are sometimes biased in the negative voltage direction during the off-state period in order to ensure the voltage blocking capability against noise signals.

The gate drive has a strong influence on the performance of GTO thyristors in turn-off operation. Figure 16 shows examples of the storage time t_S and peak turn-off gate current I_{GQM} versus negative gate current rise rate di_{GQ}/dt curves for

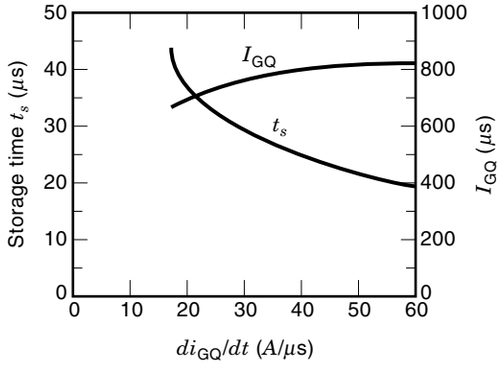

Figure 16. Storage time and peak turn-off gate current vs. negative gate current rise rate. The storage time increases with a lower rate of negative gate current rise, so it is important to keep dig/dt over the critical value in order to ensure safe turn-off operation.

Table 1. Example Set of the Main Characteristics of a 4500 V-4000 A GTO Thyristor

Parameter	Symbol	Units	Values	Main Measurement Conditions
Repetitive peak off-state voltage	V_{DRM}	V	4500	V_{RG} = 5 V
Controllable on-state current	I_{TQRM}	A	4000	V_D = 0.5 V_{DRM}, C_S = 6 μF, L_S = 0.2 μH
RMS on-state current	$I_{T(RMS)}$	A	1600	
Surge on-state current	I_{TSM}	kA	34	1 ms conduction, 1/2 sine
Rate of rise of on-state current	di/dt	A/μs	500	V_D = 2500 V, I_{TM} = 4000 A,
Rate of rise of off-state voltage	dv_D/dt	V/μs	1000	V_D = 0.5 V_{DRM}, V_{GR} = 5 V
Peak on-state voltage	V_{TM}	V	5.0	I_{TM} = 4000 A,
Peak off-state current	I_{DRM}	mA	120	V_D = V_{DRM}, V_{GR} = 5 V
Turn-on time	t_{gt}	μs	10 max.	V_D = 0.5 V_{DRM}, I_{TM} = 4000 A, C_S = 6 μF
Storage time	t_S	μs	27 typ.	V_D = 0.5 V_{DRM}, I_{TM} = 4000 A, C_S = 6 μF,
Turn-off time	t_{gq}	μs	40 max.	di_g/dt = 40 A/μs
Max. junction temperature	T_{jmax}	°C	125	

a 3000 A GTO thyristor. The storage time decreases much more with high di_{GQ}/dt than the peak turn-off gate current increases. It is very necessary to avoid di_{GQ}/dt values below 20 A/μs for these GTO thyristors in order to ensure safe turn-off. For the series connection, which is usually applied to high voltage power converters such as power transmission equipment, a uniform gate turn-off for all GTO thyristors is required. When some of the GTO thyristors are advanced in turn-off, they must be exposed to the total applied voltage of the converter valve. Hence it is important to select the GTO thyristors which have uniform turn-off characteristics, and also to control the timing of the turn-off gate pulse to accomplish simultaneous turn-off of all devices connected in series. Suitable snubber circuits also must be provided to mitigate the effect of imbalance of these characteristics.

RATINGS OF GTO THYRISTORS

The highest ratings of GTO thyristors reported to date are 4500 and 6000 V devices with a 4000 and 6000 A turn-off capabilities. Table 1 shows representative characteristics for the 4500 V 4000 A GTO thyristor. It should be noted that each characteristic is very strongly influenced by the measurement conditions. For example, the storage time t_s and the turn-off time t_{gq} increase with decreasing di_g/dt, as described in the previous section, and they are influenced by the waveforms of the turn-off gate currents. Since these switching characteristics strongly depend on the operating temperature, their maximum values at the maximum junction temperature are commonly shown in the device's rating charts.

REVERSE CONDUCTING GTO THYRISTORS

GTO thyristors are commonly used with an antiparallel connecting rectifier diode for freewheeling operation in inverter or chopper applications. Much effort was made in development of monolithic reverse conducting GTO thyristors (RC-GTO thyristors) (22). The RC-GTO thyristor has many advantages including reduction of not only the size and weight of the equipment, but also reduction of stray inductance in the wiring. To realize that device, two problems had to be solved: (1) isolation between the thyristor and diode, that is, since both the GTO thyristor and diode share a common blocking junction, gate current can flow through the common p-base into the anode of the diode, unless precautions are taken to prevent this; (2) there are relatively high forward voltage drops of the diode, because the n-base thickness of most GTO thyristors is much thicker than comparably rated diodes and the design of the diode section is far from ideal. Figure 17 is a cross-sectional view of the developed RC-GTO thyristor, and Fig. 18 is a pellet top view (23). For the first problem, an unique isolation structure was employed, in which a groove can be etched into the p-base to introduce impedance between the GTO thyristor p-base and the diode. For the second prob-

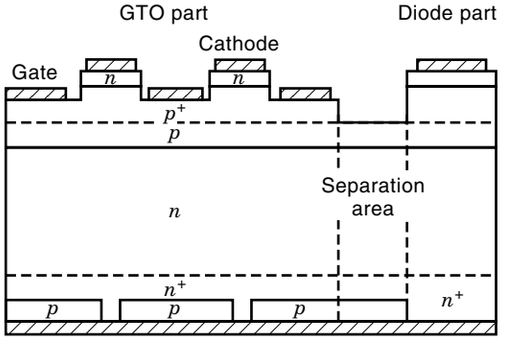

Figure 17. A cross-sectional view of the reverse conducting GTO thyristor (23). A groove can be etched into the p-base for the electrical isolation between the GTO thyristor and the diode regions.

Figure 18. A top view of the reverse conducting GTO thyristor (4500 V, 3000 A) (23). The diode is located at the periphery of the device.

lem, a $n+$-buffer layer which is laid between the n-base and p-emitter is applied in order to reduce the effective base thickness. At present, many high power rated RC-GTO thyristors are available for commercial use.

PUNCH-THROUGH (*pnipn*) TYPE GTO THYRISTORS

In order to improve the performance of GTO thyristors, especially in the tradeoff relationship between the turn-off losses and the on-state voltage, punch-through type GTO thyristors have been developed. They have an $n+$-buffer layer between n-base and p-emitter as shown in Fig. 19, which has already been used in other kinds of power devices such as IGBTs and reverse conducting thyristors (RCTs). For the buffer layer design, the resistivity of the n-base can be increased, so that the device can block a given voltage at reduced n-base thickness, and the on-state voltage is reduced correspondingly. To apply this structure in the GTO thyristor with anode shorting, the anode shorting ratio is very important for turn-off trigger gain and turn-on switching characteristics. The shorting resistance will be reduced to an extremely low value by the $n+$-buffer layer and it results in the triggering gate current becoming too large. Another important design point is how to decrease the spike voltage V_{DSP} at the fall time period, because the thinner base thickness will be generally accompanied by a lower sustain voltage V_c as discussed in the SOA section, which leads to reduced turn-off capability. Proton irradiation technology was used to reduce the V_{DSP}, which strongly depends on carrier distribution in the n-base layer during the current conducting state. The carrier distribution can be controlled within a small area of the base layer permeated depth using proton irradiation. From experimental studies on a proper anode short structure to reduce the V_{DSP}, and a high voltage large current punch-through type GTO thyristor was developed in 1995 (8). Figure 20 shows its turn-off waveforms. A very small tail current can be achieved and the turn-off loss is significantly reduced due to the punch-through effect in the n-base layer.

HARD DRIVE OPERATION OF GTO THYRISTORS

Conventionally, GTO thyristors are driven with a large protective snubber capacitance due to the limitation of their narrow SOA. However, the use of such a snubber capacitance leads to several problems, the most obvious being the large power losses and operational frequency limitations due to the time constants of the snubber circuits. These problems have

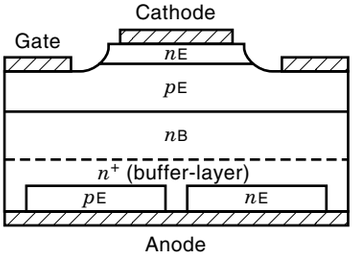

Figure 19. A cross-section of the segment structure with $n+$-buffer layer. It can block a given voltage at reduced n-base thickness.

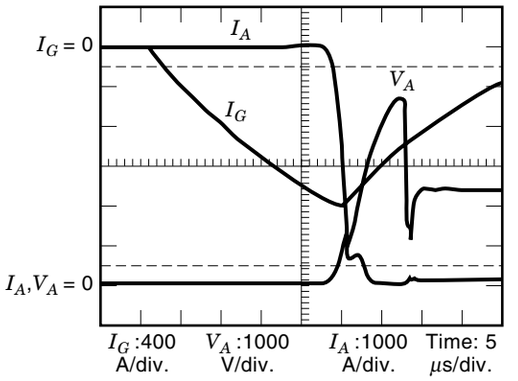

Figure 20. Typical waveforms during turn-off for the punch-through type GTO thyristor (8). A very small tail current can be achieved and turn-off loss is significantly reduced due to the punch-through effect in the n-base layer.

provided an incentive to develop ways of using a GTO thyristor without a snubber. One approach focused on optimizing device structural parameters and its fabrication processes to get uniform turn-off operation in the GTO segment and also in all segments of the device (24). Other approaches have centered on the gate driver circuit for SOA improvements. Wirth (25) proposed a drive technique in which GTO thyristors could be operated at currents well beyond the rated I_{TQRM} without turn-off snubbers by use of a gate drive circuit, that was capable of very high rates of reverse gate current, so as to ensure a turn-off gain of much less than one. A fundamental difference exists between a conventional gate drive and the proposed gate drive in the turn-off process. In the latter case, the entire anode current is commutated from cathode emitter to the gate in a very short time while holding the *p-n-p* transistor part of the thyristor in a saturated state. Since the *n-p-n* transistor part is completely inactive thereafter, the *p-n-p* transistor is deprived of a base-current, and then turns off. Then the current crowding problems inherent in the conventional gate drive process can be eliminated completely and a square SOA can be achieved.

However, there was one obstacle to the realization of the hard gate drive technique to high power GTO thristor applications; an extremely high voltage is induced between the cathode and gate electrode in the device by applying such a high dI_G/dt gate current due to the gate-circuit inductance. In order to reduce the induced voltage to less than the cathode emitter's breakdown voltage of about 20 V, the gate-circuit inductance has to be reduced significantly, as well as the internal inductance existing in the gate to cathode contacts of the device. In 1996, Grüning et al. (26) developed a new type GTO thyristor and gate circuit to overcome this problem. They used a special flat-band gate-cable, a low impedance multilayer printed circuit board, and a special coaxial housing structure, to get a reduction to less than a 5 nH overall gate circuit inductance. These techniques were used to get the first hard drive for a 3 kA 4.5 kV GTO thyristor. Figure 21 shows a photo of the low inductance gate driver with the coaxial GTO thyristor. Comparisons of its characteristics with those of a conventional type GTO thyristor and gate drive are made in Table 2. The characteristics of samples marked HD- are for the hard gate drives, and samples with T- are for the GTO

Table 2. Comparison of Conventional Drive and Hard Drive of GTO Thyristor (26)

3 kA, 4.5 kV, 125°C	Conv. GTO	HD-GTO	T-GTO	HD-TGTO
	(Typical values, not spec limited values)			
On-state voltage V_{TM}	3.2 V	3.2 V	1.9 V	1.9 V
Turn-off energy E_{off}	10 Ws at 6 μF	13 Ws at 0 μF	3.8 Ws at 6 μF	10 Ws at 6 μF
Turn-on energy E_{on} [d]	5 Ws at 500 A/μs	1 Ws at 3000 A/μs	0.2 Ws at 500 A/μs	0.5 Ws at 3000 A/μs
Snubber require C_s	3 to 6 μF	0 to 3 μF	3 to 6 μF	0 to 3 μF
RMS current I_{rms} at T_C = 85°C	1800 A	1800 A	2400 A	2400 A
On-state loss at 1 kA dc	2300 W	2300 W	1500 W	1500 W
Peak turn-off current I_{TGQ}	3 kA	3 to 6 kA	3 kA	3 to 6 kA
Gate drive power at I_{ft} = 500Hz, 1150 A_{rms} [c]	80 W	30 W	30 W	15 W
Max turn-off dv/dt	1000 V/μs[a]	3500 V/μs[b]	1000 V/μs[a]	3000 V/μs[b]
I_{gt} at 25°C	3 A	3 A	0.3 A	0.3 A
Gate stored charge Q_{gq}	8000 μC	2000 μC	8000 μC	2000 μC

[a] rating [b] characteristic [c] PWM operation in H-bridge, output frequency f = 50 Hz [d] I_{GM} = 50 A, @50 A/μs for standard drive, I_{GM} = 1000A, @1000 A/μs for hard drive

thyristor which has a punch-through and a special p-emitter structure (called a "Transparent Emitter") (27). The on-state loss of the T-GTO, thanks to its thinner base and buffer layer, is 40% lower than that of a standard GTO. With the snubber the turn-off loss it is 2.5 times lower. Additional advantages are a dramatic reduction of storage time to less than 2 μs, and a reduction in fall time to around 1 μs. Thus, the series connection of GTO thyristors is facilitated by the very low dispersion associated with these times.

The GCT thyristor (gate commutated turn-off thyristor), which is a new type of GTO thyristor related to the same concept of the hard-drive GTO thyristor, has been developed by Satou et al. (28), and already used practically in a back-to-back converter with a high power of 100 MW. Furthermore, the applications of GCT thyristors were investigated designs of much higher power systems such as 1,500 MW (29).

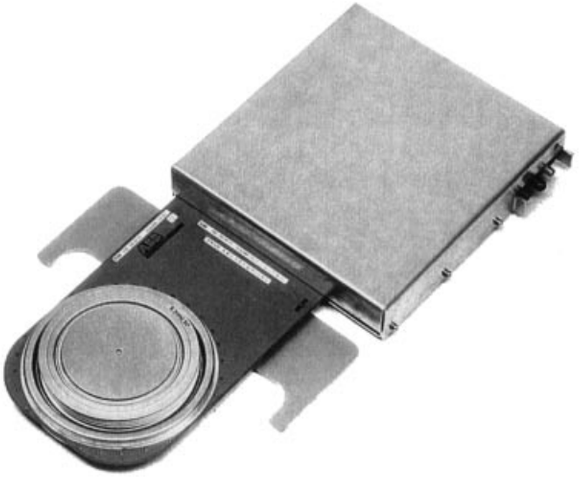

Figure 21. A low inductance gate driver with coaxial GTO thyristor (26). A low impedance multilayer printed circuit board and a special coaxial housing structure are used to get a reduction to less than a 5 nH overall gate circuit inductance.

BIBLIOGRAPHY

1. R. H. van Ligten and D. Navon, Base turn-off on *pnpn* switches, *IRE WESCON Convention Record,* Part 3 on Electron Devices, 1960, pp. 49–52.
2. J. M. Goldey, I. M. Mackintosh, and I. M. Ross, Turn-off gain in *pnpn* triodes, *Solid-State Electron,* **3**: 119–122, 1961.
3. E. D. Wolley, Gate turn-off in *p-n-p-n* devices, *IEEE Trans. Electron Devices,* **ED-13**: 590–597, 1966.
4. T. C. New et al., High power gate-controlled switch, *IEEE Trans. Electron Devices,* **ED-17**: 706–710, 1970.
5. E. D. Wolley et al., Characteristics of a 200-amp gate turn-off thyristor, *IEEE Conf. Record, Industrial Applications Soc. Meeting,* 251–255, 1973.
6. M. Azuma, M. Kurata, and K. Takigami, 2500-V 600-A gate turn-off thyristor (GTO), *IEEE Trans. Electron Devices,* **ED-29**: 270–274, 1981.
7. T. Nagano, T. Yatsuo, and M. Okamura, Characteristics of a 3000V, 1000A gate turn-off thyristor, *IEEE Conf. Record, Industrial Applications Soc. Meeting,* 750–753, 1981.
8. T. Nakagawa et al., A new high power low loss GTO, *Proc. Int. Sympo. on Power Semiconductor Devices,* 84–88, 1995.
9. M. Azuma, A. Nakagawa, and K. Takigami, High power gate turn-off thyristors, *Japan, J. Appl. Phys.,* **17-1**: 275–281, 1978.
10. M. Lundqvist, H. Bleichner, and E. Nordiander, An optical system for bilateral recombination-radiation diagnostics of the carrier redistribution in switching power devices, *IEEE Trans. Instrum. Meas.,* **40**: 956–961, 1991.
11. M. Azuma, M. Kurata, and H. Ohashi, Design considerations for high power GTO's, *Japan. J. Appl. Phys.,* **20-1**: 93–98, 1981.
12. H. Ohashi and A. Nakagawa, A study on GTO turn-off failure mechanism, *IEEE Int. Electron Device Meeting, Tech. Digest,* 414–417, 1981.
13. Y. Satou, T. Yatsuo, and S. Sakurada, A new buried-gate GTO structure having a large safe operating area, *IEEE Trans. Electron Devices,* **ED-37**: 2034–2038, 1990.
14. H. Bleichner et al., Measurements of failure phenomena in inductively loaded multi-cathode GTO thyristors, *IEEE Trans. Electron Devices,* **ED-41**: 251–257, 1994.
15. A. Nakagawa, A time- and temperature-dependent two-dimensional simulation of GTO turn-off process II-inductive load case, *Solid-State Electronics,* **28**: 677–687, 1985.

16. I. Omura and A. Nakagawa, 4.5kV GTO turn-off failure analysis under an inductive load including snubber, gate circuit and various parastics, *Proc. Int. Symp. on Power Semiconductor Devices,* 112–117, 1992.
17. M. Bakowski and U. Gustafsson, The two basic failure modes in the GTO modeling and experiment, *Proc. 1995 Int. Symp. on Power Semiconductor Devices,* 354–368, 1995.
18. T. Yatsuo et al., Ultrahigh-voltage high-current gate turn-off thyristors, *IEEE Trans. Electron Devices,* **ED-31**: 1681–1686, 1984.
19. P. D. Taylor, W. J. Findlay, and R. T. Denyer, High-voltage high-current GTO thyristors, *IEE Proc.,* **132** (6): 238–243, 1985.
20. T. Yatsuo, S. Kimura, and Y. Satou, Design considerations for large-current GTO's, *IEEE Trans. Electron Devices,* **ED-36**: 1196–1202, 1989.
21. C. M. Johnson et al., Correlation between local segment characteristics and dynamic current redistribution in GTO power thyristor, *Proc. 1991 Int. Symp. Power Semiconductor Devices,* 121–127, 1991.
22. H. Matsuda et al., 2.5kV–800A monolithic reverse conducting gate turn-off thyristor, *IEEE Conf. Record, Industrial Applications Soc. Meeting,* 871–875, 1985.
23. O. Hashimoto et al., 4.5 kV 3000A high power reverse conducting gate turn-off thyristor, *IEEE Power Electronics Specialists Conf. Record,* 915–920, 1988.
24. T. Nagano et al., A snubberless GTO, *IEEE Power Electronics Specialists Conf. Record,* 383–387, 1982.
25. F. Wirth, High speed, snubberless operation of GTO's using a new gate drive technique, *IEEE Conf. Record, Industrial Applications Soc. Meeting,* 453–457, 1986.
26. H. Grüning et al., High-power hard-driven GTO module for 4.5kV/3kA snubberless operation, *Proc. Power Conversion Intelligent Motion (PCIM),* 169–183, 1996.
27. S. Eicher et al., Punchthrough type GTO with buffer layer and homogeneous low efficiency anode structure, *Proc. 1996 Int. Symp. Power Semiconductor Devices,* 261–264, 1996.
28. K. Satou et al., A new high power device GCT (gate commutated turn-off) thyristor, *7th European Conf. on Power Electronics and Applications* (ECPEA) '97, 1997.
29. H. Yonezawa et al., Self-commutated back-to-back system using gate-turn-off thyristor, *Proc. IEEJ Power and Energy Soc., Annual Conf.,* session II, 1024–1026, 1997.

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THYRISTORS, INVERTER. See INVERTER THYRISTORS.