INVERTER THYRISTORS

Thyristors are typically three-terminal devices that have at least a four-layer structure (i.e., three p–n junctions) for the main power handling section of the device. The control terminal of the thyristor, called the gate electrode, may be connected to an integrated and extremely complicated structure as part of the device. The other two terminals, called the anode and cathode, handle the high applied potential and con-

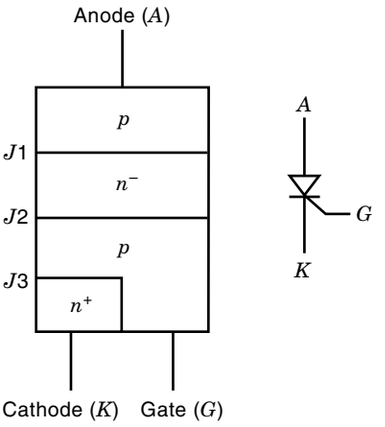

Figure 1. Four-layer structure of a thyristor with the corresponding circuit symbol.

duct the major current through the thyristor. Figure 1 shows a conceptual view of a typical thyristor with the three p–n junctions and the external electrodes labeled. Also shown in the figure is the thyristor circuit symbol used in electrical schematics.

Thyristors are used to approximate ideal closed (no voltage drop) or open (no current flow) switches for control of power flow in a circuit. This differs from low-level digital switching circuits in that digital systems are primarily designed to deliver two distinct small voltage levels while conducting small currents (ideally zero). Power electronic circuits, though, must have the capability of delivering large currents and be able to withstand large voltages. All thyristor types are controllable in switching from a forward-blocking state (very little current flows) into a forward-conduction state (large forward current flows). Some thyristors are also controllable in switching from forward-conduction back to a forward-blocking state. The particular design of a thyristor will often determine its application.

Typically, thyristors are used at the highest energy levels in power conditioning circuits because they are designed to handle the largest currents and voltages of any device technology (systems with voltages above approximately) 1.5 kV or currents above 100 A). Many medium-power circuits (systems operating at less than 1.5 kV or 100 A) and particularly low-power circuits (systems operating below 100 V or several amperes) generally make use of power bipolar transistors, power metal-oxide-silicon-field-effects-transistor (MOSFETs) or insulated gate bipolar transistors (IGBTs), as the main switching elements, because of the relative ease in controlling them. Diodes are used throughout all levels of power conditioning circuits and systems.

A thyristor used in some ac power circuits (50 Hz or 60 Hz in commercial utilities or 400 Hz in aircraft) to control ac power flow can be made to optimize internal power loss at the expense of switching speed. These thyristors are called phase-control devices, because they are generally turned from a forward-blocking into a forward-conducting state at some specified phase angle of the applied sinusoidal anode–cathode voltage waveform. A second class of thyristors is used in association with dc sources or in converting ac power at one amplitude and frequency into ac power at another amplitude and frequency, and must generally switch on and off relatively quickly. A typical application for the second class of thyristors is in converting a dc voltage or current into an ac voltage or current. A circuit that performs this operation is often called an inverter, and the associated thyristors used are referred to as inverter thyristors.

There are four major types of thyristors: (1) silicon-controlled rectifier (SCR), (2) gate turn-off thyristor (GTO), (3) MOS-controlled thyristor (MCT) and its various forms, and the (4) static induction thyristor (SITh). MCTs are so-named because many parallel enhancement-mode, MOSFET structures of one charge type are integrated into the thyristor for turn-on and many more MOSFETs of the other charge type are integrated into the thyristor for turn-off. MCTs are presently limited to operation at medium-power levels. Other types of integrated MOS-thyristor structures can be operated at high-power levels, but these devices are not commonly available or are produced for specific applications. An SITh or field controlled thyristor (FCTh) has essentially the same construction as a power diode with a gate structure that can pinch-off anode current flow. High power SIThs have a subsurface gate (buried-gate) structure to allow larger cathode areas to be utilized, and hence larger current densities are possible. The advantages of using MCTs, derivative forms of the MCT, or SIThs is that they are essentially voltage-controlled devices, (e.g., little control current is required for turn-on or turn-off, compared to a GTO) and therefore require simplified control circuits attached to the gate electrode. Detailed discussion of variations of MCTs and SIThs, as well as additional references on these devices are discussed by Hudgins in Ref. 1. SCRs and GTOs operate at all power levels. Most power converter circuits incorporating thyristors make use of either SCRs or GTOs, and hence this article will focus on these two devices.

THYRISTOR BEHAVIOR

Almost all power semiconductor devices are made from silicon, Si, though some limited commercial devices are available using gallium-arsenide, GaAs, and silicon–carbide, SiC. The latter two semiconductor types will not be discussed directly because of the lack of general availability and usage. However, the physical description and general behavior of thyristors is immaterial to the semiconductor used, though the specific discussion and any numbers cited will be associated with silicon devices.

A high resistivity region of silicon is present in all power semiconductor devices. It is this region, the n-base and associated junction, J_2, of Fig. 1, that must support the large applied forward voltages that occur when the switch is in its off state (nonconducting). The n-base is typically doped with phosphorous atoms at a concentration of around 10^{14} cm^{-3}. The n-base can be 10s to 100s of μm thick to support large voltages. High-voltage thyristors are generally made by diffusing aluminum or gallium into both surfaces of a silicon wafer to obtain deep junctions with the n-base. The doping profile of the p-regions ranges from about 10^{15} to 10^{17} cm^{-3}. These p-regions can be up to about 10 μm thick. The cathode region (typically only a few μm thick) is formed by using phosphorus at a doping density of 10^{18} cm^{-3} to 10^{20} cm^{-3}.

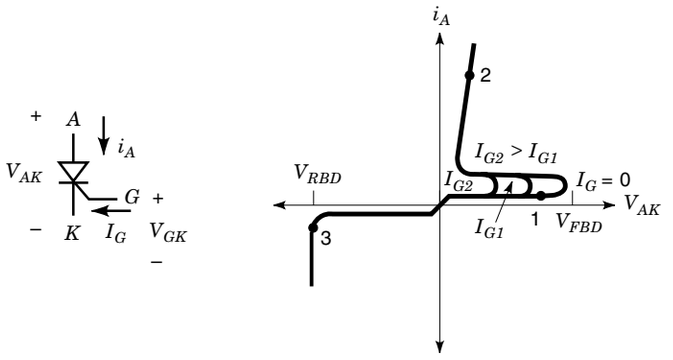

Figure 2. Dc operating characteristic curve for a thyristor and the associated voltages and currents shown on the circuit symbol.

The first quadrant in Fig. 2 illustrates the dc operation of a thyristor under forward-applied voltage or forward-conduction conditions. The higher the forward-blocking voltage rating of the thyristor, the thicker the *n*-base region must be. Increasing the thickness of this high resistivity region, though, results in slower turn-on and turn-off (i.e., longer switching times and/or lower frequency of switching cycles because of more stored charge). For example, a device rated for a forward-blocking voltage of 5 kV will by its physical construction switch much more slowly than one rated for 100 V. In addition, the thicker high resistivity region of the 5 kV device will cause a larger forward voltage drop during conduction than the 100 V device carrying the same current. Impurity atoms, such as platinum or gold, or, electron or proton irradiation are used to create charge-carrier recombination sites in the thyristor. These recombination sites reduce the minority carrier lifetime. A reduced carrier lifetime shortens the switching times (in particular the turn-off or recovery time) at the expense of increasing the forward conduction drop. There are other effects associated with the relative thickness and lay-out of the various regions that make up modern thyristors, but the major trade-off between forward-blocking voltage rating and switching times, and between forward-blocking voltage and forward voltage drop during conduction should be kept in mind. In signal electronics the analogous trade-off appears as a lowering of amplification to achieve higher operating frequencies, and is often referred to as the gain-bandwidth product.

With zero gate current and positive v_{AK}, the forward characteristic in the off- or blocking-state is determined by the center junction, J_2, which is reverse-biased. The forward-blocking operating point, 1, is shown on the lower portion of the curve in Fig. 2. At this operating point very little current flows through the device. However, if the applied voltage exceeds the forward-blocking voltage, the thyristor switches to its on- or conducting-state (shown as operating point 2). It should be noted that no high-power thyristor will survive being turned on by the application of excessive forward voltage with the exception of those with specific "self-protection" features integrated into them. The effect of gate current is to lower the blocking voltage at which switching takes place.

This switching behavior can be explained in terms of the two-transistor analog shown in Fig. 3. The two transistors are regeneratively coupled so that if the sum of their forward current gains (α's) exceeds unity, each drives the other into saturation. Equation (1) describes the condition necessary for the thyristor to move from a forward-blocking state into the forward-conduction state. The forward-current gain (expressed as the ratio of collector current to emitter current) of the *pnp* transistor is denoted by α_p, and that of the *npn* as α_n. The center junction, J_2, is reverse biased under forward-applied voltage (positive v_{AK}). The associated electric field in the depletion region around the junction can result in significant carrier multiplication, denoted as a multiplying factor, M [see (2)], on the current components, I_{co} and i_G.

$$i_A = \frac{MI_{co} + M\alpha_n i_G}{1 - M(\alpha_n + \alpha_p)} \tag{1}$$

In the forward-blocking state, the leakage current, I_{co}, is small, both α's are small, and their sum is less than unity. Gate current increases the current in both transistors, increasing their α's. When the sum of the two α's equals unity, the thyristor switches to its on-state (latches). This condition can also be reached, without any gate current, by increasing the forward applied voltage so that carrier multiplication at J_2 increases the internal leakage current, thus increasing the two α's.

The reverse thyristor characteristic, quadrant III of Fig. 2, is determined by the outer two junctions (J_1 and J_3), which are reverse-biased in this operating mode (applied v_{AK} is negative). Symmetric thyristors are designed so that J_1 will reach reverse breakdown due to carrier multiplication at an applied reverse potential near the forward breakdown value (operating point 3 in Fig. 2). The forward and reverse blocking junctions are generally fabricated at the same time using a long (10 to 50 h) high-temperature (~1250°C) diffusion process producing symmetric blocking characteristics. Usually, the forward blocking capability is reduced below 90% of the reverse capability by the edge termination techniques used. These will be discussed later. Asymmetric devices are made to reach reverse breakdown at a much lower voltage than that applied in the forward direction. Asymmetric devices are generally used in applications when only forward voltage is to be applied (including many inverter designs). The advantages are that the asymmetric thyristors have a lower forward drop and shorter switching times, because of a thinner *n*-base, than in symmetric devices.

The form of the gate-to-cathode *VI* characteristic of SCRs and GTOs is similar to that of a diode. With positive gate bias, the gate-cathode junction is forward-biased and permits the flow of a large current in the presence of a low-voltage drop. When negative gate voltage is applied to an SCR, the

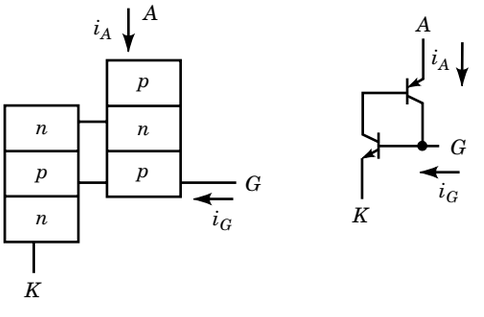

Figure 3. Two-transistor equivalent circuit used to describe the switching behavior of a thyristor.

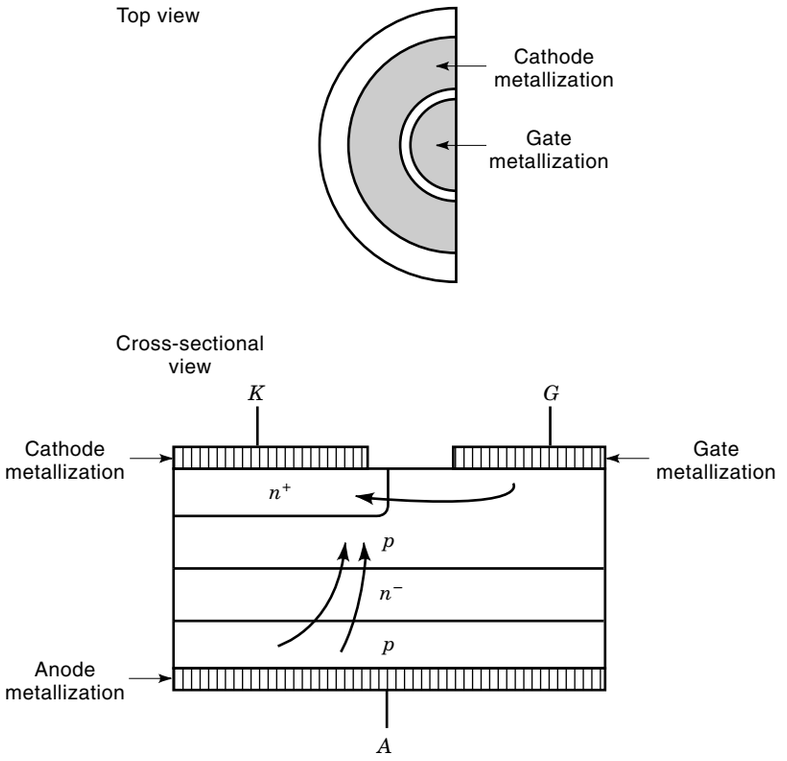

Figure 4. Initial turn-on of a center-fired SCR showing anode current flow near the cathode region closest to the gate (not to scale).

gate-cathode junction is reverse-biased and prevents the flow of current until the avalanche breakdown voltage is reached. In a GTO, a negative gate voltage is applied to provide a low impedance path for anode current to flow out of the device instead of out the cathode. In this way the cathode region (base-emitter junction of the equivalent *npn* transistor) turns off, thus pulling the equivalent *npn* transistor out of conduction. This causes the entire thyristor to return to its blocking state. The problem with the GTO is that the gate-drive circuitry is typically required to sink from 10% to 25% of the anode current to achieve turn-off. Indeed, in many of the newest GTOs, the gate current required for turn-off approaches the anode current value (unity turn-off gain).

The time rate of rise of anode current (di/dt) during turn-on and the time rate of rise of anode-cathode voltage (dv/dt) during turn-off are important parameters to control for ensuring proper and reliable operation. All thyristors have maximum limits for di/dt and dv/dt that must not be exceeded. Devices capable of conducting large currents in the on-state are necessarily made with large surface areas through which the current flows. During turn-on, localized areas (near the gate region) of a device begin to conduct current. The initial turn-on of an SCR is shown in Fig. 4. The cross section illustrates how injected gate current flows to the nearest cathode region, causing this portion of the *npn* transistor to begin conducting. The *pnp* transistor then follows the *npn* into conduction such that anode current begins flowing only into a small portion of the cathode region. If the local current density becomes too large (in excess of several thousand amperes per square centimeter), then heating will damage the device. Sufficient time (referred to as plasma spreading time) must be allowed for the entire cathode area to begin conducting before the localized currents become too high and the device's di/dt rating is exceeded. In many higher frequency applications of thyristors, the entire cathode is never fully in conduction. To prevent di/dt failure it is only necessary that the rate of increase of the conduction area generally exceed the di/dt rate in such a way that the internal junction temperature does not exceed a specific critical value (typically about 350°C). The critical temperature decreases with increasing blocking voltage. Sometimes series inductance is added to limit di/dt below the recommended maximum value though this causes circuit design problems. Another way to increase the di/dt rating of a device is to increase the amount of gate-cathode periphery. Inverter SCRs are designed so that there is a large amount of gate edge next to a significant amount of cathode edge. A top surface view of two typical gate-cathode patterns is shown in Fig. 5. An inverter SCR often has a stated maximum di/dt limit of about 2000 A/μs. Hudgins and Portnoy (3) have shown this value to be conservative, and by using excessive gate current under certain operating conditions, an inverter SCR can be operated reliably at 10,000 A/μs to 20,000 A/μs.

A GTO takes the interdigitation of the gate and cathode to the extreme. In Fig. 6 a cross section of a GTO shows the amount of interdigitation. A GTO often has cathode islands that are formed by etching the Si. A metal plate can be placed on the top to connect the individual cathodes into a large ar-

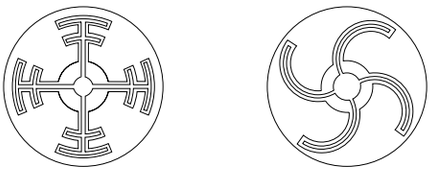

Figure 5. Involute (left) and snow-flake (right) patterns for the gate-cathode periphery of inverter thyristors.

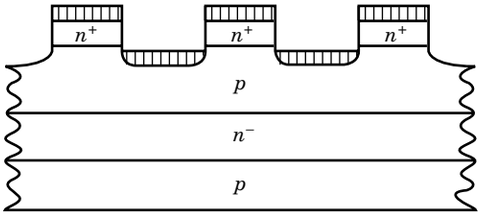

Figure 6. Cross section of a GTO showing the cathode islands.

rangement of electrically parallel cathodes. The gate metallization is placed so that the gate surrounding each cathode is electrically in parallel as well. This construction not only allows high di/dt values to be reached, as in an inverter SCR, but also provides the capability to turn off the anode current by shunting it away from the individual cathodes and out the gate electrode upon reverse biasing of the gate. The movement of anode current away from the cathode allows the emitter-base junction of the equivalent *npn* transistor to recover into a non-conducting state, thus pulling the *npn* and by necessity, the *pnp*, out of conduction. During turn-off, current is decreasing while voltage across the device is increasing. If the forward voltage becomes too high while sufficient current is still flowing, then the device will drop back into its conduction mode instead of completing its turn-off cycle. Also during turn-off, the power dissipation can become excessive if the current and voltage are simultaneously too large. Both of these turn-off problems can damage the device as well as other portions of the circuit.

Another switching problem that occurs is associated primarily with thyristors, though other power electronic devices suffer some degradation of performance from the same problem. This problem is that thyristors can self-trigger into a forward-conduction mode from a forward-blocking mode if the rate of rise of forward anode-cathode voltage is too large. This triggering method is due to displacement current through the associated junction capacitances (capacitance at J_2 dominates because it is reverse biased under forward applied voltage). The displacement current contributes to the leakage current, I_{co}, shown in Eq. (1). SCRs and GTOs, therefore, have a maximum dv/dt rating that should not be exceeded (typical values are 100 V/μs to 1,000 V/μs). This mode of turn-on is generally destructive except for a class of two-terminal thyristor devices (RBDTs) specifically designed for dv/dt triggering. Switching into a reverse-conducting from a reverse-blocking state due to an applied reverse dv/dt is not possible because the values of the reverse α's of the equivalent transistors can never be made large enough to cause the necessary feedback (latching) effect. An external capacitor is often placed between the anode and cathode of the thyristor to help control the dv/dt experienced. Capacitors and other components that are used to form such protection circuits, known as snubbers, are used with all power semiconductor devices. Snubber circuits are discussed in many power electronics texts such as Mohan et al. (4).

SCR and GTO Ratings

All power electronic devices must be derated (e.g., power dissipation levels, current conduction, voltage blocking, and switching frequency must be reduced), when operating above room temperature (defined as about 25°C). Bipolar-type devices like SCRs and GTOs have thermal runaway problems, in that if allowed to conduct unlimited current, these devices will heat up internally causing more current to flow, thus generating more heat, and so forth until destruction.

The present best voltage hold-off ratings for SCRs and GTOs is above 6 kV. Continuing development will push this limit higher. The pulsed current rating for these devices is easily tens of kiloamperes. A gate signal of 0.1 A to 100 A peak is typical for triggering an SCR or GTO from forward-blocking into forward-conduction. These thyristors are being produced in silicon with diameters greater than 100 mm. The improvement of GTO performance has caused and will continue to affect the decline in the use of SCRs, except at the very highest power levels.

A summary of some of the maximum rating which must be considered when choosing a thyristor for a given application is provided in Table 1. Thyristor types shown in parentheses indicate a maximum rating unique to that device. Both forward and reverse repetitive and nonrepetitive voltage ratings must be considered, and a properly rated device must be chosen so that the maximum voltage ratings are never exceeded. In most cases, either forward or reverse voltage transients in excess of the nonrepetitive maximum ratings result in destruction of the device. The maximum rms or average current ratings given are usually those which cause the junction to reach its maximum rated temperature. Because the maximum current will depend upon the current waveform and upon thermal conditions external to the device, the rating is usually shown as a function of case temperature and conduction angle. The peak single half-cycle surge-current rating must be considered, and in applications where the thyristor must be protected from damage by overloads, a fuse with an I^2t rating smaller than the maximum rated value for the device must be used. Maximum ratings for both forward and reverse gate voltage, current, and power also must not be exceeded.

Table 1. Thyristor Maximum Ratings Specified by Manufacturers

Symbol	Definition
V_{RRM}	Peak repetitive reverse voltage
V_{RSM}	Peak nonrepetitive reverse voltage
V_{DRM}	Peak repetitive forward off-state voltage
V_{DSM}	Peak nonrepetitive forward off-state voltage
$I_{T(rms)}$	rms forward current
$I_{T(AV)}$	Average forward current
I_{TSM}	Surge forward current
I_{TGQ}(GTO)	Peak controllable current
I^2t	Nonrepetitive pulse overcurrent capability
P_T	Maximum power dissipation
di/dt	Critical rate of rise of on-state current
dv/dt	Critical rate of rise of off-state voltage
P_{GM}(P_{FGM} for GTO)	Peak gate forward power dissipation
P_{RGM}(GTO)	Peak gate reverse power dissipation
V_{FGM}	Peak forward gate voltage
V_{RGM}	Peak reverse gate voltage
I_{FGM}	Peak forward gate current
I_{RGM}(GTO)	Peak reverse gate current
T_j	Junction temperature

Table 2. Typical Thyristor Characteristics Specified by Manufacturers

Symbol	Definition
V_{TM}	On-state voltage drop (at specified temperature and forward current)
I_{DRM}	Maximum forward off-state current (at specified temperature and forward voltage)
I_{RRM}	Maximum reverse blocking current (at specified temperature and reverse voltage)
V_{GT}	Gate trigger voltage (at specified temperature and forward applied voltage)
V_{GD}	Gate nontrigger voltage (at specified temperature and forward applied voltage)
I_{GT}	Gate trigger current (at specified temperature and forward applied voltage)
I_{gt}(GTO)	Turn-on time (under specified switching conditions)
t_q	Turn-off time (under specified switching conditions)
t_D	Turn-on delay time (for specified test)
$R_{\Theta JC}$	Junction-to-case thermal resistance

The maximum rated operating junction temperature, T_J, must not be exceeded, since device performance, in particular voltage-blocking capability, will be degraded. Junction temperature cannot be measured directly but must be calculated from a knowledge of steady-state thermal resistance, $R_{\Theta JC}$, and the average power dissipation. For transients or surges, the transient thermal impedance ($Z_{\Theta JC}$) curve must be used (provided in manufacturers' data sheets). The maximum average power dissipation, P_T, is related to the maximum rated operating junction temperature and the case temperature by the steady-state thermal resistance. In general, both the maximum dissipation and its derating with increasing case temperature are provided.

The number and type of thyristor characteristics specified varies widely from one manufacturer to another. Some characteristics are given only as typical values of minima or maxima, while many characteristics are displayed graphically. Table 2 summarizes some of the typical characteristics provided. Thyristor types shown in parentheses indicate a characteristic unique to that device. Gate conditions of both voltage and current to ensure either nontriggered or triggered device operation are included. The turn-on and turn-off transients of the thyristor are characterized by switching times like the turn-off time listed in Table 2. The turn-on transient can be divided into three intervals: (1) gate-delay interval, (2) turn-on of initial area, and (3) spreading interval. The gate-delay interval is simply the time between application of a turn-on pulse at the gate and the time the initial area turns on. This delay decreases with increasing gate drive current and is of the order of a few microseconds. The second interval, the time required for turn-on of the initial area, is quite short, typically less than 1 μs. In general, the initial area turned on is a small percentage of the total useful device area. After the initial area turns on, conduction spreads (spreading interval or plasma spreading time) throughout the device in tens of microseconds for small or high-speed inverter devices to hundreds of microseconds for large phase-control devices.

THYRISTOR PHYSICS AND DESIGN

There are many subtleties of power device fabrication and design that are made to improve the switching times, forward voltage drop during conduction, dv/dt, di/dt, and other ratings. The improvement in one rating can often result in a lowering of performance with respect to another parameter. The following description of the detailed structure of thyristors is based on device designers' optimization of generally agreed-upon desirable characteristics, such as forward voltage drop during conduction, voltage-blocking capability, switching times, and others.

Temperature Dependence

Several dominant physical parameters associated with semiconductor devices are sensitive to temperature variations, causing their dependent device characteristics to change dramatically. The most important of these parameters are: (1) the minority carrier lifetimes (which control the high-level injection lifetimes), (2) the hole and electron mobilities, (3) the impact ionization collision cross sections, and (4) the free-carrier concentrations (primarily the ionized impurity-atom concentration). Almost all of the impurity atoms are ionized at temperatures above 0°C, and so further discussion of the temperature effects on ionization is not relevant for normal operation.

Cathode and Anode Shorts

The increase in the effective collision cross sections, as the temperature drops below room temperature, primarily affects the blocking voltage of the thyristors. Devices produced by some manufacturers have been shown to increase their forward and reverse breakdown voltages with increasing temperature (~125° to 160°C) up to the point at which the increasing gain causes the device to switch into conduction (forward). The forward-blocking voltage of yet a different SCR has been shown to be reduced from 1350 V at room temperature to 950 V at −175°C in a near linear fashion (5). Above room temperature, the forward-blocking capability is again reduced due to changes in the minority carrier lifetime (the change in collision cross section becomes secondary to the minority lifetime effects). As the temperature in the thyristor increases above 25°C, the minority carrier lifetime and the corresponding diffusion lengths in the n- and p-bases increase as well. This leads to an increase in the α's of the equivalent transistors. The differences in behavior point out the complex interactions of various physical mechanisms that are produced by different processing parameters and device designs. Discussion of the details of the minority carrier diffusion length and its role in determining the current gain factor, α, can be found in Sze (6). Referring to Eq. (1), it is seen that a lower applied bias will give a carrier multiplication factor, M, sufficient to switch the device from a forward-blocking state into conduction because of this increase of the α's with increasing temperature. Placing a shunt resistor in parallel with the base–emitter junction of the equivalent npn transistor (shown in Fig. 7) will result in an effective current gain, $\alpha_{n\text{eff}}$, that is lower than α_n, as given by Eq. (2), where v_{GK} is the applied gate-cathode voltage, R_s is the equivalent lumped value for the distributed shunting structure, and the remaining factors form the appropriate current factor based on the applied bias and characteristics of the gate–cathode junction. The shunt current path is implemented by providing intermittent shorts, called cathode shorts, between the p-gate

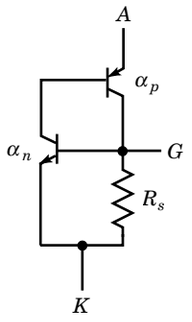

Figure 7. Shunt resistor incorporated to bypass the gate-cathode junction (base–emitter of the *npn* transistor) thus lowering the effective current gain.

region and the n^+-cathode region in the thyristor as illustrated in Fig. 8.

$$\alpha_{n\text{eff}} = \alpha_n \left(\frac{1}{1 + \dfrac{v_{\text{GK}}\alpha_n}{R_s I_0 e^{\frac{qv_{\text{GK}}}{kT}}}} \right) \tag{2}$$

Low values of anode current (e.g., those associated with an increase in temperature under forward-blocking conditions) will flow through the shunt path to the cathode contact, bypassing the n^+-region and keeping the device out of its forward-conduction mode. As the anode current becomes large, the potential drop across the shunt resistance will be sufficient to forward bias the gate-cathode junction, J_3, and bring the thyristor into forward conduction. The cathode shorts also provide a path for displacement current to flow without forward biasing J_3. The dv/dt rating of the thyristor is thus improved as well as the forward-blocking characteristics by using cathode shorts. The shorts do, however, cause a lowering of cathode current handling capability because of the loss of some of the cathode area (n^+-region) to the shorting pattern, an increase in the necessary gate current to obtain switching from forward-blocking to forward-conduction, and an increase in complexity of manufacturing of the thyristor. The cathode shorts consume about 5% of the cathode area of a phase-control device and 10% to 20% of an inverter-grade device.

A further increase in forward-blocking capability can be obtained by introducing anode shorts (reduces α_p in a similar manner that cathode shorts reduce α_n) as well as the cathode

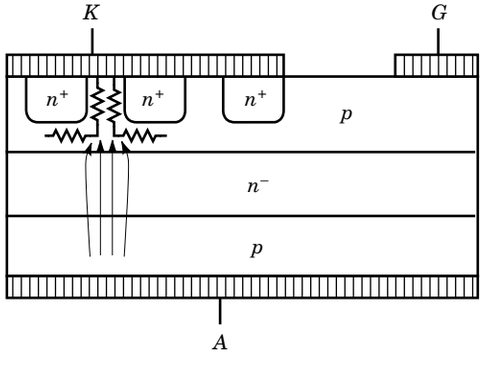

Figure 8. Cross section showing cathode shorts implemented on a thyristor.

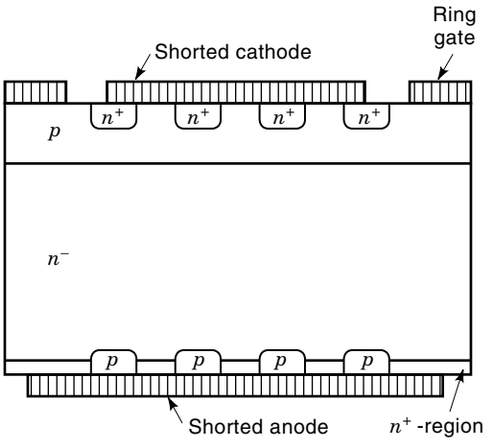

Figure 9. Thyristor cross section showing anode and cathode shorts.

shorts. An illustration of this is provided in Fig. 9. In this structure both J_1 and J_3 are shorted so that the forward-blocking capability of the thyristor is completely determined by the avalanche breakdown characteristics of J_2. Anode shorts will result in the complete loss of reverse-blocking capability and is only for thyristors being used in asymmetric circuit applications (i.e., only forward applied voltages).

Amplifying Gate

The cathode-shorting structure will reduce the gate sensitivity dramatically. To increase this sensitivity and yet retain the benefits of the cathode-shorts, a structure called an amplifying gate (or regenerative gate) is used. When the gate current (1) is injected into the *p*-base through the pilot gate contact (Fig. 10), electrons are injected into the *p*-base by the n^+ emitter with a certain emitter injection efficiency. These electrons traverse through the *p*-base (time taken for this process is called the transit time) and accumulate near the depletion region. This negative charge accumulation leads to injection of holes from the anode. At this time the device turns-on after a certain delay, dictated by the *p*-base transit time, and the pilot anode current (2) begins to flow through a small region near the pilot gate contact as shown in Fig. 10. This flow of pilot anode current corresponds to the initial sharp rise in the

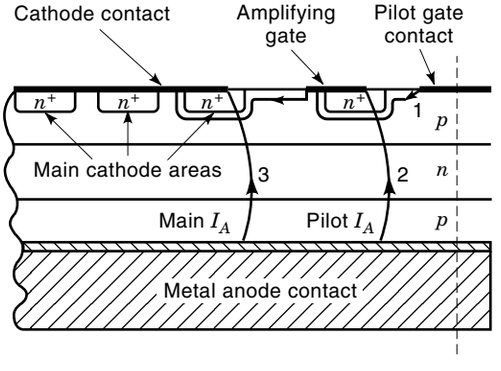

Figure 10. Cross section of a thyristor showing the turn-on process with an amplifying gate structure.

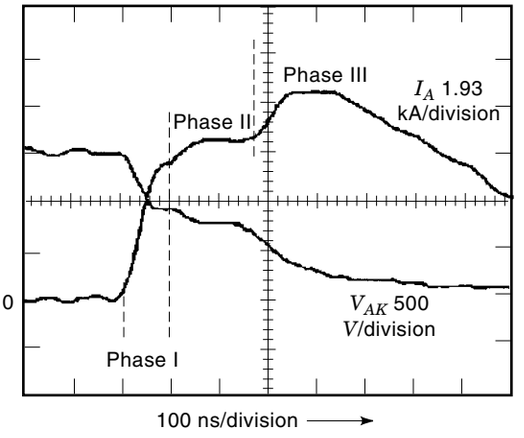

Figure 11. Anode current waveform during turn-on at a high di/dt level.

anode current waveform (Phase I), shown in Fig. 11. The device then goes into Phase II, during which the anode current remains farily constant, suggesting that the resistance of the region has reached its lower limit. This is due to the fact that the pilot anode current 2 takes a finite time to traverse through the p-base laterally and become the gate current for the main cathode area. The n^+ emitters start to inject electrons which traverse the p-base vertically and after a certain finite time (transit time of the p-base) reach the depletion region. The time taken by these processes is the reason for observing this characteristic Phase II interval. The width of the Phase II interval is comparable to the switching delay, suggesting that the p-base transit time is of primary importance. Once the main cathode region turns-on, the resistance of the device decreases and the anode current begins to rise again (transition from Phase II to Phase III). From here on the plasma spreading velocity will dictate the rate at which the conduction area will increase. The current density during Phase I and Phase II can be quite large, leading to a considerable increase in the local temperature, and device failure if it is operated in excess of the manufacturer's specifications. It can be concluded that the amplifying gate will increase gate sensitivity at the expense of some di/dt capability, as demonstrated by Sankaran et al. (7). This lowering of di/dt capability can be somewhat offset by an increase in gate-cathode interdigitation as previously illustrated in Fig. 5.

Forward-Conduction and Temperature

It is well-known that recombination centers are more efficient at lower temperatures. This shows up as a decrease in the effective carrier lifetime and hence a larger potential drop during forward conduction and a shorter recovery time during turn-off, as shown by Hudgins et al. (8). The n-base in a thyristor is under high-level injection conditions during forward conduction and as such, recombination events there are described by the effective high-level carrier lifetime, τ_{HL}.

A plot of the anode current during turn-off, at various temperatures, for a typical GTO is shown in Fig. 12. The associated high-level lifetime values at each temperature can be extracted by using an exponential fit to the tail current during turn-off. From the curves, the temperature dependence between $-125°$ and 125°C is approximately given by Eq. (3). The temperature exponent, α is 0.36 for the currents in Fig. 12. The values of the prefactor and the temperature coefficient in Eq. (3) will vary slightly depending on the details of device fabrication and design.

$$\tau_{HL} = 2.5 \times 10^{-7} \left(\frac{T}{300}\right)^{\alpha} \tag{3}$$

Electron and hole mobilities increase as the lattice temperature decreases because of reduced phonon interaction. Below about -175°C the mobilities decrease because of impurity scattering. For the temperature range of interest this last scattering effect is negligible so that the mobilities are considered to only decrease as the temperature increases above room temperature. Empirical temperature dependencies for the electron, μ_n, and hole, μ_p, mobilities are taken from Arora et al. (9). The room temperature parameters for the electron mobility are taken from Baccarani et al. (10). A useful relation is the ratio of the mobilities, b, given in Eq. (4) as:

$$b = \frac{\mu_n}{\mu_p} = 2.75 \left(\frac{T}{300}\right)^{-0.22} \tag{4}$$

The n-base in a thyristor operates under high-level injection conditions and as such can be assumed to behave similarly to a p–i–n structure during forward conduction. Ambipolar transport describes the behavior with an associated characteristic diffusion length given in Eq. (5) as:

$$L_a = \sqrt{D_a \tau_{HL}} \tag{5}$$

where the ambipolar diffusivity, D_a, is given by Eq. (6).

$$D_a = \frac{2kT}{q} \cdot \frac{\mu_n \mu_p}{\mu_n + \mu_p} \tag{6}$$

The potential drop across the center section of the p–i–n structure can be found from the ambipolar transport equation from Herlett (11). A defined parameter, B, is given in Eq. (7).

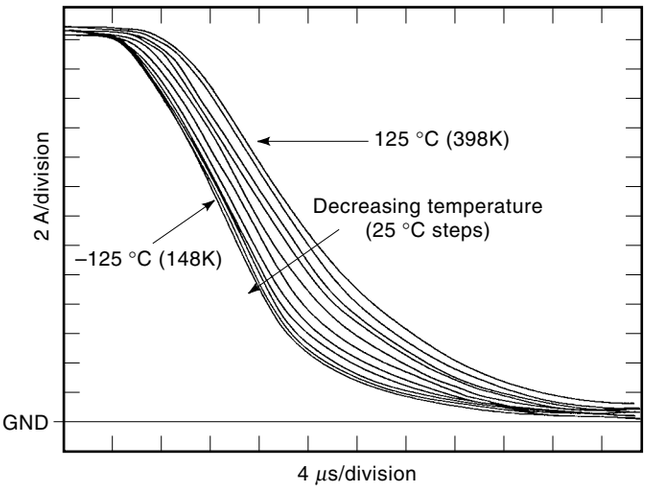

Figure 12. GTO anode current during turn-off at various operating temperatures.

$$B = \frac{\mu_n - \mu_p}{\mu_n + \mu_p} = \frac{2.75\left(\frac{T}{300}\right)^{-0.22} - 1}{2.75\left(\frac{T}{300}\right)^{-0.22} + 1} \tag{7}$$

From Eqs. (3)–(7) and the solution given by Herlet (11) and Hudgins (8), an approximate relation between the temperature and the forward potential drop across the n-base of a thyristor is found as shown in Eq. (8). Carrier-carrier scattering, Auger recombination, and recombination in the p- and n-emitters have not been directly taken into account in the derivation of Eq. (8). The recombination effects become particularly more important as the temperature drops below −100°C (175 K) because the temperature dependence of the high-level lifetime changes from the simple form given in Eq. (3).

Including the junction potential drops in the device, the temperature dependence of the intrinsic carrier concentration, n_i, and the bandgap energy, along with the n-base potential drop from Eq. (8), gives the temperature dependent equation relating anode current density, J, and the anode-cathode voltage, V_{AK}, in Eq. (9). Comparison of the forward drop predicted by Eq. (9) to the measured performance of inverter-grade SCRs from Menhart et al. (5), at nearly identical current densities, shows similar behavior between −100° and 25°C.

$$V_n = \frac{kT}{q}\left\{\frac{8b}{(b+1)^2}\cdot\frac{\sinh\left(\frac{d}{L_a}\right)}{\sqrt{1-B^2\tanh^2\left(\frac{d}{L_a}\right)}}\cdot\arctan\left[\sqrt{1-B^2\tanh^2\left(\frac{d}{L_a}\right)}\cdot\sinh\left(\frac{d}{L_a}\right)\right] + B\ln\left[\frac{1+B\tanh^2\left(\frac{d}{L_a}\right)}{1-B\tanh^2\left(\frac{d}{L_a}\right)}\right]\right\} \tag{8}$$

$$J = \frac{2qD_a n_i}{d}\cdot\left[\frac{d}{L_a}\tanh\left(\frac{d}{L_a}\right)\right]\left[1-B^2\tanh^4\left(\frac{d}{L_a}\right)\right]^{-1/2} e^{-qV_n/2kT}\cdot e^{qV_{AK}/2kT} \tag{9}$$

Surface and Edge Terminations

Thyristors are often made with planar diffusion technology to create the cathode region. Formation of these regions creates cylindrical curvature of the metallurgical gate-cathode junction. Under reverse bias, the curvature of the associated depletion region results in electric field crowding along the curved section of the n^+ diffused region. The field crowding seriously reduces the breakdown potential below that expected for the bulk semiconductor. A floating field ring, an extra n^+ diffused region with no electrical connection at the surface, is often added to modify the electric field profile and thus reduce it to a value below or at the field strength in the bulk. An illustration of a single floating field ring is shown in Fig. 13. The spacing, W, between the main cathode region and the field ring is critical. Multiple rings can also be employed to further modify the electric field in high-voltage rated thyristors. Another common method for altering the electric field

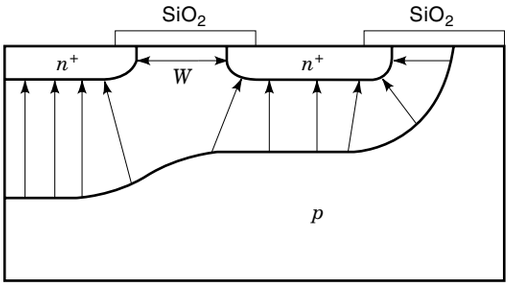

Figure 13. Cross section of a thyristor showing a floating field ring to lower the electric field intensity near the curved portion of the main n^+ region.

at the surface is by using a field plate as shown in cross section in Fig. 14. By forcing the potential over the oxide to be the same as at the surface of the n^+ region, the depletion region can be extended so that the electric field intensity is reduced near the curved portion of the diffused n^+ region. A common practice is to use field plates with floating field rings to obtain optimum breakdown performance. Detailed discussions of field rings and field plates are given by Ghandi (12) and Baliga (13).

High-voltage thyristors are made from single wafers of Si and must have edge terminations other than floating field rings or field plates to promote bulk breakdown and limit leakage current at the surface. Controlled bevel angles can be created using lapping and polishing techniques during production of large-area thyristors. Two types of bevel junctions can be created: (1) a positive bevel defined as one in which the junction area decreases when moving from the highly doped to the lightly doped side of the depletion region, and (2) a negative bevel defined as one in which the junction area increases when moving from the highly doped to the lightly doped side of the depletion region. In practice, the negative bevel must be lapped at an extremely shallow angle to reduce the surface field below the field intensity in the bulk. All positive bevel angles between 0° and 90° result in a lower surface field than in the bulk. Figure 15 shows the use of a positive bevel for the J_1 junction and a shallow negative bevel for the J_2 and J_3 junctions on a thyristor cross-section to make maximum use of the Si area for conduction and still reduce the surface electric field. The beveling and passivation reduces the electric field strength to a level at which the passivation materials (varnishes or RTV rubbers) are capable of maintaining a stable blocking voltage characteristic over the life of

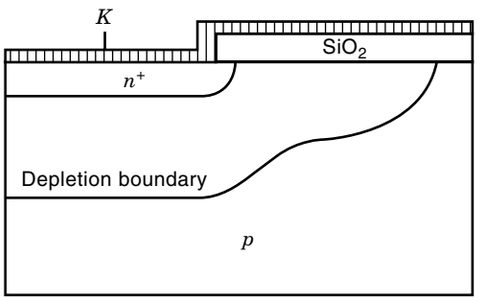

Figure 14. Cross section of a thyristor with a field plate used to lower the electric field intensity near the curved portion of the n^+ region.

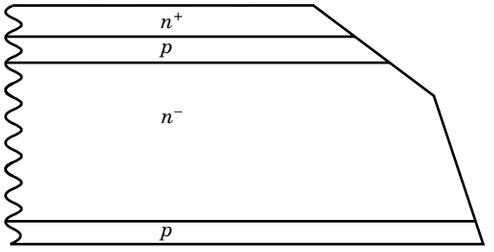

Figure 15. Cross section of a thyristor showing the steep positive bevel (lower pn^- junction) and a shallow negative bevel (upper pn^- and pn^+ junctions) used for edge termination on large-area thyristors.

the device. More details of the use of beveling can be found in Ghandi (12) and Baliga (13).

Packaging

Thyristors are available in a wide variety of packages, from small plastic ones for low-power (i.e., TO-247), to stud-mount packages for medium-power, to press-pack (also called flat-pack) for the highest power devices. The press-packs must be mounted under pressure to obtain proper electrical and thermal contact between the device and the external metal electrodes. Special force-calibrated clamps are made for this purpose. Many medium power thyristors of all types are appearing in modules where a half- or full-bridge (and associated antiparallel diodes) is put together in one package. The basic half-bridge module has three power terminals: plus, minus, and phase. Smaller modules employ wire bonded chips on aluminum oxide, aluminum nitride, or insulated metal baseplates. Advanced modules differ from traditional high power commercial modules in several ways. The baseplate is metalized AlN (aluminum nitride) ceramic rather than the typical 0.125 in. thick nickel-plated copper baseplate with a soldered metalized ceramic substrate for electrical isolation. This AlN baseplate stack provides a low thermal resistance from die to heatsink. The copper terminal power buses are attached by solder to the devices in a wirebond-free, low-inductance, low-resistance, device interconnect configuration. The balance of the assembly is typical for module manufacturing with attachment of shells, use of dielectric gels, and hard epoxies and adhesives to seal the finished module.

FUTURE TRENDS FOR THYRISTORS

The highest power handling devices continue to be bipolar thyristors. High powered thyristors are large diameter devices, some well in excess of 100 mm. Some effort in improving the voltage hold-off capability and overvoltage protection of conventional SCRs is underway by incorporating a lateral high resistivity region to help dissipate the energy during breakover, Shimizu et al. (14). This is a device that incorporates some self-protection from excessive dv/dt values referred to earlier. Most effort, though, is being placed in the further development of high performance GTO thyristors because of their controllability and to a lesser extent in optically triggered structures that feature gate circuit isolation.

High voltage GTO thyristors with symmetric blocking capability require thick n-base regions to support the high electric field. The addition of an n^+ buffer layer next to the p^+-anode allows high voltage blocking and a low forward voltage drop during conduction because of the thinner n-base required. Cylindrical anode shorts have been incorporated to facilitate excess carrier removal from the n-base during turn-off and still retain the high blocking capability, Ogura et al. (15). Some of the design trade-offs between the n-base width and turn-off energy losses in these structures have been discussed by Yatsuo et al. (16). A similar GTO incorporating an n^+-buffer layer and a *pin* structure has been fabricated by Kekura et al. (17), that can control up to 1 kA (at a forward drop of 4 V) with a forward-blocking capability of 8 kV. A reverse conducting GTO has been fabricated that can block 6 kV in the forward direction, interrupt a peak current of 3 kA, and has a turn-off gain of about 5 kA, Takahashi et al. (18).

Optically gated thyristors have traditionally been used in power utility applications where series stacks of devices are necessary to achieve the high voltages required. Isolation between gate drive circuits for circuits such as static var compensators and high voltage dc to ac inverters have driven the development of this class of devices. One of the most recent devices, by Watanabe et al. (19), can block 6 kV forward and reverse, conduct 2.5 kA average current, and maintains a di/dt capability of 300 A/μs, and a dv/dt capability of 3000 V/μs, with a required trigger power of 10 mW. An integrated light triggered and light quenched static induction thyristor has been produced that can block 1.2 kV and conduct up to 20 A (at a forward drop of 2.5 V), Saito et al. (20). This device is an integration of a normally off buried-gate static induction photothyristor and a normally off p-channel darlington surface-gate static induction phototransistor. The optical trigger and quenching power required is less than 5 mW and 0.2 mW, respectively.

In more recent years, most development efforts have gone into continued integration of the gating and control electronics into thyristor modules, and the use of MOS-technology to create gate structures integrated into the thyristor itself (e.g., the MCT), Beker et al. (21). Many variations of this theme are being developed and some technologies should rise above the others in the years to come.

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