

Figure 1. General analog signal processing circuit.

In recent years, the trend to smaller and cheaper electronic systems has resulted in mixed-mode integrated systems where both digital and analog signal processing circuits are manufactured in the same chip (3).

Analog signal processing circuits can be divided in two categories: linear and nonlinear circuits. Among linear circuits for signal processing are filters (4) which use amplifiers, adders, and integrators. High-frequency signal processing is an area where analog circuits are the main signal processors.

For nonlinear analog signal processing, the most important circuits are data converters, where comparators are widely used, as well as adders and integrators. Instrumentation and control (5) are also areas that use analog signal processing circuits intensively, for example, to measure ac signals or to control positioning motors.

This article is divided into two parts. The first part covers linear circuits, such as adders and integrators, and circuits that use them, such as filters. The second part covers nonlinear circuits, such as comparators, limiters, log and antilog amplifiers, and their applications. Because most analog signal processing circuits use operational amplifiers, a brief section on op-amps is included.

OPERATIONAL AMPLIFIERS

An operational amplifier (op-amp), shown in Fig. 1, is a three-terminal device that has a high-input impedance Z_{in} , a low output impedance Z_o , and a very high gain A (6). For an ideal op-amp, these quantities are

$$\begin{aligned} Z_{in} &\rightarrow \infty \\ Z_o &= 0 \\ A &\rightarrow \infty \end{aligned} \quad (1)$$

The op-amp input–output relationship is given by

$$V_{out} = A(V_+ - V_-) \quad (2)$$

The input terminal with a plus sign is called the noninverting input, and the input terminal with a minus sign is called the inverting input.

ANALOG PROCESSING CIRCUITS

Analog signal processing is still the primary mode of signal processing in many applications, despite the tremendous development in digital signal processing circuitry. For example, at high frequencies signal processing is implemented with very simple analog circuits. Very low-power applications are also realized with analog circuitry. In addition, even in systems using digital signal processing, it is necessary to include some form of analog signal processing and data conversion as an interface for analog systems (1,2).

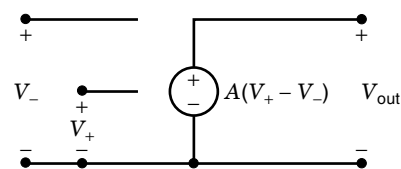


Figure 2. Operational amplifier characteristics.

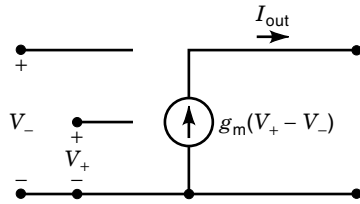


Figure 3. Operational amplifier macromodel.

The op-amp variables are shown in Fig. 1. In addition to Eqs. (1) and (2), the very high input impedance forces

$$I_+ = I_- = 0 \tag{3}$$

A macromodel for an ideal op-amp, where $A \rightarrow \infty$, is given in Fig. 2. Note that $Z_o = 0$, and $Z_{in} \rightarrow \infty$. Furthermore, because V_{out} is finite when $A \rightarrow \infty$, $(V_+ - V_-)$ must be very small. That is,

$$V_+ = V_- \tag{4}$$

Another type of op-amp that has the macromodel shown in Fig. 3, also has a high input impedance, but it has as the output variable an output current given by (6)

$$I_{out} = g_m(V_+ - V_-) \tag{5}$$

Note that now the output impedance is infinite because the output element is a current source. The value of the transconductance g_m is a function of the bias current I_{bias} . Thus,

$$g_m = g_m(I_{bias}) \tag{6}$$

Because the gain factor for this op-amp is the transconductance g_m , this op-amp is called an operational transconductance amplifier (OTA). The symbol for an OTA is shown in Fig. 4. Usually, the OTA has a higher operating frequency than the conventional voltage mode op-amp and thus, it is usually found in high-frequency circuits.

LINEAR CIRCUITS FOR SIGNAL PROCESSING

The simplest circuit in linear signal processing is the inverting amplifier (2) shown in Fig. 5(a). Because no current flows into the inverting input of the op-amp, by Kirchhoff's

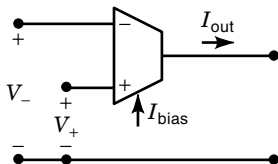
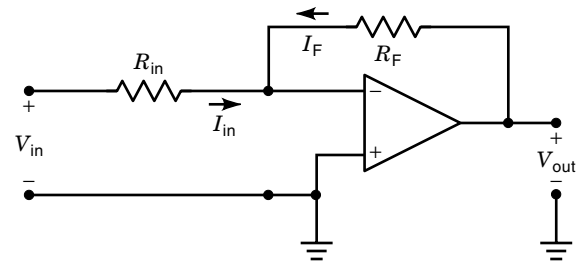
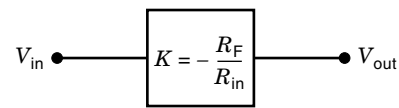


Figure 4. OTA macromodel.



(a)



(b)

Figure 5. Inverting amplifier. (a) Circuit; (b) block, diagram.

current law

$$I_{in} + I_F = 0 \tag{7}$$

In addition, because $V_- = 0$ due to the infinite op-amp gain,

$$I_{in} = \frac{V_{in}}{R_{in}} \tag{8}$$

and

$$i_F = \frac{V_{out}}{R_F} \tag{9}$$

Thus,

$$\frac{V_{in}}{R_{in}} + \frac{V_{out}}{R_F} = 0 \tag{10}$$

which can be rewritten as

$$V_{out} = -\frac{R_F}{R_{in}} V_{in} \tag{11}$$

Thus, the output voltage is given by the product of the input voltage and the inverting amplifier gain $-R_F/R_{in}$. Figure 5(b) shows a block diagram for the inverting amplifier. An inverting unity gain amplifier is obtained by making $R_{in} = R_F = R$ as shown in Fig. 6. Now let us consider the circuit

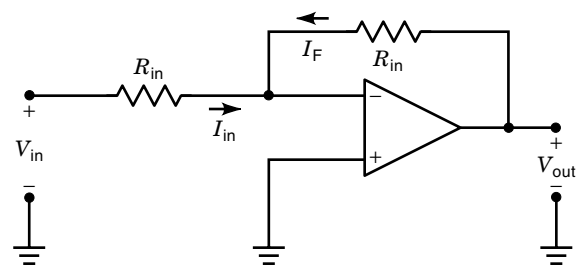


Figure 6. Inverting adder. (a) Circuit; (b) block diagram.

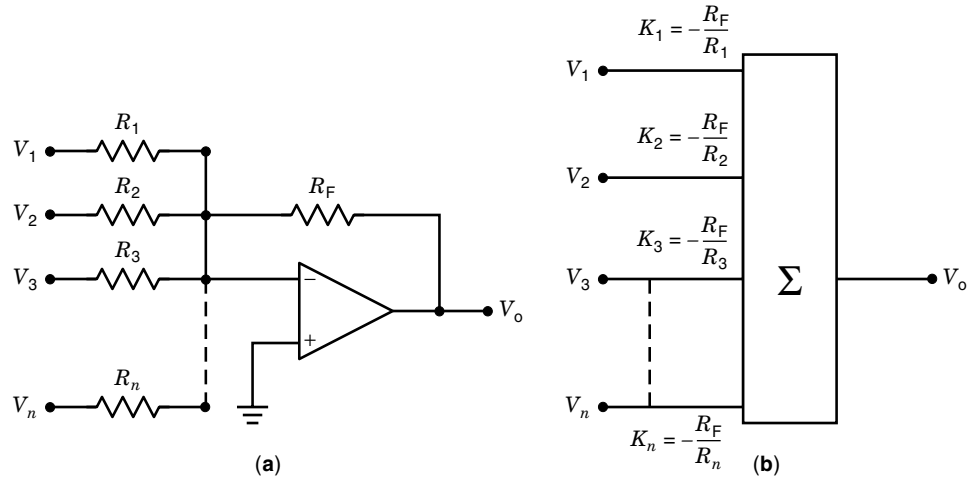


Figure 7. Two input inverting adder. (a) Circuit; (b) block diagram.

shown in Fig. 7 (8). The currents i_k are

$$I_1 = \frac{V_1}{R_1} \tag{12a}$$

$$I_2 = \frac{V_2}{R_2} \tag{12b}$$

⋮

and

$$I_F = \frac{V_o}{R_F} \tag{13}$$

Furthermore, because no current flows into the inverting input, by Kirchoff's current law

$$I_1 + I_2 + \dots + I_n + I_F = 0 \tag{14}$$

Thus,

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \dots + \frac{V_n}{R_n} + \frac{V_o}{R_F} = 0 \tag{15}$$

Solving for V_o ,

$$V_o = -\frac{R_F}{R_1}V_1 - \frac{R_F}{R_2}V_2 - \dots - \frac{R_F}{R_n}V_n \tag{16}$$

Thus, we have obtained an inverting adder. Each input is amplified by the factor $-R_F/R_i$. A block diagram for the inverting adder is shown in Fig. 7(b).

EXAMPLE 1. Figure 8(a) shows a two-input inverting adder. The output voltage is given by

$$V_o = -\frac{10 \text{ k}\Omega}{5 \text{ k}\Omega}V_1 - \frac{10 \text{ k}\Omega}{1 \text{ k}\Omega}V_2 \tag{17}$$

Thus,

$$V_o = -2V_1 - 10V_2 \tag{18}$$

A block diagram is shown in Fig. 8(b).

A more general inverting adder (2) is shown in Fig. 9. Here each impedance Z_i is given by the T-circuit in Fig. 10. The input short circuit impedances at nodes 1 and 2 are given by

$$\begin{aligned} Z_{sc}(s) &= \left. \frac{V_1(s)}{I_2(s)} \right|_{V_2(s)=0} = \left. \frac{V_2(s)}{I_1(s)} \right|_{V_1(s)=0} \\ &= \frac{Z_1(s)Z_2(s) + Z_2(s)Z_3(s) + Z_1(s)Z_3(s)}{Z_2(s)} \end{aligned} \tag{19}$$

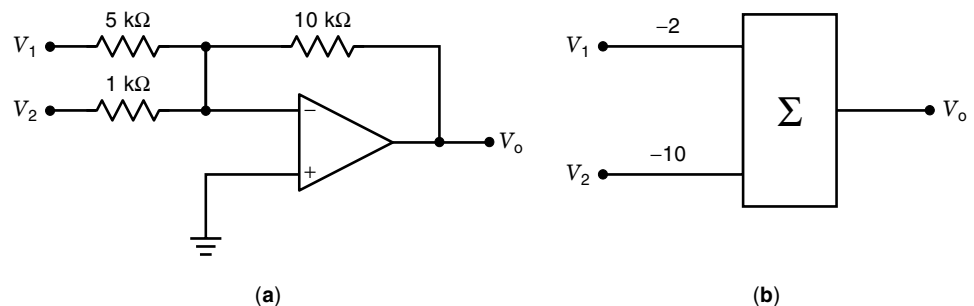


Figure 8. General inverting adder.

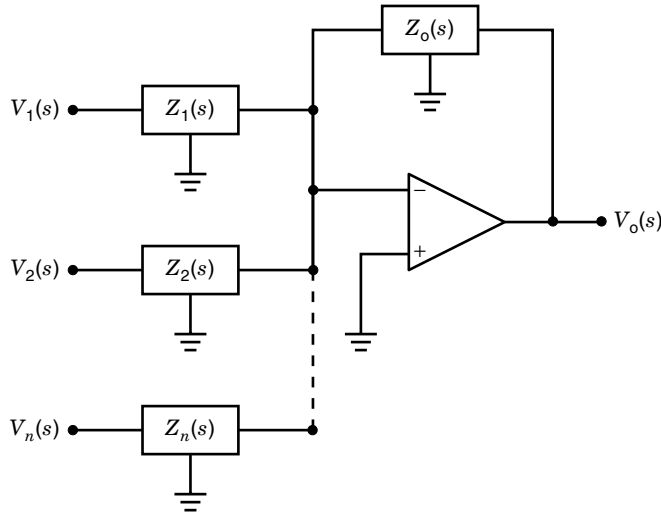


Figure 9. Tee network.

As with the inverting adder, Kirchhoff's current law at node V_g gives

$$\frac{V_1(s)}{Z_1(s)} + \frac{V_2(s)}{Z_2(s)} + \dots + \frac{V_n(s)}{Z_n(s)} + \frac{V_o(s)}{Z_o(s)} = 0 \quad (20)$$

Solving for V_o ,

$$V_o(s) = -\frac{Z_o(s)}{Z_1(s)}V_1(s) - \frac{Z_o(s)}{Z_2(s)}V_2(s) - \dots - \frac{Z_o(s)}{Z_n(s)}V_n(s) \quad (21)$$

EXAMPLE 2. We want the circuit shown in Fig. 11 to have an inverting gain of 100. By solving Eq. (19) with $R_1 = R_3 = 10 \text{ k}\Omega$, $R_2 = 102.04 \text{ }\Omega$.

A noninverting amplifier is shown in Fig. 12. Because the op-amp forces the inverting input voltage to be equal to the noninverting input voltage, the currents I_1 and I_2 are given by

$$I_1 = \frac{V_1}{R_1} \quad (22)$$

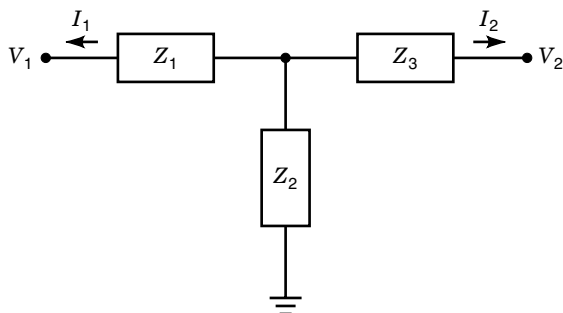


Figure 10. Amplifier with a gain of 100.

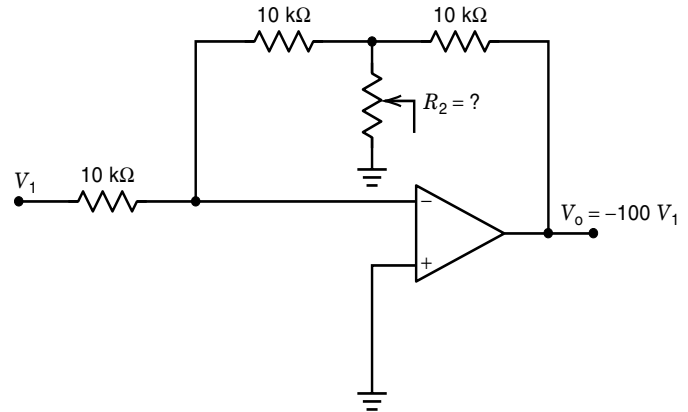


Figure 11. Noninverting amplifier.

and

$$I_2 = \frac{V_o - V_1}{R_2} \quad (23)$$

Using Kirchhoff's current law at the inverting input node,

$$I_2 = I_1 \quad (24)$$

Thus,

$$\frac{V_o - V_1}{R_2} = \frac{V_1}{R_1} \quad (25)$$

Solving for V_o ,

$$\begin{aligned} V_o &= \frac{R_1 + R_2}{R_1} V_1 \\ &= \left(1 + \frac{R_2}{R_1}\right) V_1 \end{aligned} \quad (26)$$

We readily see that the amplification factor for the noninverting amplifier is always greater than unity.

EXAMPLE 3. If we desire to design a noninverting amplifier with a gain of 3, we can choose $R_2 = 2 \text{ k}\Omega$ and $R_1 = 1 \text{ k}\Omega$. Thus,

$$1 + \frac{R_2}{R_1} = 1 + \frac{2 \text{ k}\Omega}{1 \text{ k}\Omega} = 3 \quad (27)$$

The final circuit is shown in Fig. 13.

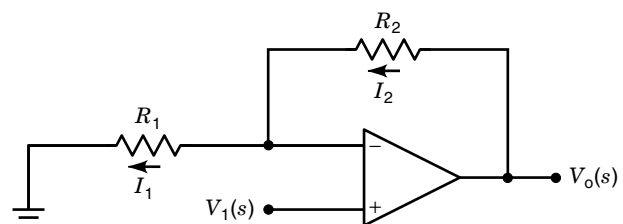


Figure 12. Noninverting amplifier with a gain of three.

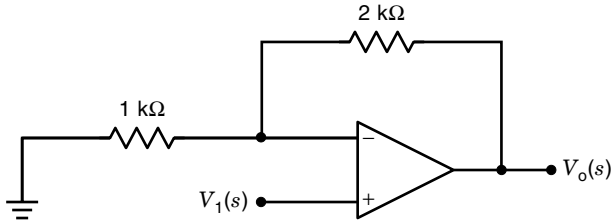


Figure 13. General noninverting amplifier.

A general inverting amplifier is shown in Fig. 14. Similarly to the noninverting amplifier, the output voltage is given by

$$V_o(s) = \left[1 + \frac{Z_2(s)}{Z_1(s)} \right] V_1(s) \quad (28)$$

As before, the gain is noninverting and greater than unity. If $Z_2(s) = 0$ (short circuit), the circuit equation is

$$V_o(s) = V_1(s) \quad (29)$$

that is, we have a unity gain amplifier. Note that $Z_1(s)$ has no effect and can be deleted (an open circuit.) The resulting circuit, shown in Fig. 15 is also called a voltage follower because the output voltage follows the input voltage. Now let us consider the circuit (9) in Fig. 16. Voltage V_+ is given by

$$V_+ = \frac{R_3}{R_2 + R_3} V_2 \quad (30)$$

Using superposition, voltage V_- is given by

$$V_- = \frac{R_o}{R_o + R_1} V_1 + \frac{R_1}{R_o + R_1} V_2 \quad (31)$$

Because the op-amp forces both voltages V_- and V_+ to be equal,

$$\frac{R_3}{R_2 + R_3} V_2 = \frac{R_o}{R_o + R_1} V_1 + \frac{R_1}{R_o + R_1} V_2 \quad (32)$$

Solving for V_o ,

$$V_o = \frac{R_3(R_o + R_1)}{R_1(R_2 + R_3)} V_2 - \frac{R_o}{R_1} V_1 \quad (33)$$

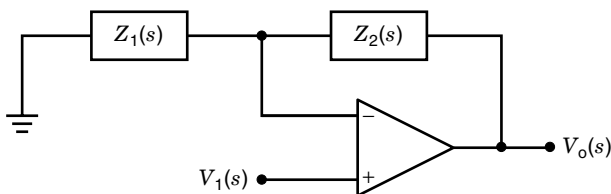


Figure 14. Voltage follower.

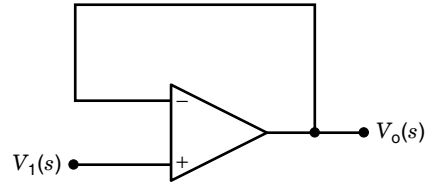


Figure 15. Differential amplifier.

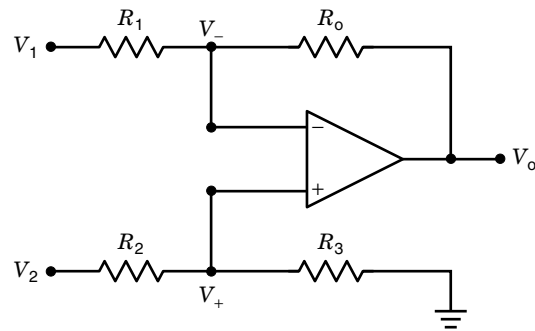
Thus, we see that the circuit takes the difference of the input voltages. Therefore, this circuit is called a differential amplifier. By choosing $R_o = R_3$ and $R_1 = R_2$, we can write Eq. (33) as

$$V_o = \frac{R_o}{R_1} (V_2 - V_1) \quad (34)$$

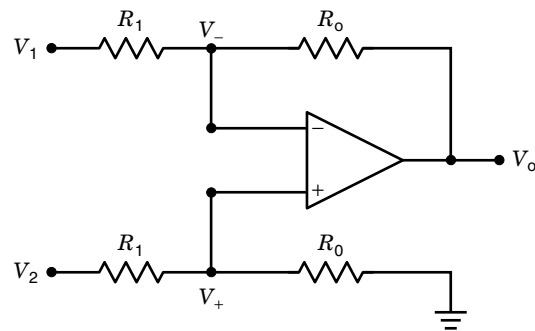
which gives the input voltage difference amplified by the factor R_o/R_1 .

EXAMPLE 4. It is desired to find an amplifier whose output voltage is given by

$$V_o = 10(V_2 - V_1)$$



(a)



(b)

Figure 16. Differential amplifier with a gain of 10.

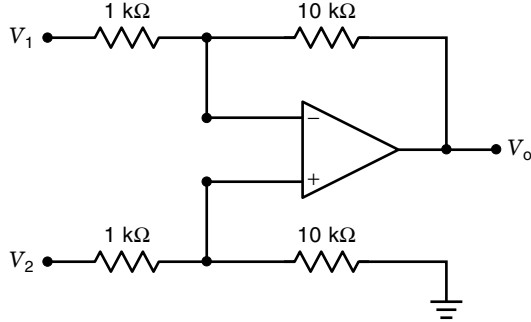


Figure 17. General inverting and noninverting amplifier.

By choosing $R_0 = R_3 = 10 \text{ k}\Omega$ and $R_1 = R_2 = 1 \text{ k}\Omega$ in Fig. 16, we obtain the desired output voltage. The final circuit realization is shown in Fig. 17.

A differential amplifier (2) can be extended to the general combined inverting and noninverting amplifier shown in Fig. 18. Kirchhoff's current law at nodes A and B gives

$$V_A \left[\frac{1}{Z_{IS}(s)} + \frac{1}{Z_{I1}(s)} + \cdots + \frac{1}{Z_{Im}(s)} + \frac{1}{Z_o(s)} \right] = \frac{V_o(s)}{Z_o(s)} + \sum_{i=1}^m \frac{V_{Ii}(s)}{Z_{Ii}(s)} \quad (35)$$

and

$$V_B \left[\frac{1}{Z_{NS}(s)} + \frac{1}{Z_{N1}(s)} + \cdots + \frac{1}{Z_{Nn}(s)} \right] = \sum_{k=1}^n \frac{V_{Nk}(s)}{Z_{Nk}(s)} \quad (36)$$

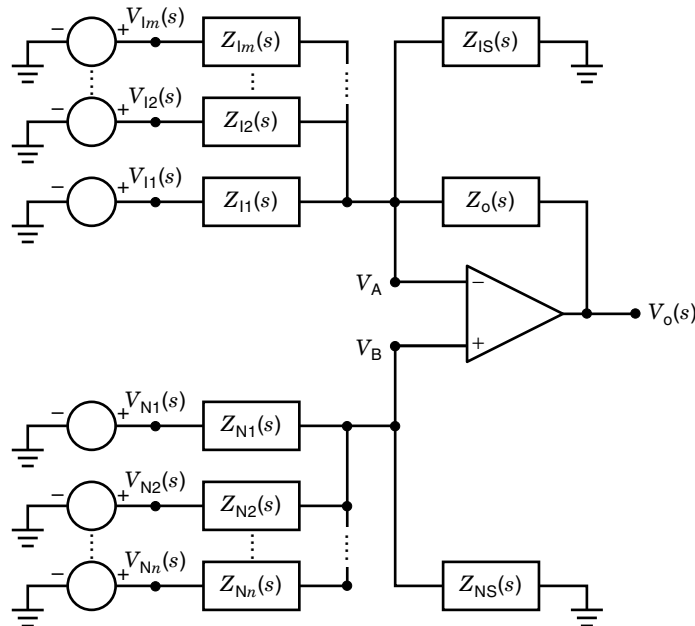


Figure 18. Inverting and noninverting adder.

Defining impedances $Z_A(s)$ and $Z_B(s)$ by

$$\frac{1}{Z_A(s)} = \left[\frac{1}{Z_{IS}(s)} + \sum_{i=1}^m \frac{1}{Z_{Ii}(s)} + \frac{1}{Z_o(s)} \right] \quad (37)$$

and

$$\frac{1}{Z_B(s)} = \left[\frac{1}{Z_{NS}(s)} + \sum_{k=1}^n \frac{1}{Z_{Nk}(s)} \right] \quad (38)$$

and because for an ideal op-amp,

$$V_A = V_B \quad (39)$$

from Eqs. (35)–(39) we can write

$$\frac{V_A}{Z_A(s)} = \frac{V_o(s)}{Z_o(s)} + \sum_{i=1}^m \frac{V_{Ii}(s)}{Z_{Ii}(s)} \quad (40)$$

and

$$\frac{V_B}{Z_B(s)} = \sum_{k=1}^n \frac{V_{Nk}(s)}{Z_{Nk}(s)} \quad (41)$$

Finally, from Eqs. (40) and (41) together with Eq. (39), we can write

$$\frac{V_o(s)}{Z_o(s)} = \sum_{i=1}^m \frac{V_{Ii}(s)}{Z_{Ii}(s)} + \frac{V_B}{Z_A(s)} \quad (42)$$

Solving for V_o ,

$$V_o(s) = Z_o(s) \left[\frac{Z_B(s)}{Z_A(s)} \sum_{k=1}^n \frac{V_{Nk}(s)}{Z_{Nk}(s)} - \sum_{i=1}^m \frac{V_{Ni}(s)}{Z_{Ii}(s)} \right] \quad (43)$$

This equation allows us to design combined inverting and noninverting adders. Each inverting input has a gain

$$G_{Ii}(s) = -\frac{Z_o(s)}{Z_{Ii}(s)} \quad (44)$$

and each noninverting input has a gain given by

$$G_{Nk}(s) = \frac{Z_B(s) Z_o(s)}{Z_A(s) Z_{Nk}(s)} \quad (45)$$

The values of $Z_{IS}(s)$ and $Z_{NS}(s)$ can be picked such that $Z_A(s) = Z_B(s)$, so that the noninverting gains are given by

$$G_{Nk}(s) = \frac{Z_o(s)}{Z_{Nk}(s)} \quad (46)$$

EXAMPLE 5. Consider the circuit in Fig. 19(a). Suppose we want

$$V_o = 2V_{N1} + 3V_{N2} - 4V_{I1} - 2V_{I2}$$

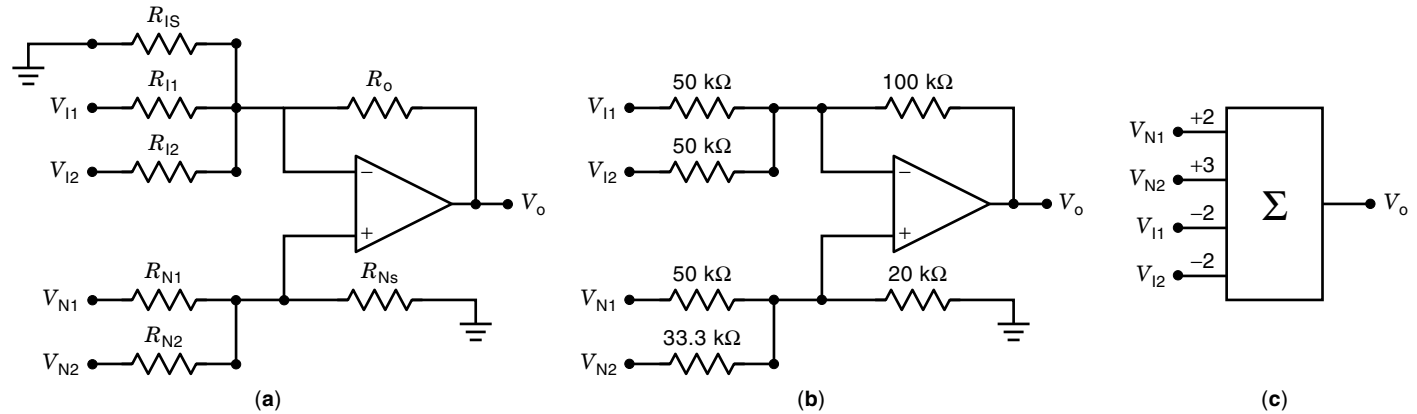


Figure 19. Inverting and noninverting amplifier. (a) Schematic circuit; (b) block diagram.

We start by picking $R_o = 100 \text{ k}\Omega$. We set $R_A = R_B$ by a proper choice of R_{1S} and R_{NS} (usually this can be done by making any one infinite.) From our desired output

$$\begin{aligned} G_{N1} &= 2 \\ G_{N2} &= 3 \\ G_{I1} &= -2 \\ G_{I2} &= -2 \end{aligned}$$

From Eq. (46) for the noninverting gains

$$R_{N1} = \frac{R_o}{G_{N1}} = \frac{100 \text{ k}\Omega}{2} = 50 \text{ k}\Omega$$

and

$$R_{N2} = \frac{R_o}{G_{N2}} = \frac{100 \text{ k}\Omega}{3} = 33.3 \text{ k}\Omega$$

and for the inverting gains

$$R_{I1} = \frac{R_o}{G_{I1}} = \frac{100 \text{ k}\Omega}{-2} = 50 \text{ k}\Omega$$

and

$$R_{I2} = \frac{R_o}{G_{I2}} = \frac{100 \text{ k}\Omega}{-2} = 50 \text{ k}\Omega$$

From Eqs. (37) and (38)

$$\begin{aligned} R_A &= R_{1S} \parallel R_{I1} \parallel R_{I2} \parallel R_o = R_{1S} \parallel 20 \text{ k}\Omega \\ R_B &= R_{NS} \parallel R_{N1} \parallel R_{N2} = R_{NS} \parallel 25 \text{ k}\Omega \end{aligned}$$

By setting $R_{1S} = \infty$,

$$R_A = 20 \text{ k}\Omega$$

Then, the value that makes $R_A = R_B$ is

$$R_{NS} = 100 \text{ k}\Omega$$

The final circuit is shown in Fig. 19(b), and a block diagram is shown in Fig. 19(c).

INTEGRATORS

Integrators are basic building blocks in analog signal processing (10). For example, state variable filters such as the KHN (11) and Tow-Thomas (12) filters are based on integrators within a loop. The most popular integrator circuit is the inverting Miller integrator depicted in Fig. 20. For an ideal op-amp, its transfer function is given by

$$\frac{V_{out}}{V_{in}} = -\frac{1}{sRC} \quad (47)$$

As can be seen, this integrator has its pole at the origin.

Another widely used integrator circuit is the inverting lossy integrator shown in Fig. 21. Its transfer function is

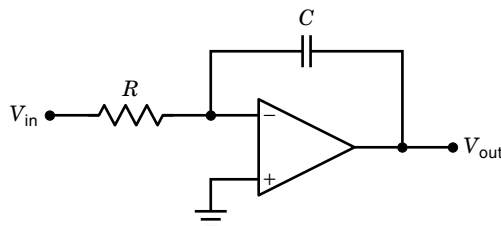


Figure 20. Miller inverting integrator.

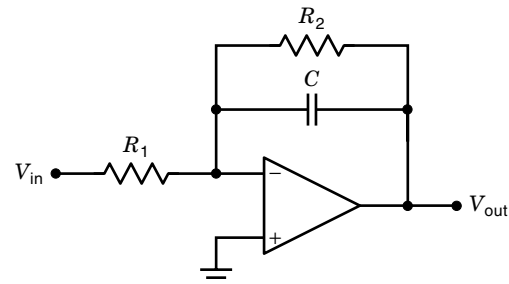


Figure 21. Lossy inverting integrator.

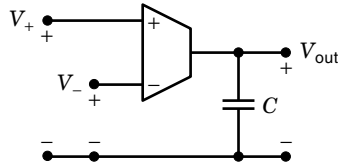


Figure 22. OTA based integrator.

given by

$$\frac{V_{out}}{V_{in}} = -\frac{1}{R_1 C} \frac{1}{s + \frac{1}{R_2 C}} \quad (48)$$

From this transfer function we see that a pole is located on the negative real axis at

$$s = -\frac{1}{R_2 C} \quad (49)$$

Now if we take into account the finite op-amp gain A_0 , routine circuit analysis gives the inverting Miller integrator transfer function as

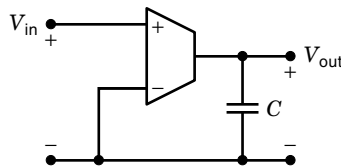
$$\frac{V_{out}}{V_{in}} = -\frac{A_0}{1 + (1 + A_0)sRC} \quad (50)$$

Note that the pole shifts from the origin to a location on the negative real axis given by

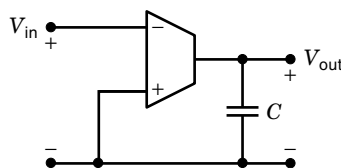
$$s = -\frac{1}{(1 + A_0)RC} \quad (51)$$

Because A_0 is very large, this pole is very close to the origin but on the negative real axis. Thus, the Miller integrator for very high frequencies behaves like a lossy integrator.

Other sources of error in the inverting Miller integrator are the op-amp dc offset voltage and bias current (8). Because



(a)



(b)

Figure 23. (a) Non-inverting integrator. (b) Inverting integrator.

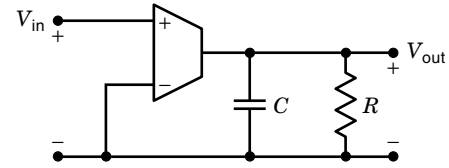


Figure 24. OTA-based lossy integrator with external resistor.

of these dc errors, the integrator output consists of two components, namely, the integrator signal term and an error term. Thus, now V_{out} is given by

$$V_{out}(t) = -\frac{1}{RC} \int V_{in}(t) dt + \frac{1}{RC} \int V_{os}(t) dt + \frac{1}{C} \int I_D(t) dt + V_{DS} \quad (52)$$

An option for high-frequency applications is using an operational transconductance amplifier (OTA). Because $I_{out} = g_m(V_+ - V_-)$ in an OTA, by loading the OTA with a capacitor, as shown in Fig. 22, we obtain (13)

$$V_{out} = \frac{I_{out}}{sC} = \frac{g_m(V_+ - V_-)}{sC} \quad (53)$$

If any one of the input voltages is zero, we obtain either an inverting or a noninverting integrator, as shown in Fig. 23 for an inverting integrator. Note that OTA-based integrators are open loop integrators. We can realize a lossy integrator with the circuit in Fig. 24. In this case the transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m}{C}}{s + \frac{1}{RC}} \quad (54)$$

We can also realize a lossy integrator by producing a resistor with the OTA, as shown in Fig. 25. In this case the transfer function achieved is given by

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m}{C}}{s + \frac{g_m}{C}} \quad (55)$$

If we require realizing Eq. 55 with different numerator and denominator coefficients, then we can use an additional OTA to produce the resistor, as shown in Fig. 26. The resulting

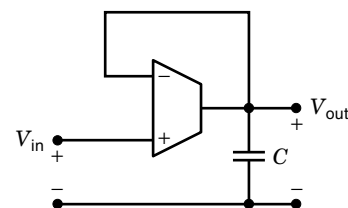


Figure 25. OTA-based lossy integrator without external resistor. The OTA feedback realizes the resistor.

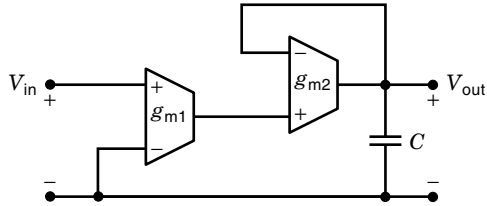


Figure 26. OTA-based lossy integrator with different coefficients.

transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_{m1}}{C}}{s + \frac{g_{m2}}{C}} \quad (56)$$

There are some advantages when using OTAs in integrators:

1. The operating frequency range is greatly increased.
2. The dynamic range is also increased because now we have a current as the output variable for the operational amplifier.
3. Modern OTAs require lower supply voltages.

EXAMPLE 6. As an application of integrators, let us consider the circuit shown in Fig. 27. This circuit is known as a state variable filter, or KHN filter (11), after its inventors. As can be seen, this circuit is formed by two Miller inverting integrators and an inverting and noninverting adder. The transfer function is given by

$$\frac{V_{BP}(s)}{V_1(s)} = \frac{-\left[\frac{1 + R_6/R_5}{1 + R_3/R_4} \frac{s}{R_1 C_1}\right]}{s^2 + \frac{s}{R_1 C_1} \frac{1 + R_6/R_5}{1 + R_4/R_3} + \frac{R_6/R_5}{R_1 R_2 C_1 C_2}}$$

The first op-amp realizes the adder and the last two op-amps realize the integrators.

EXAMPLE 7. Another very popular filter realization is the Tow–Thomas filter (12). This filter is shown in Fig. 28(a). It consists of a lossy integrator followed by a noninverting integrator. The noninverting integrator is formed by a Miller inverting integrator cascaded with a unity inverting amplifier. An alternative realization of this filter using OTAs is shown in Fig. 28(b).

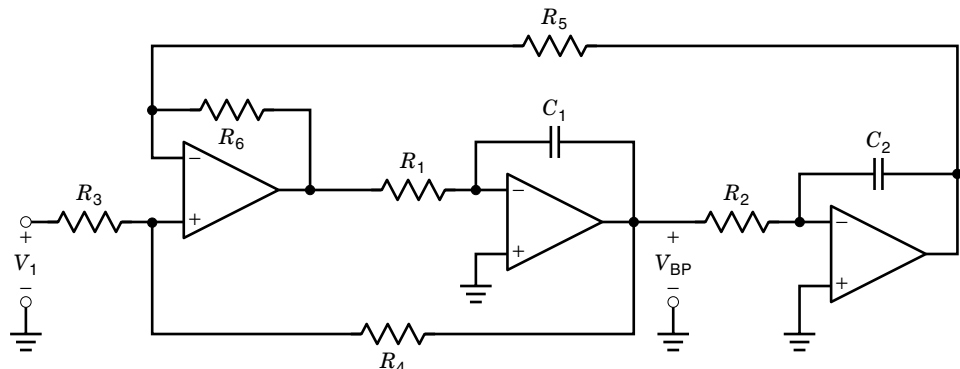


Figure 27. KHN biquad filter.

NONLINEAR ANALOG SIGNAL PROCESSING CIRCUITS

The general form of a nonlinear analog signal processing circuit (2) is shown in Fig. 29, where f is a nonlinear function of the current I_N . In Fig. 29, the output voltage is given by

$$V_{out} = f(I_N) \quad (57)$$

Because no current flows into the inverting input of the op-amp

$$I_N = -I_1 - I_2 \quad (58)$$

and, because the inverting input voltage is zero due to the infinite gain

$$I_1 = \frac{V_{in1}}{R_1} \quad (59a)$$

and

$$I_2 = \frac{V_{in2}}{R_2} \quad (59b)$$

Thus,

$$V_{out} = f\left(-\frac{V_{in1}}{R_1} - \frac{V_{in2}}{R_2}\right) \quad (60)$$

COMPARATORS

A comparator is a circuit that has the transfer characteristic shown in Fig. 30. Here we have a comparison level E_R . The function of this circuit is to compare the input voltage V_{in} with the reference voltage E_R and decide which one is larger. The ideal comparator is described by

$$V_{out} = \begin{cases} L_+ & V_{in} > E_R \\ 0 & V_{in} = E_R \\ L_- & V_{in} < E_R \end{cases} \quad (61)$$

This function is plotted in Fig. 31.

Now let us consider the circuit shown in Fig. 32. The function $f(\cdot)$ is realized by a zener diode [see Fig. 33(a)] for which an ideal description is given by

$$f(i_N) = \begin{cases} E_z & I_N < 0 \\ 0 & I_N > 0 \end{cases} \quad (62)$$

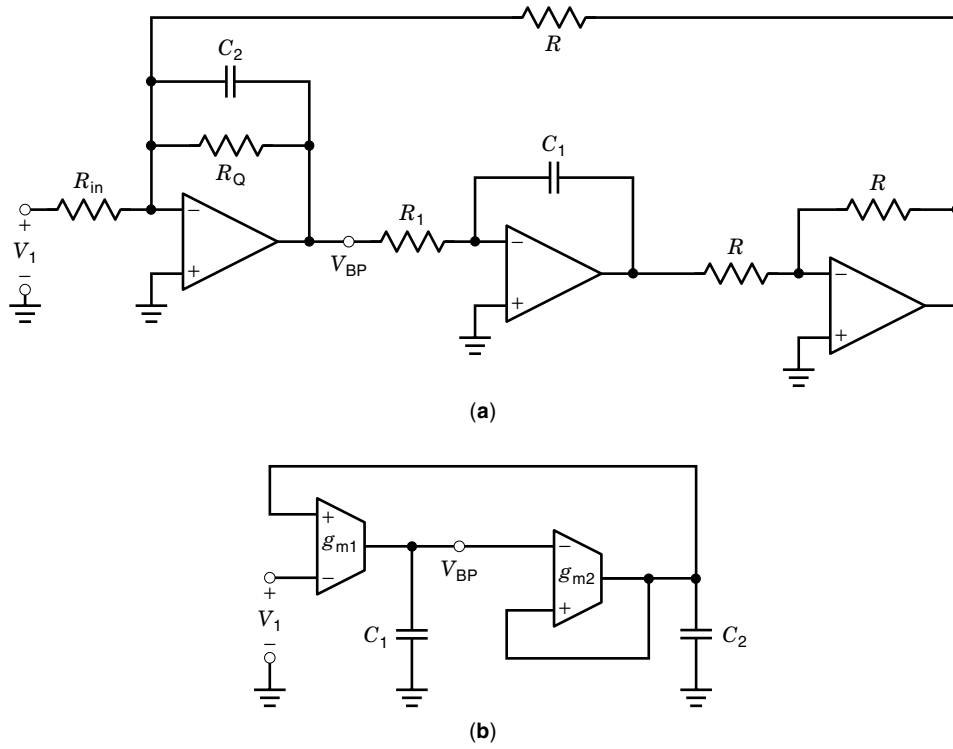


Figure 28. Tow-Thomas biquad filter. (a) With voltage mode op-amps; (b) with OTAs.

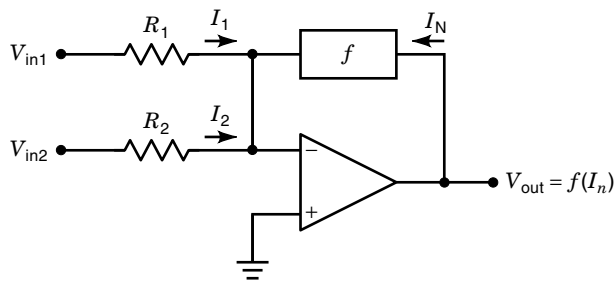


Figure 29. General nonlinear signal processing circuit. F is a nonlinear function.

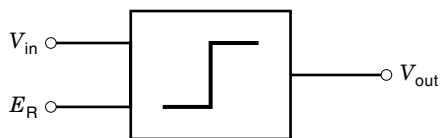


Figure 30. Block diagram for a comparator circuit.

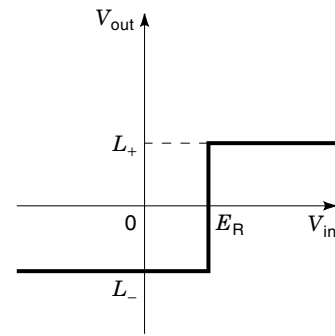


Figure 31. Transfer characteristic for a comparator.

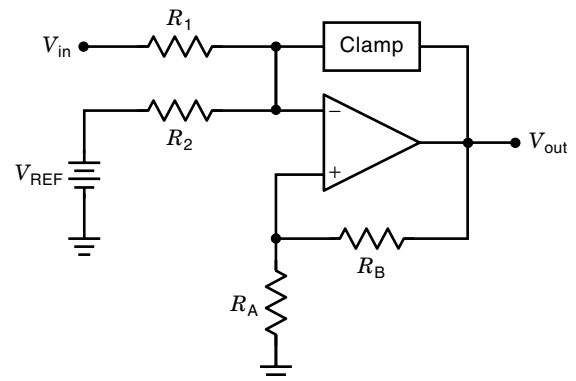


Figure 32. Comparator circuit.

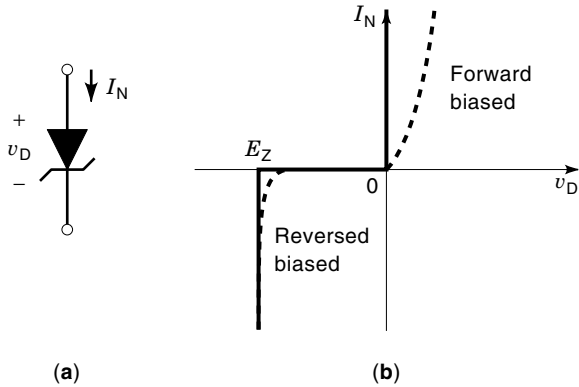


Figure 33. Zener diode. (a) Symbol and variables; (b) I - V characteristic.

as shown in Fig. 33(a). For our circuit,

$$I_1 = \frac{V_{in}}{R_1} \quad (63)$$

and

$$I_2 = \frac{V_{REF}}{R_2} \quad (64)$$

The current I_N is given by

$$I_N = -\frac{V_{in}}{R_1} - \frac{V_{REF}}{R_2} \quad (65)$$

Thus,

$$V_{out} = f\left(-\frac{V_{in}}{R_1} - \frac{V_{REF}}{R_2}\right) \quad (66)$$

Using Eq. (62) in Eq. (66),

$$V_{out} = \begin{cases} E_Z & V_{in} < -V_{REF} \frac{R_1}{R_2} \\ 0 & V_{in} > -V_{REF} \frac{R_1}{R_2} \end{cases} \quad (67)$$

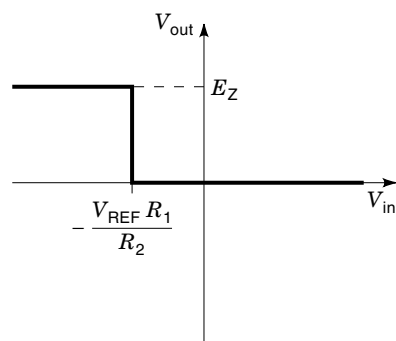


Figure 34. Transfer characteristic for the comparator from Fig. 32.

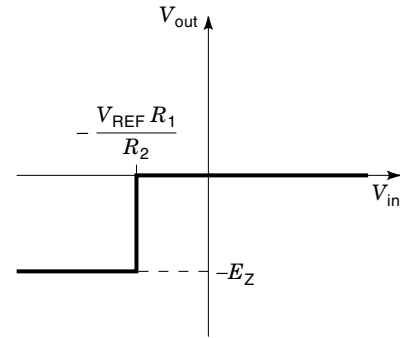


Figure 35. Transfer characteristic for the comparator from Fig. 32 with the zener diode reversed.

that is, the circuit compares the input voltage V_{in} with the reference voltage $-V_{REF}R_1/R_2$. If V_{in} is either smaller or greater than $-V_{REF}R_1/R_2$, then V_{out} is chosen according to Eq. (62). Thus the circuit is a comparator. Its transfer characteristic is shown in Fig. 34. This is equal to the comparator characteristic from Fig. 31 with a sign reversal. By reversing the diode, we get the characteristic shown in Fig. 35. Figure 36 shows a bipolar comparator using a double-anode zener diode. Using two zener diodes with different zener voltages we obtain different output voltages.

A related circuit is the limiter whose function is shown in Fig. 37. A limiter is realized by adding resistive feedback to a comparator, as shown in Fig. 38(a). The circuit acts as a voltage amplifier with gain R_f/R_{in} as long as the output voltage is between $-E_{z2}$ and E_{z1} . When this condition does not hold, then the output is clamped either to E_{z1} for positive output voltage or to $-E_{z2}$ when the output voltage is negative. Thus, the two zener diodes act as a level clamp or feedback limiter

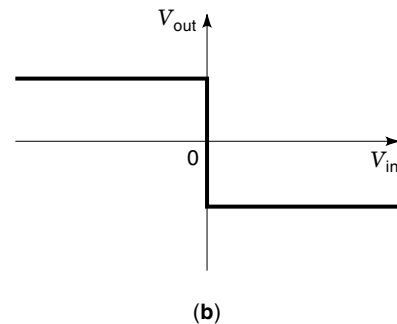
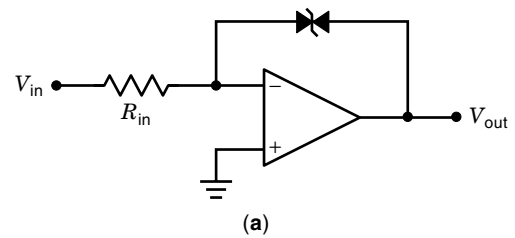


Figure 36. Comparator using double-anode zener diodes. (a) Circuit; (b) transfer characteristic.

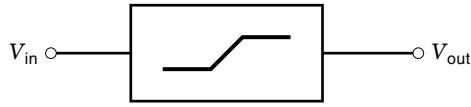


Figure 37. Block diagram for a limiter circuit.

whose purpose is to limit output level excursions but otherwise do not affect the inverting amplifier behavior. This characteristic is shown in Fig. 38(b).

Let us consider the circuit in Fig. 39(a). There are two combinations of possible diode states.

1. D_1 ON, D_2 OFF. If V_{in} is sufficiently positive, V_{out} will be sufficiently negative and eventually e_1 reaches 0 V, and D_1 turns on. Node e_1 acts as a virtual ground, and the output voltage is given by [see Fig. 39(c)]

$$V_{out} = -\frac{E_1 R_B}{R_A} \quad (68)$$

2. D_1 OFF, D_2 ON. This state is reached when V_{in} is negative. Then V_{out} becomes positive, e_2 is eventually 0 V, and D_2 turns ON. Similar to state 1, the equivalent circuit is shown in Fig. 39(d), and V_{out} is given by

$$V_{out} = +\frac{E_2 R_D}{R_C} \quad (69)$$

3. The transfer characteristic is shown in Fig. 39(b). The slopes in the limiting region are given as follows:
For state 1,

$$\frac{dV_{out}}{dV_{in}} = -\frac{R_B}{R_A} \quad (70)$$

and for state 2,

$$\frac{dV_{out}}{dV_{in}} = -\frac{R_D}{R_C} \quad (71)$$

As can be seen the slopes are nonzero. In addition there is rounding in the corners because of the nonideal diode

characteristics. This comparator is called a soft comparator because there is rounding in the corners and nonzero slopes.

A hard comparator, where the clamp levels are well controlled, is shown in Fig. 40. The input-output transfer characteristic for the comparator is shown in Fig. 41. Here the diodes are substituted by transistors. The operation is similar to the comparator from Fig. 39, but the slopes are reduced by the transistors β 's (2).

Suppression of Leakage Currents and Stray Capacitances

If the design calls for a precision comparator where the clamp levels are to be as accurate as possible, then we have to suppress leakage currents from the diodes D_1 and D_2 in the clamp circuit which tend to create an offset error similar to an op-amp offset current. In addition, the use of low resistance values helps to improve circuit speed and reduces the effects of offset currents and parasitic capacitances. The comparator of Fig. 39 is improved in Fig. 42 with extra diodes D_3 and D_4 and resistor R_5 to suppress leakage currents and establish precision comparator levels (2).

HYSTERESIS

A comparator is improved by adding positive feedback to create a hysteresis loop. Hysteresis is usually added to a comparator to give some noise immunity. Figure 43 shows an example (2) where hysteresis adds noise immunity to a comparator. Let us consider the circuit shown in Fig. 44 which is a comparator with positive feedback added. Without the positive feedback, a fast amplifier presents a positive oscillation at the output [see Fig. 43(a).] If the amount of positive feedback is small, the amount of hysteresis in Fig. 45 is given by

$$E_H = \frac{R_A E_W}{R_A + E_W} \quad (72)$$

And, usually, E_H is small, on the order of 10 mV to 20 mV. Figure 43(b) shows how noise immunity has been added to the comparator.

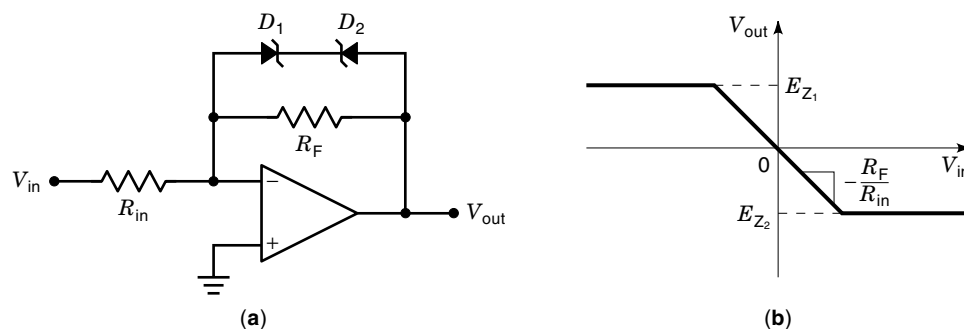


Figure 38. Limiter circuit. (a) Schematic circuit; (b) transfer characteristic.

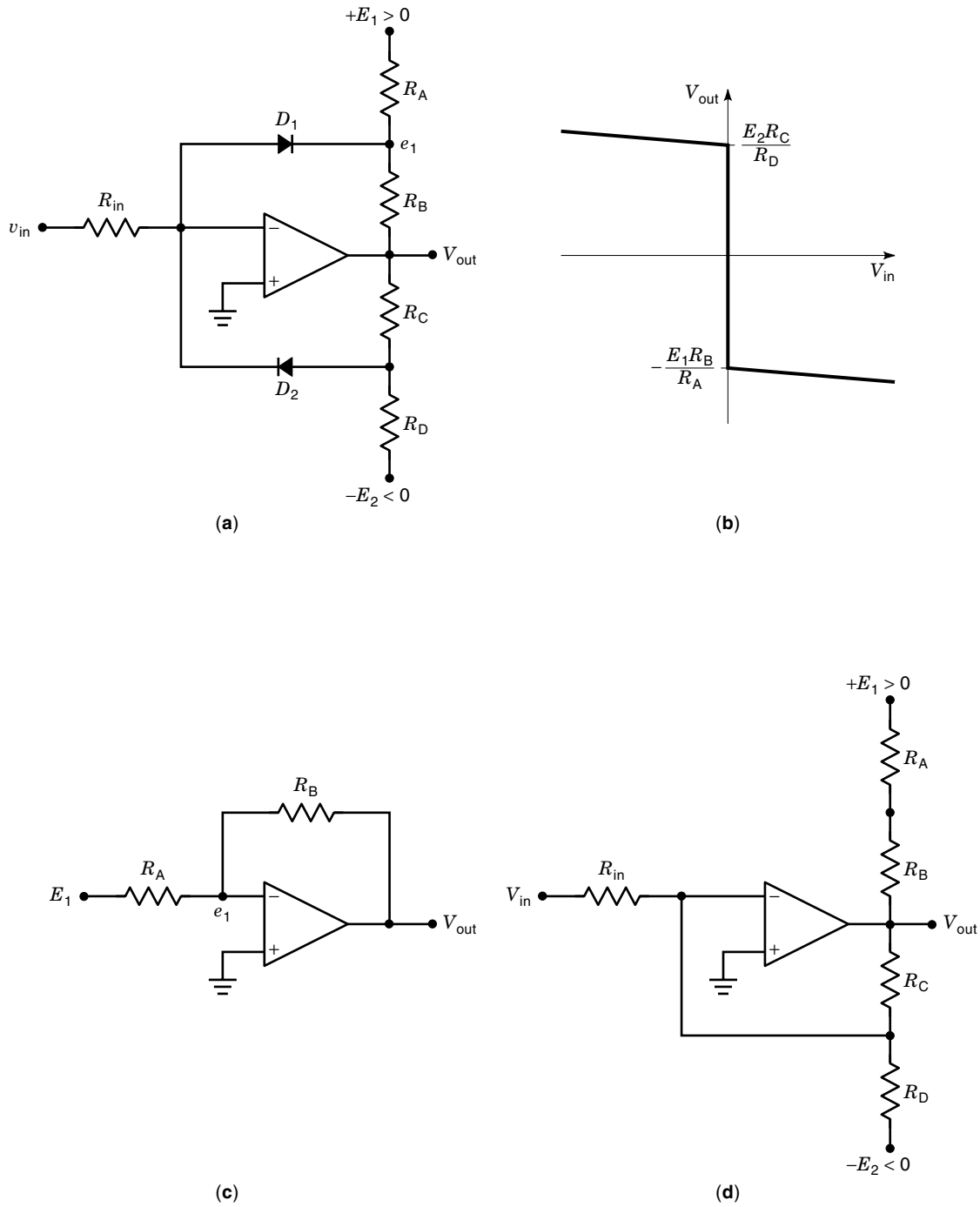


Figure 39. Improved comparator. (a) Schematic circuit; (b) transfer characteristic; (c) equivalent circuit for state 1; (d) equivalent circuit for state 2.

A more accurate circuit is shown in Fig. 46. The dimensions of the hysteresis loop are given by

$$L_+ = \frac{R_2 E_P}{R_1} \quad (73a)$$

$$L_- = -\frac{R_3 E_N}{R_4} \quad (73b)$$

$$S_+ = \frac{R_3 R_6 E_P}{R_4 R_7} \quad (73c)$$

$$S_- = \frac{R_2 R_6 E_N}{R_1 R_7} \quad (73d)$$

The hysteresis loop is shown in Fig. 47.

LOGARITHMIC AMPLIFIERS

Logarithmic amplifiers, simply called log amplifiers (8), are extensively used to produce multipliers and signal compres-

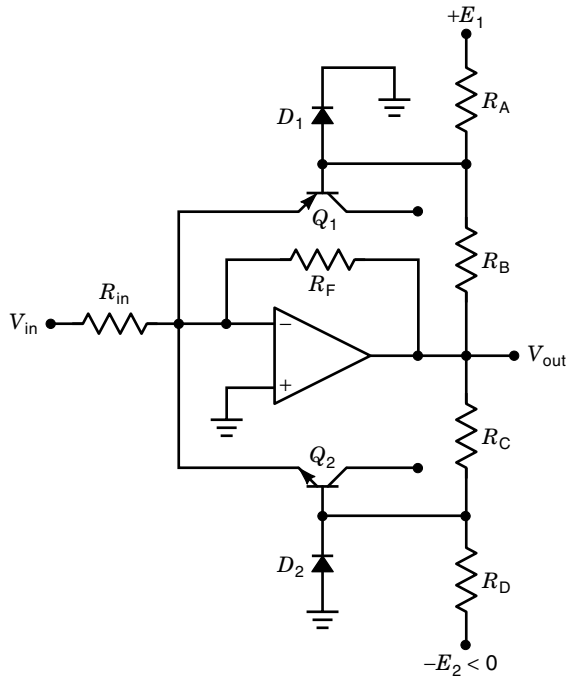


Figure 40. Transistor-based improved comparator.

sors. Figure 48 shows a basic log amplifier circuit. Note that the transistor collector is connected to the virtual ground node. Because the base is also grounded, the transistor voltage-current relationship is

$$I_C = \alpha I_S (e^{-qV_0/kT} - 1) \tag{74}$$

Where $kT/q \approx 25$ mV at 25°C. Equation 74 can be rewritten as

$$V_0 = -\frac{kT}{q} \ln \left(\frac{I_0}{\alpha I_S} + 1 \right) \tag{75}$$

Also, because $\alpha \approx 1$

$$\frac{I_0}{\alpha I_S} \gg 1 \tag{76}$$

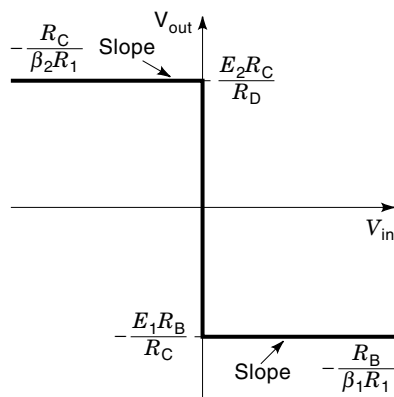


Figure 41. Transfer characteristic for the comparator from Fig. 40.

and

$$I_C = I_1 = \frac{V_{in}}{R_1} \tag{77}$$

then

$$V_0 = -\frac{kT}{q} \ln \frac{V_{in}}{R I_S} \tag{78}$$

Thus, we obtain an output voltage proportional to the logarithm of the input voltage. The only constraint is that $V_{in} > 0$.

External compensation is usually needed (2) for frequency stability. This compensation can be achieved with a capacitor C_C in parallel with the feedback element which in our case is the transistor. Unfortunately, this solution lowers the gain as the operating frequency increases. To compensate for this, we add a series resistor r_c in series with the emitter, placing a limit on the negative feedback resistance through the transistor. This scheme is shown in Fig. 49. Values for C_C and r_c are best determined empirically because parasitic effects play a large role but they are usually in the range of 100 pF for C_C and 1 kΩ for r_c . Note that Eq. 78 for the log amplifier is temperature-sensitive. Furthermore, I_S is also temperature-dependent. A solution for this problem is provided by the circuit shown in Fig. 50. Resistor R_{TC} has a positive temperature coefficient. It can be shown that

$$V_{out} = -\left(1 + \frac{R_2}{R_{TC}}\right) \frac{kT}{q} \ln \frac{V_{in}}{V_{REF}} \tag{79}$$

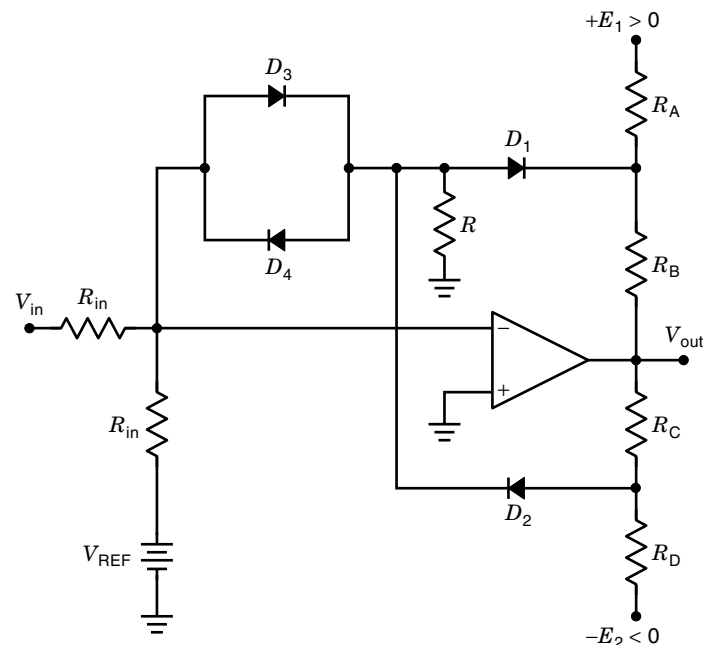


Figure 42. Scheme to reduce leakage currents and stray capacitance.

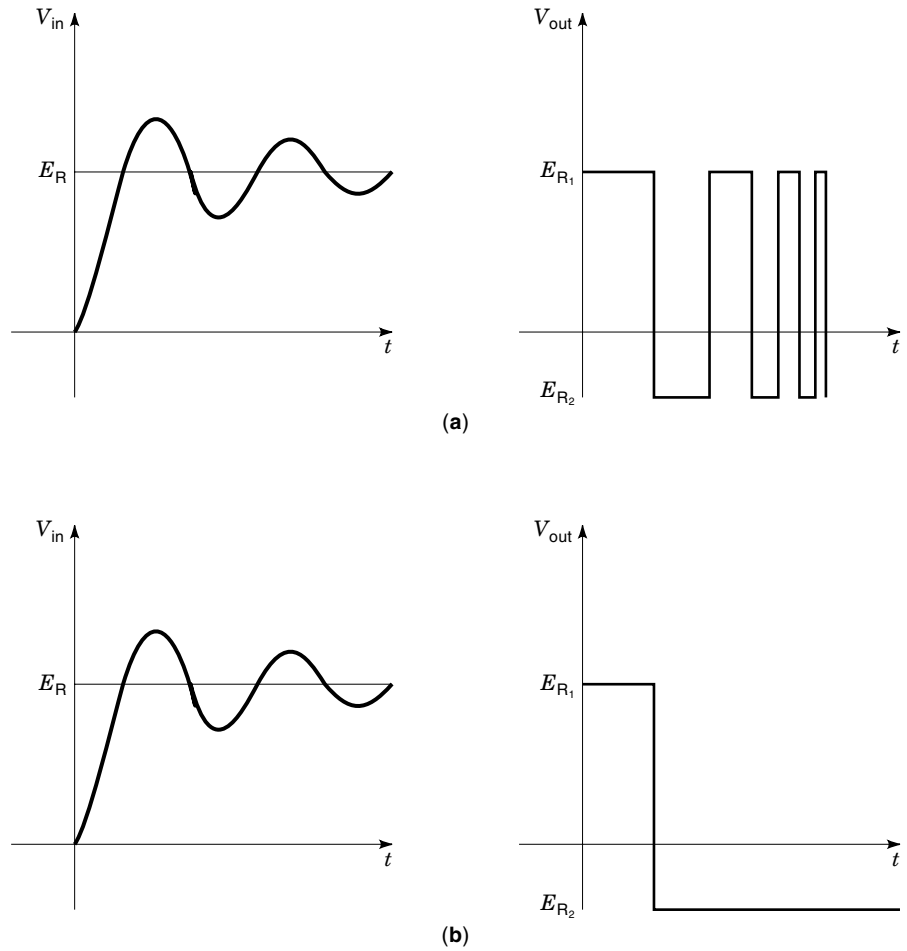


Figure 43. Noise immunity in comparator circuits. (a) Comparator without positive feedback; (b) comparator with positive feedback. The noise immunity is evident.

Note that as T increases, the factor kT/q also increases, but because R_{TC} has a positive temperature coefficient, the first factor in Eq. 79 decreases. By properly matching temperature coefficients and resistor values, negligible variation of V_{out} with temperature is achieved.

Antilog Amplifiers

A basic antilog amplifier (8) is shown in Fig. 51. Because

$$V_{out} = - \left(1 + \frac{R_2}{R_{TC}} \right) \frac{kT}{q} \ln \frac{V_{in}}{V_{REF}} \quad (80)$$

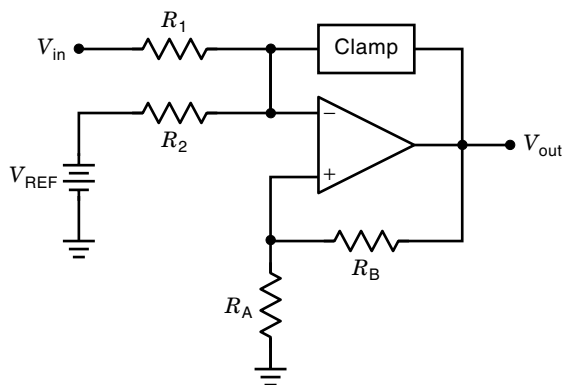


Figure 44. Comparator with added positive feedback to provide hysteresis and noise immunity.

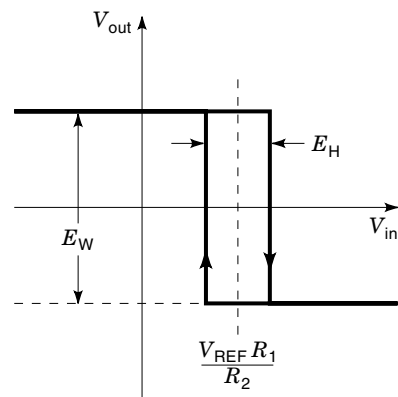


Figure 45. Hysteresis loop for the comparator in Fig. 43.

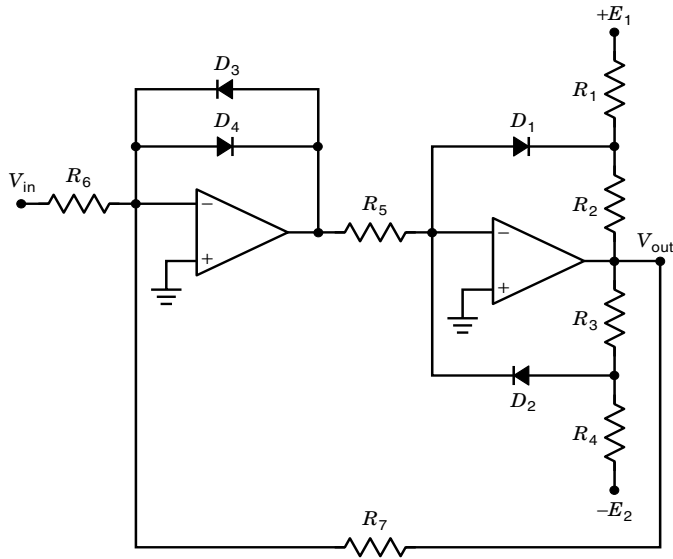


Figure 46. Improved circuit with hysteresis loop.

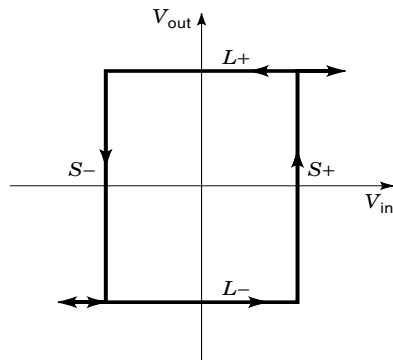


Figure 47. Hysteresis loop for the circuit in Fig. 46.

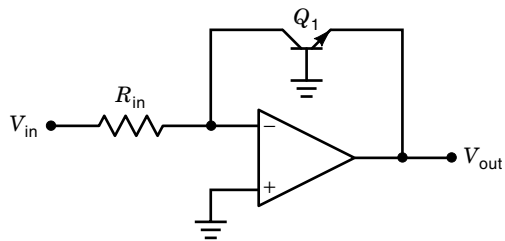


Figure 48. Logarithmic amplifier.

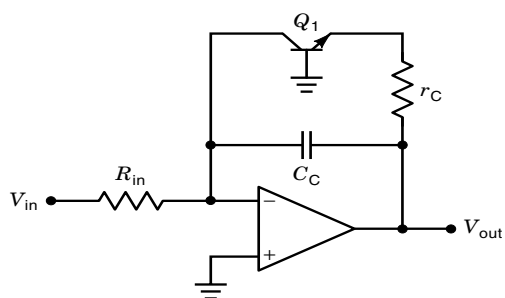


Figure 49. Logarithmic amplifier with compensation.

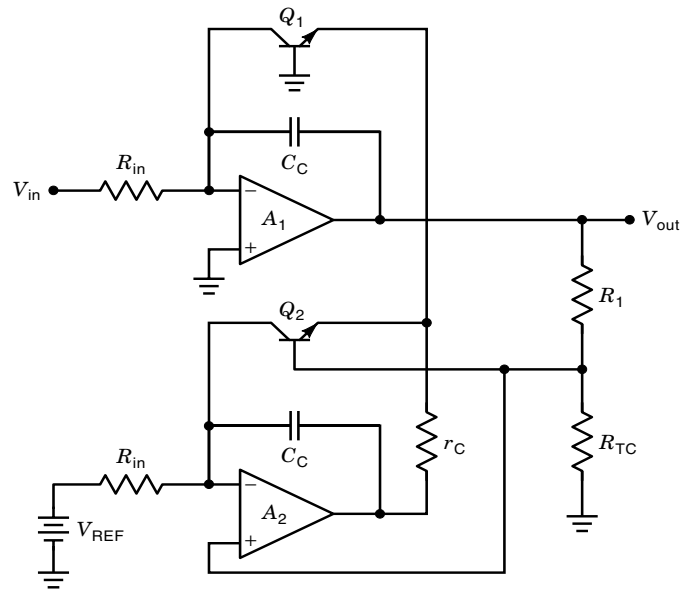


Figure 50. Improved temperature-insensitive logarithmic amplifier. Includes compensation circuit.

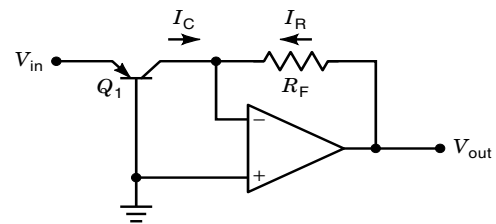


Figure 51. Antilog amplifier.

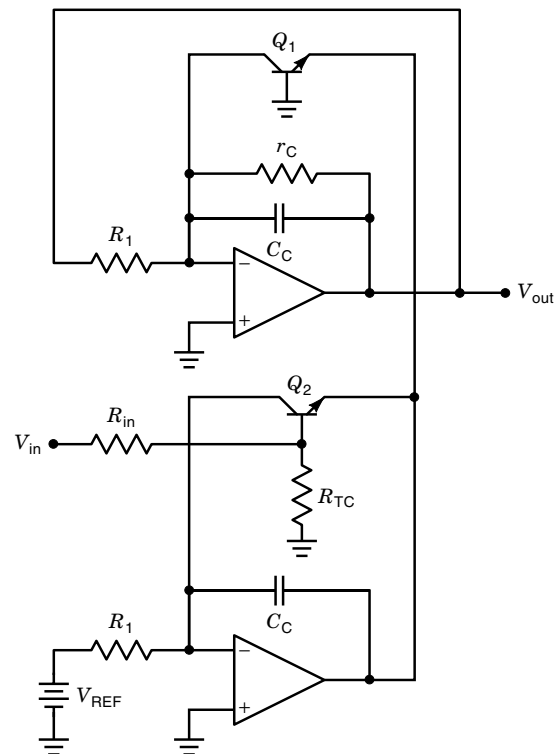


Figure 52. Improved antilog amplifier.

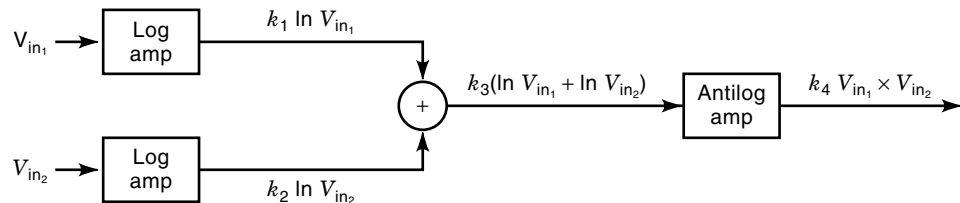


Figure 53. Multiplier circuit realized with log and antilog amplifiers.

For V_{out} , assuming $\alpha \approx 1$ and $I_C/\alpha I_S \gg 1$, we obtain

$$V_{\text{out}} = -RI_S e^{-qV_{\text{in}}/kT} \quad (81)$$

This is equivalent of saying that V_{out} is the antilog of V_{in} . This circuit has the same drawbacks as the log amplifier for stability and temperature dependence. A better circuit is shown in Fig. 52 which includes the compensation circuit (2).

It can be shown that

$$V_{\text{out}} = V_{\text{REF}} \exp \left[-V_{\text{in}} \frac{q}{kT} \frac{R_{\text{TC}}}{R_2 + R_{\text{TC}}} \right] \quad (82)$$

EXAMPLE 8. The most popular application of log and antilog amplifiers is in the realization of multipliers. Figure 53 shows a block diagram of such a multiplier. Each input is fed into a log amp. Then, the logs of the inputs are summed. Recall that the sum of the logarithms is the logarithm of the product. Finally, the antilog amp outputs this product. Then the output has the form

$$V_{\text{out}} = K \cdot V_{\text{in1}} \cdot V_{\text{in2}} \quad (83)$$

where K is a constant that depends upon the circuit parameters. The only limitation in the circuit is that the input signal and reference voltage must have the same polarity for each log amplifier. Thus, our multiplier is a one-quadrant multiplier.

Other useful applications of multipliers are frequency doublers, amplitude modulation, phase detection, oscillators, and automatic gain control (9).

CONCLUDING REMARKS

We have presented circuits for analog signal processing. The circuits are all based on operational amplifiers. Although the most commonly used op-amp is the conventional voltage mode op-amp, simply called op-amp, we have also included the operational transconductance amplifier (OTA) usually found in high-frequency integrated circuits. The circuits presented are those currently used in analog signal processing, and in many cases they are off-the-shelf parts.

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