ANALOG INTEGRATED CIRCUITS

Although digital signal processing brings great advantages such as robustness, flexibility, and precision, analog circuits still play a vital role in today's electronic systems. Interface circuits between the digital processor and the analog "real world" are required, and these analog circuits must operate to demanding specifications to ensure that the performance of the digital sections is not compromised.

Analog integrated-circuit (IC) design exploits the operation of transistors in their active region of operation. Thus the performance of an analog IC is generally closely related to the parameters of the process. Bipolar processes offer high-gain and high-frequency performance, and the fairly recent development of complementary bipolar processes, which offer fast vertical p–n–p as well as n–p–n transistors, has made possible the implementation of analog circuits that exploit this process symmetry. Complementary metal oxide semiconductor (CMOS) processes offer the potential for low-power operation at low processing cost, and since CMOS is the technology of choice for digital ICs, the drive in analog IC design is to ex-

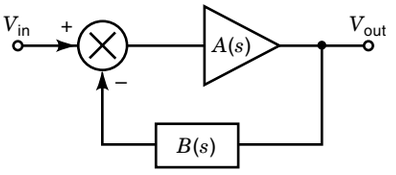


Figure 1. In a system with negative feedback, a proportion of the output signal is subtracted from the input signal, and the resultant "error" signal is applied to the forward amplifier.

ploit CMOS where possible to enable mixed-mode designs to be fully integrated.

When compared to discrete circuit implementation, analog IC design offers close matching between devices, and small device and interconnect dimensions, leading to higher operating frequencies and reduced power consumption. However, the absolute tolerance of integrated components is generally poor, leading to the need for tunability or for robust circuits that are not sensitive to component variations.

This section outlines various circuit design techniques and circuit architectures for the implementation of high-performance analog integrated circuits. The techniques are introduced at a general level to give the reader an appreciation of the important issues involved, and although particular circuit architectures may be shown as an example, the general principles will apply on a wider scale. The core analog design methodology is current-mode analog signal processing, a design style that clearly illustrates the impact process technology has on analog circuit theory, circuit design, and application.

AMPLIFIER ARCHITECTURES

This section describes the relationship between the open-loop architecture of an amplifier and the resulting closed-loop performance. Techniques for achieving maximum bandwidth for a given closed-loop operation are outlined that are inherently suited for IC realization, and the most common IC operational amplifier architectures are described (see also the section entitled "Operational Amplifiers"). Since amplifiers with high open-loop gain are generally used in closed-loop applications, a discussion of negative feedback and stability is given as an introduction.

Negative Feedback and Stability

Negative feedback is often employed around amplifiers with high open-loop gain to achieve a well-defined closed-loop gain and an improved frequency response. In effect the high gain is reduced in exchange for a wider, flatter bandwidth. The classical negative feedback system is shown in Fig. 1. Analyzing this system gives the well-known expression for the closed-loop gain $A_C(s)$:

$$A_C(s) = A(s)/[1 + B(s)A(s)] \tag{1}$$

where $A(s)$ is the open-loop gain of the amplifier and $B(s)$ is the feedback fraction. $T(s) = B(s)A(s)$ is referred to as the loop gain, and the behavior of $T(s)$ with frequency is a key parameter in feedback system design, particularly for determining stability. Clearly if $|T(s)| \gg 1$ or $|A(s)| \gg |A_C(s)|$, then the closed-loop gain is virtually independent of the open-loop gain, and

$$A_C(s) \approx 1/B(s) \tag{2}$$

The closed-loop gain is thus defined by the external feedback components, which can be very accurately manufactured; this is the most attractive and desirable feature of negative-feedback systems. However, though negative feedback is desirable, it results in potential instability when additional negative phase shift is introduced into the loop gain $T(s)$, as then the negative feedback tends to become positive. The phase margin Φ_M is a common figure of merit used to indicate how far the amplifier is from becoming an oscillator. Φ_M is defined as

$$\Phi_M = 180^\circ + \Phi(|T(s)| = 1) \tag{3}$$

If $\Phi_M = 0^\circ$, then the phase of the loop gain $T(s)$ is exactly -180° when the loop-gain magnitude is unity [$|T(s)| = 1$]. From Eq. (1) the closed-loop gain magnitude $|A_C(s)|$ will be infinite, and the circuit will act as an oscillator. For stable operation a phase margin of greater than zero is required, and generally the target is to make $\Phi_M \geq 45^\circ$ for reasonably stable performance. However, excessive Φ_M is undesirable if settling time is an important parameter in a particular application.

To ensure that the amplifier is unconditionally stable, stability must be guaranteed for all values of feedback factor $B(s)$. This is done by maintaining a phase margin $\Phi_M > 0^\circ$ for 100% feedback, that is, when $|B(s)| = 1$. If the feedback network B is taken to be resistive, then any additional phase lag in the loop gain comes from the open-loop amplifier $A(s)$. Tailoring the phase response of $A(s)$ so that the phase lag is less than 180° when $|A(s)| < 1$ will ensure that the amplifier is unconditionally stable.

Two-Pole Amplifiers With Negative Feedback. IC amplifiers typically exhibit a two-pole response in their open-loop gain characteristics, and the relative location in frequency of these two poles is critical in determining the stability of the amplifier under closed-loop operation. It is the IC designer's objective to position these open-loop poles to best advantage so as to achieve maximum bandwidth consistent with versatile and stable performance. Each pole will contribute a low-pass filter function to the open-loop gain expression, and thus the open-loop gain $A(s)$ is given by

$$A(s) = A_0/(1 + s/\omega_{P1})(1 + s/\omega_{P2}) \tag{4}$$

where A_0 is the dc open-loop gain and ω_{P1} and ω_{P2} are the pole frequencies. Each pole introduces 45° of phase lag at the pole frequency $\omega = \omega_P$ and a further 45° at $\omega \geq 10\omega_P$. A typical plot of $A(s)$ versus ω is shown in Fig. 2. At low frequencies where $\omega \ll \omega_{P1}$ the gain is flat; then at ω_{P1} the gain begins to fall at a rate increasing to -20 dB/decade. This roll-off eventually steepens to -40 dB/decade as the second pole is passed at ω_{P2}.

With respect to the phase plot in Fig. 2, at $\omega = \omega_{P1}$ it can be seen that the output lags the input by 45°, rising to 135° at ω_{P2}, to finally 180° at $\omega \geq 10\omega_{P2}$. To ensure unconditionally

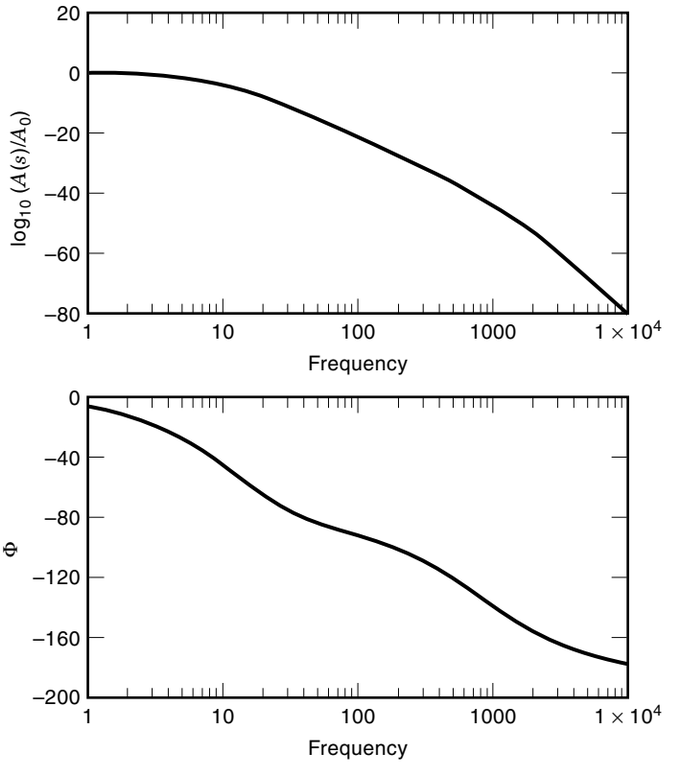


Figure 2. Typical open-loop gain magnitude and phase response for a two-pole amplifier.

stable performance, the second pole must be sufficiently far from the first to achieve adequate phase margin. Figure 3 shows curves of dc open-loop gain A_0 versus the ratio N of the two pole frequencies ($N = \omega_{P1}/\omega_{P2}$) for different values of phase margin. So for a given value of A_0, say $A_0 = 1000$, in order to obtain a phase margin of 45° the ratio N must be approximately 700.

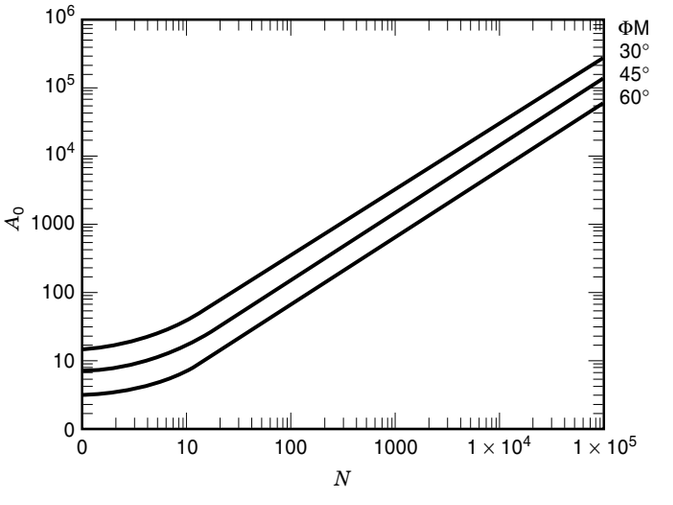


Figure 3. The graphs of open-loop dc gain $A(s)$ versus the open-loop pole ratio ($N = \omega_{P2}/\omega_{P1}$) for a two-pole amplifier show that an increased phase margin (ϕ_M) is obtained by either increasing N or reducing A_0.

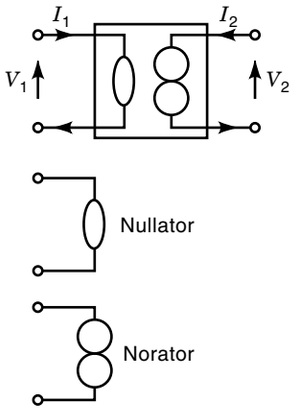


Figure 4. Generalized two-port amplifier, known as the "nullor."

For a further discussion of negative feedback, stability, and phase margin, see Ref. 1.

Early Concepts in Amplifier Theory: The Ideal Amplifier

The amplification of signals is perhaps the most fundamental operation in analog signal processing, and in the early days amplifier circuit topologies were generally optimized for specific applications. However, the desirability of a general-purpose high-gain analog amplifier was recognized by system designers and IC manufacturers alike, since the application of negative feedback allows many analog circuit functions (or *operations*) to be implemented accurately and simply. A general-purpose device would also bring economies of scale, reducing the price and allowing ICs to be used in situations where they may have previously been avoided on the basis of cost. *Operational amplifiers* were thus featured among the first generation of commercially available ICs; however, the concept of an amplifier with high open-loop gain dates back many decades.

In 1954 Tellegen introduced the concept of an *ideal amplifier* (2) as a general building block for the implementation of linear and nonlinear analog systems. This ideal device was a two-port circuit with four associated variables—V_1, I_1 at the input port and V_2, I_2 at the output port. When represented geometrically in four-dimensional space the device could be defined by the planes $V_1 = 0$, $I_1 = 0$ and V_2, I_2 arbitrary. The amplifier would therefore exhibit an infinite power gain between the input and output ports.

In 1964 Carlin proposed the concept of the *nullor* (3), which was a two-port circuit comprising an input nullator and an output norator, as shown in Fig. 4. The port voltage and current of a nullator are always zero, while the port voltage and current of a norator can independently take any value; both components therefore have an undefined impedance. The nullor satisfies the definition of an ideal amplifier as given by Tellegen in Ref. 2. As an electrical circuit component, the transfer properties of the nullor only become well defined if an external network provides for feedback from the output to the input port, as shown in Fig. 5. The output variables (V_2, I_2) will then be determined by the external network in such a way that the input conditions ($V_1 = 0$, $I_1 = 0$) are satisfied. Depending on the nature of the external feedback network,

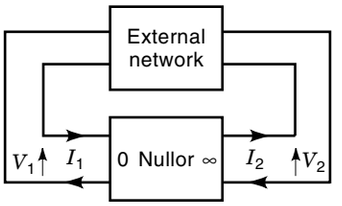


Figure 5. The application of negative feedback around the nullor causes the output voltage and current to be at the levels that ensure that the input port conditions ($I_1 = V_1 = 0$) are satisfied.

many linear and nonlinear analog transfer functions can be implemented. In addition, the external network can usually be chosen such that the resulting transfer function is independent of any source or load. The nullor is thus particularly suitable for separating two stages of an analog system that are mismatched in terms of impedance, thereby eliminating loading effects and allowing stages to be easily cascaded.

The Ideal Amplifier Set

The nullor is the most general case of a universal ideal amplifier, but in practice the undefined input and output resistance levels make this device difficult to implement. Tellegen recognized this problem and proposed a set of four ideal amplifiers (2), each with a well-defined input resistance (R_I) and output resistance (R_O). These four ideal amplifiers are the following.

1. *The Voltage Amplifier (A_V).* This device has an open-circuit input port ($R_I = \infty$), a short-circuit output port ($R_O = 0$), and an open-loop voltage gain ($V_2 = A_V V_1$).
2. *The Current Amplifier (A_I).* This device has a short-circuit input port ($R_I = 0$), an open-circuit output port ($R_O = \infty$), and an open-loop current gain ($I_2 = A_I I_1$).
3. *The Transresistance Amplifier (R_T).* This device has short-circuit input and output ports ($R_I = R_O = 0$), and an open-loop transresistance gain ($V_2 = R_T I_1$).
4. *The Transconductance Amplifier (G_T).* This device has open-circuit input and output ports ($R_I = R_O = \infty$) and an open-loop transconductance gain ($I_2 = G_T V_1$).

For each amplifier, the available power gain is infinite, and the output voltage or output current is directly proportional to the input voltage or input current, independent of any loading effects.

The differing levels of input and output resistance among the various amplifier types suggests that each might perform differently when presented with the same external network. To investigate this further we return to Tellegen's ideal amplifier set (A_V, A_I, R_T, G_T) and derive the transfer functions obtained when each amplifier is configured in turn to implement the various closed-loop functions shown in Fig. 6. These circuits are chosen for the varying combinations of input source and output drive that they impose on the ideal amplifier. The transfer functions for these circuits are obtained by replacing the ideal amplifier by each of the specific types (A_V, A_I, etc.) in turn, and the results are summarized in Table 1 (note $G = 1 + R_2/R_1$).

This table offers valuable insight into the operation of the various amplifier types, since the relationship between the

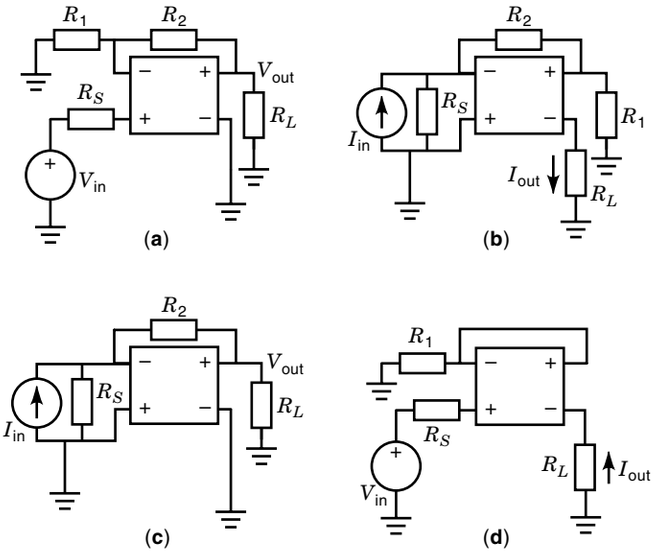


Figure 6. The use of resistive negative feedback allows any one of the four basic closed-loop amplifier configurations to be implemented. In each case the closed-loop gain is precisely defined by the external resistors, provided that the amplifier has a very high open-loop gain. (a) *V–V* Amplifier, (b) *I–I* amplifier, (c) *I–V* amplifier, (d) *V–I* amplifier.

closed-loop transfer function and the circuit components can be clearly seen. Each single transfer function within the table has been divided into two parts. The first term or factor is dependent only on the external feedback resistors and defines the ideal closed-loop gain (that which would be obtained if the amplifier was an ideal nullor). The second term or factor is dependent on the open-loop gain of the amplifier and the magnitude of the source and load resistance, in addition to the gain-setting resistor values. To approximate the behavior of an ideal nullor, the closed-loop transfer functions should be entirely independent of both source and load resistance, and this can be achieved if each amplifier has an infinite open-loop gain (that is, if $A_V = A_I = R_T = G_T = \infty$). The second terms will then become unity, and Table 1 will condense as shown in Table 2. If each of the four amplifier types have infinite open-loop gain, it is irrelevant which particular type is chosen to implement a particular application, since the resulting closed-loop transfer functions reduce to the same basic form.

Closed-Loop Frequency Response

The ideal amplifier requirement of infinite open-loop gain is not possible to achieve, and practical devices have open-loop gains that are both finite and frequency dependent. Assume for simplicity that the amplifier open-loop gain $A(s)$ has a single dominant pole, which can be written as

$$A(s) = A_0/(1 + s/\omega_a) \tag{5}$$

where A_0 is the open-loop dc gain magnitude and ω_a is the open-loop 3 dB bandwidth. At frequencies greater than ω_a,

$$A(s) \approx (A_0\omega_a)/s = \mathrm{GB}/s \tag{6}$$

Table 1. Closed-Loop Amplifier Transfer Functions

	(a) V–V Amplifier	(b) I–I Amplifier	(c) I–V Amplifier	(d) V–I Amplifier
1. A_V	$\left(1+\frac{R_2}{R_1}\right)\left(\frac{A_V}{A_V+1+\frac{R_2}{R_1}}\right)$	$\left(1+\frac{R_2}{R_1}\right)\left(\frac{A_V+1/G}{A_V+1+\frac{R_2}{R_S}+\frac{R_L}{R_1}+\frac{GR_L}{R_S}}\right)$	$R_2\left(\frac{A_V}{A_V+1+\frac{R_2}{R_S}}\right)$	$\frac{1}{R_1}\left(\frac{A_V}{A_V+1+\frac{R_L}{R_1}}\right)$
2. A_I	$\left(1+\frac{R_2}{R_1}\right)\left(\frac{A_I+1/G}{A_I+1+\frac{R_2}{R_L}+\frac{R_S}{R_1}+\frac{GR_S}{R_L}}\right)$	$\left(1+\frac{R_2}{R_1}\right)\left(\frac{A_I}{A_I+1+\frac{R_2}{R_1}}\right)$	$R_2\left(\frac{A_I}{A_I+1+\frac{R_2}{R_L}}\right)$	$\frac{1}{R_1}\left(\frac{A_I}{A_I+1+\frac{R_S}{R_1}}\right)$
3. R_T	$\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_T}{R_T+R_2+GR_S}\right)$	$\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_T}{R_T+R_2+GR_L}\right)$	$R_2\left(\frac{R_T}{R_T+R_2}\right)$	$\frac{1}{R_1}\left(\frac{R_T-R_1}{R_T+R_S+R_L+\frac{R_SR_L}{R_1}}\right)$
4. G_T	$\left(1+\frac{R_2}{R_1}\right)\left(\frac{G_T}{G_T+\frac{1}{R_1}+\frac{G}{R_L}}\right)$	$\left(1+\frac{R_2}{R_1}\right)\left(\frac{G_T}{G_T+\frac{1}{R_1}+\frac{G}{R_S}}\right)$	$R_2\left(\frac{G_T-1/R_2}{G_T+\frac{1}{R_L}+\frac{1}{R_S}+\frac{R_2}{R_LR_S}}\right)$	$\frac{1}{R_1}\left(\frac{G_T}{G_T+\frac{1}{R_1}}\right)$

where GB is known as the gain–bandwidth product of the amplifier. The second terms or factors in Table 1 mainly have the form

$$T(s) = A(s)/[A(s) + K] \tag{7}$$

Substituting Eq. (6) into Eq. (7):

$$T(s) = (\text{GB}/s)/[(\text{GB}/s) + K] = 1/(1 + sK/\text{GB}) \tag{8}$$

The closed-loop bandwidth of the circuit is thus equal to GB/K. Since GB is fixed by the open-loop characteristics of the amplifier, the closed-loop bandwidth of a particular circuit will depend on the associated value of K for that circuit. From Table 1, a list of K values for each of the circuit configurations in Fig. 6 can be compiled as shown in Table 3 (note $G = 1 + R_2/R_1$).

Note that some of the entries in Table 1 also contain an additional term in the numerator, $T(s) = [A(s) \pm Z]/[A(s) + K]$. This numerator term indicates a zero in the closed-loop response, at a frequency $\omega = \text{GB}/Z$. If this zero frequency is much higher than that of the pole, then the closed-loop bandwidth will still be determined by the pole K value. However if $Z > K$ then the closed-loop response will exhibit peaking and may become unstable. In this situation, additional external components would be required to bring the pole frequency down below the zero and to restore stability. For the present we assume that all circuits have $K \gg Z$, and thus the Z term can be neglected.

The K values in Table 3 indicate how the bandwidth of each circuit depends on the components external to the amplifier. In the majority of cases the circuit bandwidth is dependent on the source and/or the load resistance, unlike the situation with an ideal (infinite-gain) amplifier. The four emboldened diagonal K values, however, are independent of source and load resistance, and their actual values are identical to the closed-loop gain terms in Table 1. For each of these circuits the product of the closed-loop gain and the closed-loop bandwidth remains constant, and there is a gain-bandwidth conflict.

Circuit 1(a) in Tables 1 and 3 represents the conventional voltage operational amplifier with voltage-sampling voltage feedback, and the fixed gain-bandwidth product is a well-known limitation of this device. However, the other entries in column 1 show clearly why operational current, transresistance, or transconductance amplifiers have not been popular in realizing voltage amplifier applications, since their K values are related to the source and/or load impedance. These circuits would thus exhibit an ill-defined bandwidth if the source or load conditions were not accurately known, and more seriously could become unstable if the source or load impedance was reactive. Conversely, the other entries in row 1 show that a voltage operational amplifier is not such a good choice for implementing circuits with closed-loop current, transconductance, or transresistance gain, again because of the poorly defined K values. This reinforces the knowledge that a voltage operational amplifier is best suited for the implementation of closed-loop voltage-mode circuits. In effect, the dominance of the voltage operational amplifier over any other amplifier type has restricted analog signal processing to circuit 1(a).

Source and Load Isolation

Apart from the four emboldened diagonal entries, all the circuits in Table 3 have closed-loop bandwidths that are depen-

Table 2. Ideal Closed-Loop Amplifier Transfer Functions

All Amplifiers	(a) V–V Amplifier	(b) I–I Amplifier	(c) I–V Amplifier	(d) V–I Amplifier
(A_V, A_I, R_T, G_T)	$1 + R_2/R_1$	$1 + R_2/R_1$	R_2	$1/R_1$

Table 3. Closed-Loop Amplifier *K* Values

	(a) *V–V* Amplifier	(b) *I–I* Amplifier	(c) *I–V* Amplifier	(d) *V–I* Amplifier
1. A_V	$\mathbf{1 + R_2/R_1}$	$1 + \frac{R_2}{R_S} + \frac{R_L}{R_1} + \frac{GR_L}{R_S}$	$1 + R_2/R_S$	$1 + R_L/R_1$
2. A_I	$1 + \frac{R_2}{R_L} + \frac{R_S}{R_1}\frac{GR_S}{R_L}$	$\mathbf{1 + R_2/R_1}$	$1 + R_2/R_L$	$1 + R_S/R_1$
3. R_T	$R_2 + GR_S$	$R_2 + GR_L$	$\boldsymbol{R_2}$	$R_S + R_L\frac{R_S R_L}{R_1}$
4. G_T	$\frac{1}{R_1} + \frac{G}{R_L}$	$\frac{1}{R_1} + \frac{G}{R_S}$	$\frac{1}{R_S} + \frac{1}{R_L} + \frac{R_2}{R_S R_L}$	$\mathbf{1/R_1}$

dent on the source and/or load impedance. This situation arises if the open-loop input resistance of the amplifier is comparable to the output resistance of the source, or if the open-loop output resistance of the amplifier is comparable to the load resistance. The resulting interaction between the amplifier and the source or load could be eliminated by the use of voltage followers and current followers, whose ideal properties have already been described in a previous section. The followers would be used to isolate the source and load resistance from the amplifier circuit. Figure 7 shows an example of a voltage amplifier based on a current operational amplifier (A_I).

In this circuit example, source and load isolation is achieved using voltage followers. Conversely, current followers should be used to isolate a voltage operational amplifier (A_V) from a current source or load. Isolation of the amplifier using current and voltage followers thus allows the source and load terms (R_S and R_L) to be eliminated from Table 3 and the K values simplify to those shown in Table 4. Entries marked CF_I or VF_I indicate the addition of an input current follower or voltage-follower, respectively, while those marked CF_O or VF_O indicate the addition of an output current follower or voltage follower, respectively.

Table 4 reveals some interesting facts regarding the relationship between closed-loop gain and closed-loop bandwidth. For example, the only circuits that still have bandwidth dependent on gain are the diagonal circuits that were highlighted in Table 3. These circuits do not seem so attractive now when it is considered that none of the other entries suffer from the gain–bandwidth conflict. Some entries [e.g., 3(a), 3(b), 4(a), 4(b)] have K values that are determined by a single feedback component, leaving the other component free to set the gain independently. Moreover, several entries have K values that are equal to unity, indicating that these particular amplifiers will achieve a maximum bandwidth equal to GB, regardless of the value of closed-loop gain, source, or load resistance.

In spite of the obvious benefits in terms of speed of some of the amplifier architectures listed in Table 4, in practice the voltage operational amplifier (A_V) is still the most popular building block of analog electronics and is generally used to implement closed-loop voltage-mode amplifiers. This is perhaps because the implementation of high-performance voltage and current followers for source and load isolation is nontrivial, since the frequency response of the followers would have to be significantly higher than the main amplifier so as not to degrade the overall performance. However, advances in process technology are now making this approach feasible, leading to the development of new amplifier architectures such as the current-feedback operational amplifier described later.

Practical Amplifier Implementations

Voltage Operational Amplifier. Of the four amplifier types described by Tellegen, the voltage operational amplifier (A_V) has emerged as the dominant architecture almost to the exclusion of all others, and this situation has a partly historical explanation. Early high-gain amplifiers were implemented using discrete thermionic valves that were inherently voltage-controlled devices, and a controlled voltage output allowed stages to be easily cascaded. The resulting voltage operational amplifier architectures were translated to silicon with the development of IC technologies, and the device has since become ubiquitous to the area of analog signal processing. The architecture of the voltage operational amplifier has several attractive features: for example, the differential pair input stage is very good at rejecting common-mode signals. In addition, a voltage operational amplifier only requires a single-ended output to provide negative feedback and drive a load simultaneously, and the implementation of a single-ended output stage is a much simpler task than the design of a fully differential or balanced output.

On the negative side, the architecture of the voltage operational amplifier produces certain inherent limitations in both

Table 4. *K* Values with Source and Load Isolation

	(a) *V–V* Amplifier	(b) *I–I* Amplifier	(c) *I–V* Amplifier	(d) *V–I* Amplifier
1. A_V	$1 + R_2/R_1$	1 (CF_I, CF_O)	1 (CF_I)	1 (CF_O)
2. A_I	1 (VF_I, VF_O)	$1 + R_2/R_1$	1 (VF_O)	1 (VF_I)
3. R_T	R_2 (VF_I)	R_2 (CF_O)	R_2	R_2[a] (VF_I, CF_O)
4. G_T	$1/R_1$ (VF_O)	$1/R_1$ (CF_I)	$1/R_1$[a] (CF_I, VF_O)	$1/R_1$

[a] The K values in these cases become zero when the source and load resistances are neglected—that is, the closed-loop pole is at infinity. These circuits both contain a zero in the transfer function as described by Table 3, where it was also stated that, for stability, the closed-loop pole must be lower in frequency than this closed-loop zero. Adding an additional external resistor (R_2 for circuit 3D, R_1 for circuit 4C) ensures that a closed-loop pole will be present with the K values given here.

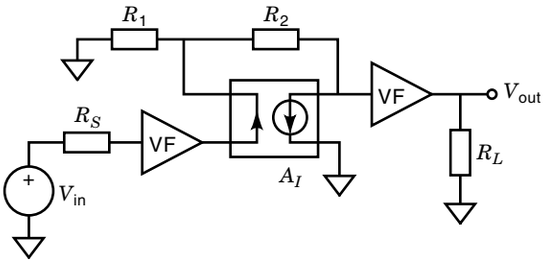


Figure 7. The use of unity-gain-voltage followers (VF) with infinite input resistance and zero output resistance effectively isolates the closed-loop amplifier from the source and load impedances.

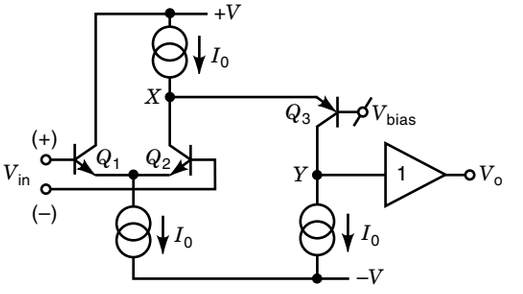


Figure 9. Architecture of a typical single-stage voltage operational amplifier.

performance and versatility. The performance of the voltage operational amplifier is typically limited by a fixed gain–bandwidth product and a slew rate the maximum value of which is determined by the input stage bias current. The versatility of the voltage operational amplifier is constrained by the single-ended output, since the device cannot be easily configured in closed loop to provide a controlled output current (this feature requires the provision of a differential current output). The voltage operational amplifier is therefore primarily intended for the implementation of closed-loop voltage processing (or *voltage-mode*) circuits, and as a result most analog circuits and systems have been predominantly voltage driven. Since it is often desirable to maximize signal swings while minimizing the total power consumption, voltage-mode circuits generally contain many high impedance nodes to minimize the total current consumption.

A schematic of the classical two-stage voltage-feedback operational amplifier is shown in Fig. 8, comprising a long-tail pair input stage, a second gain stage, and an output-voltage buffer to provide load-current drive capability. The amplifier structure in Fig. 8 has two internal high-impedance nodes, node X and node Y. These high-impedance nodes are responsible for introducing two dominant poles into the frequency response, and their relative location is critical in determining the stability of the amplifier. Generally node X is the dominant pole (i.e., at a lower frequency), and additional compensation capacitance (C_p) is typically added at this node to further reduce the dominant pole frequency, thus increasing the pole separation and improving phase margin (see Fig. 3). Any

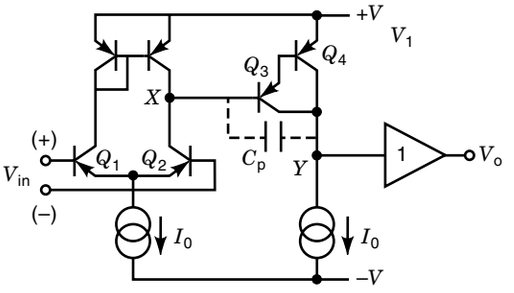


Figure 8. Standard two-stage voltage operational amplifier architecture. The input stage (Q_1, Q_2) provides differential-to-single-ended conversion, high common-mode rejection, and voltage gain, while the second stage (Q_3, Q_4) provides further voltage gain. The output-voltage buffer provides load-current drive capability.

additional capacitance at node Y will reduce the frequency of this nondominant pole, thus reducing the pole separation and phase margin once more.

Figure 9 shows a typical simplified circuit schematic of a single-stage voltage operational amplifier. The input is a differential emitter-coupled pair followed by a folded cascade transistor and an output buffer. The key difference between this architecture and the two-stage design shown in Fig. 8 is that in Fig. 9 node X is a low-impedance node, and so the only high-impedance node in the circuit is node Y. Interestingly the higher-frequency nondominant pole of the two-stage amplifier has now become the dominant frequency pole of the single-stage design, which leads to several advantages.

1. The frequency performance of the amplifier is extended. This frequency extension does not lead to a deterioration in phase margin, but simply means that the phase margin problem is shifted up in the frequency domain.
2. Capacitance at the high-impedance Y node reduces bandwidth but now improves phase margin.
3. A single value of a few picofarads (pF) of grounded capacitor at Y will now act as a satisfactory compensation capacitor, unlike the large capacitor value required in the two-stage design.
4. The slewing capability of this single-stage structure is very good as a result of the much smaller compensation capacitor.

Clearly it is much more straightforward to develop a stable amplifier for high-frequency applications if it has essentially only one voltage gain stage; thus designers of high-frequency operational amplifiers generally opt for a single-gain-stage architecture.

For more details on the transistor-level design of voltage operational amplifiers, see Ref. 1.

Current-Feedback Operational Amplifiers. The current-feedback operational amplifier is a device that has emerged as a high-speed alternative to the voltage operational amplifier (4). The architecture of this device comprises a transresistance operational amplifier (R_T) with an additional input voltage follower (VF); thus it has its origin in circuit 3(a) in Table 4. The current-feedback operational amplifier is intended to be configured in closed-loop form in much the same way as a conventional voltage operational amplifier, but with voltage-sampling current feedback applied from the output back to

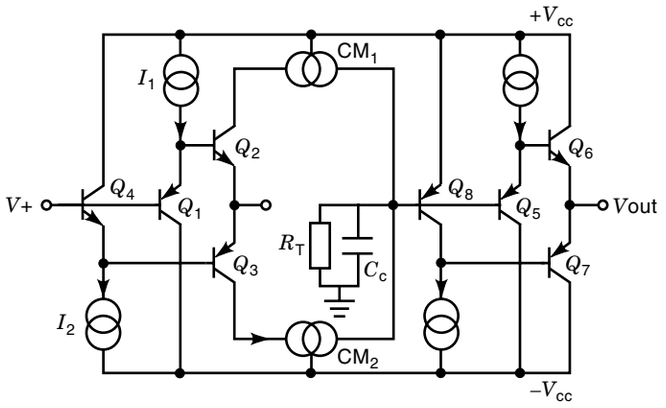


Figure 10. Basic architecture of a current-feedback operational amplifier, where CM_1 and CM_2 represent current mirrors.

the low-resistance input. The resulting closed-loop circuit has a bandwidth that is determined by the feedback resistor R_2, leaving R_1 free to set the gain independently, and there is no fixed gain–bandwidth product. As well as achieving closed-loop bandwidth independent of closed-loop gain, the current-feedback operational amplifier has a much higher slew-rate capability than a conventional voltage operational amplifier. The bias current of the input stage differential pair puts an upper limit on the slew rate of most voltage operational amplifiers; in the current-feedback operational amplifier there is no such limiting factor, and slew rates of 1000 V/μs are commonly quoted for commercial devices.

Figure 10 shows a simplified transistor-level architecture of a typical current-feedback operational amplifier. The noninverting input is a high-impedance input that is buffered to a low-impedance inverting terminal via a class AB complementary common-collector stage (Q_1 to Q_4). In practice a higher-performance topology would be employed for this input buffer to eliminate voltage offsets. The inverting input is a low-impedance current input to which feedback is applied. In contrast, both the noninverting and inverting inputs of a voltage operational amplifier are of high impedance.

In Fig. 10, the collector currents of Q_3 and Q_4 are transferred by current mirrors CM_1 and CM_2 to a high-impedance node, represented by resistance R_T and capacitance C_C. Ideally the bias currents I_1 and I_2 will be canceled at the gain node, giving zero offset current. The resulting voltage at this high-impedance node is then transferred to the output by the voltage buffer (Q_5 to Q_8), which provides the necessary low-output impedance for current driving.

As outlined in Table 4, the magnitude of R_2 determines the position of the closed-loop dominant pole f_P, since $f_P = 1/(2\pi C_C R_2)$. This closed-loop pole must be much lower in frequency than any parasitic poles within the circuit to maintain an acceptable phase margin and to ensure closed-loop stability.

Note that the architecture of Fig. 10 is highly symmetrical in that signal currents are carried by both n–p–n and p–n–p devices. This is in contrast to the traditional voltage operational amplifier architecture of Fig. 8, where signal currents flow through n–p–n devices only. Thus the current-feedback operational amplifier requires transistors of both polarities to exhibit high-speed performance. This type of architecture has only recently become commercially feasible with the development of complementary bipolar processes, which allow both n–p–n and p–n–p transistors to be fabricated as high-speed vertical devices.

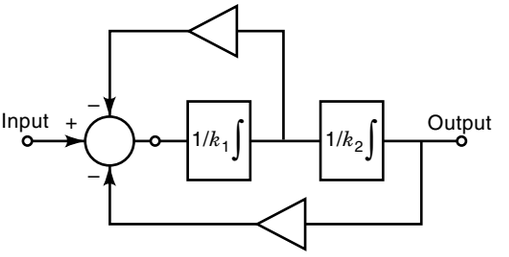


Figure 11. Connection of two ideal integrators to implement a second-order (biquadratic) filter.

TRANSCONDUCTOR–CAPACITOR FILTERS

In the following section, a method of implementing integrated continuous-time filters using transconductors and capacitors (known as Gm-C filters) is described. A basic outline of the approach and certain aspects of transconductor design and performance are considered.

Gm-C Filters

There are three main methods for the implementation of IC continuous-time filters of high order, namely, the cascade approach, the multiple-loop feedback or coupled-biquad approach, and the LC-ladder simulation approach (5). In the first two methods, the high-order function is factorized into subnetworks of second-order sections. The resulting second-order biquad network can thus be considered as an intermediate building block for high-order filters. As shown in the block diagram of Fig. 11, the second-order filter is typically composed of two integrators embedded in negative-feedback loops. For LC-ladder simulation (third approach), integrators are again used to simulate the performance of individual inductors (gyrator filter method) or to simulate the overall ladder filter response (signal-flow graph method). Therefore most continuous-time filters contain integrators as basic building blocks.

To date, the most popular technique for realizing high-frequency continuous-time integrators is to use transconductors and capacitors (G_m–C) (6). The popularity of this approach stems from the fact that transconductors are generally open-loop structures and thus are simple to implement in monolithic form, generally have higher bandwidth than operational amplifiers, and can be tuned electronically (7). Figure 12

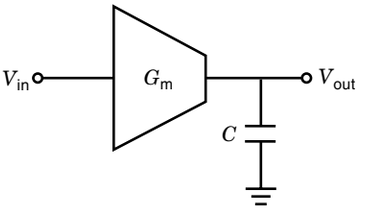


Figure 12. Voltage-mode transconductor–capacitor (G_m–C) integrator.

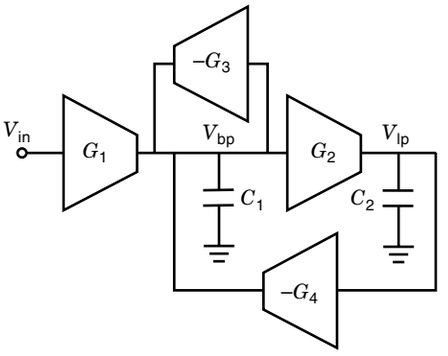


Figure 13. Negative feedback is applied around integrators (G_1, C_1) and (G_2, C_2) via transconductors G_3 and G_4 to implement a voltage-mode G_m–C biquad filter.

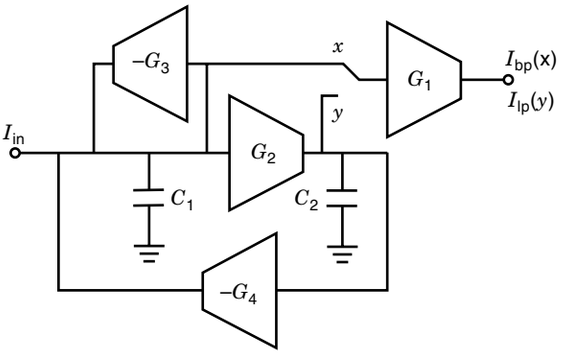


Figure 15. Equivalent current-mode G_m–C biquad filter.

shows a conventional G_m–C integrator, comprising a transconductor, which converts an input voltage into an output current, and a capacitor, which integrates this current to produce an output voltage.

A G_m–C second-order filter can be implemented by interconnecting two integrators as shown in Fig. 13. This circuit simultaneously provides both low-pass and bandpass outputs. The circuits shown in Figs. 12 and 13 are classified as *voltage-mode* circuits, since input and output signals are represented by voltage quantities.

Figures 14 and 15 show current-mode implementations of a G_m–C integrator and biquad filter, respectively, since now the input and output signals are represented by currents. The voltage transfer function of the circuit of Fig. 13 and the current transfer function of the circuit of Fig. 15 are identical and are given by

$$\begin{aligned} T_{lp}(s) &= V_{lp}(s)/V_{in}(s) = I_{lp}(s)/I_{in}(s) \\ &= [G_1(s)G_2(s)]/[s^2C_1C_2 + sG_3(s)C_2 + G_2(s)G_4(s)] \end{aligned} \tag{9}$$

$$\begin{aligned} T_{bp}(s) &= V_{bp}(s)/V_{in}(s) = I_{bp}(s)/I_{in}(s) \\ &= [sG_1(s)C_2]/[s^2C_1C_2 + sG_3(s)C_2 + G_2(s)G_4(s)] \end{aligned} \tag{10}$$

Since the voltage-mode and current-mode biquad filters are essentially adjoint networks (8), then both circuits will exhibit the same sensitivity to component variations. This transfer-function equivalence also implies that both circuits should exhibit similar levels of distortion, caused (for example) by the nonlinear characteristics of the constituent transconductors and capacitors. Although both filter circuits should theoretically exhibit the same small and large signal performance, various other important features such as power supply voltage and current, power consumption, and dynamic range, will differ between the two.

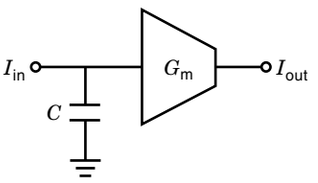


Figure 14. Current-mode transconductor–capacitor integrator.

Transconductor Design Considerations

The performance of a G_m–C integrator or filter relies heavily upon the various characteristics of the transconductor employed. Two important performance criteria are linearity and equivalent input noise, since both will have a major influence on the resulting dynamic range.

The literature available on high-frequency transconductor design is exhaustive (9), and we describe here simple generic examples purely for comparative purposes and not to present a state-of-the-art design. The circuits of Figs. 16 and 17 show transconductors that exploit, respectively, the V–I characteristics of the bipolar transistor (BJT) operating in the forward active region and the metal oxide semiconductor field-effect transistor (MOSFET) operating in the saturation region. The resulting transconductance gain can thus be varied by changing the device bias current. Differential BJT and MOSFET transconductor designs are shown in Figs. 18 and 19, respectively. The advantage of differential structures is that the linearity of the output signal is generally improved by the cancellation of even-order distortion terms.

Various attempts can be made to increase the linearity of the transconductors of Figs. 16 to 19. However since a trade-off between linearity and speed or noise is common in transconductor design, a more linear transconductor is likely to possess a higher noise level and operate at a lower maximum frequency. For example, the linearity of a transconductor can be improved by emitter or source degeneration but at the expense of lower transconductance gain, lower speed, and higher noise.

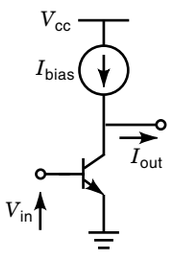


Figure 16. A bipolar transistor (BJT) performs voltage-to-current conversion and thus may be used as a simple transconductor. However the resulting transconductance gain ($G_m = I_C/V_T$) is linear only for small input signal levels, due to the exponential characteristics of the BJT.

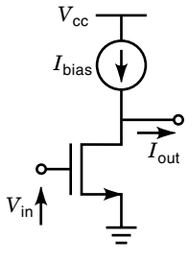


Figure 17. A single MOSFET may be also used as a simple transconductor. However the square-law V–I characteristics of the device again result in a linear transconductance gain only for small input signal levels [$G_m = (2I_D KW/L)^{1/2}$].

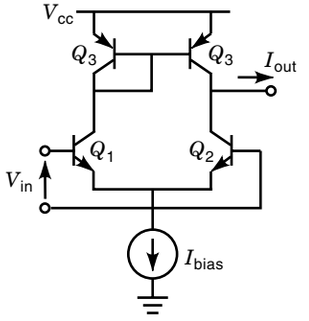


Figure 18. A differential stage extends the input linear range of the simple BJT transconductor.

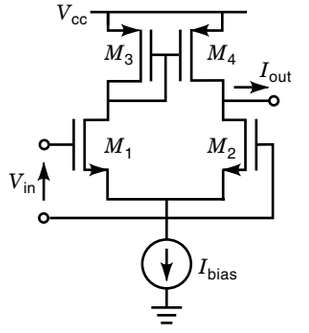


Figure 19. Differential MOSFET transconductor for extended input linear range.

G_m–C filters that employ simple open-loop transconductors such as those shown in Figs. 16 to 19 can operate at very high frequencies, but fairly high levels of output distortion result from the nonlinear operation of the active device. An ideal transconductor would exhibit a gain that remains constant regardless of the input voltage magnitude. In practice this is not the case; beyond a certain input signal level (V_{max}) the transconductance gain will start to vary, and thus the output current is no longer linearly dependent on the input voltage. This will result in an amplitude-dependent transconductance and thus output signal distortion (6). To avoid these problems, the input voltage level must be less than V_{max} to ensure that the transconductor exhibits linear V–I conversion (10).

The dynamic range of a transconductor is defined as the difference between the maximum and minimum input signal levels that can be linearly processed by the transconductor (i.e., DR = $V_{max} - V_{min}$). The maximum input signal V_{max} is generally limited by large-signal distortion as outlined previously, while the minimum input signal V_{min} is generally limited by noise. Any transconductor can be represented as a noiseless device plus an equivalent input-referred noise voltage v_n and noise current i_n. These noise sources can be expressed as

$$v_n^2 = F_V(kT\Delta\omega)/\pi G \tag{11}$$

$$i_n^2 = F_I(kTG\Delta\omega)/\pi \tag{12}$$

where k is Boltzmann's constant, T is absolute temperature, G is the transconductance gain, F_V is the voltage noise factor, and F_I is the current noise factor. By neglecting any noise generated by the biasing circuitry, the values of G, F_V, and F_I of the transconductors in Figs. 16 to 19 can be derived as listed in Table 5. In Table 5, g_m represents the device transconductance, R_E represents resistive emitter degeneration, R_S represents resistive source degeneration, and β represents the bipolar transistor forward current gain. Note that for bipolar transistors, shot noise from the collector-base junction is assumed to be the dominant noise source and for MOS transistors, thermal channel noise is assumed to be the dominant noise source.

The values given in Table 5 show that in all cases F_V is significantly larger than F_I. For ease of analysis in the following sections we will restrict our interest only to transconductors that have equivalent noise sources that can be approximated by Eqs. (11) and (12).

Comparison Between Voltage-Mode and Current-Mode Biquad Filters

As shown in Ref. 10, the voltage-mode filter of Fig. 13 and the current-mode filter of Fig. 15 possess a comparable degree of

Table 5. Voltage Noise Factor and Current Noise Factor of Various Transconductors

Circuit	G	F_V	F_I
Fig. 16	g_m	1	$1/\beta$
Fig. 17	g_m	$\frac{4}{3}$	0
Fig. 16 with R_E	$1/R_E$	$(1 + 2g_mR_E)/(1 + g_mR_E)$	$(1 + g_mR_E)/\beta$
Fig. 17 with R_S	$1/R_S$	$(2/3)(2 + 3g_mR_S)/(1 + g_mR_S)$	0
Fig. 19	g_{m1}	$(8/3)(1 + g_{m3}/g_{m1})$	0

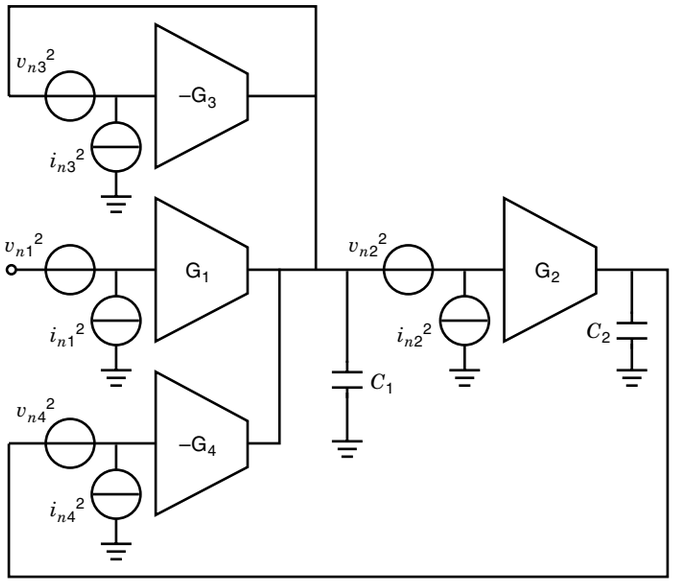


Figure 20. Voltage-mode G_m–C biquad filter with transconductor noise sources explicitly shown.

linearity if identical transconductors are used in both circuits. Hence the main difference in dynamic range of both types of filters lies in their noise performance.

Figures 20 and 21 show the voltage-mode and current-mode G_m–C biquad filters, respectively, with transconductor input-referred noise sources. None of the input-referred noise sources in the voltage-mode filter topology will directly contribute to the output signal, and thus the bandwidth of the output noise is shaped by the filter topology. This is, however, not the case for the current-mode filter, where the input-referred noise source of transconductor (G_1) directly contributes to the output signal, and thus this noise contribution is not shaped by the filter transfer function. Therefore the integrated output noise of the current-mode biquad filter is typically much higher than its voltage-mode counterpart.

In order to compare the current-mode and voltage-mode biquad filters, each filter can be represented by an appropriate figure of merit F_M, defined as

$$F_M = (DR\omega_o^2)/P_Q^2 \tag{13}$$

where DR is the filter dynamic range, ω_o is the operating frequency (i.e., speed), and P_Q is the power consumption. This figure of merit is simply a measurement of the efficiency of the filter. It is shown in Ref. 10 that with respect to the figure of merit, the voltage-mode G_m–C biquad is the design with higher performance, due to the increase in DR for a given P_Q.

TRANSLINEAR CIRCUITS

The Bipolar Translinear Principle

The translinear principle provides a simple and elegant method of realizing mathematical functions, with quite complex functions often implemented by a small number of transistors. Translinear circuits come close to true current-mode operation, since all input and output signals are in the form of currents, and the voltage swings within the circuit need not be considered at all in order to analyze the circuit behavior. Obviously the relationship between the device current and junction voltage is fundamental to the operation of translinear circuits, and voltage swings within the circuit will occur as a result of changes in the current levels. However, the voltage swings in translinear circuits are fairly small; these voltage swings are changes in base-emitter junction voltage (∂V_{BE}) due to changes in the transistor collector current (∂I_C). The limited voltage swings throughout the circuit means that junction capacitors do not have to be significantly charged and discharged, and thus translinear circuits can often operate up to very high speeds, and additionally translinear circuits generally avoid the problem of slew-rate limiting, which occurs when a limited current is available to charge a node capacitance. This freedom from capacitive slewing is one of the reasons for choosing to process signals in the current-mode domain. An excellent treatment of translinear circuits can be found in Ref. 11.

The *translinear principle* was originally proposed in 1975 (12) and was formulated for bipolar transistors. The translin-

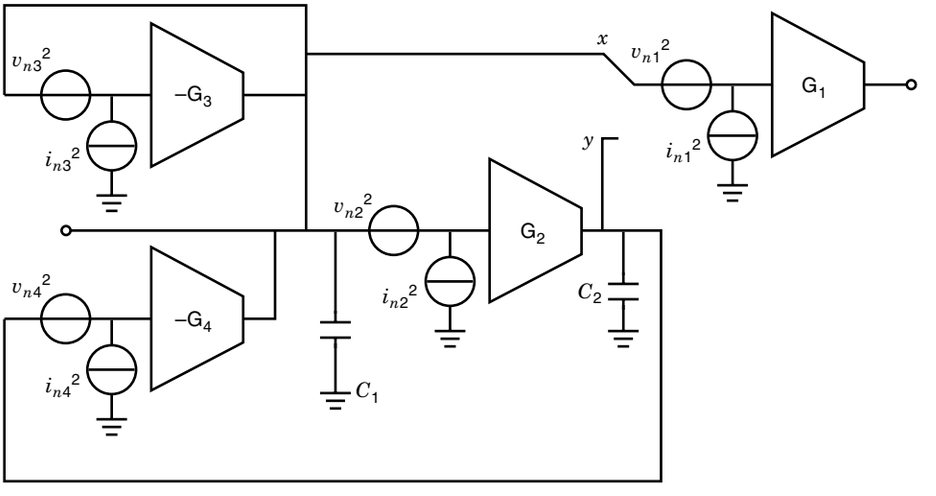


Figure 21. Current-mode G_m–C biquad filter with transconductor noise sources explicitly shown.

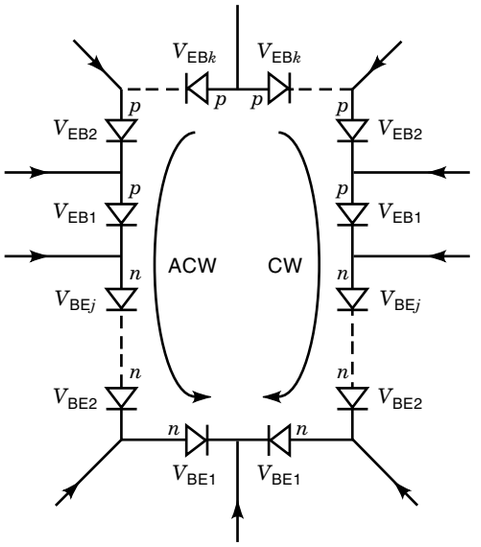


Figure 22. General translinear loop, containing j n–p–n base-emitter junctions and k p–n–p base-emitter junctions in each direction. External currents may flow into or out of the loop at each junction node.

ear principle exploits the linear relationship between transconductance ($\partial I_C/\partial V_{BE}$) and collector current in a bipolar transistor.

$$I_C = I_S \exp(V_{BE}/V_T) \tag{14}$$

$$\partial I_C/\partial V_{BE} = (I_S/V_T)\exp(V_{BE}/V_T) = I_C/V_T \tag{15}$$

where I_C represents the collector current, I_S is the saturation current, V_{BE} is the base emitter junction voltage, and V_T is the thermal voltage.

The translinear principle applies to circuits in which a number of forward-biased base-emitter (V_{BE}) junctions are connected in a continuous loop. The transistors within the loop can be identified as clockwise (CW) or anticlockwise (ACW), depending on the direction of current flow through the junction. The transistors may be n–p–n or p–n–p, but the complete loop must satisfy the following conditions:

1. The number of CW n–p–n V_{BE} junctions is equal to the number of ACW n–p–n V_{BE} junctions.
2. The number of CW p–n–p V_{BE} junctions is equal to the number of ACW p–n–p V_{BE} junctions.

If these conditions are satisfied, then there must be an even number of V_{BE} junctions within the loop.

Consider a loop as shown in Fig. 22 where there are j n–p–n V_{BE} junctions in each direction, and k p–n–p V_{BE} junctions in each direction. Applying KVL around the loop means that the sum of the clockwise junction voltages must be equal to the sum of the anticlockwise junction voltages:

$$\left(\sum V_{BEj} + \sum V_{EBk}\right)_{CW} = \left(\sum V_{BEj} + \sum V_{EBk}\right)_{ACW} \tag{16}$$

The terms on the left-hand side of Eq. (16) refer to clockwise junctions, while the terms on the right-hand side refer to anticlockwise junctions. This notation will be preserved in all equations following. Equation (16) can be rewritten as

$$\sum V_T \ln(I_{Cj}/I_{Sn}) + \sum V_T \ln(I_{Ck}/I_{Sp}) = \sum V_T \ln(I_{Cj}/I_{Sn}) + \sum V_T \ln(I_{Ck}/I_{Sp}) \tag{17}$$

I_{Cj} and I_{Ck} represent the collector currents associated with the respective n–p–n and p–n–p V_{BE} junctions within the loop. I_{Sn} and I_{Sp} represent the n–p–n and p–n–p saturation currents and can be expressed in terms of saturation current densities (J_S) and emitter areas (A), $I_{Sn} = J_{Sn}A$, $I_{Sp} = J_{Sp}A$. Assuming that all devices are at the same temperature and thus have the same thermal voltage, the V_T terms can be cancelled from Eq. (17),

$$\sum \ln(I_{Cj}/J_{Sn}A_j) = \sum \ln(I_{Ck}/J_{Sp}A_k) = \sum \ln(I_{Cj}/J_{Sn}A_j) + \sum \ln(I_{Ck}/J_{Sp}A_k) \tag{18}$$

$$\left[(J_{Sn})^j (J_{Sp})^k\right]^{-1} \ln \prod_{j,k} \{(I_{Cj}I_{Ck})/(A_jA_k)\} = [(J_{Sn})^j (J_{Sp})^k]^{-1} \ln \prod_{j,k} \{(I_{Cj}I_{Ck})/(A_jA_k)\} \tag{19}$$

The J_{Sn} and J_{Sp} terms will cancel from both sides of Eq. (19) (assuming good transistor matching), and by taking antilogarithms,

$$\prod (I_{Cj}I_{Ck})/(A_jA_k) = \prod (I_{Cj}I_{Ck})/(A_jA_k) \tag{20}$$

Equation (20) is a statement of the bipolar translinear principle: in a translinear loop, the product of the clockwise junction current densities is equal to the product of the anticlockwise junction current densities. The translinear principle is fundamentally insensitive to temperature and process parameters, but relies on the tight matching of transistors within the translinear loop. The translinear principle is thus a technique for IC design, since the levels of matching required cannot be achieved with discrete devices.

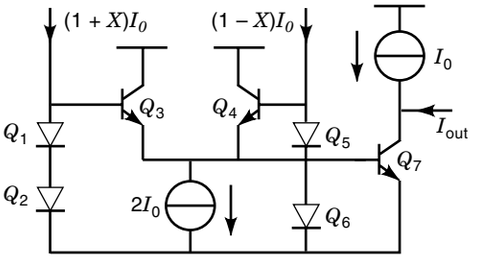


Figure 23. A two-quadrant translinear squaring circuit.

Common Translinear Circuits

The translinear principle finds many applications in the area of *real-time* analog signal processing and is particularly useful for implementing nonlinear functions such as vector sum and difference, multiplication, and division. A number of useful nonlinear functions are outlined in the following section.

Two Quadrant Squarer. Figure 23 shows a two-quadrant squarer circuit. A translinear loop is formed by devices Q_1,

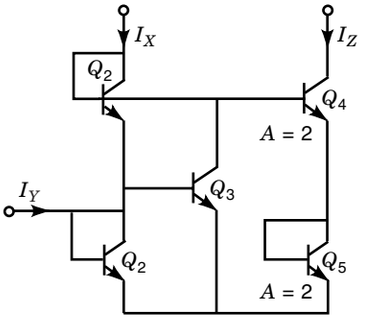


Figure 24. Vector sum circuit.

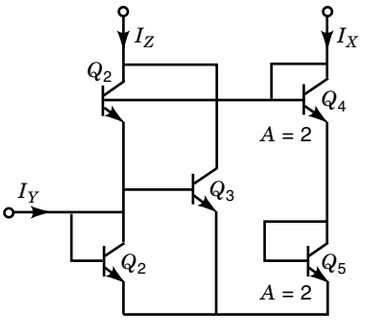


Figure 25. Vector sum circuit.

Q_2, Q_3, and Q_7, where $I_{C1}I_{C2} = I_{C3}I_{C7}$. Substituting the appropriate device collector currents, we obtain

$$(1+X)^2 I_0^2 = I_{C3}I_{C7} \tag{21}$$

A second translinear loop is formed by devices Q_4, Q_5, Q_6, and Q_7, where $I_{C5}I_{C6} = I_{C4}I_{C7}$, and thus:

$$(1-X)^2 I_0^2 = I_{C4}I_{C7} \tag{22}$$

Also by inspection:

$$I_{C4} = 2I_0 - I_{C3} \tag{23}$$

$$I_{C7} = (1+X^2)I_0 \tag{24}$$

Combining Eqs. (21)–(24) gives

$$I_{out} = I_{C7} - I_0 = X^2 I_0 \tag{25}$$

Vector Sum and Difference. Referring to Fig. 24, devices Q_2, Q_1, Q_4, and Q_5 form a translinear loop where Q_4 and Q_5 have double the emitter area of Q_1 and Q_2, thus:

$$I_{C1}I_{C2} = \frac{I_{C4}}{2}\frac{I_{C5}}{2} \tag{26}$$

The device currents can be obtained as

$$I_{C4} = I_{C5} = I_Z \tag{27}$$

$$I_{C1} = (I_X - I_{C3}) = (I_X - I_{C2}) \tag{28}$$

$$I_{C2} = I_{C1} + I_Y = (I_X - I_{C2}) + I_Y \tag{29}$$

$$I_{C2} = I_{C3} \tag{30}$$

Combining Eqs. (26)–(30) gives

$$I_{C2} = (I_X + I_Y)/2 \quad \text{and} \quad I_{C1} = (I_X - I_Y)/2 \tag{31}$$

$$\left(\frac{I_X - I_Y}{2}\right)\left(\frac{I_X + I_Y}{2}\right) = \frac{I_Z^2}{4} \tag{32}$$

$$I_Z = (I_X^2 - I_Y^2)^{1/2} \tag{33}$$

Equation (33) demonstrates that this circuit calculates the vector difference of two input signals. To implement a vector sum, the output current should be exchanged with one of the inputs as shown in Fig. 25. The translinear loop expression is the same as Eq. (26):

$$I_{C1}I_{C2} = \frac{I_{C4}}{2}\frac{I_{C5}}{2} \tag{34}$$

Substituting the appropriate device currents gives the result:

$$I_Z = (I_X^2 + I_Y^2)^{1/2} \tag{35}$$

Equation (35) describes a vector sum calculation.

Analog Mixers and Multipliers. A very important commercial application of the translinear principle is in the implementation of analog multipliers, since these circuits are embedded in many analog IC systems. Applications include automatic gain control, frequency conversion, modulation and demodulation. Figure 26 shows a basic analog multiplier cell, with differential input currents $(1 + X)I_X$ and $(1 - X)I_X$. X thus represents the input signal modulation on a fixed bias current I_X. Differential output currents $(1 + Y)I_Y$, $(1 - Y)I_Y$ are taken from the inner pair of transistors, which are biased by a current source $2I_Y$. Applying the translinear principle to this circuit, we may write:

$$I_{C1}I_{C2} = I_{C3}I_{C4} \tag{36}$$

Neglecting base currents within the circuit leads to

$$I_{C1} = (1+X)I_X,\ I_{C2} = (1-Y)I_Y,\ I_{C3} = (1-X)I_X,\ I_{C4} = (1+Y)I_Y \tag{37}$$

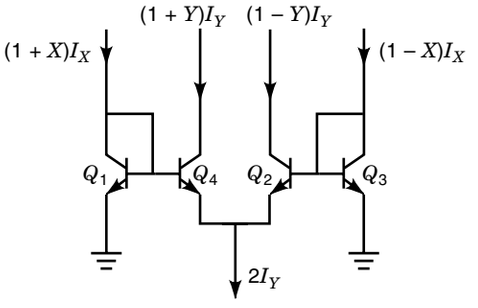
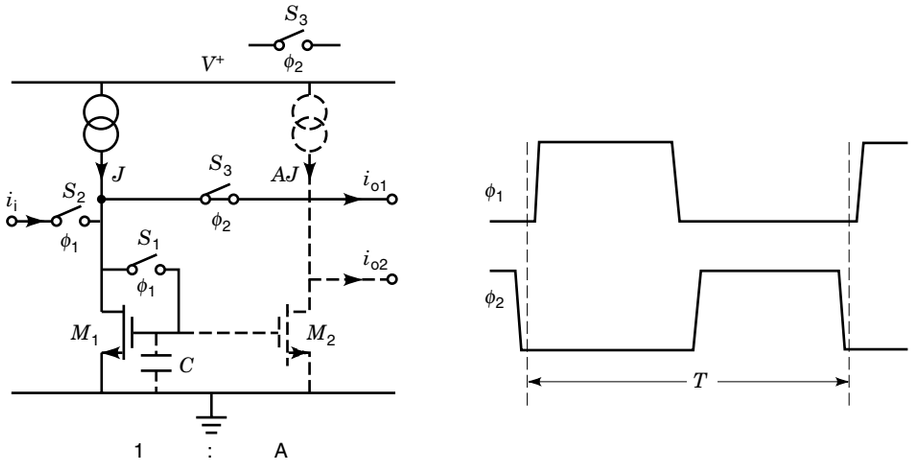


Figure 26. Four-transistor translinear loop used to multiply two input current signals I_X and I_Y.



(**a**) Circuit structure (**b**) Clock waveforms

Figure 27. Basic switched-current memory cell.

Combining Eqs. (36) and (37) leads to the result:

$$X = Y \tag{38}$$

If I_Y is also a fixed bias current, then the currents in the inner pair of transistors are an exact replica of the currents in the outer pair. The current gain A_I is determined by the ratio of input and output quiescent bias current levels, since

$$A_I = [(1+Y)I_Y]/[(1+X)I_X] = I_Y/I_X \tag{39}$$

In this case, the circuit of Fig. 26 is acting as a constant gain cell. If the "tail" current I_Y is also varied, then a multiplication of the two signals is obtained, and this principle is exploited in frequency conversion analog mixers.

An analysis of the cell, including first-order base currents, produces the same result that $X = Y$, and so this cell is *immune* to first-order base current errors. Since the transistors are being used to provide wideband current gain (rather than voltage gain), there are no large voltage swings in the circuit, and thus the cell is not so susceptible to capacitive bandwidth-limiting.

A four-transistor translinear loop (Q_1, Q_2, Q_3, Q_4) forms the core of the double-balanced mixer cell shown in Fig. 27, which is widely used for frequency conversion in wireless communication systems. The collector currents of the differential pair Q_5 and Q_6 are controlled by input voltage V_B, thus

$$I_{C5} = (1+X)I_Q,\ I_{C6} = (1-X)I_Q \tag{40}$$

where X is proportional to V_B. The collector currents of transistors Q_1 – Q_4 are controlled by the input voltage V_A, thus

$$I_{C1} = (1+Y)I_{C5},\ I_{C2} = (1-Y)I_{C5},\ I_{C3} = (1-Y)I_{C6}$$
$$I_{C4} = (1+Y)I_{C6} \tag{41}$$

where Y is proportional to V_A. Thus the differential output current is

$$I_{O1} - I_{O2} = (I_{C1} + I_{C3}) - (I_{C2} + I_{C5}) = (XY)I_Q \tag{42}$$

The multiplication of two input voltages is thus achieved.

SWITCHED-CURRENT PROCESSING

On-chip analog interface circuits are generally a costly part of an IC generally because the cost of inclusion of analog components on primarily a digital process technology is high. In recent years, the quest for ever smaller and cheaper electronic systems has led manufacturers to integrate entire systems onto a single chip. It is now becoming common to find that a single mixed analog and digital (mixed-mode) IC contains both a digital signal processor and all the analog interface circuits required to interact with its external analog transducers and sensors.

An important building block for front-end processing is the analog-to-digital converter (ADC) and the Σ–Δ *modulation* technique (13). This technique is an attempt to trade precision in the analog amplitude domain for precision in the digital time domain by the well-known *oversampling* technique. Now while such a technique places less stringent demands on analog performance, the realization of an oversampling converter in both standard digital CMOS and GaAs MESFET process technologies still requires the use of analog components such as an integrator. An integrator generally requires the use of a linear floating capacitor and so a second layer of polysilicon is required to implement this capacitor, which adds to the overall cost of the technology. The switched-current technique was introduced to overcome this problem. The technique performs precision integration on a single-polysilicon digital CMOS process. In one technology analog precision is traded for digital precision, and in the other analog process technology is traded for digital process technology.

The Switched-Current Approach

While mixed-mode integrated circuits are advantageous from both economic and systems design viewpoints, combining both analog and digital circuits on a single chip makes the circuit design and simulation process considerably more complex. As a typical mixed-mode integrated circuit contains primarily digital circuits, it is natural that the processing technology be tailored to optimize digital performance. Traditionally, the switched-capacitor technique has been employed extensively in the analog interface portion of mixed-mode designs such as

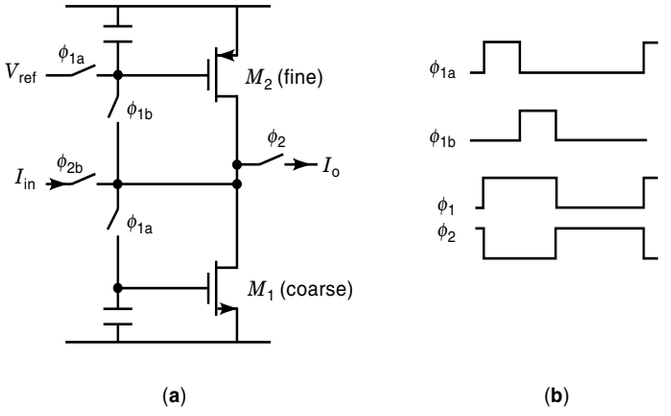


Figure 28. (a) Two-step memory cell (17); (b) clock waveforms.

data converters. The second layer of polysilicon required is not required in pure digital signal processing and may even become unavailable as process dimensions shrink to the deep submicrometer range. This trend towards submicrometer processes is also leading to reduced power supply voltages, which in turn makes the realization of wide dynamic range, high-gain, high-speed operational amplifiers more difficult. The difficulties faced by switched-capacitor (SC) techniques and other voltage-mode analog interface circuits in coping with the advance of digital processing and technology has revived interest in current-mode techniques (14), and in particular an alternative current-mode analog sampled data technique known as switched currents (SI) (15). Unlike SC techniques SI circuits do not require linear floating capacitors or operational amplifiers, and this makes the technique most eminently suited to exploiting pure digital technology for Σ–Δ modulator implementation, for example. Furthermore, the SI technique, as the name implies, operates with current samples and so voltage excursions are limited, leading to the potential for high-speed low-voltage operation. The signal-to-noise ratio may be a problem due to low-voltage excursions, but if the structure is placed within an environment that can tolerate this performance, then the approach is acceptable.

SI Memory Cell. The basis of the SI integrator is the memory cell. The idea on which the switched-current memory cell is based is that an MOS transistor requires no gate current in order to maintain a constant flow of current between its drain and source terminals. The first application of this idea seems to date back to 1972 and was that of storing the current generated by a photodiode (16). However, its use as a discrete time analog signal processing technique is more recent. The basic element of the technique is the so-called switched-current memory (15) or current copier cell, shown in Fig. 27, which functions as a simple current track-and-hold element.

During phase ϕ_1 the input current i_i adds to bias J; transistor M_1 is connected as a diode and so its gate-source capacitance charges up to the V_{GS} due to i_i. During phase ϕ_2, M_1's gate-source capacitance stores the value of V_{GS} and so maintains a drain current output equal to the original input. The cell is essentially acting as a half-wave discontinuous current mirror, or a simple current sample-and-hold analog delay. What has been effectively realized is a half delay $z^{-1/2}$; a cascade of two memories gives a full delay, and with feedback a difference equation is formed to give integration following the classical z transformation.

Much work can be found in the literature (15) on cell performance optimization, in particular, minimizing errors, which in a sense is equivalent to maximizing voltage gain in an operational amplifier used in SC applications. Note that in the memory cell the function of the gate capacitance is to store charge and not transfer charge as in SC techniques. Hence the capacitor can be nonlinear; for this reason single polysilicon technology can be employed.

Figure 28 shows the recently introduced high-performance two-step switched-current (so-called S^{2}I) memory cell and the clock waveforms proposed in Ref. 17. The basic idea is that during phase ϕ_{1a} the coarse memory transistor M_1 is connected as a diode and samples the input while the fine memory M_2 provides the bias. During phase ϕ_{1b} the gate switch of the coarse cell M_1 is open and the transistor holds its gate source voltage on the parasitic gate capacitor C_{GS}. The gate is now isolated and consequently M_1's drain-source current continues to flow during ϕ_{1b}, that is, it is memorized via the nonlinear C_{GS}.

The fine memory cell M_2 is now connected as a diode and will sample the difference between the input current and stored input, namely the error current. During the output phase ϕ_2, the error created in M_1 is subtracted by the same error memorized in M_2 and therefore the output current is ideally free of error. Note that the charge injection from the fine memory switch is treated as an offset and can be automatically canceled when the cell is used in a delay cell or an integrator. Techniques have been recently proposed that allow an increase in the number of fine cells to further reduce errors (18).

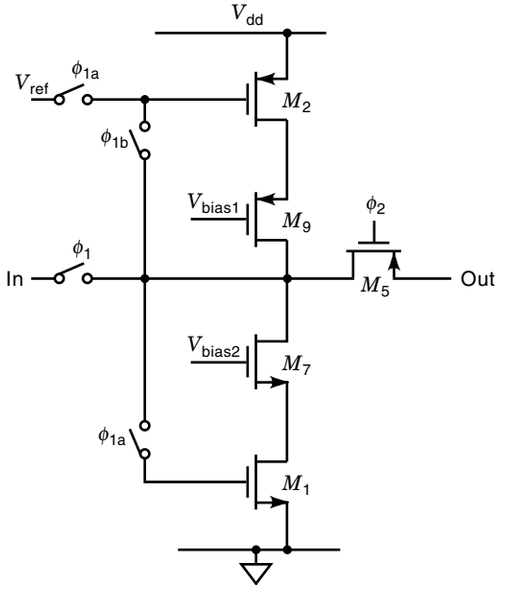


Figure 29. Cascaded S^{2}I memory cell.

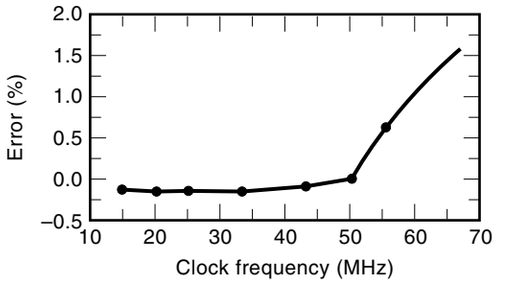


Figure 30. Memory current error versus sampling frequency.

To reduce the effects of channel length modulation a cascaded version of the memory cell is shown in Fig. 29. A simulated performance of the cell based upon parameters of a 0.8 μm CMOS technology and HSPICE is shown in Fig. 30. The curve shows percentage error in cell current versus clock frequency. A maximum error in output current of -0.18% is achieved over an input signal range of ± 50 μA. The error remains constant up to a clock frequency of 50 MHz, beyond which the error begins to rise quite rapidly. Trade-offs have to be made among speed, accuracy, dynamic range, noise, etc., similar to those in SC circuits (19). When designing the cascaded cell various procedures can be employed. The following design procedure can be adopted for optimizing cell performance (20); the optimization is in an approximate priority order. Note that $V_{\rm dd}$ = supply voltage, $L_{\rm x}/W_{\rm x}$ refers to gate length and width of device $M_{\rm x}$, $R_{\rm on}$ represents the switch "on" resistance, $V_{\rm ds}$ = drain–source voltage.

1. Choose $V_{\rm ref}$ close to $V_{dd}/2$, where $V_{dd}/2$ is the bias voltage.
2. Choose L_1 and L_2 close to minimum size to obtain the fastest settling.
3. Set the appropriate bias current by setting M_2 and adjust M_1's width to satisfy the condition $g_{\rm m1} = g_{\rm m2}$.
4. Design the switch such that $1/R_{\rm on}C_{\rm GS}$ is not the dominant pole. Use the minimum length and an aspect ratio of about 4.
5. Choose $L_7 = L_9$ and $L_1 = L_2$ for balance.
6. Adjust the widths of cascade transistors M_7 and M_9 to minimize the V_{ds} variations M_1 and M_2, while adjusting V_{B1} and V_{B2} to ensure the devices are saturated for $I_{\rm in} = \pm I_{\rm in\,max}$.
7. Choose L_5 = minimum size and $(W/L)_5 = 25$ to get a good trade-off between on-resistance and stray capacitance.
8. Finally adjust the width of M_1 and M_2 to get critically damped behavior, giving close to optimum settling performance.

Probably the most attractive performance potential for the SI memory is that of speed at low voltage, and several detailed chapters almost entirely devoted to enhanced SI memory performance can be found in Ref. 15. In memory-cell design, transistor sizing is a very important procedure and many judicious decisions have to be made.

Switched-Current Integrator. A lossless integrator can be easily realised by introducing a feedback loop around a delay cell as shown in Fig. 31. Essentially two memory cells are cascaded to form a delay, and the output of the second is fed back to the input of the first. The integrator output $i_{\rm out1}$ is formed by copying the current in the M_3–M_4 branch, and this gives a noninverting output with a forward Euler transformation of

$$H_{\rm n}(z) = \frac{i_{\rm out1}(z)}{i_{\rm in}(z)} = \frac{\alpha z^{-1}}{1 - z^{-1}} \tag{43}$$

and by using an inverting output (copying the M_1/M_2 current) the transfer becomes

$$H_{\rm i}(z) = \frac{i_{\rm out1}(z)}{i_{\rm in}(z)} = \frac{\alpha z^{-1/2}}{1 - z^{-1}} \tag{44}$$

which is the midpoint transformation of a continuous-time noninverting lossless integrator.

GaAs Memory-Cell Development

Traditionally circuits implemented in gallium arsenide technology have proved to be capable of higher operating speeds than their silicon counterparts due to the lower parasitic elements associated with the process combined with the higher electron mobility of the MESFET.

A first-generation GaAs MESFET switched-current memory cell was proposed in Ref. 21. The main problem with this

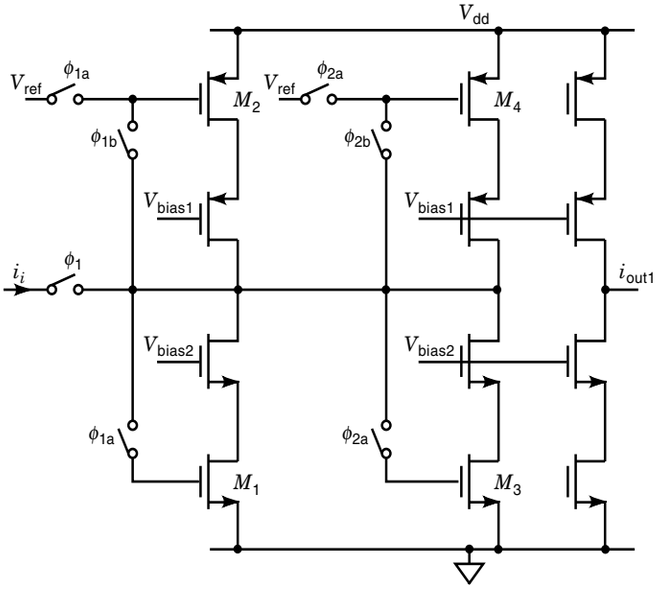


Figure 31. Lossless integrator.

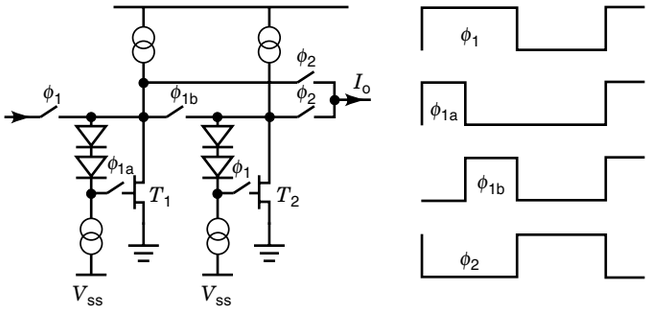


Figure 32. GaAs MESFET S²I memory cell (22).

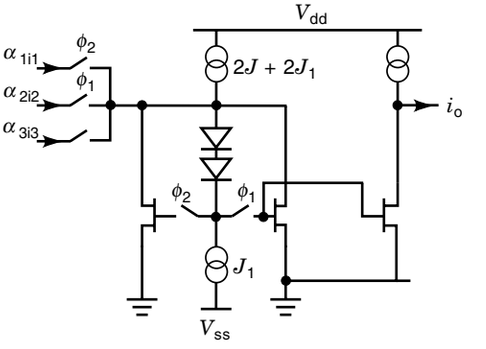


Figure 33. Generalized GaAs MESFET switched-current integrator.

first-generation GaAs MESFET memory cell (Fig. 12), used in the previous GaAs modulator design is that it exhibits a degree of nonlinearity under large-signal conditions that will introduce offset, gain error, and distortion components to the signals. The operation of the first-generation cell is also sensitive to the device mismatch, which is relatively large in GaAs MESFET technology. Therefore, a memory cell with better linearity and lower process sensitivity needs to be developed.

Second-Generation Two-Step GaAs Cell. Although techniques such as dummy switches and differential circuits have been used to reduce charge injection, they can only partially cancel the errors. The S²I CMOS memory cell, which uses a two-step cancellation scheme, has proved to be the most effective. However, the S²I scheme used in CMOS cells cannot be duplicated directly in GaAs MESFET cells since p-channel MESFETs are not available. Here we show a modified S²I cell that suits a GaAs MESFET realization (22). The cell and the clock waveforms are shown in Fig. 32. Due to the Schottky diode gate, a GaAs MESFET cannot be connected as a diode as in the case of a CMOS second-generation memory cell. This problem can be solved by using a diode chain and a current source to shift the input dc level down to a value which is low enough to avoid gate conductance while the difference between the input and gate voltage keeps the memory FET in saturation as shown in Fig. 32. Since the diode-current source branch is only used as biasing, the current can be designed to be quite small. Instead of using a p-channel transistor as a fine memory, the cell uses two identical n-channel memory cells T_1 and T_2, which function as coarse and fine memories, respectively. During phase ϕ_{1a}, the coarse memory T_1 samples the input in the same way as a normal second-generation cell. During ϕ_{1b}, the fine-memory cell samples the difference between the input and the memorized input by T_1, which is the signal-dependent error current. During the output phase ϕ_2, the input current is disconnected and the output is formed by the difference in current between the two memories, which to first order will be identical to the input current since the error has been subtracted.

A potential advantage of the modified S²I memory cell over the conventional S²I memory cell is that more fine cells can be cascaded to further cancel the residual error if the first-order cancellation is not enough.

Generalized Second-Generation GaAs Integrator. A generalized switched-current integrator made from the superposition of forward and backward Euler and feed-forward inputs and realized in GaAs MESFET memory cells is shown in Fig. 33. For simplicity, only general second-generation cells are shown in the circuit. It can be seen that the level shifting stage is shared by the two cells. If the S²I cells are used in the integrator, the level-shifting stages for the coarse and fine cells can be shared, respectively, in the same way by the two cell stages. The transfer function of the integrator is given by

$$i_{\text{out}}(z) = \frac{A_1 z^{-1}}{1 - Bz^{-1}} i_1(z) - \frac{A_2}{1 - Bz^{-1}} i_2(z) - \frac{A_3(1 - z^{-1})}{1 - Bz^{-1}} i_3(z) \tag{45}$$

where A_1, A_2, A_3, and B are scaling factors determined by transistor aspect ratios.

Simulations of the S²I current memory cell were performed to analyze the total harmonic distortion (THD). Results showed that the THD was less than 0.05%, and the circuit functions with a clock rate up to 1 GHz.

Simulation of the S²I Cell: Clock Scheme and Clock Signals. The following three-phase clock scheme is used for clocking the S²I cell. Phases ϕ_{1ax} (Fig. 34) and ϕ_{1bx} are shortened versions of phases ϕ_{1a} and ϕ_{1b} used to control the equivalent transistor switches in the S²I cell of Fig. 28 to ensure that the currents are stored properly in the memory transistors before the next phase is entered. As can be seen from Fig. 34, the ϕ_{1a} signal does not go low before ϕ_{1ax} has reached 0 V. This is slightly restrictive, but for simplicity it should be acceptable. In addition to the clocks shown in the figure, inverted versions of

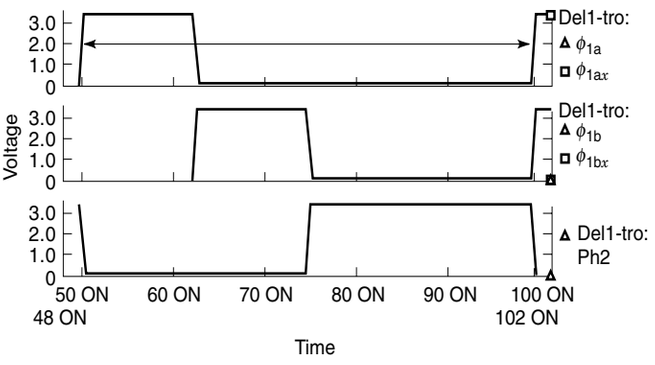


Figure 34. Clock scheme.

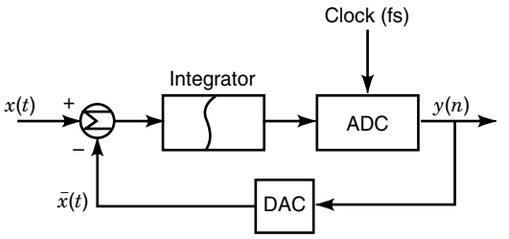


Figure 35. First-order Σ–Δ modulator.

ϕ_{1a} and ϕ_{1b} were used to control the charge-injection cancellation transistors.

Switched circuits often make use of many different clock signals for controlling switches. To be able to vary the clock frequency without changing tens of numbers, the SPICE PARAM OPTION should be used.

In summary the principal advantages of using SI techniques is the compatibility with the on-chip DSP and thus economical advantages of utilizing a standard digital VLSI process.

Sampling Delay Jitter and Σ–Δ Converters

Oversampling converters have become popular for high-resolution data conversion because they tolerate relatively imprecise analog circuits. As with switched currents most of the processing makes use of a technology where fine-line very-large-scale integrated (VLSI) digital circuits can be realized. Its noise-shaping property is very well suited for signal processing applications. So far, to facilitate the very-high-frequency sampling, oversampling modulators such as Σ–Δ converters have been mostly used for relatively low-frequency applications, such as voice telephony. However, recently the frequency range has increased to the megahertz band for wireless applications. With an oversampling ratio ($f_{\text{sample}}/f_{\text{signal}}$) of 256, this translates to a sampling frequency in the gigahertz range. At this frequency a major concern is the integrity of the sampling clock. Currently, state-of-the-art sampling clocks exhibit maximum *jitters* at around a few picoseconds, and at gigahertz values this jitter degrades the dynamic range of the system, for example, *jitter noise.* Many algorithms and circuits have been designed to minimize the effects of sampling clock jitter (23). It is shown that clock jittering does introduce white noise into a system. However, oversampling usually overshadows this effect because of the higher levels of quantization noise.

The simplest form of a Σ–Δ modulator is the first-order loop shown in the block diagram of Fig. 35. Although not shown, there is a subsequent digital decimation filter following the loop. Its primary function is to filter out noise that could alias back into the baseband. In addition, the decimator resamples the signal at a lower frequency equal to the Nyquist rate. The input to the integrator is the difference between the input signal $x(t)$ and the quantized output value $y(n)$ converted back to the predicted analog signal $x'(t)$. For an ideal digital-to-analog converter (DAC) and negligible delays in the circuit, this difference input signal $x(t)$ and the feedback analog signal $x'(t)$ are equal to the quantization error. The net effect of the feedback loop structure is that it preferentially acts as a low-pass filter of the signal and a high-pass filter of the quantization noise. The resultant output spectrum has a shaped quantization noise that is moved out of the pass band. A number of modulators can be cascaded to achieve higher-order noise shaping. For example, a two-stage modulator will give a signal-to-noise ratio of ideally

$$\text{SNR}_{\text{dB}} = 20\log_{10}\left(\frac{\text{in}_{\text{rms}}}{n_{0(\text{output})}}\right) = \frac{\dfrac{\Delta/2}{\sqrt{2}}}{\dfrac{\Delta}{\sqrt{12}}\dfrac{\pi^2}{\sqrt{5}}\left(\dfrac{2}{\text{OSR}}\right)^{5/2}}$$

$$= \frac{30}{2\pi^2}\left(\frac{2}{\text{OSR}}\right)^{-5/2}$$

where OSR is the oversampling ratio and in_{rms} is the average (root mean square) input signal power. Since the actual sampling is done inside the ADC loop, then nonuniform sampling caused by clock jitter may prove to be a non-negligible source of error. The effect of clock jitter is to cause the quantization error term summed before the input of the integrator to be $x(t) - x'(t - \alpha t)$ where αt is a random variable that is probably Gaussian distributed due to the central limit theorem. The delay jitter caused here is in addition to any random delays that may occur in the DAC. Together, the total delay is a source of potential instability.

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