BIPOLAR MEMORY CIRCUITS

One of the main forces driving the exponential growth in computer system performance is advancing technology. The development of semiconductor devices leading to VLSI design has made it possible to build more complex circuits in ever smaller spaces. Today the feature size in a VLSI chip has been reduced to 0.35 μm, and central processor chips are running at over 300 MHz. Memory, however, has not kept pace with the speed of improvements in CPU chips. To be sure, there is need for new technologies or improvements in old technologies for memory circuits.

Emitter coupled logic (ECL) using bipolar technology offers potential for the design of faster memories. This nonsaturated form of digital logic eliminates transistor storage time, a speed-limiting characteristic, and thus permits very high speeds of operation (1). Conventional bipolar ECL technology represents the state of the art in silicon speed, providing system propagation delays in the subnanosecond range, though at the price of very high power dissipation (1.5 mW or more per gate, which is way too much for VLSI densities) (2). So far technological advances have made it possible to fabricate bipolar ECL devices that take about 1/20th the area of conventional ECL devices with speeds comparable to the fastest ECL, consuming only 1/10th the power (2).

With the achievement of low power, high speed, and high density, bipolar technology is expected to be used widely in high-performance digital circuits (3). As more highly integrated bipolar and bipolar/MOS chips come into common use, the gap between low-cost workstations and high-performance servers will be further narrowed (3).

However, such miniaturization and improvements in speed require that the circuits be tested for faults. Many of the physical failures and defects in ICs can be modeled by transistor level shorts and opens (4). The importance of transistor-level modeling is evident in a higher coverage of faults in simple logic circuits compared with that at the gate level (5). Studies of failures at the transistor level help in developing precise models for faults at this level (4). The major fault models at the transistor level are stuck-at faults, stuck-shorts, and opens of the transistor and interconnects and bridging faults (6).

The issue of fault modeling of 1-level and 2-level ECL gates has been addressed in (7,8), where augmented fault models were presented that offer higher coverage of physical failures. Since testing of sequential circuits is difficult, the usual approach is to convert the problem into the simpler one of testing combinational circuits. Design for testability is used to provide direct access to inputs and outputs of combinational blocks (5,9). If it is assumed that most faults within a storage element can be modeled as stuck-at-0/1 faults on the outputs, then such faults become equivalent to the stuck-at faults in the combinational logic surrounding the storage elements, and they do not need to be explicitly considered.

While much work has been done on examining physical failures in CMOS latch cells (10,11,12,13), not much attention has been paid to ECL storage elements. Inadequacy of the minimal fault model in representing physical failures for

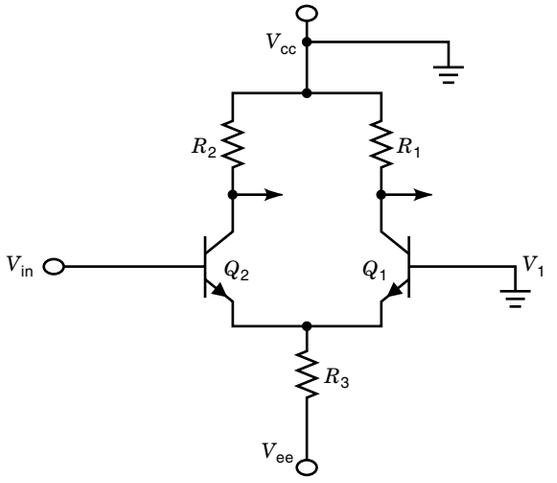

Figure 1. A differential amplifier.

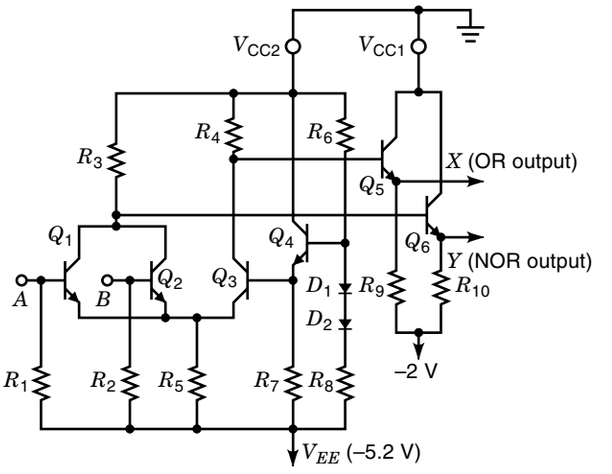

Figure 3. Circuit diagram of a 2-input ECL OR/NOR gate.

CMOS storage elements is considered in (14), and the enhanced fault model presented provides a higher explicit coverage than the minimal fault model. In this article, we examine a differential amplifier that forms the building block of a basic ECL circuit and describe an OR/NOR gate. Then we focus on some early bipolar memory designs, current ECL memory design, and faults in ECL memories, their detection and analysis.

EMITTER COUPLED LOGIC

ECL bipolar circuits use a differential amplifier configuration to control current levels so as to avoid saturation. Control of emitter current or collector current is achieved using the differential amplifier circuit shown in Figure 1. Transistors Q_1 and Q_2 are arranged in a differential amplifier configuration. Transistor Q_1 conducts in its active region as long as input V_{in} is less than V_1, which is grounded as shown in Figure 1. When V_{in} starts exceeding V_1, the current I_E through R_3 splits between transistors Q_1 and Q_2. As V_{in} starts exceeding V_1 even by a small amount, Q_1 turns OFF and Q_2 turns ON, fully remaining in the active region. The collector outputs of both the transistors are always in opposite states. The collectors of Q_1 and Q_2 provide complementary output signals.

This amplifier, with the addition of emitter follower output stages, forms the basis of the basic OR/NOR gate of ECL (15). Emitter coupled logic refers to the manner in which the emitters of the differential amplifier are connected within the integrated circuit (15). The differential amplifier provides high-input impedances and voltage gain within the circuit. Emitter follower outputs restore the logic levels and provide low-output impedance for good line driving and high fanout capability (1).

Basic ECL Gate

Figure 2 shows the block diagram of a fundamental ECL gate, which consists of a current-steering differential amplifier connected by inputs, a temperature and voltage compensated bias network for providing stable voltage bias to the differential amplifier, and emitter follower outputs. Figure 3 shows the basic gate circuit diagram of the Motorola MECL 10 K family (1), used as the basic building block in most present-day implementations of ECL logic designs.

This basic building block is an OR/NOR gate. The operation of an ECL OR/NOR gate can be explained by referring to Fig. 3. Transistors Q_1, Q_2 along with Q_3 form a differential amplifier with a base voltage of Q_3 (VB_3) derived from an internal reference circuit. The transistor stage Q_4 is a tempera-

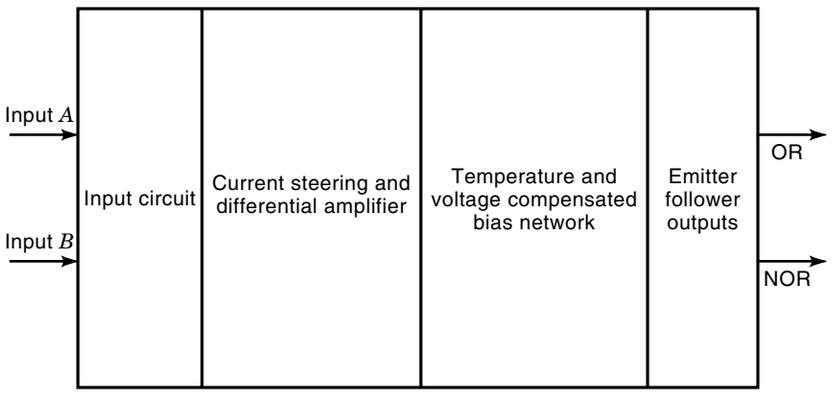

Figure 2. Block diagram of a fundamental ECL OR/NOR gate.

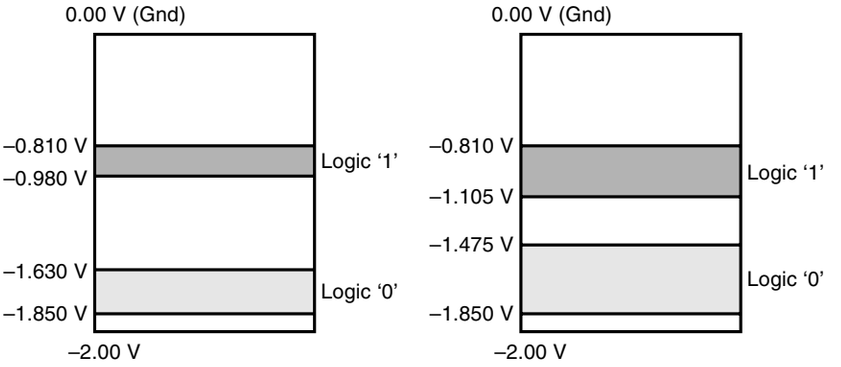

Figure 4. Output and input ECL voltage levels.

ture and voltage compensation network that provides stable reference (V_{BB}) at the center of the output voltage swing. The functioning of the ECL OR/NOR gate can be summarized as follows: The transistor Q_3 will conduct only when the input transistors Q_1 and Q_2 are held OFF with low input voltages as V_{IL}. As soon as any one of the transistors is turned ON (i.e., an input transition to V_{IH}), Q_3 turns OFF. The turning OFF of Q_3 causes output of Q_5 (OR output) to go to V_{OH} and that of Q_6 (NOR output) to go to V_{OL}. Similarly, when the input signals revert to a low state, Q_1 and Q_2 are turned OFF again, and Q_3 gets turned ON. The collector voltages resulting from the switching action of Q_1, Q_2, and Q_3 are transferred through the emitter followers to the output terminals. Hence the circuit provides logic OR and NOR functions in positive logic, or AND and NAND in the negative logic. No inverters are needed in ECL, since every gate provides a direct as well as a complemented output.

The input transistors have their bases held to the V_{EE} line by the pull-down resistors (R_1 and R_2) which provide a leakage current path. Unused input terminals can be left floating without risk of noise coupling to the differential amplifier inputs. The 50 KΩ input resistances maintain logic '0' at inputs with inputs disconnected. The emitter follower output provides sufficient drive capability and also changes the output voltage levels so that the input high and low voltages are compatible. The output of emitter followers are left open without internal load resistances, which allows the connection of matching transmission line and matching impedance/loads at the receive end according to the user's requirement and thus increases speed and reduces power consumption. In using the faster type of ECL gate with no output pull-down resistance, there is a choice of load resistance between using 50 Ω to −2 V or using 510 Ω to the V_{EE} line. A 50 Ω resistor is usually connected to −2 V when transmission lines are used for driving. In practice, V_{CC1} and V_{CC2} are connected to ground, and V_{EE} is connected to −5.2 V.

The reference voltage V_{BB} that tracks V_{CC} is approximately −1.3 V. The reason for using separate V_{CC} connections ($V_{CC1,2}$ connected to ground) is to minimize the effects of crosstalk interference from fast transients. The output logic levels are between −1.63 V and −1.85 V for V_{OL} and −0.810 V and −0.980 for V_{OH}. Transistor Q_4 along with the diode and resistor network forms the temperature and voltage compensated bias network. Transistors Q_5 and Q_6 constitute the emitter follower outputs. Resistors R_9 and R_{10} are connected externally and are not provided internally by the ECL OR/NOR gate. The logic voltage levels for MECL 10 K gates are shown in Fig. 4.

Just as with the complex gates in nMOS and CMOS, multilevel implementations are possible in ECL. One of the techniques is called series gating in which transistor pairs are stacked one above the other in tiers so that current can be steered through different paths. This technique is illustrated in Fig. 5 where there are two tiers of transistor pairs implementing the function $(A + B) \cdot (C + D)$ and its complement $\overline{(A + B) \cdot (C + D)}$. The penalty for the additional functionality is an increase in the propagation delay; however, this generally is less than in the case where the function is decomposed into two or more gates (3). Series gating techniques are used, for example, in the construction of shift registers that make up the diagnostic chain in the integer unit (IU) and floating-point controller (FPC) (3).

ECL MEMORIES

As mentioned earlier, in order to keep up with the improvements in CPU speeds, memory access time has to be reduced correspondingly. Bipolar ECL memories provide a speed advantage over CMOS memories. For this reason speed-critical designs will benefit from the use of ECL memories. One of the oldest bipolar memory designs was the emitter coupled cell,

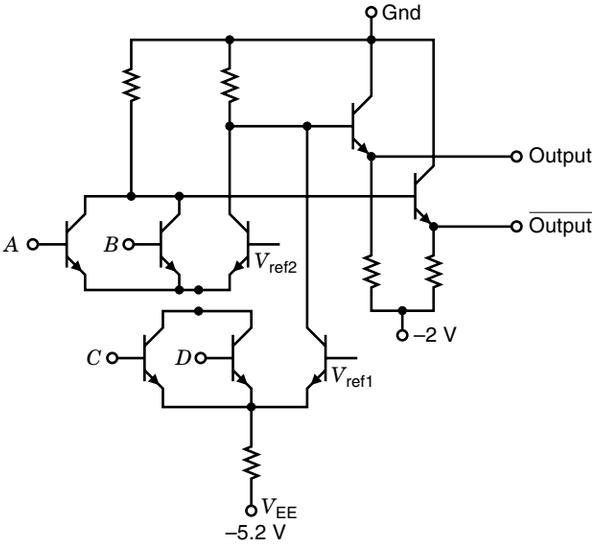

Figure 5. Two-level series gating implementation.

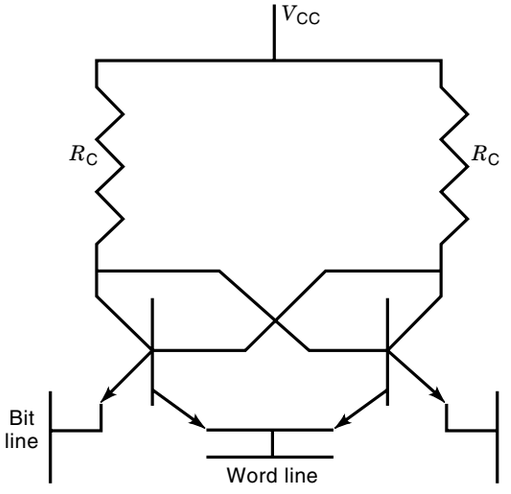

Figure 6. An emitter coupled cell.

shown in Fig. 6 (16,17). This circuit uses TTL logic levels to accommodate single-layer metal technology. The standby power of the unselected cells is determined by the current through the resistor R_C. This resistor also limits the cell read current that drives the cell parasitic capacitance from the standby to the selected state. The cell size of this bipolar memory measured 30 square mils, with a 6 μm single-layer metal process and an access time of 70 ns and 500 mw power dissipation.

Another form of a bipolar memory cell used a diode coupling (18). The standby current in this circuit, as shown in Fig. 7, is controlled by the resistors. When selected, the internal cell resistors provide the base drive of the ON side transistors, while the bit line current is provided by the collector. Thus the bit line current can be several times the standby current. Successful designs included 256 and 1024 bit RAMs.

A simple ECL memory cell is shown in Figure 8. This was achieved using a dual-level metal configuration. Although the collector current of the ON transistor is supplied by the same resistor in the standby and selected states, the voltage across the resistor is increased when the cell is selected. Standby logic swings were very low, about 200 mV to 300 mV.

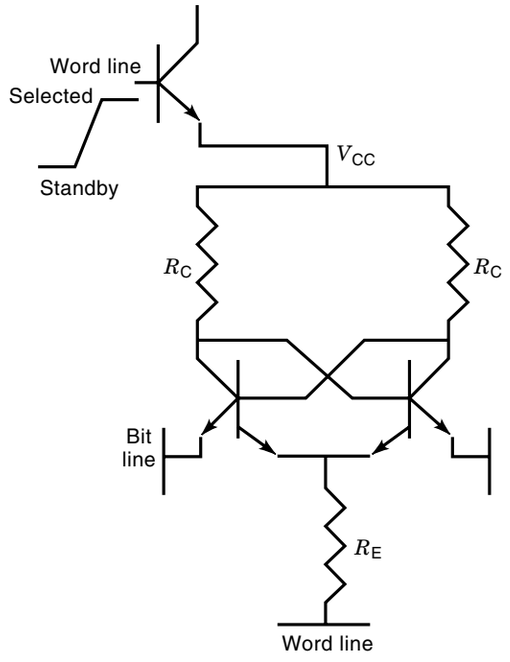

Figure 8. A simple ECL memory cell.

The high performance that was achieved with the low logic swing ECL systems was successfully applied later to TTL systems. A simple circuit is used to translate from TTL logic levels to ECL logic levels. The lack of a high-performance PNP made the translation from ECL to TTL much more difficult. The power and delay penalties were significant, but since RAMs generally have few outputs, the penalties were acceptable.

Technological advances enabling oxide isolation sufficiently increased component density. Low voltage swing techniques could be applied to 256 bit and 1024 bit RAMs. In the cell structure shown in Fig. 8, the read to standby current ratio is limited by the current that can be supplied by the resistor R_E. This design led to the development of the switched collector impedance and diode bypass circuits shown in Fig. 9. This design was used in both 1 k and 4 k RAMs

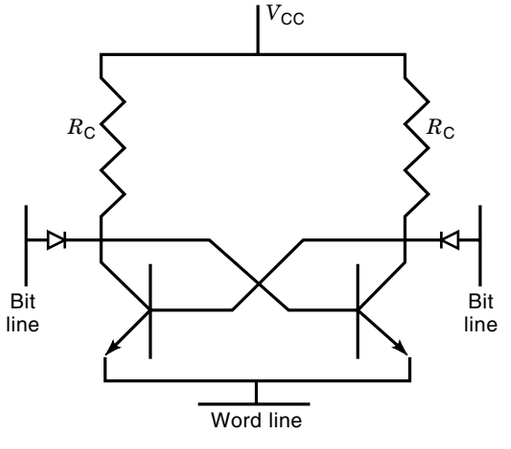

Figure 7. Bipolar memory cell using diode coupling.

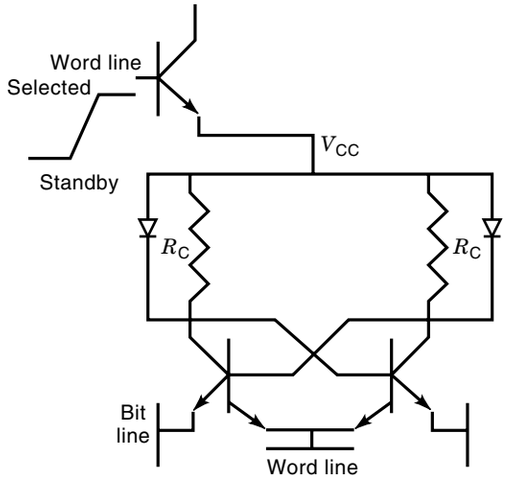

Figure 9. Oxide isolated diode bypass cell.

with access time and power dissipation of 35 ns and 900 mW, respectively. By replacing the diode with a Schottky diode, the access time could be reduced to 7.5 ns in a 1 kbit RAM (19).

The problem using the Schottky diode was that it limited the differential voltage in the standby mode. By adding an extra parasitic cell capacitance, the differential voltage was maintained at acceptable levels. Even 4 k RAMs were designed with access time of 3 ns and power dissipation of 1.5 W. But the Schottky diode needed special protection from alpha particle currents.

The cross-coupled SCR cell (17,20) was used in both the diode coupled and emitter coupled cells. This configuration of the emitter coupled cell achieved design memories as large as 16 k to 64 k at access times as low as 5 ns. But poor frequency characteristics of the *pnp* transistor limited the width of the write signal.

The I^2L, integrated injection logic was an innovation aimed at reducing the standby power dissipation and the cell area. The initial cell area was 9000 μm^2, and a 9.35 mm^2 die achieved 140 ns access time with 400 mw power dissipation. The technique was refined to 315 μm^2 for up to 64 k dynamic RAM with a 50 ns access time. But by this time MOS memories were on the market and I^2L memories could not compete.

ECL Storage Elements

The preceding description of some of the early published work in bipolar memory cell design, as well as other unpublished designs, have led us to the current ECL memory cell designs described in this article. The current ECL storage elements voltage levels between −1.85 V and −1.45 V are recognized as logic low and between −1.15 V and −0.75 V as logic high. The intermediate level between −1.45 V and −1.15 V is termed 'indeterminate' logic level. Though the input low-logic level (V_{IL}) is between −1.85 V and −1.45 V, an input between −5.2 V and −1.45 V is valid as logic '0'. Similarly, though the input high-logic level (V_{IH}) is between −1.15 V and −0.75 V, an input between −1.15 V and 0.00 V is also logic '1'. These voltage levels can occur under some faults in ECL storage elements. Such a situation does not occur in CMOS devices, since the output voltage levels reach the extreme voltage levels of 0 V and 5 V for logic '0' and '1', respectively, unlike in ECL devices.

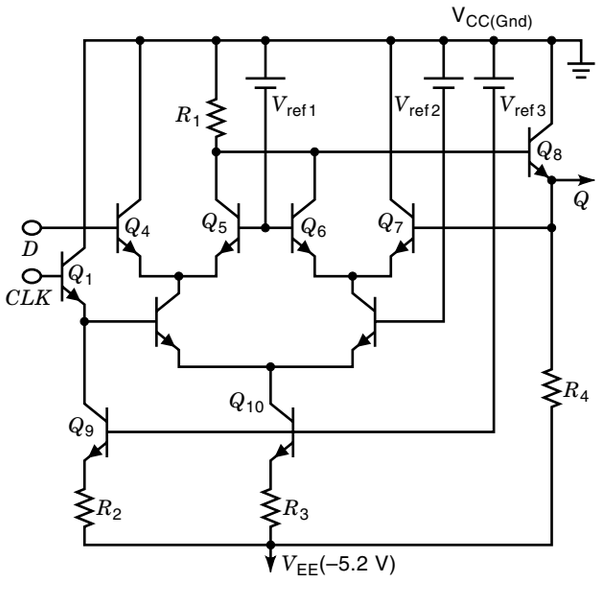

Figure 10. Two ECL memory cell designs.

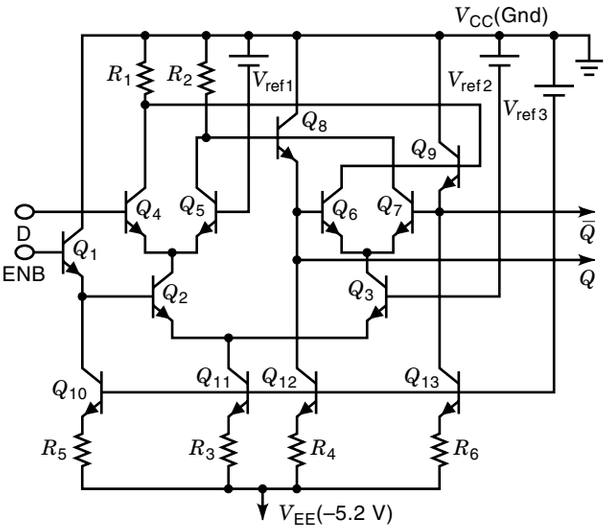

Figure 11. Two ECL memory cell designs.

The ECL storage element given in (21) has been modified to provide complementary output ($\overline{Q}$) as shown in Fig. 10. V_{ref1} and V_{ref2} form the reference voltages for the differential amplifiers. V_{ref3} along with transistors Q_9 and Q_{10}, and resistors R_2 and R_3 form the current sinks. When the clock input is high, the logic level at input D is clocked into the storage element. The clocked input value is maintained by the feedback provided by transistor Q_7. Simultaneous true (Q) and complementary ($\overline{Q}$) outputs are provided by the ECL storage element. Another storage element (21) is shown in Fig. 11; it is based on using a differential amplifier with bilateral drive. In this scheme true and complementary outputs are directly available. The power supply voltage applied to the ECL storage element at V_{ee} is −5.2 V.

FAULTS IN ECL MEMORIES

The transistor-level shorts and opens model many of the physical failures and defects in ICs (4). Analyses of faults in simple logic circuits suggest that the transistor-level testing provides a higher coverage of faults compared to that at the gate level (5). It is necessary to study the effects of failures at the transistor level and develop accurate fault models at this level (4). The major fault models at transistor level are stuck-at faults, stuck-shorts, and opens of transistor and interconnects, and bridging faults (6).

Stuck-at Model for Storage Elements

Most approaches for modeling faults rely on the assumption that the faults in storage elements can be modeled as stuck-at faults at the inputs and outputs. In many situations the faults are considered in the combinational logic, so it is im-

plicitly assumed that any internal faults in a storage element can be shown to be equivalent to either a stuck-at-output or a stuck-at-input, which in turn may appear as a stuck-at-output of the combinational logic surrounding the storage element. This is termed a minimal fault model. Stuck-at-0/1 fault at the input(output) of a storage element is equivalent to the stuck-at-0/1 fault of the combinational logic output feeding (input being fed) by the storage element. Most design for testability (DFT) approaches rely on the assumption that the faults in storage elements can be modeled as stuck-at faults at the inputs and outputs. For example, in level-sensitive scan design (LSSD) implementations, stuck-at faults at the outputs of latches are considered as stuck-at faults at the inputs of the combinational circuit driven by the storage elements. Similarly stuck-at faults at the inputs of latches are considered as stuck-at faults at the outputs of the combinational circuit driving the storage elements. In addition the DFT schemes rely on a large number of complex storage elements.

Enhanced Fault Model

In this section we evaluate the response of two different ECL storage elements for various faults. Both storage elements are examined for all possible hard failures. The kind of hard failures considered include all possible opens and shorts of resistors and the transistor junction opens and shorts. Figure 12 shows the naming convention used for (a) shorts and (b) opens between various junctions of the bipolar transistor. For simulating shorts between various junctions of the bipolar transistors, a low resistance of $\approx 1\ \Omega$ was connected between the terminals, and for opens, a resistance of $\approx 10\ M\Omega$ was connected between the respective terminals. The objective is to find a good functional fault model that adequately describes the functional behavior of faulty storage elements. Minimal fault model as well as enhanced fault models are examined for their effectiveness in representing the faults.

The enhanced fault model proposed in (14) has been shown to provide a higher explicit fault coverage for CMOS storage elements. *Data*-feed-through faults, which are remarkably different from stuck-at-0/1 faults were proposed. Such faults cause the storage element to become either *data*- or $\overline{data}$-feed-through, which can lead to a timing problem or coupling between combinational blocks separated by the storage elements (22). In the two different ECL storage elements examined in this work, *data*- and $\overline{data}$-feed-through faults were observed and defined (14) as follows:

Definition 1 A faulty storage element is said to have a feed-through fault if it becomes *data*-feed-through or $\overline{data}$-feed-through. A faulty storage cell is said to be *data*-feed-through when its behavior becomes combinational such that $R(s, t_i) = f(y)$ for each $t_i \in T$, where y is the data part of t_i.

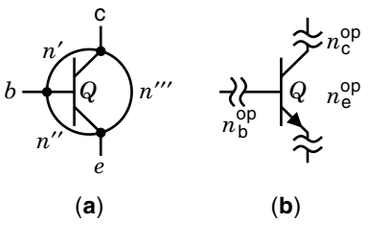

Figure 12. Naming convention used for transistors: (a) Shorts; (b) opens.

Table 1. Behavior of ECL Storage Element-1 Under Opens and Shorts

Faulty Behavior of ECL SE-1		
Faults	Output Behavior (Q)	Model
$9'''$, $1'$, $4'$, $9''$, $8''$, 1_c^{op}, 4_c^{op}, 9_b^{op}, $10'''$	Fault-free	Fault-free
$1'''$, $4'''$, $2''$, $3''$, $R_2^{sh@}$, $5''$, $8'$, $9'$, $10''$, 1_b^{op}, 1_e^{op}, 2_e^{op}, 2_b^{op}, 2_e^{op}, R_4^{op}, 4_b^{op}, 5_c^{op}, 5_e^{op}, 10_c^{op}, $7'$, 10_e^{op}, R_3^{op}, $4''$, R_1^{sh}	1	Stuck-at-1
$3'''$, $5'''$, 4_e^{op}, $5'$, $8'''$, $R_3^{sh@}$, R_4^{sh}, $6'$, $10'$, 8_c^{op}, 8_b^{op}, 8_e^{op}, R_1^{op}	0	Stuck-at-0
$2'''$, 3_b^{op}, 3_e^{op}, 9_c^{op}, 9_e^{op}, R_2^{op}	D(*data*-feed-through)	Feed-through
$6'''$, 7_e^{op}	UL-1	—
$7'''$, $3'$, $6''$, $7''$, 3_c^{op}, 6_c^{op}, 6_e^{op}, 7_b^{op}, 10_b^{op}	UL-0	—
5_b^{op}, 6_b^{op}, 7_c^{op}	Indeterminate	—
$1''$, $2'$	Complex behavior	—

Note: op = open; sh = short; e, b, c = emitter, base, collector; @ = abnormal current.

The definition above can be modified to include $\overline{data}$-feed-through faults:

Definition 2 A faulty storage element is said to have a feed-through fault if it becomes $\overline{data}$-feed-through. A faulty storage cell is said to be *data*-feed-through when its behavior becomes combinational such that $R(s, t_i) = f(\overline{y})$ for each $t_i \in T$, where $\overline{y}$ is the $\overline{data}$ part of t_i, and where $T = \{t_1, . . ., t_n\}$ are the set of all possible input combinations. For an elementary synchronous storage element with input D and a control signal CLK, and $n = 4$, $R(s, t_i)$ is the response of the cell to the input vector t_i applied to the cell when the cell is at state s.

To avoid glitches and hazards in clocked storage elements, the clock is applied when the data are stable. The latch is race free if the data are stable when clock is active (10). Hence data (D) are allowed to change only when clock (CLK) is low. Certain faults cause changes in the behavior of the synchronous storage element in the latch phase, though it might function properly in the transparent phase. This causes the cell to be unable-to-latch 1(0), and this condition is defined (14) below.

Definition 3 Let the state of a faulty synchronous elementary storage element during the transition from the transparent phase to the latch phase be $Q = 1(0)$. If the state of the cell becomes 0(1) during the latch phase irrespective of data input, then the cell is said to be unable-to-latch 1(0). The notation $UL - 1(UL - 0)$ is used to describe this.

The ECL storage element-1 was analyzed for all input vectors under shorts and opens between the junctions of all transistors. The outputs were verified by performing SPICE (23) simulations and the results are tabulated in Table 1. While

Table 2. Q Output of ECL Storage Element-1 Under Opens and Shorts

Faulty Behavior of ECL SE-2 Q Output		
Faults	Output Behavior (Q)	Model
$1'$, $6''$, $7'$, $8''$, $R_1^{sh^*}$, $9''$, $10''$, $10'''$, $12''$, $12'''$, $13''$, $13'''$, 10_b^{op}, R_6^{op}, $3'$, $11'''$, R_5^{op}, 1_c^{op}, 10_b^{op}, 12_b^{op}	Fault-free	Fault-free
$1'''^*$, $2''^*$, $3''^*$, $3'''$, $4'''$, $5'''$, $6'$, $8'$, $10'$, $11''^*$, $R_2^{sh^*}$, $R_5^{sh^{*@}}$, 1_b^{op}, 1_e^{op}, 2_b^{op}, 2_e^{op}, 5_e^{op}, 11_c^{op}, 11_e^{op}, R_3^{op}, R_4^{op}, $8'''$, 12_c^{op}	1	Stuck-at-1
4_e^{op}, $5'$, $11'^*$, $12'$, $R_4^{sh^{*@}}$, 8_c^{op}, 8_b^{op}, 8_e^{op}, $R_2^{op^*}$, $R_3^{sh^{*@}}$	0	Stuck-at-0
$2'''$, 3_b^{op}, 3_e^{op}, 10_c^{op}, 10_e^{op}	D(*data*-feed-through)	Feed-through
$7'''$, $9'''$, 6_c^{op}, 6_e^{op}, 13_c^{op}	UL-1	—
$4'$, $6'''$, $7''$, $13'^*$, 3_c^{op}, 7_c^{op}, 7_e^{op}, 9_c^{op}, 9_b^{op}, 9_e^{op}, R_1^{op}	UL-0	—
$2'$, $4''$, $5''$, 6_b^{op}, 2_c^{op}, 4_b^{op}, 5_c^{op}, 5_b^{op}, 7_b^{op}, 12_e^{op}, 11_b^{op}, R_5^{op}	Indeterminate	—
$1''^*$, $9'^*$, 4_c^{op}, $R_6^{sh@}$,	Complex behavior	—

Note: op = open; sh = short; e, b, c = emitter, base, collector; * = loss of complementarity; @ = abnormal current.

some faults do not cause any appreciable change in the logic level exhibiting fault-free level, some faults manifest as stuck-at-1 or stuck-at-0. Six faults cause the cell to be transparent with Q output being the same as D, and therefore the cell exhibits *data*-feed-through. For one of the faults, the output becomes a logical function of the clock signal, which is considered complex behavior. Behavior exhibiting unable to latch-1 and unable to latch-0 are observed for 2 and 9 faults, respectively.

Out of the 68 faults considered, 46 faults (67.6%), are covered by the minimal fault model, while the enhanced fault model covers 17 more, resulting in 63 faults (92.6%). Three of the faults manifesting as indeterminate output and 2 of the faults exhibiting complex behavior cannot be modeled either by the minimal fault model or by the enhanced fault model.

The results obtained for ECL storage element-2 Q output are summarized in Table 2. Twenty faults do not cause any appreciable change in the logic level at Q output and exhibit fault-free output. Some faults are manifest as stuck-at-1 or stuck-at-0. Five faults cause the cell to exhibit *data*-feed-through. For 4 of the faults the output becomes a logical function of the clock signal, which is considered complex behavior. Behavior exhibiting unable to latch-1 and unable to latch-0 are observed for 5 and 11 faults, respectively. Out of the 90 faults considered, 53 faults (58.8%) are covered by the minimal fault model, while the enhanced fault model covers 21 more, resulting in 74 faults (82.2%). Twelve faults are manifest as indeterminate output, and 3 faults exhibit complex behavior that cannot be modeled either by the minimal fault model or by the enhanced fault model.

The results obtained for ECL storage element-2 $\overline{Q}$ output are summarized in Table 3. Twenty faults do not cause any appreciable change in the logic level at $\overline{Q}$ output and exhibit fault-free output. Some faults manifest as stuck-at-1 or stuck-at-0. Seven faults cause the cell to exhibit $\overline{data}$-feed-through. For two of the faults, the output becomes a logical function of the clock signal, which is considered complex behavior. Behavior exhibiting unable to latch-1 and unable to latch-0 are observed for 5 and 10 faults, respectively. Out of the 90 faults considered, 53 faults (58.8%), are covered by the minimal fault model, while the enhanced fault model covers 22 more resulting in 75 faults (83.3%). Thirteen faults manifesting as indeterminate output and 2 faults exhibiting complex behavior cannot be modeled either by minimal fault model or by the enhanced fault model.

Two faults (R_2^{sh} and R_3^{sh}) in ECL storage element-1 and four faults (R_3^{sh}, R_4^{sh}, R_5^{sh} and R_6^{sh}) in ECL storage element-2 cause an increase current drawn by the device. Normal current drawn by the device is ≈6 mA, but under the above-mentioned faults the current drawn by the device increases to 1.3 A, a 200-fold increase. A current monitor of the power supply current (I_{EE}) can be used to detect the enhanced current drawn by the device, and work is underway to develop such a scheme.

Careful observations of Tables 2 and 3 indicate that for 14 of the physical failures (15%) marked*, the input test vectors cause both the true and complementary outputs to exhibit similar outputs (00 or 11); in other words, they exhibit *loss of complementarity*. Under fault-free conditions, the Q and $\overline{Q}$ outputs exhibit fault-free dissimilar outputs (01 or 10). A sim-

Table 3. $\overline{Q}$ Output of ECL Storage Element-1 Under Opens and Shorts

Faulty Behavior of ECL SE-2 $\overline{Q}$ Output		
Faults	Output Behavior ($\overline{Q}$)	Model
$1'$, $7'$, $7''$, $8'$, $11''^*$, $8''$, $9''$, $10''$, $10'''$, $12''$, $12'''$, $13''$, $13'''$, 1_c^{op}, 10_b^{op}, 12_b^{op}, $3'$, 12_e^{op}, 13_b^{op}, R_4^{op}	Fault-free	Fault-free
$1'''^*$, $2''^*$, $3''^*$, $9'^*$, $11''^*$, $12'$, $R_1^{sh^*}$, 4_c^{op}, 4_e^{op}, 11_c^{op}, $9'''$, 11_e^{op}, R_3^{op}, 13_c^{op}	1	Stuck-at-1
$3'''$, $4'''$, $5'''$, $2'$, $4'$, $6'$, $10'$, $R_5^{sh^{*@}}$, 1_b^{op}, $R_3^{sh^{*@}}$, $R_6^{sh^{*@}}$, 9_c^{op}, 9_b^{op}, 1_e^{op}, 2_b^{op}, 2_e^{op}, $11'^*$, 9_e^{op}, R_1^{op}	0	Stuck-at-0
$1''^*$, $2'''$, 3_b^{op}, $R_4^{sh^{*@}}$, 3_e^{op}, 10_c^{op}, 10_e^{op}	$\overline{Data}$-feed-through	Feed-through
$6'''$, $R_2^{sh^*}$, 7_c^{op}, 7_e^{op}, 12_c^{op}	UL-1	—
$7'''$, $8'''$, $13'^*$, 3_c^{op}, 6_c^{op}, 6_e^{op}, 8_c^{op}, 8_b^{op}, 8_e^{op}, $R_2^{op^*}$	UL-0	—
2_c^{op}, 4_b^{op}, 5_c^{op}, 5_b^{op}, 5_e^{op}, 6_b^{op}, 7_b^{op}, $4''$, $5''$, 11_b^{op}, 13_e^{op}, R_5^{op}, R_6^{op}	Indeterminate	—
$5'$, $6''$	Complex behavior	—

Note: op = open; sh = short; e, b, c = emitter, base, collector; * = loss of complementarity; @ = abnormal current.

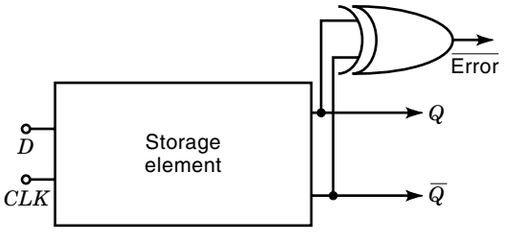

Figure 13. Ex-OR to detect *loss of complementarity.*

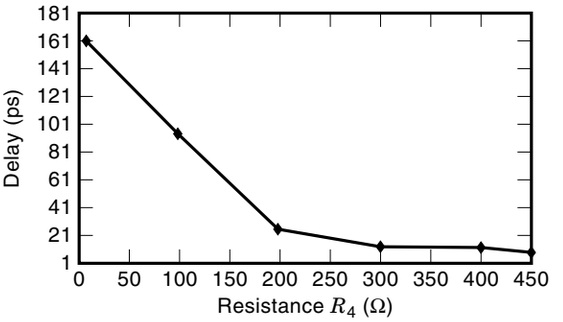

Figure 14. Delay in output response for $\overline{Q}$ output with decreasing R_4 resistance.

ple testable design using an exclusive-OR or an exclusive-NOR gate can detect the *loss of complementarity* occurring at the outputs of ECL storage elements. However, use of an exclusive-OR or exclusive-NOR to detect *loss of complementarity* may be a severe penalty to pay in terms of area overhead. Nevertheless, this approach is effective, and a scheme to implement this logic with a fewer number of transistors is underway.

In Fig. 13 a simple design-for-testability approach for detecting such failures is presented that uses an exclusive-OR gate connected to the output of the ECL storage element. The output of the exclusive-OR gate is termed an $\overline{ERROR}$ signal. When the true and complementary output of the storage element is fault-free dissimilar output (i.e., 01 or 10), the $\overline{ERROR}$ signal is a 1, indicating that $\overline{ERROR}$ = 1 and *ERROR* = 0 (i.e., no error). Whenever any of the faults cause the outputs of the storage element to exhibit erroneous *loss of complementarity* (i.e., 00 or 11), the $\overline{ERROR}$ signal becomes a 0, indicating that an error has occurred. An exclusive-NOR gate can be used in place of the exclusive-OR gate, and the *ERROR* signal is interpreted accordingly. Use of an exclusive-OR or NOR to detect *loss of complementarity* increases the area overhead, so there might be a severe penalty, especially given the number of storage elements generally used in a circuit.

BEHAVIOR OF FAULTS IN ECL STORAGE ELEMENTS

The effectiveness of the fault model in representing physical failures indicates a need for a more accurate fault models to better represent physical failures at the transistor level. The results inferred from the elementary fault model can be used to obtain fault models for complex storage elements. Improved fault models that accurately represent physical failures may significantly reduce test generation and fault simulation efforts significantly.

An enhanced fault model was suggested for the behavior of ECL storage elements under the various faults presented above (24). Fault modeling of ECL storage elements (24) showed stuck-at-1, stuck-at-0, and loss of complementarity for ECL storage elements with true and complementary outputs. Delay faults as well as enhanced power supply current were observed under certain physical failures in ECL storage elements. One of the faults in ECL storage elements causing delay in the output response at the complementary output ($\overline{Q}$) was with a short in the current source resistance R_4 or with a parametric drift causing a decrease in the current source resistance R_4. SPICE (23) simulations showed the delay of the ECL storage element under fault-free conditions (resistance R_4 = 450 Ω) to be 7.7 ps. When the value of the resistance R_4 was decreased due to a short in the resistance or due to parametric drifts causing a decrease in resistance, the result was a delay of ≈1.62 ps for R_4 = 10 Ω at the complementary output ($\overline{Q}$). This indicates an increase of almost two orders of magnitude in delay. A plot illustrating the output delay under decreasing resistance values of R_4 is shown in Fig. 14. As the resistance value is decreased, until about 200 Ω, the increase

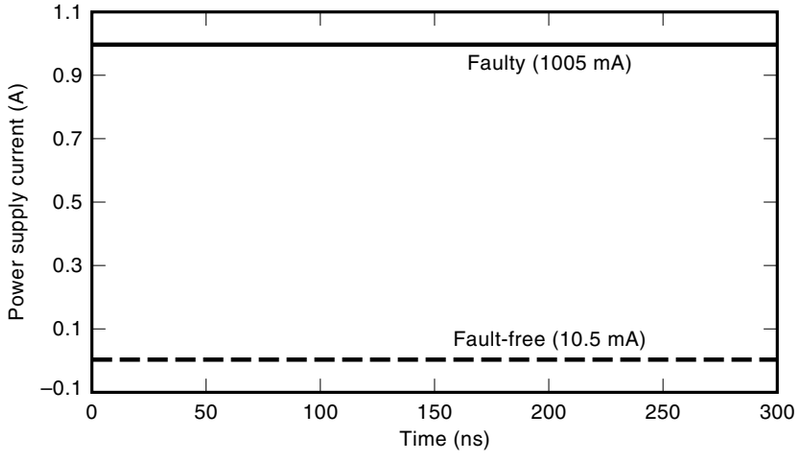

Figure 15. Fault-free and faulty power supply current.

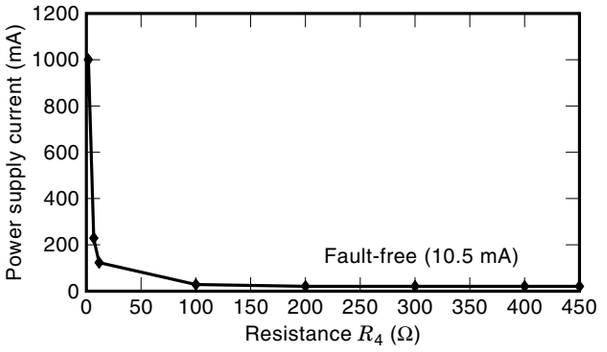

Figure 16. Power supply current for various R_4 resistance values.

in delay is less. Further decrease in resistance causes an appreciable delay in the output response.

The fault-free current drawn by the ECL storage element is ≈10.5 mA. Under the same fault, with a short in resistance R_4 or with parametric drift causing a decrease in resistance R_4 with a delay in the output response, the power supply current drawn by the device increases dramatically. Figure 15 shows fault-free as well as faulty currents under various input conditions. It can be seen that the power supply current drawn by the device is constant even with input changes. The fault-free current drawn by the ECL storage element is 10.5 mA, whereas the power supply current under faulty conditions with resistance $R_4 = 1\ \Omega$ is ≈1005 mA. The increase in current under fault is approximately two orders of magnitude higher than for the fault-free ECL storage element. The plot in Fig. 16 shows the power supply current drawn by the ECL storage element by varying resistance R_4. The increase in current with a decrease in resistance is fairly slow up to ≈100 Ω. Any further decrease in resistance R_4 results in a faster increase in the power supply current.

DETECTION OF CERTAIN FAULTS

Summarizing the preceding discussion, it can be seen that the shorts with resistance R_4 or with a decrease in resistance of R_4 are manifest as delay faults and as an increase in the power supply current drawn by the device. Testing for delay faults to detect minute differences in delay is more difficult than detecting enhanced power supply currents.

A power supply current monitoring circuit is shown in Fig. 17 for detecting enhanced power supply current drawn by the ECL storage element. The current monitor output (CM_{out}) provides a logic '1' output under fault-free conditions. As the power supply current drawn by the ECL storage element increases due to a decrease in resistance R_4, the voltage in the current-sensing resistance R_S drops further. The larger voltage drop in resistance R_S causes the power supply current-sensing transistor (T_S) to turn ON, which in turn causes the output to switch to logic '0'. The current monitor output is shown in Fig. 18 for fault-free and faulty conditions. The current monitor output shows ECL logic level '1' under fault-free conditions and logic level '0' under faulty conditions with a decrease in the value of resistance R_4. For faulty output conditions (logic level '0'), the current monitor in Fig. 18 shows pulsed outputs caused by the slightly relaxed tolerances used for SPICE (23) simulations which allow the output to converge. However, under faulty conditions the current monitor output is ECL logic level '0'. Thus it can detect enhanced power supply current drawn by the ECL storage element.

Unlike CMOS devices, ECL devices draw constant power supply current irrespective of the frequency of operation. The sensitivity of the current monitor can be varied by varying the value of the current-sensing resistance (R_S). The voltage drop in resistance R_S during fault-free operation is ≈0.3 V with $R_S = 20\ \Omega$. The power supply voltage needs to be increased to −5.5 V ($V_{EE} = -5.5$ V) to compensate for the voltage drop in resistance R_S. This would enable −5.2 V to be applied to the ECL storage element, ensuring proper performance of the ECL storage element.

Our earlier work on fault modeling of ECL storage elements (24), and described above, demonstrates stuck-at-1, stuck-at-0, and loss of complementarity for ECL storage elements with true and complementary outputs. Certain faults in ECL devices cause an enhanced power supply to be drawn by the device. Figure 19 gives a plot of the current drawn by an ECL gate under fault-free and faulty conditions. The dotted line shows the current drawn by the device under fault-free condition, and the solid line shows the current drawn by the device under certain faults. SPICE (23) simulations indicate that the current drawn under faulty conditions is almost 100 times higher than that of under fault-free conditions. Hence a current-sensing circuit can be used to detect such faults. Certain faults in ECL devices exhibit delays in the output response. Detection of delay faults are difficult, however.

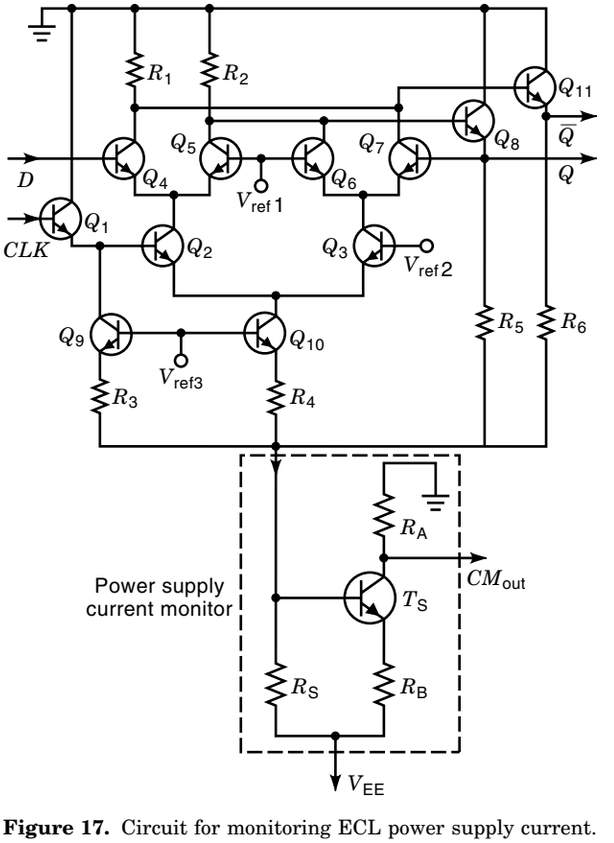

Figure 17. Circuit for monitoring ECL power supply current.

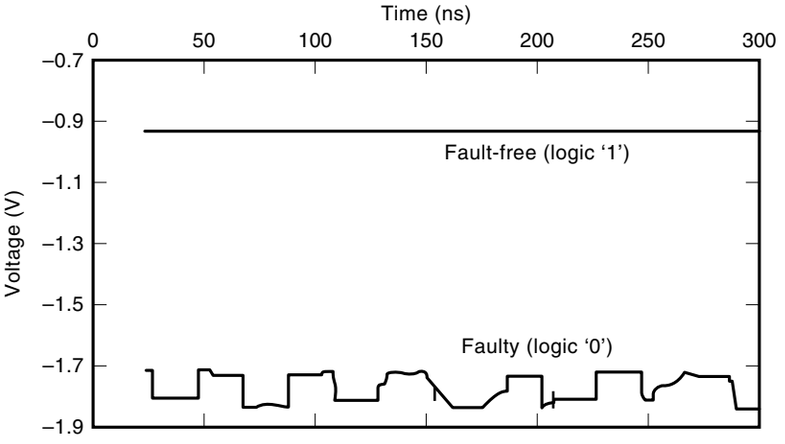

Figure 18. Power supply current monitor outputs (CM_{out}) under fault-free and faulty conditions.

A testable design to detect loss of complementarity, enhanced current, and delay faults in ECL storage elements is proposed. The proposed testable design can be used for detection of faults on-line. The proposed testable design for detection of the faults in ECL storage elements can significantly improve test time and effort. The test of the article will cover the design and implementation of this testable design for ECL storage elements, which has been proved to be useful for fault-tolerant systems.

BRIDGING FAULTS: MODELING AND ANALYSIS

A type of fault that is prominent in ECL memories is the bridging fault. The bridging fault has long been regarded as a failure mode in digital systems (25,26,27). Bridging faults can occur within an integrated circuit or a printed circuit board during manufacturing or at a later stage. The main explanation for the occurrence of bridging faults is a defect in the manufacturing process. In the photolithography stage of the manufacturing process, diffraction, and proximity are the prime sources of the excess metal leading to bridging faults. Impurities and diffusion of metals are other sources responsible for such faults. Studies based on layout-level defects using statistical data from fabrication processes reveal that bridging faults can be as high as 30 to 50% of all faults (28,29). Hence bridging is an important failure mode that needs careful and systematic analysis.

Detailed examinations of bridging faults in nMOS/CMOS have been presented in (30,31), and in ECL in (32,33). Malaiya et al. (30) placed bridging faults into three categories: bridging within a logic element, bridging of logical nodes without feedback, and bridging of logical nodes with feedback.

Input and Output Bridging Faults

In this section we assume hard shorts for the bridging faults under consideration. First we state a property of ECL that is widely used in ECL logic design.

Assertion 1 Connecting two ECL emitter follower output nodes results in an OR operation between the affected nodes.

A formal proof can be found in (34). Consider the output f_a without the connection (C_1) for the emitter follower output

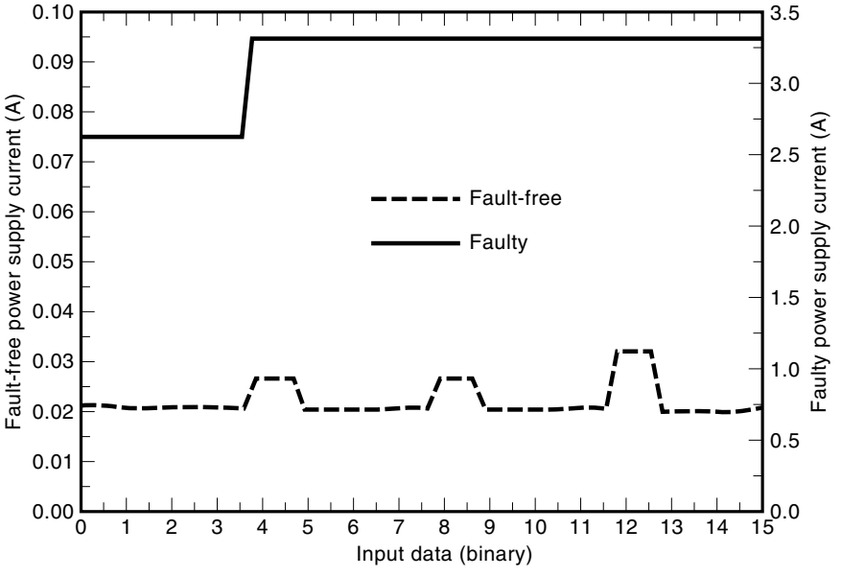

Figure 19. Current drawn by an ECL gate under fault, causing enhanced current, and fault-free conditions.

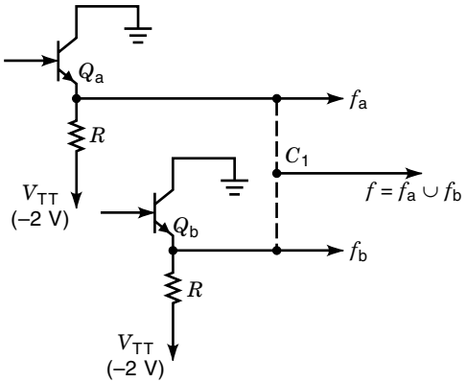

Figure 20. Two ECL output connected together (wired-OR).

stages shown in Figure 20. The base terminal of the emitter follower transistor Q_a is driven by the differential amplifier transistors of the ECL device. For ECL logic low level at the output (-1.75 V), the base voltage of transistor Q_a is ≈ -0.98 V with a V_{BE} drop of 0.77 V provides -1.75 V at the output. Similarly, when the emitter follower output is at ECL logic high level (≈ -0.89 V), the base voltage of Q_a is (≈ -0.05 V), with a V_{BE} drop of 0.84 V providing ≈ -0.89 V at the output as $\approx$22.5 mA flow through the transistor.

Consider the connection (C_1) between outputs f_a and f_b which is composed of two of the emitter follower output stages shown in Fig. 20. The output logic level will be ECL low level ≈ -1.75 V iff the base voltage of both the transistors (Q_a and Q_b) is at -0.98 V. If the base voltage at the transistors Q_a and Q_b is at -0.05 V, then the output goes to -0.89 V. For the case where the base of the transistors Q_a is at -0.05 V and Q_b is at -0.98 V, the output corresponding to transistor Q_a will be at -0.89 V, yielding logic low level. Since both emitter follower outputs are connected together, -0.89 V also appears at the emitter of Q_b. Since the base of transistor Q_b is at -0.98 V and the emitter is at -0.89 V, the base–emitter junction is reverse biased; hence the output is maintained at -0.89 V, thus realizing OR operation.

The above argument can be easily extended to more than two ECL emitter follower output nodes provided that there are no maximum fanout and fanin restrictions. Since a deliberate connection results in an OR operation, this type of connection is referred to as wired-OR, a feature common in ECL designs. An ECL circuit provides simultaneously true and complementary outputs. The output and its complement are available in ECL. An interesting observation due to the availability of true and complementary outputs in conjunction with the wired-OR property of ECL (1) is summarized below under output bridging conditions. First, we define a hard bridging fault and a short as a bridging or a connection with a negligible resistance.

Assertion 2 In an ECL device a hard bridging fault or a short between the true and complementary outputs results in stuck-at-1 at both the true and complementary outputs.

Proof Consider a fault-free ECL gate. If the true output is at logic level '0', then the complementary output has to be at logic level '1', and vice versa. From Assertion 1 it is known that the short would result in a wired-OR between the true and complementary outputs. At the ECL gate, either the true or the complementary output will be at logic level '1', which results in logic level '1' at both the true and complementary outputs. This is the same as both true and complementary outputs being stuck-at-1. QED

Consider the bridging faults at the input of ECL devices. ECL devices need ECL voltage-compatible levels to operate. Hence an ECL device input is driven either by another ECL device or by a pull-down circuitry (resistance R in conjunction with V_{TT}, shown in Figure 20) in order to provide ECL–compatible input signals. This leads to the theorem given below.

Assertion 3 In a fault-free ECL gate, if a short occurs between any two logical input nodes, then the logic level at the affected nodes is the logical OR of the fault-free logic levels at the two nodes.

Proof An input node of an ECL device is driven by a pull-down circuit (a resistor with or without an emitter follower stage connected to -2 V). Hence a bridging fault at the input of an ECL device is equivalent to an output bridging fault of the previous ECL output stage. By Assertion 1, the affected nodes of the previous output stage would result in a logical OR and in turn in a logical OR of the affected input nodes. QED

Hence, by the theorem above, the logical OR is equivalent to a wired-OR between the affected nodes. In order to study these effects, Malaiya et al. (30) classified bridging faults into three categories: bridging within a logic element, bridging of logical nodes without feedback, and bridging of logical nodes with feedback. The effects of bridging faults in ECL devices are examined next using the above classification. The following definitions are used to aid in the discussion of these classes of bridging faults.

Definition 1 A logic element is defined as an ECL gate or a complex ECL gate.

Definition 2 A logical node is defined as a node where ECL logic levels are maintained, namely a node where specific voltage levels indicate logic levels '0' or '1'. In ECL devices the input and output nodes are defined as logical nodes.

We define a logic element as a gate or a complex gate. A logical node is defined as a node where ECL logic levels are maintained, which is a node where specific voltage levels indicate logic levels '0' or '1'. In ECL devices input and output nodes are logical nodes.

Bridging of Logical Nodes without Feedback

Recapitulating our discussion so far, we have seen that an output bridging (a hard short) results in a wired-OR between the affected nodes. An input bridging also results in a wired-OR due to the fact that this bridging fault is equivalent to the bridging of the previous stage, resulting in a wired-OR between the affected nodes.

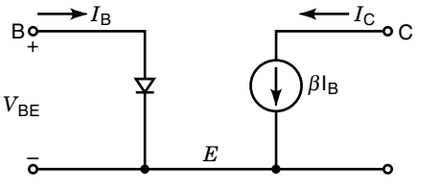

Figure 21. Large signal model for bipolar transistor.

Since bridging is not a deliberate feature, it is not always a hard short and in general can exhibit significant resistance. A very high resistance may imply a bridging fault of no consequence. The range of resistance exhibiting significant impact on the logic values needs to be studied. To study the effects of bridging faults in ECL under varying bridging resistances, we use the bipolar transistor large-signal model.

The large-signal model of the transistor shown in Fig. 21 which is suitable for bias-circuit calculations consists of a base-emitter diode and a controlled collector current generator (35). In this model the collector voltage ideally has no influence on the collector current, and the collector node acts as a high-impedance current source. Here the collector current (I_C) is expressed as

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

where I_S is the saturation current, V_{BE} is the base to emitter voltage drop, and V_T is the threshold voltage.

The case of two ECL output stages is shown in Fig. 22 with unknown bridging resistance R_X [32,33]. When the logic levels at V_1 and V_2 are the same, namely 00(11), then due to the wired-OR property of ECL, these same logic levels 00(11) are maintained at V_1 and V_2. When one of the nodes is at logic level low (0) and the other at logic level high (1) with a bridging resistance of a significant value ($R_X > 0\ \Omega$), the voltage levels at the nodes will not necessarily be at logic level '0' or '1'. The voltage levels at the nodes are computed using the model presented, and then the range of bridging resistances affecting the logic levels is determined.

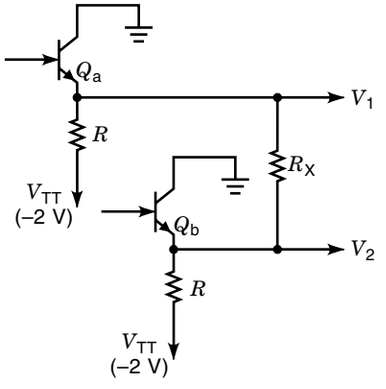

Figure 22. Output bridging fault in ECL with unknown resistance R_x.

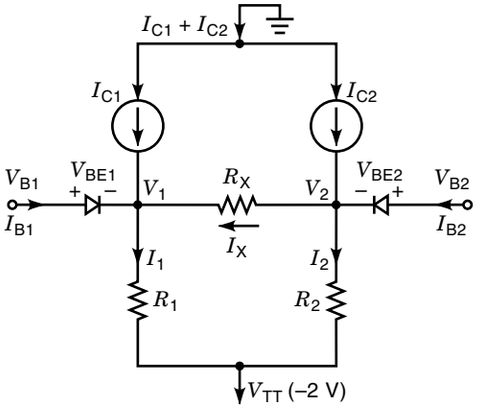

Figure 23. Equivalent large signal model.

An equivalent transistor-level model for the two ECL output stages with the bridging resistances is shown in Fig. 23. Referring to Fig. 23, we can find V_1 and V_1 under different values of bridging resistances (R_X) when one of the nodes is at logic level '1' and the other is at logic level '0'. It can be seen that when both the nodes are at logic levels '00'('11'), the bridging resistance does not alter the logic levels at the two nodes.

Since one of the ECL output nodes is considered to be at logic level '0' and the other at logic level '1', we let the transistor Q_1 emitter output be at logic level '0' and Q_2 output be at logic level '1'. As bridging resistance is introduced, the voltage levels will change or settle at a value depending on the bridging resistance. In the case of the MECL OR/NOR (1) device, the base voltage of the emitter follower is -0.98 V for output logic level '0'(-1.75 V), and the base voltage of the emitter follower is -0.05 V for output logic level '1' (-0.98 V). The output logic levels are fixed and determined by driving the circuitry transistors (Q_1, Q_2, Q_3).

Referring to Fig. 23, currents $I_1 I_2$ and I_X can be expressed as

$$I_1 = I_{C1} + I_{B1} + I_X$$
$$I_2 = I_{C2} + I_{B2} - I_X$$
$$I_X = \frac{(V_2 - V_1)}{R_X} \tag{1}$$

Since $R_1 = R_2 = R$, voltages V_1 and V_1 can be expressed as

$$V_1 - V_{TT} = (I_{C1} + I_{B1} + I_X)R \tag{2}$$
$$V_2 - V_{TT} = (I_{C2} + I_{B2} + I_X)R \tag{3}$$

Total current I can be expressed as

$$I = I_{B1} + I_{C1} + I_{B2} + I_{C2} \tag{4}$$

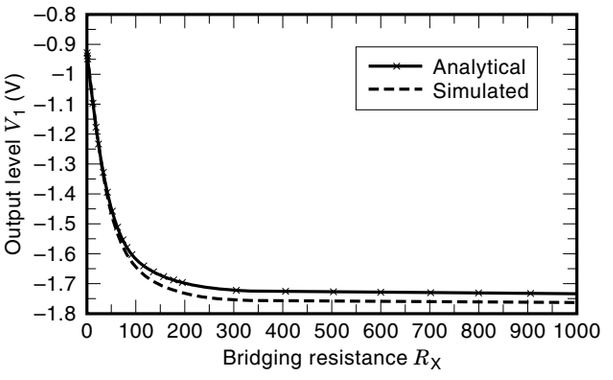

Figure 24. Output level as a function of bridging resistance, according to Equations (7) and (8), and SPICE simulations.

where I_{B1}, I_{C1}, I_{B2}, and I_{C2} are given by

$$I_{C1} = I_S \exp\left(\frac{V_{BE1}}{V_T}\right)$$

$$I_{B1} = \frac{1}{\beta}\left[I_S \exp\left(\frac{V_{BE1}}{V_T}\right)\right]$$

$$I_{C2} = I_S \exp\left(\frac{V_{BE2}}{V_T}\right)$$

$$I_{B2} = \frac{1}{\beta}\left[I_S \exp\left(\frac{V_{BE2}}{V_T}\right)\right]$$

From Fig. 23 it can be seen that

$$V_1 = V_{B1} - V_{BE1} \tag{5}$$

$$V_2 = V_{B2} - V_{BE2} \tag{6}$$

$$V_{BE1} = \left[\frac{(1+\beta)}{\beta} I_S \exp\left(\frac{V_{BE2}}{V_T}\right) R + V_{B1}\left(\frac{R}{R_X}\right) - V_{B2}\left(1+\frac{R}{R_X}\right) + V_{TT} + V_{BE2}\left(1+\frac{R}{R_X}\right)\right]\left(\frac{R_X}{R}\right) \tag{7}$$

$$V_{BE2} = \left[\frac{(1+\beta)}{\beta} I_S \exp\left(\frac{V_{BE1}}{V_T}\right) R - V_{B1}\left(1+\frac{R}{R_X}\right) + V_{B2}\left(\frac{R}{R_X}\right) + V_{TT} - V_{BE1}\left(-1-\frac{R}{R_X}\right)\right]\left(\frac{R_X}{R}\right) \tag{8}$$

Since we started with V_2 at logic level 'high', that is, $V_{B2} \approx -0.05$ V and $V_{BE2} \approx 0.84$ V, the resulting V_2 is ($V_2 = 0.05 + (-0.84) = -0.89$ V). The exact values of V_{BE1} and V_{BE2} are computed iteratively for different values of bridging resistances (R_X), satisfying equations (7) and (8). V_{BE1} and V_{BE2} thus obtained are substituted into Equations (5) and (6) to obtain the logic levels at V_1 and V_2. The output voltage level at V_1 was computed iteratively using the above two expressions (7) and (8) for varying bridging resistances (R_X) and the analytical curve depicted in Fig. 24. The SPICE simulation shown by the dotted line in Figure 24 confirms its close relationship to the analytical result. Beyond about 100 Ω, there is a slight bias from the analytical curve because default SPICE transistor parameters were used for the SPICE simulation instead of the exact SPICE parameters of the ECL device which are not precisely known.

An interesting bridging fault to study for varying bridging resistances is that of an ECL device with bridging between the true and complementary outputs; this is shown in Fig. 25. The SPICE simulation for V_1 output is shown in the figure for varying bridging resistances. At the V_1 output the bridging fault gets sensitized for input vector $AB = 00$. The inferences drawn from this simulation are as follows:

1. For bridging resistances less than about 9 Ω, the logic level is same as that of a hard short. This corresponds to the wired-OR condition.

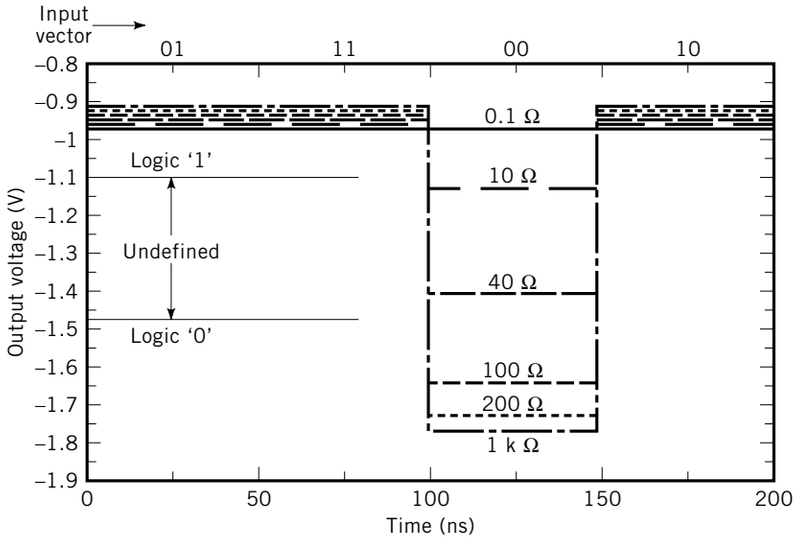

Figure 25. Output voltage under varying bridging resistances.

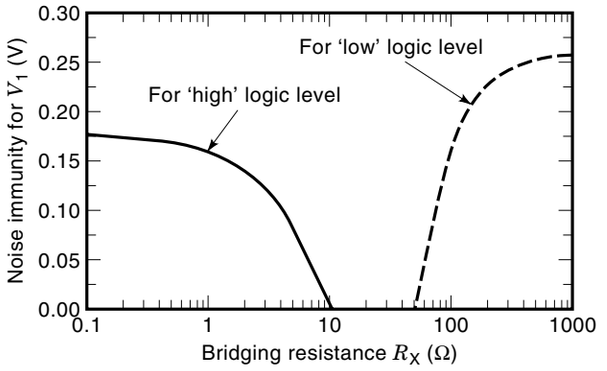

Figure 26. The noise immunity for V_1: Normal logic value 'L' with noise immunity of 0.26 V.

2. When bridging resistance is greater than 9 Ω and less than about 55 Ω, the logic level is in the 'undefined' level.
3. For bridging resistance values greater than 55 Ω, the logic level stays on the correct side (logic '0'), but the noise immunity is degraded near the above-mentioned resistance value.
4. When bridging resistance is greater than about 1 kΩ, the bridging is of no consequence.

In *n*MOS/CMOS the 'undefined' level is interpreted by the successive stage as either a '1' or a '0' depending on the logic threshold. Since ECL devices operate in a nonsaturating form of digital logic, an undefined logic level input to a successive stage may cause an 'undefined' voltage level to appear at the output.

Estimation of noise immunity for both nodes was carried out. The voltage level at the two nodes V_1 and V_2 was obtained under varying bridging resistances. Noise immunity for the high logic level was estimated by computing the difference between the node voltage and V_{IHmin} (minimum input voltage for logic level 'high'). Similarly noise immunity for the low logic level was estimated by computing the difference between V_{ILmax} (maximum input voltage for logic level 'low') and the node voltage.

Figure 26 shows the noise immunity for node V_1 under 'low' and 'high' logic level conditions. It can be seen that under high bridging resistances, the logic level stays on the correct side (logic level 'L'). As the value of the bridging resistance is lowered (≈55 Ω), the noise immunity of the node V_1 for logic level 'L' keeps getting lower and approaches zero. Further lowering the value of bridging resistance pushes the node V_1 to an undefined level. Continuing the process of lowering the value of the bridging resistance results in logic level 'H' at the node V_1 which is a faulty logic level, and its noise immunity is depicted as "for 'HIGH' Logic level". A logic device being driven by this node may interpret this faulty logic level correctly even though the logic level is on the incorrect side of the logic threshold. Node V_2 remains at logic level 'H' irrespective of the bridging resistance because of the wired-OR property of ECL. Depending on the value of the bridging resistance, the voltage level at this node also changes slightly but not appreciably enough to switch to the incorrect side. The noise immunity of node V_2 is shown in Fig. 27.

BRIDGING OF LOGICAL NODES WITH FEEDBACK

Logical nodes can derive their logic value from one another due to bridging. When the feedback path caused by bridging contains clocked storage elements, the behavior of the combinational blocks involved may get modified but not result in any extra states. If the feedback loop does not contain clocked storage elements, then asynchronous feedback paths will be frequently introduced, transforming the combinational block into an asynchronous sequential circuit. It has been shown that if a feedback loop contains an odd number of inversions, then oscillations can occur (36). Under such bridging faults any oscillations will cause undefined voltage levels at the output. The anomalous behavior seen in this class of bridging faults depends on propagation delay, rise time, fall time, and analog transfer characteristics of the bipolar transistors used in the device.

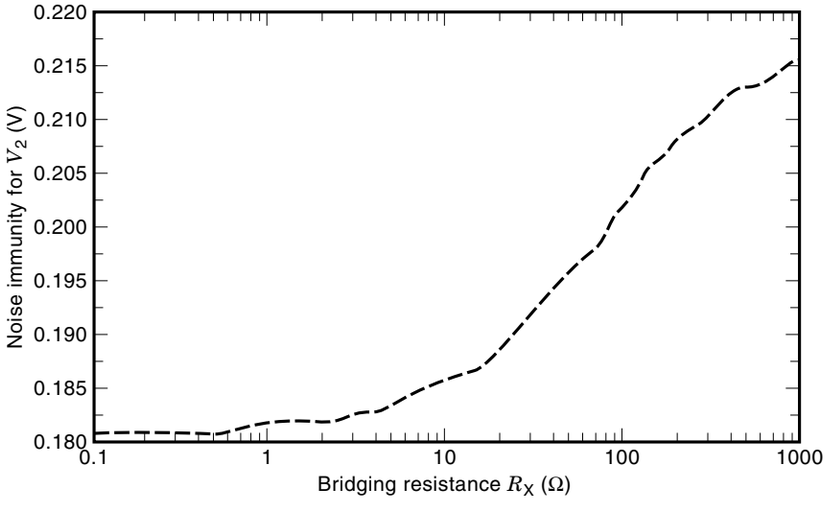

Figure 27. Noise immunity for V_2: Normal logic value 'H' with noise immunity of 0.215 V.

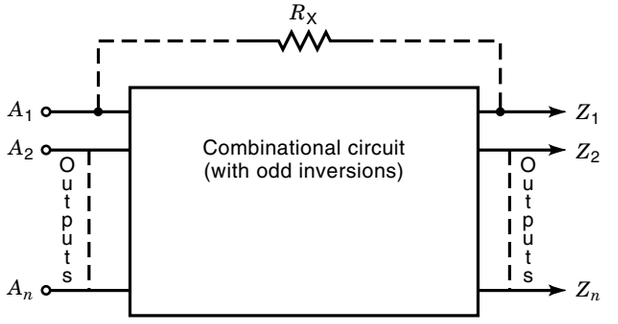

Figure 28. Combinational circuit illustrating bridging fault with feedback.

To analyze bridging faults of this class, consider the diagram in Fig. 28, where input A_1 is bridged with output Z_1 through a sufficient bridging resistance (R_X). Assume that an input vector is applied under which there is a sensitized path from A_1 to Z_1 through an odd number of inversions. We have seen that ECL logical input and output nodes have the property of wired-OR, that is, logic level '1' dominates '0'. When A_1 is logic level '1', Z_1 is '0' without feedback bridging, so a stable situation persists despite the feedback bridging. The situation will be different in the presence of feedback bridging, when A_1 is '0'. Consider the case where rise and fall times are much smaller compared to propagation delay. Then the output level (Z_1) changes after the propagation delay. In the above situation oscillations will occur where the propagation delay determines the clock period of oscillations.

In contrast, when the propagation delay is smaller than the rise or fall times, the output will start changing before the input has time to stabilize. This leads to a situation where a rising or falling input signal starts influencing itself in the opposite direction before it reaches the switching threshold. This behavior needs to be analyzed using a dynamic analysis that takes into account the transistor characteristics, node capacitances, and so on since a static analysis alone does not suffice.

The two cases are illustrated in ECL devices using ECL OR/NOR gates with a feedback bridging fault obtained by SPICE simulation. The ECL devices provide true and complementary outputs. The complementary output on a single device is a special case of an odd number of inversions investigated with one level of inversion. When the propagation delay is small, for example, one ECL OR/NOR gate, oscillations do not occur, and the voltage level is stabilized at the intermediate level (undefined). Effects of bridging resistance under feedback bridging conditions were studied. For low bridging resistances the voltage level stabilized at the intermediate level. However, as the value of bridging resistance was increased, the effect of bridging became insignificant, resulting in correct logic levels.

When propagation delay is sufficiently large (with three or more inversions of ECL stages), oscillations will occur. When the bridging resistance (R_X) is sufficiently small, the oscillations will touch either '0' or '1'. When propagation delay is just sufficiently large enough for oscillations, it will cause signals to cross the threshold voltage, and the requirement for oscillation (30) to occur is observed to be

$$t_{pd} > \frac{t_r + t_f}{2}$$

where t_{pd} is the propagation delay, t_r is the rise-time, and t_f is the fall-time.

Example The SPICE (23) simulation using a specific set of parameters for a chain of ECL OR/NOR gates exhibited the following characteristics: t_{pd}/gate = 0.36 ns, t_r = 0.2 ns, and t_f = 0.3 ns. These characteristics suggest that oscillations will occur with a propagation delay of 0.36 ns for the device chain. Simulations do not exhibit oscillations with one device, but oscillations do occur with a device chain of 3 (t_{pd} = 1.08 ns), as shown in Fig. 29(b)–(c) for output signals with no bridging and with feedback bridging, respectively.

CONCLUSION

The exponential growth in computer system performance has been mostly due to the advances in CMOS VLSI technology. Developments in CMOS VLSI designs have made tremendous inroads in realizing compact circuits with feature sizes today ranging below 0.35 μm. Present-day processor chips perform at 300 MHz and beyond. Semiconductor memories have not kept pace with the speed improvements in processor chip speeds. However, some advances in ECL technology have made it possible to fabricate bipolar ECL devices that occupy less space and consume lower power. As low power, high speed, and high density are achieved, ECL technology is expected to find wide application in various high-performance digital circuits. Already highly integrated bipolar and bipolar/MOS chips are coming into common use, further narrowing the gap between low-cost workstations and high-performance servers.

To keep up with the speed improvements in processor chips, the memory access times have to be reduced correspondingly. Bipolar ECL memories provide a speed advantage over CMOS memories, and speed critical designs have been shown to benefit from the use of bipolar ECL memories. We have considered early bipolar ECL memory designs as well as some present-day ECL memory designs examples.

Rapid advances, increasing complexities, and shrinking device geometries in VLSI have enabled complex integrated circuits to be manufactured for extremely complex systems at lower costs. Various modes of failures can occur in such complex VLSI devices, out of which, transistor-level shorts and opens model many of the failure modes and defects in ICs. To analyze the various modes of failures and their effects, failures in bipolar ECL memory designs were examined in detail using both simple and enhanced fault models. Physical failures in two different ECL storage elements were analyzed. The results showed that fault coverage may not be obtained using the minimal fault model for ECL storage elements. The enhanced fault model provides higher explicit coverage of physical failures compared to the minimal fault model. The enhanced fault model includes faults that cause the cell to become *data* or $\overline{data}$-feed-through as well as faults that cause the cell unable to latch high or low signals. When modest

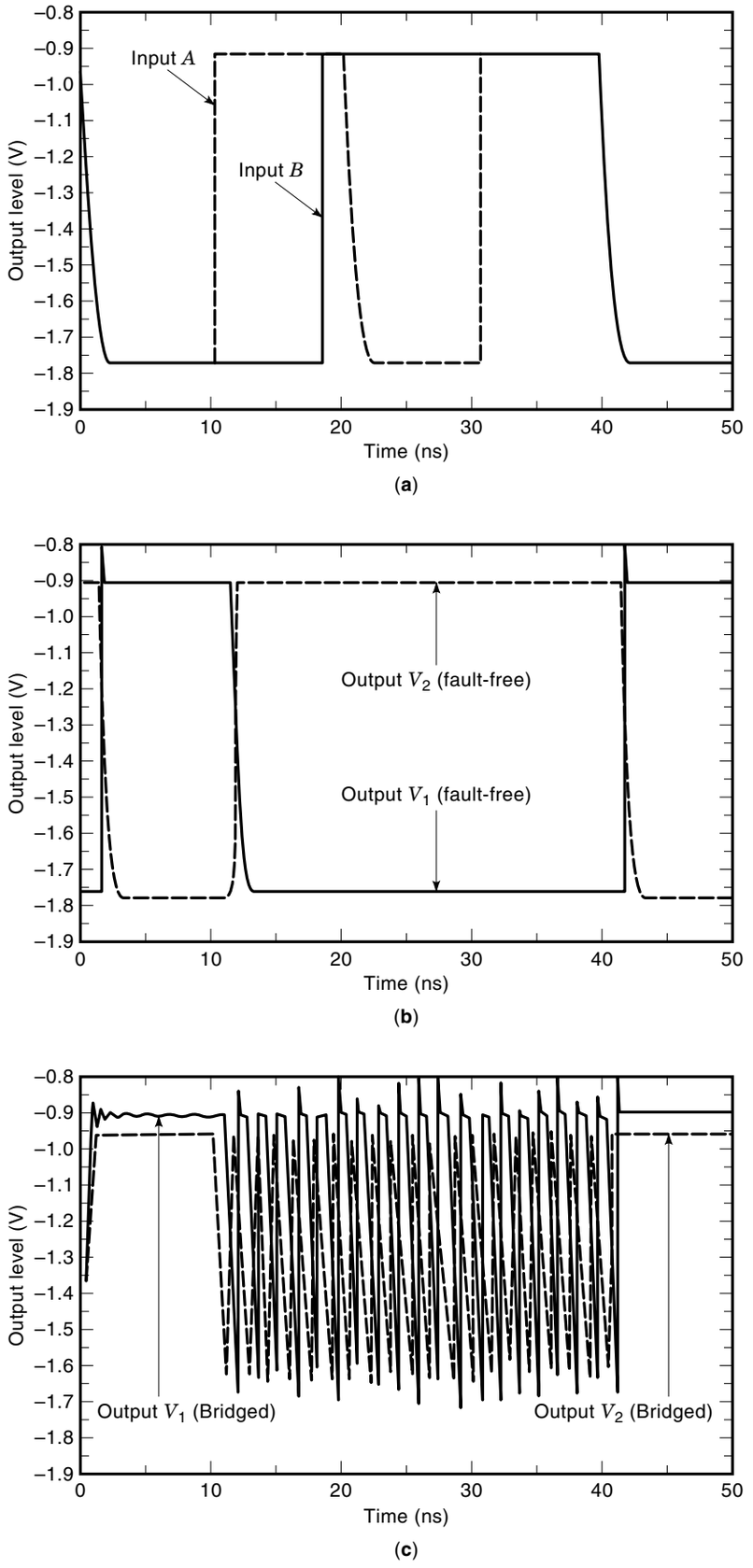

Figure 29. Oscillations under feedback bridging: (a) Input signals, (b) fault-free outputs, (c) oscillations under feedback bridging.

fault coverage is needed, the minimal fault model may be sufficient. However, in situations where higher fault coverage is sought, the enhanced fault model can provide higher coverage of physical failures. Power supply current monitoring can be used for detection of certain types of faults in ECL storage elements. A testable design approach using the exclusive-OR gate is presented for detecting *loss of complementarity* in ECL storage elements with true and complementary outputs.

A detailed transistor-level analysis was performed in order to study bridging faults in ECL. A case of a bridging fault manifest as a struck-at fault was shown. Effects of bridging of logical nodes in ECL without feedback and with feedback were fully studied, and a method for computing output voltage levels under certain bridging conditions was developed. SPICE simulations seem to be closely related to the developed analytical model. Also considered were bridging of ECL logical nodes with feedback exhibiting oscillations under certain conditions, and the effects of bridging faults and bridging resistances on output logic levels in ECL and on noise immunity.

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SANKARAN M. MENON
PHANINDRA K. MANNAVA
South Dakota School of Mines and Technology