EMITTER-COUPLED LOGIC

DIGITAL LOGICI

BIPOLAR CIRCUITS

Emitter-coupled logic (ECL) is a digital logic circuit technique utilizing bipolar *npn* transistors. The basic component of an ECL digital logic circuit is the emitter-coupled pair of *npn* transistors, which have the emitter nodes connected together. The base voltages control how the total emitter current is split between the two transistors. Configurations of emitter-coupled transistors implement logic functions such as inverter, nand, nor, exclusive-or, latch, and flipflop. Important performance criteria include static (dc), transient (ac), and power dissipation.

HISTORICAL OVERVIEW

ECL was invented at Motorola in the early 1960s (1) as a fast, high-power digital circuit technique using silicon bipolar transistors. The fast delay time is due to the reduced voltage logic swing, which is typically between 300 mV and 800 mV with a 5.2 V power supply compared to the full-rail logic swing between V_{DD} and ground in CMOS (complementary metal-oxide semiconductor) circuits. Also, ECL circuits avoid transistor saturation by using forward active transistor operation to minimize switching time. On the other hand, in TTL (transistor-transistor logic) circuits, the transistors operate in saturation and require a longer time to switch off, leading to longer propagation delays. The high power in ECL circuits is due to the constant current drain in each logic gate, regardless of whether the circuit is switching or not. In CMOS circuits, power is dissipated only during the switching event.

Further improvements in the bipolar fabrication process have reduced the parasitic capacitances and resistances, leading to faster circuit operation at lower currents. Thus, ECL has moved into the realm of very large scale integrated (VLSI) circuits while maintaining its speed advantage over other circuit technologies. Because of the large power dissipation, however, ECL is most appropriate for applications where fast circuit switching is the primary consideration, such as high-speed test equipment, telecommunications, and high-performance computing. ECL circuits were historically fabricated in silicon using *npn* bipolar transistors because the *npn* transistors switch faster than *pnp* transistors. Silicon remains the most economical material for semiconductor processing. However, for ECL circuits, the true speed advantage is realized more effectively with other devices such as SiGe heterojunction bipolar transistors (HBT) and InP double heterojunction bipolar transistor (DHBT) (7)–(11).

EMITTER-COUPLED PAIR

The most fundamental component of an ECL circuit is the emitter-coupled pair that connects the emitter terminals of *npn* bipolar transistors. This analysis applies to silicon bipolar transistors. The basic ECL gate, shown in Fig. 1(a), contains two *npn* bipolar transistors (Q_1 and Q_2), two load resistors (R_{L1} and R_{L2}), and an ideal current source (I_{CS}). The input signal is V_I and the two output signals are V_{O1} and V_{O2}. Two power supply voltages, V_{CC} and V_{EE}, and one reference voltage, V_R, are also required. Typically, V_{CC} is tied to ground (0 V) and the voltage of V_{EE} is -4.5 V to -5.2 V. Note that the emitter terminals of the *npn* transistors are connected together, hence the name emitter-coupled logic. The current source is connected to the common emitter node to bias the transistors in the forward active region. The load resistors, tied between the collector nodes and V_{CC}, convert the current signal to a voltage signal to drive fan-out gates, not shown in the schematic.

The circuit in Fig. 1(a) operates as follows. The input signal V_I steers the current I_{CS} through Q_1 or Q_2. When the input signal V_I is greater than the reference voltage V_R, transistor Q_1 is ON, current flows through Q_1 and R_{L1} to pull V_{O1} to a low logic level. Also, no current flows through Q_2 and V_{O2} is pulled up to V_{CC} (the high logic level). In the other state, input signal V_I is less than V_R and current flows through Q_2 and R_{L2} to pull V_{O2} to a low logic level. Also, V_{O1} is pulled to V_{CC}. As a result, the output V_{O1} is the inversion of the input signal and is called the NOR output. The output V_{O2} is the true of the input signal and is called the OR output. This circuit serves as an inverter and as a buffer logic gate with OR and NOR being complementary outputs.

In emitter-coupled circuits, the *npn* bipolar transistor, shown in Fig. 2(a), is operated in the forward active region with $V_{BE} > 0$ and $V_{BC} < 0$. In reality, V_{BC} may be positive but not greater than 0.5 V_{BE}. For silicon transistors, V_{BE} is 700 to 800 mV. Strictly speaking, the saturation region is defined as $V_{BE} > 0$ and $V_{BC} > 0$, which usually results in a long delay to turn the transistor OFF. However, if V_{BC} is small, such as below 400 mV, the turn-off delay from saturation is approximately the same as the turn-off time from the forward active region. The terminal currents, I_B, I_E, and I_C, are shown flowing in the direction of positive current for an *npn* transistor in forward-active mode.

The simplest model of the large-signal model of the *npn* bipolar transistor is shown in Fig. 2(b) where the Ebers–Moll model (2) has been simplified to account for forward-active operation, and parasitic resistances and capacitances have been neglected. The diode D_E accounts for the base–emitter junction while the dependent current source models the current gain effect.

A more detailed model is shown in Fig. 2(c). While ECL designers use a more complex model than that shown in Fig. 2(c), the model does include the principal elements to account for the transistor behavior. The diode D_E accounts for the base–emitter junction while the dependent current source models the current gain effect. The terminal resistances, R_B, R_E, and R_C, account for the contact resistance and bulk resistance from the terminal to the intrinsic transistor. The capacitances C_{BE} and C_{BC} model the total capacitance associated with the base–emitter and base–collector junctions, respectively. The total capacitance includes the junction capacitance (due to fixed ionic charges) and the diffusion capacitance (due to mobile charge carriers). The

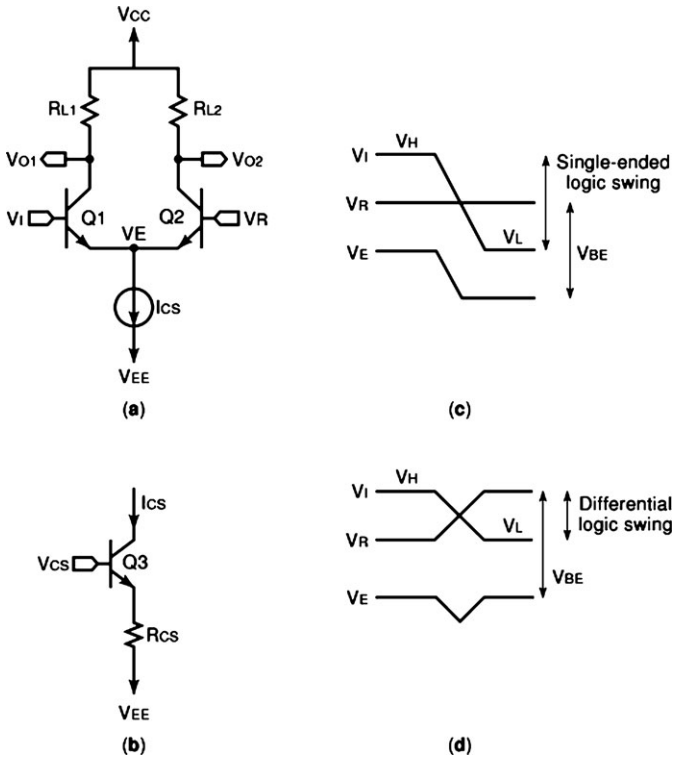

Figure 1. Emitter-coupled logic. (a) ECL buffer/inverter. (b) Current source, replaces the ideal current source in (a). (c) Single-ended logic levels. V_H is the logic high level and V_L is the logic low level. The reference voltage is in the middle of the logic swing. The emitter voltage is V_{BE} below the higher base voltage. (d) Differential logic signals. V_R is the complement of V_I. The emitter voltage remains at the same level except during the signal transition.

third capacitance, C_{CS}, models the total capacitance associated with the collector–substrate junction, as found in an integrated circuit. Typically, C_{CS} includes only junction capacitance since the collector–substrate junction is reverse-biased where the diffusion capacitance is negligible.

Using the simple transistor model in Fig. 2(b) in the for ward active region, the collector current, IC, is

$$I_C = I_S(e^{V_{BE}/V_T}) \tag{1}$$

where I_S is the reverse saturation current, V_{BE} is the base emitter voltage, $V_T = kT/q$ is the thermal voltage, K is Boltzmann's constant, T is temperature in Kelvin, and $q = 1.6e - 19$C is the electronic charge. At room temperature, $V_T = 25.9$ mV. A typical value for I_S is 1.0e–18 A for a minimum size digital circuit transistor. The base current, I_B, is

$$I_B = I_C/\beta \tag{2}$$

where β is the common emitter current gain. For *npn* transistors, β is typically 100 but can range in value from 60 to 500. Thus, the base current is only about 1% of the collector current. The emitter current is

$$I_E = I_C(\beta + 1)/\beta = I_C/\alpha \tag{3}$$

and is slightly larger than the collector current. The common base current gain is α, which ranges in value from 0.96 to 0.998. For example, if β is 100, then α is $100/101 = 0.99$. If the emitter current is 100 μA, the collector current is 99 μA.

The ratio of the collector currents of the Emitter-coupled transistors is

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}\exp(V_{BE1}/V_T)}{I_{S2}\exp(V_{BE2}/V_T)} = \exp[(V_{B1} - V_{B2})/V_T] \tag{4}$$

Note that the transistors are assumed to be identical with the same saturation current. In an integrated circuit, the emitter coupled transistors are placed side by side, carefully matched in size and layout orientation. Thus, the transistors are very nearly identical. The emitter voltage is eliminated from the equation, indicating that the collector currents are dependent only on the difference of the base terminal voltages.

A collector current ratio of 100:1 requires a difference of $V_{B1} - V_{B2} = 120$ mV at room temperature (298 K). This is a small voltage compared to the power supply voltage of 5 V. In practice, the logic swing is at least 500 mV for single-ended signals shown in Fig. 1(c). The high logic level is labeled V_H and the low logic level is labeled V_L. Another alternative is to use differential signals where V_R is the inverted signal of V_I where the voltage swing may be as low as 200 mV, as shown in Fig. 1(d). Note that the emitter voltage is V_{BE} below the higher base voltage. Thus, in the single-ended case, the emitter voltage (V_E) changes as the input signal changes, while in the differential case, the emitter voltage does not change as the input signals change except for a small fluctuation during the signal transition. The logic high level V_H is $V_{CC} - 0 \times R_L = 0$ V and the logic low level is $V_{CC} - I_{RL} \times R_L = -I_{RL} \times R_L$. The logic swing is defined to be $V_H - V_L = I_{RL} \times R_L$. If a 500 mV logic swing is desired, possible design parameters are $R_L = 200\,\Omega$ and $I_H = 2.5$ mA. For VLSI circuits, low current is critical. In this case, a better choice is $R_L = 5\,k\Omega$ and $I_{RL} = 100\,\mu$A. The problems with larger load resistance values is the increased chip area required for the larger resistors and the increased capacitance of the larger-area load resistors. To reduce the area and capacitance of diffused *p*-type resistors, polysilicon resistors are used in ECL VLSI circuits.

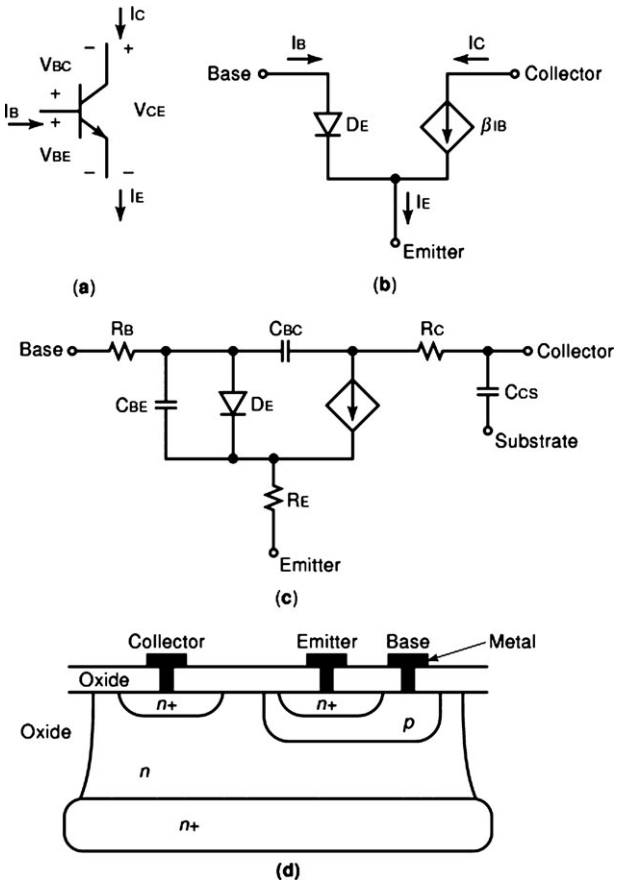

Figure 2. Bipolar junction transistor. (a) *npn* transistor symbol, terminal currents, and voltages. (b) Simple large-signal equivalent model. (c) More accurate large-signal model including parasitic capacitances and resistances. (d) Cross section of transistor in integrated circuit using oxide isolation.

The low current is a critical requirement of VLSI circuits because static power must be dissipated as heat through the integrated circuit package to keep the integrated circuit below a critical temperature for proper operation. The static power of an ECL gate is $(V_{CC} - V_{EE}) \times I_{CS}$. The total power dissipation for the entire circuit is simply the summation of the power dissipation in all individual gates.

The current in the load resistor is somewhat less than I_{CS} due to *α-losses*, that is, the small reduction in collector current compared to the emitter current. In reality, the ideal current source, I_{CS}, is formed from a transistor and resistor as shown in Fig. 1(b). The base terminal is driven by a voltage regulator generating the signal V_{CS}, which is about 1.2 to 1.6 V above V_{EE}. The current I_{CS} is

$$I_{CS} = \alpha(V_{CS} - V_{EE} - V_{EE})/R_{CS} \tag{5}$$

A commonly used circuit in ECL gates is the emitter follower, shown in Fig. 3(a). The input signal is the base of the transistor and the output signal is the emitter of the transistor. The collector is tied to V_{CC}. A current source biases the transistor in the forward-active region. The name emitter follower comes from the operation where the emitter voltage is V_{BE} below the base voltage. Thus, $V_O = V_I - V_{BE}$. This is also known as the common collector configuration since the collector is tied to "ac ground."

The emitter follower serves two purposes in ECL circuits. The first is to level-shift the base signal down by V_{BE} to accommodate different signal levels. The second purpose is to drive large fan-out loads. Consider the circuit in Fig. 3(b) where the emitter-coupled logic gate drives the emitter follower. In turn, the emitter follower drives a fan-out LOAD, which draws the current I_{FO}. In a good design, I_{FO} is much smaller than I_{EF} and I_{B1} is much smaller than I_{RL2}. Thus, the fan-out load has little effect on the logic levels of the ECL gate. In addition, the capacitance associated with LOAD, C_{L}, is charged and discharged quickly.

The cross section of an *npn* silicon bipolar transistor is shown in Fig. 2(d). The transistor is built on a *p*-type substrate and oxide-isolated from other transistors. The *n*-type epitaxial layer is the collector region. The base is *p*-type material, usually lightly doped under the emitter and heavily doped under the base contact. The emitter is n^+, heavily doped. The collector contact is also n^+ to reduce contact resistance. The terminals are formed by metal contacts through the oxide layer covering the top of the wafer.

Advantages and Disadvantages of ECL

Emitter-coupled logic has several design advantages over other types of logic circuits (3).

- Propagation delay. The propagation delay of ECL circuits is among the fastest available in any circuit technology.
- Complimentary outputs. Both true and compliment out puts are available with equal propagation delay to each output, thus improving the system timing performance.
- Transmission line drive capability. The emitter follower output has low output impedance, thus ECL is well-suited to drive low-impedance transmission lines, typically 50 Ω, although up to 130 Ω is possible. With increasing system clock, the printed circuit board interconect behaves more like a transmission line that ECL can drive.
- Constant power supply drain. The power supply drain is constant and does not change with switching signals or frequency, thus simplifying the system power supply design.
- Input pulldown resistors. Internal resistors from input pins to V_{EE} eliminate the need to connect unused input pins.
- Differential drive capability. ECL circuits are well-suited to differential input and output signals. With the high drive capability of the emitter follower output, ECL circuit can drive twisted pair lines or cables.
- Low logic swing. The small logic swing of ECL has the benefit of reduced crosstalk (a switching signal coupling charge to a neighboring constant signal, causing unwanted glitches on the neighboring signal).

However, ECL has several disadvantages:

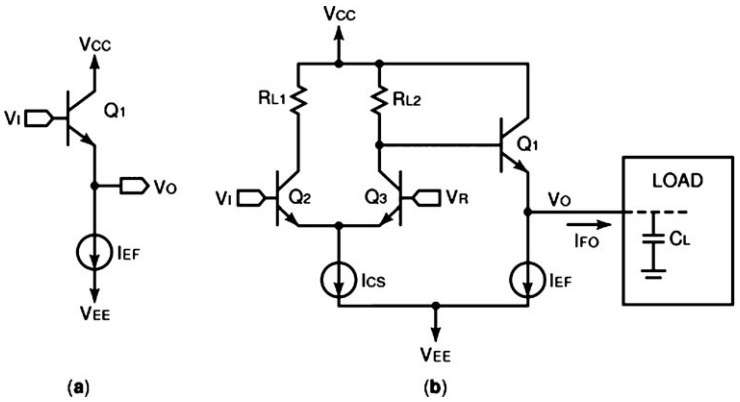

Figure 3. Emitter follower. (a) Circuit. (b) Buffer driving emitter follower that drives some fan-out load modeled by a capacitor, C_L. The current I_{EF} must be large enough to drive the fan-out load in a timely manner.

- Power dissipation. ECL has a constant power dissipation that is high compared to the almost negligible static power dissipation of CMOS. However, at high switching frequencies, the power dissipation of CMOS increases.
- Chip area. ECL occupies a relatively large chip area compared to CMOS circuits. The bipolar transistors are larger than metal-oxide semiconductor (MOS) transistors, while the resistors required for the ECL load occupy a large area compared to MOS transistors.

Logic Families

Emitter-coupled logic has been designed in several logic families with common dc (or static) specifications and similar ac (or transient) specifications. We discuss several ECL families below. MECL 10H from Motorola, Inc. has typical gate delays of 100 ps and edge rates of 1000 ps. The power supply voltage ranges from −4.5 V to −5.5 V. The power consumption per gate is 25 mW. MECL 100K from Motorola, Inc. has typical gate delays of 750 ps and edge rates of 700 ps. The power supply voltage ranges from −4.2 V to −4.8 V with a power consumption of 50 mW per gate. ECLinPS (ECL in Pico Seconds) from Motorola, Inc. was developed with high-speed system design as a primary concern. The gate delays are 500 ps maximum with flip-flop toggle frequencies of 1.0 GHz. The internal signals are all differential to minimize skew between rising and falling signals and to reduce single-ended switching noise. The variation of propagation delay as a function of temperature is less than 50 ps. The power consumption is 25 mW per gate. The chips are packaged in 28-pin plastic leaded chip carrier (PLCC) packages, which are small, square, surface mount packages with pins on all four edges. The ECLinPS 10E series is compatible with the MECL 10H family and the 100E series is compatible with the MECL 100K family.

ECLinPS Lite from Motorola, Inc. was developed with the same basic principles as ECLinPS but with even higher speed requirements. The toggle frequencies are 2.2 GHz with gate delays of 220 ps and output edge rates of 250 ps. On the other hand, the power dissipation is 75 mW per gate.

Positive emitter coupled logic (PECL) is simply ECL with V_{CC} at a positive voltage around 5 V and V_{EE} at ground or 0 V. The advantage of this design is compatibility with power supplies for CMOS and/or TTL logic circuits. However, since the logic levels in ECL are referenced to V_{CC}, special care must be taken to provide an unusually stable positive power supply voltage.

Applications

Because of the high power dissipation and fast switching speed, ECL is limited to use where the need for high performance justifies the power requirements. Examples are telecommunications, high-performance computing, instrumentation, automatic test equipment, microprocessors, multipliers, and memories (7)–(11).

PERFORMANCE

Static Characteristics

Static performance is the behavior of the circuit when the in put signals are swept slowly to eliminate time-dependent behavior such as capacitive current. The purpose of the static characteristic is to determine whether the fan-out gates correctly interpret the signal of the driving gate. The voltage transfer characteristic (VTC) relates the output voltage to the input voltage.

For the ECL system designer, the specifications from ECL databooks are the primary concern. The ECL VLSI circuit designer has two concerns. The first is to meet the specifications in the databook for the input buffers and output buffers. The second concern is to implement the maximum number of logic functions using the least power in a circuit that is robust and that operates over wide voltage and temperature ranges. This requires using complex logic gates (discussed in a later section) as well as considering the logic swing and the variation with supply voltage and operating temperature.

Static characteristics are called “dc characteristics” in most databooks. See Fig. 4 for a plot of the voltage transfer characteristic of an ECL output buffer where the solid curve is the OR output and the dashed curve is the NOR output. Two corners of the rectangular box indicate the specifications for V_{IH}, V_{OH}, V_{IL}, and V_{OL}. From a system viewpoint, the following parameters are important.

V_{OH}—output high voltage level. This is the minimum value of the output voltage for a logic HIGH.

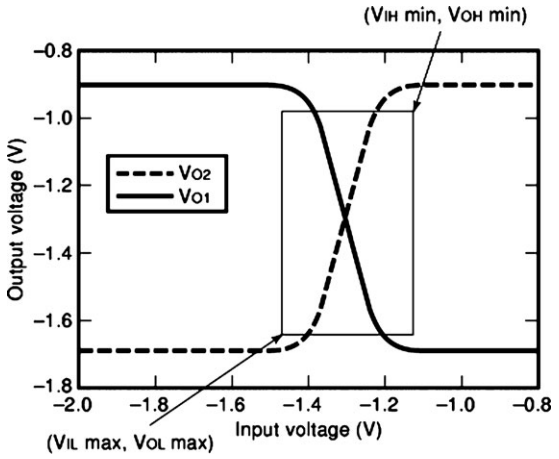

Figure 4. Voltage transfer characteristic. The specifications are indicated by the rectangle with corners (V_{IL} max, V_{OL} max) and (V_{IH} min, V_{OH} min). To meet the specifications, the curves must cross the rectangle on the upper and lower edges.

V_{OL}—output low voltage level. This is the maximum value of the output voltage for a logic LOW.

V_{IL}—input voltage recognized as a low signal. The maximum value is the worst case.

V_{IH}—input voltage recognized as a high signal. The minimum value is the worst case.

A voltage transfer curve that meets the dc specifications will pass through the rectangle in Fig. 4 on the upper and lower edges. The noise margins are defined as $NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$.

I_{IH}—input high current. This is the base current of the in put transistors plus the current through the pulldown resistor with value of 50 to 75 kΩ.

I_{IL}—input low current. Since the input transistor is OFF, the base current is negligible. Thus the input current is the current through the pulldown resistor, usually with value of 50 to 75 kΩ.

I_{EE}—power supply current.

For the ECL VLSI circuit, logic levels must be properly designed to ensure that transistors switch properly (noise margins are large enough) and that transistors do not saturate (to maintain fast switching times). Consider the circuit in Fig. 5. This is a three-input AND/NAND gate using stacked logic discussed later in this article. This circuit is an example to explain the requirements for logic levels. There are three logic levels labeled A, B, and C, which are offset by V_{BE}. We assume that $V_{BC} \leq 0.5\,V_{BE}$ to avoid deep saturation. There are two cases to consider: single-ended and differential signals. We start with the single-ended signal case that is illustrated in Fig. 5.

The single-ended swing is assumed to be $V_L = V_{OH} - V_{OL} = V_{BE}$ with a reference voltage in the middle of the single-ended swing. The output swings from 0 to $-V_{BE}$. The highest possible A voltage swing is $-0.5\,V_{BE}$ to $-1.5\,V_{BE}$ to avoid deep saturation of Q_1. Thus, V_{RA} is $-1.0\,V_{BE}$ and the emitter voltage swings from $-1.5\,V_{BE}$ to $-2.0\,V_{BE}$. The B level voltage swing is $-1.5\,V_{BE}$ to $-2.5\,V_{BE}$. Similarly, $V_{RB} = -2.0\,V_{BE}$ and the emitter voltage swings from $-2.5\,V_{BE}$ to $-3.0\,V_{BE}$. For the C level, the logic swing is $-2.5\,V_{BE}$ to $-3.5\,V_{BE}$. Similarly, $V_{RC} = -3.0\,V_{BE}$ and the emitter voltage swings from $-3.5\,V_{BE}$ to $-4.0\,V_{BE}$;. The maximum value of V_{CS} is $-3.5\,V_{BE}$, which gives a current source emitter voltage of $-4.5\,V_{BE}$. Assuming at least $0.5\,V_{BE}$ across the current source resistor, V_{EE} is $5.0\,V_{BE}$. At -55°C, when V_{BE} is about 1.0 V, V_{EE} must be around 5 V to use three levels of stacked logic. Each level of logic uses $1\,V_{BE}$ of "headroom;" thus a lower voltage supply would necessitate using fewer logic levels for single-ended logic signals.

The differential logic swing is assumed to be $0.5\,V_{BE}$ and the output swings between 0 to $-0.5\,V_{BE}$. No reference voltages are required. Note the emitter voltage does not change based on the input signal. The A voltage swing is 0 to $-0.5\,V_{BE}$. The B levels are $-1.0\,V_{BE}$ to $-1.5\,V_{BE}$ and the C levels are $-2.0\,V_{BE}$ to $-2.5\,V_{BE}$. The emitter voltage at the C level is $-3.0\,V_{BE}$. The maximum value of V_{CS} is $-2.5\,V_{BE}$, which gives a current source emitter voltage of $-3.5\,V_{BE}$. Assuming at least $0.5\,V_{BE}$ across the current source resistor, V_{EE} is $4.0\,V_{BE}$. At $-55\,^\circ$C, when V_{BE} is about 1.0 V, V_{EE} must be around 4 V to use three levels of stacked logic. Thus, differential signals use less headroom than single-ended signals.

Transient Characteristics

Transient characteristics describe the circuit behavior as a function of time. The purpose of transient characterization is to determine how fast the circuit can switch and, therefore, the maximum speed of the system. Transient characteristics are called "ac characteristics" in most databooks, although the parameters are not functions of frequency.

Propagation delay, the primary transient parameter of concern, is defined as the time from when a single-ended in put signal crosses the midpoint to when the single-ended out put signal crosses the midpoint, measured at $V_{50\%} = 0.5(V_L + V_H)$, halfway between the low and high logic levels. For differential signals, propagation delay is measured from when the signals cross each other. See Fig. 6(a) and (b). Other transient parameters are setup/hold times, rise/fall time, skew, release time, and maximum frequency.

In ECL circuits, the propagation delay is strongly dependent on the bias current in the ECL gate. See Fig. 7 for a plot of propagation delay as a function of bias current, I_{CS}. The delay is largest for small current (0.1 mA) because the circuit capacitances require a long time to charge and discharge as a result of the small bias current. As the bias current increases, the delay time decreases. The "knee" occurs around 0.4 mA where further increases in bias current do not result in significantly smaller delays. Therefore, the optimal choice of bias current is 0.3 to 0.4 mA where the power and delay are both optimized. One must also consider the delay-bias current trade-off at the extreme operating conditions (low/high V_{EE}, temperature range of $-55\,^\circ$C to $125\,^\circ$C, and slow/fast process parameters) to ensure that the ECL gate does not operate too far to the left of the optimal point under extreme conditions.

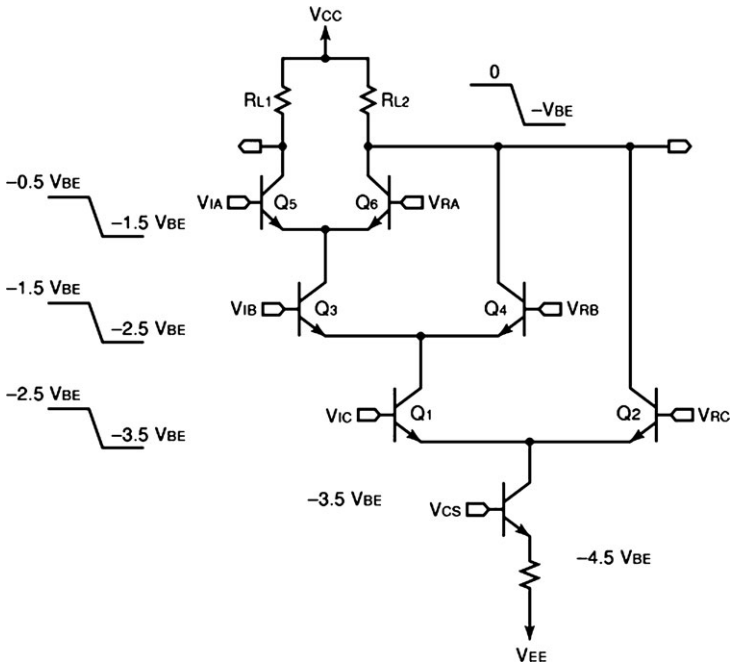

Figure 5. AND/NAND gate with 3 inputs. The signal levels are for single-ended signals showing the minimum voltage supply required to avoid saturating any transistors.

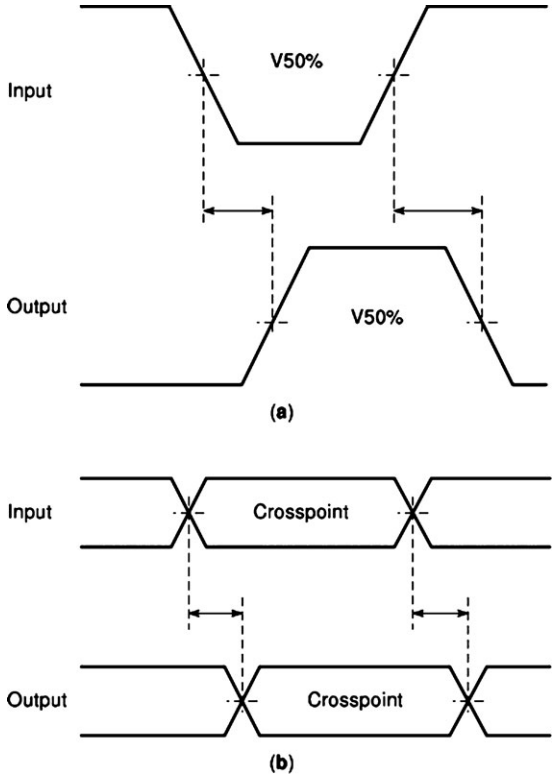

Figure 6. Transient characteristics for propagation delay. (a) With single-ended signals, propagation delay is measured at the 50% points. (b) With differential signals, propagation delay is measured when the signals cross.

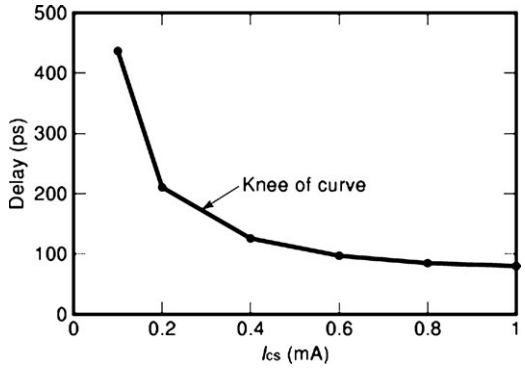

Figure 7. Delay versus bias current. The delay is long at low bias current because the small current takes a long time to charge and discharge capacitances. As bias current increases, the delay decreases. At the knee, around 0.4 mA in this example, the decrease in delay is small for increasing bias current. The optimal operating point, in terms of delay and power, is at the knee of the curve.

Power

Static power is the primary concern for ECL. The static power is the power supply potential difference times the dc current of the V_{EE} power supply. Thus, the total dc power dissipation is $P_{DC} = I_{EE} \times (V_{CC} - V_{EE})$. Dynamic power is the power dissipated during switching events. For CMOS, dynamic power is the primary concern since the static power is negligible. For ECL, the dynamic power is usually small compared to the static power, thus generating much less power supply noise than CMOS.

Layout

Layout is the task of creating the mask data for manufacturing the integrated circuit or printed circuit board from the schematic specifications. Although a good layout has many considerations, two aspects of layout practice that are especially critical to a successful ECL integrated circuit are device matching and metal width.

Device Matching. The first layout consideration is the matching required for certain devices. Emitter-coupled transistors must be matched in size, configuration, and orientation to optimize the matching of transistor parameters such as saturation current and terminal resistances. Also, the load resistors should be matched for size and orientation, particularly for differential signals. See Fig. 8(a) for a layout of the emitter-coupled gate in Fig. 1(a) with the ideal current source replaced by the circuit in Fig. 1(b). The transistors Q_1 and Q_2 are oriented in the same direction and are the same size. The bias transistor, Q_3, is also oriented in the same direction, although this is not as critical as matching Q_1 and Q_2. Also, Q_3 could be rotated 180° with no ill effect on matching, although the connection to the Q_3 collector would be more difficult. The load resistors R_{L1} and R_{L2} are exactly the same size with the same orientation. The best situation is to have all transistors in the entire integrated circuit as well as all the resistors oriented in the same direction. At the system level, a similar consideration is matching metal lines of differential signals to minimize the skew between signals. The lines should be nearly identical in length, width, metal layer, and number of vias.

Figure 8(b) shows two emitter-coupled transistors that are oriented in the same direction but are different sizes. Figure 8(c) shows two emitter-coupled transistors that are the same size but oriented in different directions. Neither layout in Fig. 8(b) and Fig. 8(c) is good ECL layout practice and should be avoided. Good device matching with discrete components is difficult while device matching in integrated circuits is quite easy. Hence, ECL is well-suited to integrated circuit implementation.

Metal Width. In the second layout consideration, the metal width of VCC and VEE must be adequate to supply the current to the circuit, since non–power-supply lines do not typically conduct enough current to cause problems. The first concern is that the metal line be wide enough to prevent electromigration of the metal because of excessive current density. The process specifications include the maximum current density, J_m, and the metal thickness, t. The design engineer controls the width and length of the metal line. See Fig. 9(a) for a three-dimensional perspective of a metal line illustrating the dimensions. If the current is I, then $I/(tW) \leq J_m$. If this rule is violated, the metal width must be increased. The second concern with metal width is the voltage drop due to the resistance of the metal and the dc current must be small enough to allow proper circuit operation. The voltage drop in VCC metal lowers the dc levels of logic signals while the voltage drop in the VEE metal raises the dc levels of logic signals. If these voltage drops are too large, the noise margin is reduced such that the transistors may not switch properly. The maximum allowable voltage drop is typically 50 mV to 100 mV from the power supply pin to any internal gate. The resistance of the metal is calculated as $R_m = \sigma L/(Wt) = (\sigma/t) \times (L/W) = (\rho_s)$ x (number of squares) where σ is the conductivity of the metal, L is the metal length, W is the metal width, t is the metal thickness. The sheet rho, $\rho_s = \sigma/t$, is a constant for any given process. To decrease the resistance, the width can be increased or the length decreased. Figure 9(b) shows a top view of a serpentine metal line. To calculate the resistance from A to B of this geometry, use this formula: $\rho_s[(L1 + L2 + L3)/W + 0.5 + 0.5]$ where the 0.5 terms are for each of the corners in the metal line. In other words, a corner is 0.5 squares of resistance.

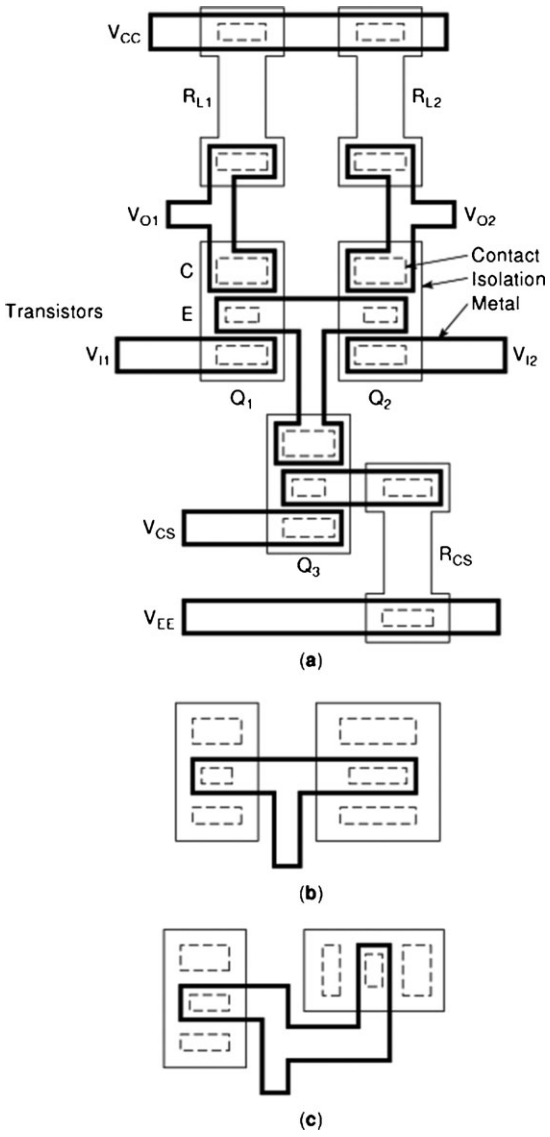

Figure 8. Integrated circuit layout. (a) Optimal layout of circuit in Fig. 1(a) with current source in Fig. 1(b). The transistors with common emitter terminals, Q_1 and Q_2, are the same size and oriented in the same direction, called matched. The load resistors are also matched. Interconnect lines are as short as possible to minimize capacitance and resistance. (b) Improper layout. The transistors are different sizes. (c) Improper layout. The transistors are oriented in different directions.

Temperature

Temperature is an important factor in the operation of semiconductor devices, including bipolar transistors and resistors. The V_{BE} of silicon bipolar transistors has a temperature coefficient of approximately −2 mV/°C. Thus, if V_{BE} at 25°C, V_{BE} at 125°C is 800 mV − (125 − 25)°C ×

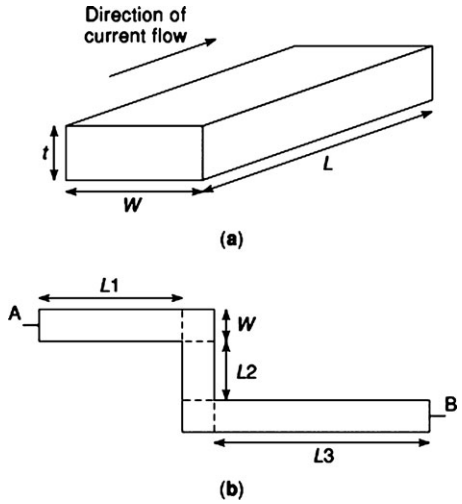

Figure 9. Metal interconnect. (a) Dimensions. The designer has control over W and L while the process engineer controls t and the material. (b) Top view of metal line to calculate equivalent resistance.

$(-2\,\text{mV}/^\circ\text{C}) = 600\,\text{mV}$. Resistors can have negative or positive temperature coefficients. For ECL devices, the effect of temperature-dependent behavior shows up in the values of V_{OH} and V_{OL} and propagation delays as functions of temperature.

FUNCTIONAL UNITS

Logic Gates

Because of the high power dissipation of ECL, well-designed circuits must implement the maximum logic function in each logic gate. This section describes four circuit configurations to increase the logic function performed without increasing the power dissipation.

The first technique is stacked logic. The basic concept is to add additional levels of emitter-coupled transistors within the logic gate. The lower level transistors act as the current sources for the higher level transistors, thus performing the AND function. See Fig. 10 for the AND/NAND gate implemented in stacked logic and compare this circuit to the inverter circuit in Fig. 1. Transistors Q_3 and Q_4 are connected between the collector of Q_1 and the load resistors. If B is low, Q_2 conducts current, pulling the AND output low. Because the emitter current to the Q_3–Q_4 pair is zero, both collector currents are zero. Thus, there is no current flowing in R_{L1} and the NAND output is high, regardless of the state of A. If B is high, then Q_1 conducts current. If A is low, Q_4 conducts current, pulling the AND output low. On the other hand, if A is high, Q_3 conducts current, pulling the NAND output low and the AND output is high. A second example of stacked logic is high, Q_3 conducts current, pulling the NAND output low and the AND output is high. A second example of stacked logic is the XOR/XNOR gate shown in Fig. 11. Another Emitter-coupled pair of transistors is added to the collector of Q_2. Using an analysis similar to the AND/NAND above, the gate is shown to implement the XOR/XNOR function. Note

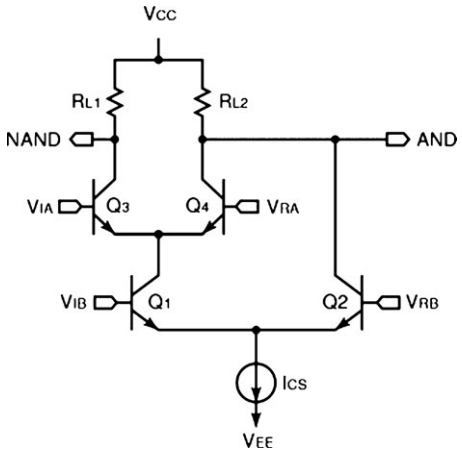

Figure 10. AND/NAND gate using stacked logic and collector dotting circuit techniques.

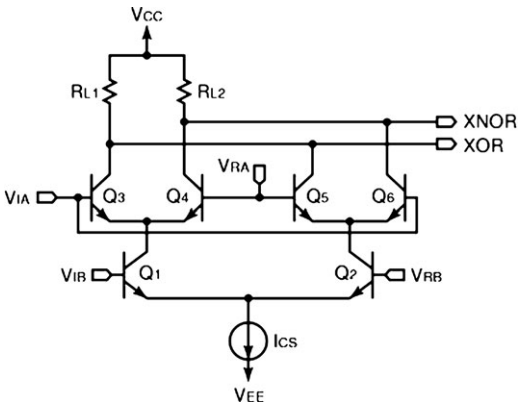

Figure 11. XOR/XNOR gate using stacked logic and collector dotting circuit techniques.

that the input signals can be single-ended or differential using stacked logic.

The XOR/XNOR circuit also demonstrates the second circuit technique called collector dotting. The collectors of Q_3 and Q_4 are connected together, as are the collectors of Q_4 and Q_6. This effectively performs the OR function by summing the collector current of all connected transistors. Therefore, current will flow in that node if current is flowing in Q_4 OR current is flowing in Q_6.

The third technique to maximize logic use of ECL is the wired OR. Transistors with the collector and emitter terminals connected in parallel while the base terminals are the input signals perform the OR function. See Fig. 12 for the OR/NOR gate. The input signals V_{I1}, V_{I2}, and V_{I3} have the same V_{L} and V_{H} levels. If V_{I1}, V_{I2}, and V_{I3} are all low, Q_1 conducts current and pulls the OR output low while the NOR output is high. If V_{I1} is high, Q_1 conducts current and pulls NOR low while OR is high. The output signals are the same level if V_{I2} or V_{I3} is high. If V_{I1}, V_{I2}, and V_{I3} are all high, the current splits between Q_1, Q_2, and Q_3 with the NOR output being pulled low. Note that the input signals must be single ended to use the wired OR circuit technique. Multiple transistors may be connected in parallel to form a multiple-input OR/NOR gate. One design concern is the capacitance added to the NOR node because of the additional

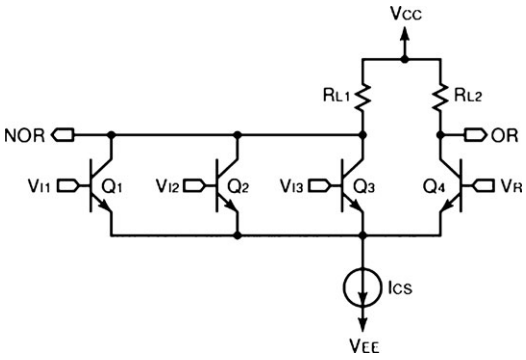

Figure 12. OR/NOR gate using parallel transistors.

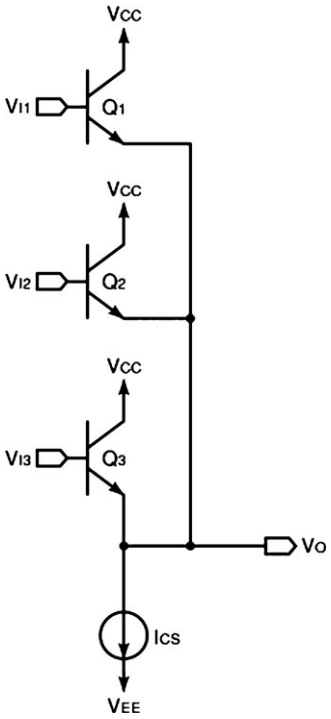

Figure 13. OR gate using emitter dotting.

transistor that delays the transitions of the NOR output.

The fourth technique is emitter dotting of emitter follower circuits. See Fig. 13. Three emitter followers are connected at the output node. The output signal V_O will be V_{BE} below the highest voltage of V_{I1}, V_{I2}, and V_{I3}. The function implemented is the OR function. The worst case condition for V_{OL} is when all inputs are high and the current is shared among all emitter follower transistors. The V_{BE} is minimum in this case, giving the highest V_{OL}. The ECL integrated circuit designer should check that adequate margin exists between the highest V_{OL} and the reference signal of the fan-out gate.

Latch and Flip-flop

Latches and flip-flops store data. An ECL latch is shown in Fig. 14(a). Stacked logic is used with the latch enable (LE) signal driving the lower emitter-coupled pair. At the upper level, the data (D) signal drives one pair while the second pair is driven by the outputs of the latch to complete the feedback loop in the latched state. Thus, if LE is high, the latch is transparent because the Data-pair is active. If LE is low, the latch is in the hold state because the feedback pair is active. Fig. 14(b) is the symbol for an ECL latch. An ECL flip-flop consists of two ECL latches as shown in Fig. 14(c). This ECL flip-flop is edge-triggered on the rising edge of the CLK signal that drives the LE of the slave latch and is inverted to drive the LE of the master latch. The Data input drives the master latch data while the output of the master latch drives the data input of the slave latch. The output of the slave latch is the output of the flip-flop.

Voltage Regulator

Reference voltages are key to the performance of ECL circuits. The reference voltage V_{CS} determines the dc current of the gates, while the reference voltages for the different logic levels determine the threshold voltages of the gates. The voltage regulator circuit is an analog circuit that generates the reference voltages using V_{CC} and V_{EE}. The design of voltage regulators is critical to the success of circuit performance. In particular, the tracking of the reference voltages with respect to power supply voltage, temperature, and process parameters ensures that the circuit meets all performance specifications under all conditions.

FUNCTIONAL VERIFICATION ALGORITHM

Because of continual improvements in the fabrication process for bipolar transistors, ECL circuits can be made in low-power versions with small transistors suitable for VLSI implementation. These circuits become quite large, requiring specialized computer-aided design tools. One such tool, ECLSIM (ECLSIMulator) (4), has been developed to simulate the functional behavior of large digital ECL circuits accurately and efficiently. In particular, ECLSIM uses expert knowledge of ECL circuit functionality to calculate node voltages and device currents from a transistor-level circuit description and input signal waveforms. The advantage of the approach is the simulation of a VLSI ECL circuit as a whole entity in a shorter simulation time than that available with a circuit simulation tool such as SPICE (5). Furthermore, the ECLSIM simulation results more accurately reflect the circuit behavior than logic level simulation results. The following sections describe the major components of ECLSIM.

Block Partitioning

The transistor-level circuit is first partitioned into blocks based on the current source tree. This can also be viewed as partitioning at the base input nodes to each gate. See Fig. 15(a) for an example of a partitioned circuit. Fig. 15(b) shows the blocks and the signal flow indicated by arrows. The dashed lines are power supply lines and the solid lines are signal lines. GND and each voltage source are placed into individual blocks. The ECL buffer is placed in block C and the emitter follower in block D. Blocks E, F, and G are the voltage regulator.

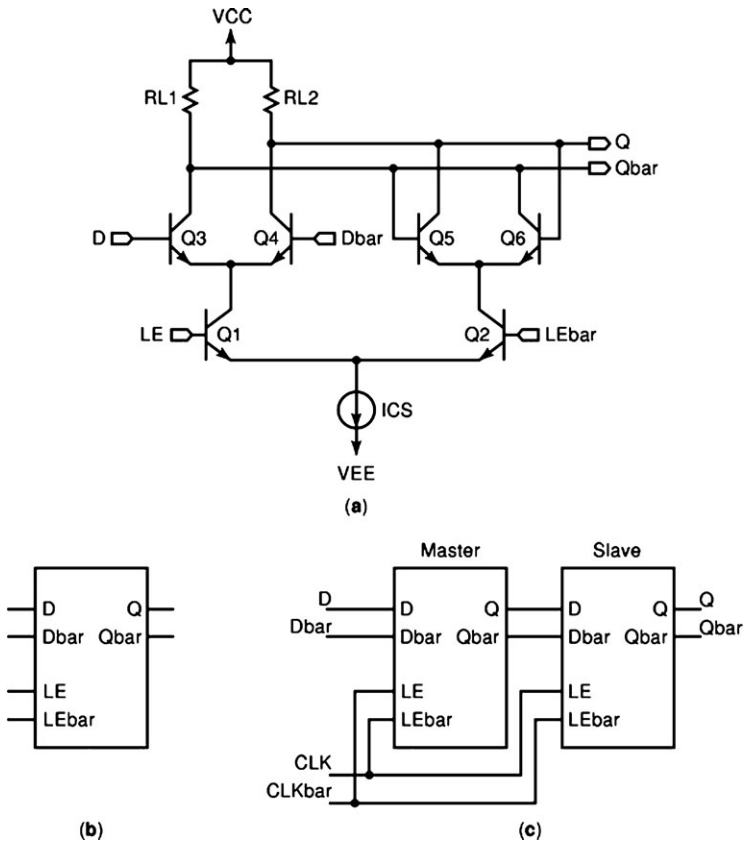

Figure 14. Latch and flip-flop. (a) Latch transistor level circuit using feedback in Q_5 and Q_6 to hold the state when data are latched. (b) Latch symbol. (c) Flip-flop, positive edge-triggered, uses two latches in series connection. The clock signal is inverted between the two latches.

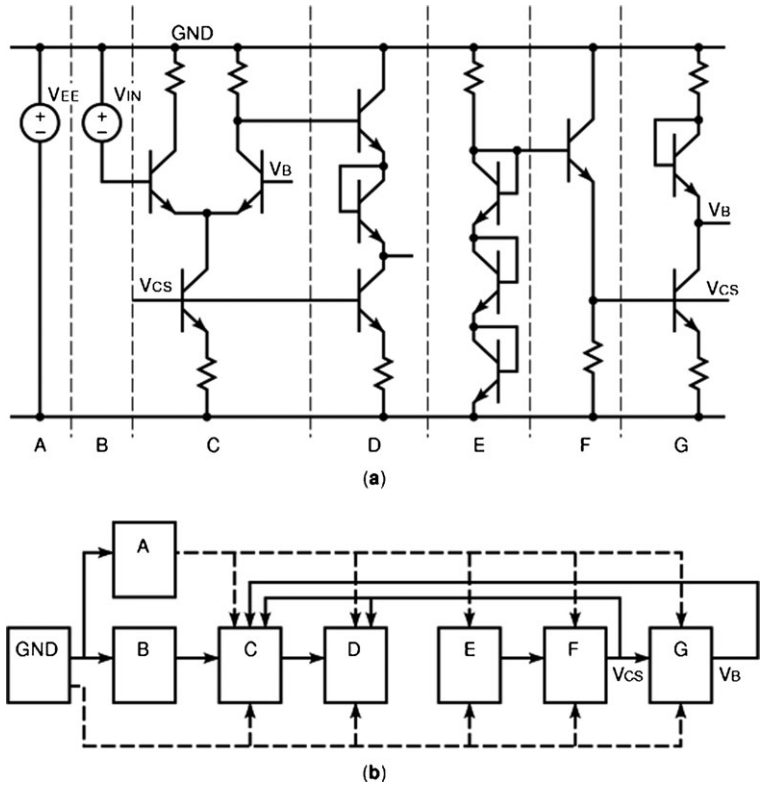

Figure 15. Block partitioning in functional verification algorithm. (a) Example circuit with buffer (C), emitter follower (D), and voltage regulator (E, F, and G). (b) Block representation with interconnection. Solid lines are signals and dashed lines are power supply connections. (Copyright by Elizabeth Jewel Brauer, 1994.)

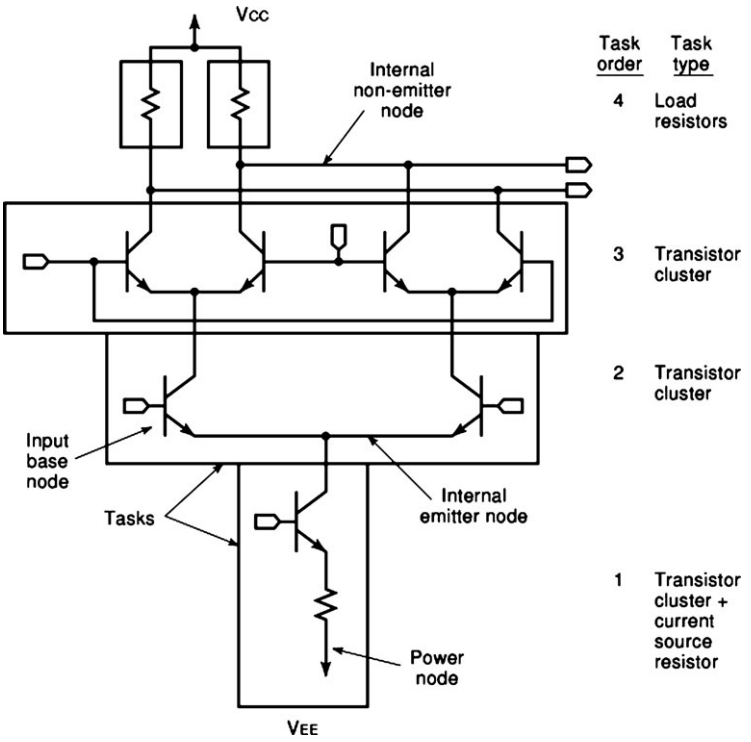

Figure 16. Task example. This is the XOR/XNOR gate from Fig. 11 divided into tasks. Nodes are identified as power nodes, input nodes, or internal nodes. The tasks are processed from 1 to 4. Either task at level 3 can be processed first and either task at level 4 can be processed first.

There are three types of nodes in a block. See the XOR/XNOR circuit in Fig. 16. One type of node is the input nodes that are the base terminal nodes. The second is the power nodes determined by the independent voltage sources not driving input nodes. The third node type is the block internal nodes, the nodes that are not input nodes or power nodes. The internal nodes are further identified as emitter nodes or nonemitter nodes, based on the connection to one or more emitter terminals. The internal node voltages and device currents are determined by the functional verification algorithm. The blocks are ordered for processing in an event-driven simulation. That is, the blocks attached to primary inputs are processed first, followed by the fan-out blocks, then the next fan-out blocks and so on, until the blocks generating the primary outputs are processed last. In this way, the simulation algorithm follows events and their effects throughout the circuit in a computationally efficient manner. Only the active blocks consume any computational resources, leading to efficient simulation. The block ordering is a natural result of the signal ordering, as shown by example in Fig. 15(b). The GND block is processed first, followed by the voltage source blocks, *A* and *B*. The voltage regulator blocks, identified during the partitioning phase [6], are simulated next using circuit simulation techniques to calculate the reference voltages accurately. The last blocks are simulated in the order of signal flow from the primary inputs. In this example, block *C* is simulated, then block *D*. For functional verification simulation, each block is divided into tasks that can be processed to calculate the unknown voltages and currents. The first type of task is a transistor cluster, based on the emitter node of emitter-coupled transistors. All transistors sharing a common emitter node are grouped into a cluster. The emitter current and base voltages are known. Thus, the collector currents can be calculated. A second task, the current source resistor, is identified as a resistor between an internal emitter node and a power node. The current is calculated from the emitter node voltages and the resistance value. The transistor cluster attached to the resistor may consist of a single transistor or multiple transistors. The third task, the load resistor, is identified as a resistor between a non-emitter node and a power node. The current is known and the power node voltage is known, leading to calculation of the non-emitter node voltage. Any remaining devices are identified as a complex load to account for any nonstandard circuit configurations. All devices are identified as belonging to one of the following tasks and the tasks are processed in the following order within each block:

1. Current source resistor + attached transistor cluster
2. Transistor clusters in order of known emitter current (up the current source tree)
3. Load resistor
4. Complex load

See Fig. 16. The transistor cluster, current source resistor, and load resistor are processed as described below. The complex load is simulated using standard circuit simulation techniques, which will simulate any circuit configuration.

Bipolar Transistor Clusters

The functional verification algorithm for ECL circuits accurately calculates internal node voltages and device currents. The basis of the algorithm is calculation of the transistor current and emitter node voltage given the base voltages and the total emitter current. Assuming that the *npn*

transistors are in the forward active region

$$I_{ci} = \frac{I_E}{\frac{1}{I_{Si}} \sum_{j=1}^{n} \frac{I_{Sj}}{\alpha_{Fj}} \exp[(V_{bj} - V_{bi})/V_T]}$$

where I_E is the known emitter current, I_S is the saturation current, α is the common-base current gain, V_b is the known base voltage, and $V_T = kT/q$ is the thermal voltage. Thus, from the base voltages and the emitter current, the collector currents can be calculated.

Resistors

The resistors are processed using Ohm's Law, $V_1 - V_2 = IR$ where V_1 and V_2 are the resistor terminal voltages, I is the current, and R is the resistance. If 3 of the 4 variables are known, the remaining variable is calculated. For a current source resistor and connected transistor cluster, iteration is required for an accurate calculation of current.

Performance

The functional verification algorithm, ECLSIM, accurately and efficiently simulates the functional behavior of ECL digital circuits. The static voltage levels are within 15 mV of the levels calculated by SPICE. The ECLSIM computational expense is 200 to 1000 times faster than SPICE2G6 or SPICE3E2.

FUTURE DIRECTIONS

Emitter-coupled logic will continue to be important for applications where speed is a primary design goal, for example, test, telecommunications, and high-performance computing. Compound semiconductors, such as InP and SiGe, are increasingly used. However, the high power requirement of ECL is a limitation in some applications, such as, portable wireless applications. Some work will continue in developing new ECL integrated circuits, although this will not be a major effort. More important, the ECL interface will continue to be an industry standard for high-speed signals.

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