GALLIUM ARSENIDE FIELD EFFECT TRANSISTOR LOGIC CIRCUITS

Gallium arsenide (GaAs) is a compound semiconductor that can be used to fabricate field effect transistors (FET). Like silicon (Si) FETs, GaAs FETs can be used to make both analog and digital integrated circuits (IC). GaAs FETs have been in use in analog microwave circuits since about the late 1960s, where they provide bandwidth, noise, and power consumption advantages over available silicon devices for certain applications (1). GaAs FETs have been in use in digital integrated circuits since about 1974 (1). Initially, their use was limited to extremely high-speed applications where logic density was not a major issue and where power consumption was less of a concern than operating speed.

Today, the use of digital GaAs FET ICs is very common in high-performance digital systems, especially if power consumption is an important issue. The speed of GaAs FET logic has surpassed the speed of Si complementary metal oxide semiconductor (CMOS) logic, Si bipolar complementary metal oxide semiconductor (BiCMOS) logic, and emitter coupled logic (ECL) implemented with silicon bipolar junction transistors (BJT), for ICs of comparable functionality and power consumption. In fact, one of the biggest advantages of GaAs FET ICs is that for a given logic function, they have a power consumption-gate delay product that is approximately one-third to one-fifth that of comparable silicon circuits (1,2). GaAs FET logic has also made tremendous advancements in integration levels and cost reduction. Commercial digital ICs with over 500,000 transistors are common and ICs with over 1 million transistors are being produced with profitable yields (3,4). The cost of such ICs is often less than that of comparable Si BiCMOS or ECL ICs.

Another advantage that GaAs FET logic has over silicon is its inherent tolerance to radiation. Research has confirmed that GaAs FET logic is very radiation hard in terms of its total dose and dose-rate characteristics (5,6). Thus, GaAs FET logic is useful in space and military systems that require radiation tolerant, high-speed logic and reduced power consumption. The major drawback of GaAs FET logic is that it is susceptible to single-event upsets, sometimes known as SEUs or soft errors (7,8). Circuit and system techniques exist to detect and correct such errors (9). However, these techniques pay a penality with respect to performance, power consumption, size, weight, system-level complexity, and the like. But, recent research has significantly reduced the sensitivity of GaAs FET logic to radiation-induced soft errors, thus reducing or eliminating the need for circuit and/or system level SEU reduction techniques (10). Further research should yield GaAs FET logic that is immune to soft errors for all practical space and military applications (11).

GALLIUM ARSENIDE METAL SEMICONDUCTOR FIELD EFFECT TRANSISTORS

One of the more common types of gallium arsenide FETs used in digital integrated circuits is the metal semiconductor field effect transistor (MESFET) (12). It is significantly different from the more familiar Si metal oxide semiconductor FET (MOSFET) in several ways. For example, the mobility of electrons in GaAs is approximately three to five times greater than in silicon (1). This is what gives GaAs logic its power consumption-gate delay product advantage over Si logic. Another significant difference between GaAs MESFETs and Si MOSFETs is the lack of a stable oxide of gallium arsenide. This makes it very difficult to fabricate an insulator between the transistor channel and the gate. This can be seen in Fig. 1. The gate of a GaAs MESFET actually contacts the semiconductor. The lack of an insulated gate in the MESFET has a tremendous influence on the use of the device for logic circuits because the gate and channel form a Schottky-barrier diode at their junction. Thus, if the gate-to-channel voltage exceeds the turn-on voltage of the diode, which is approximately 0.65 V, gate current will conduct. When the gate is forced into conduction, the input resistance and the transconductance of the device in common-source circuits, such as directly coupled FET logic (DCFL) gates and common-source amplifiers, is significantly decreased. This limits the gain of the circuit. For logic gates, the end result is a decrease in logic swing, noise

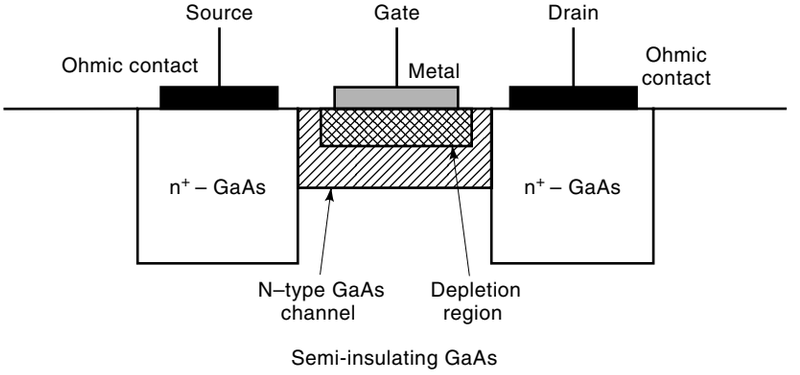

Figure 1. Profile of a GaAs *n*-channel MESFET.

margins, fan-out, and speed. It can also increase the difficulty of designing and implementing dynamic logic circuits that require the storage of charge on certain nodes in the circuit. If the charge leaks off the node, then the stored logic value will change. It should be noted that research is being conducted to develop a GaAs MESFET with an insulated gate, or at least a gate with a higher resistivity to the channel.

Another significant difference between GaAs MESFETs and Si MOSFETs is the lack of a *p*-channel GaAs MESFET device. Although *p*-channel GaAs MESFETs are theoretically possible, the mobility of holes in GaAs is approximately one-fifth that of electrons (1). Therefore, the use of *p*-channel MESFETs would eliminate the speed advantage of the GaAs N-channel MESFETs. Also, an appropriate material for forming a Schottky barrier on *p*-type GaAs has not been demonstrated. The lack of a *p*-type MESFET has a tremendous influence on GaAs logic circits because it prevents the use of the familiar complementary static logic circuits that are so popular for use with Si CMOS fabrication processes (13). However, both enhancement-mode and depletion-mode *n*-channel MESFETs are practical. Thus, static GaAs MESFET logic circuits often use circuit topologies that resemble the older, *n*MOS-style logic circuits that were popular before Si CMOS processing technology was perfected (14).

Figures 2 and 3 show typical current-voltage (I–V) curves for an *n*-channel enhancement-mode GaAs MESFET. In Fig. 2, I_D is plotted as a function of V_{GS} with V_{DS} fixed at +2.0 V, a typical value of V_{DD} for GaAs MESFET logic circuits. The threshold voltage V_T for this transistor is specified as 0.23 V. Two things are immediately apparent. First, when V_{GS} is be-

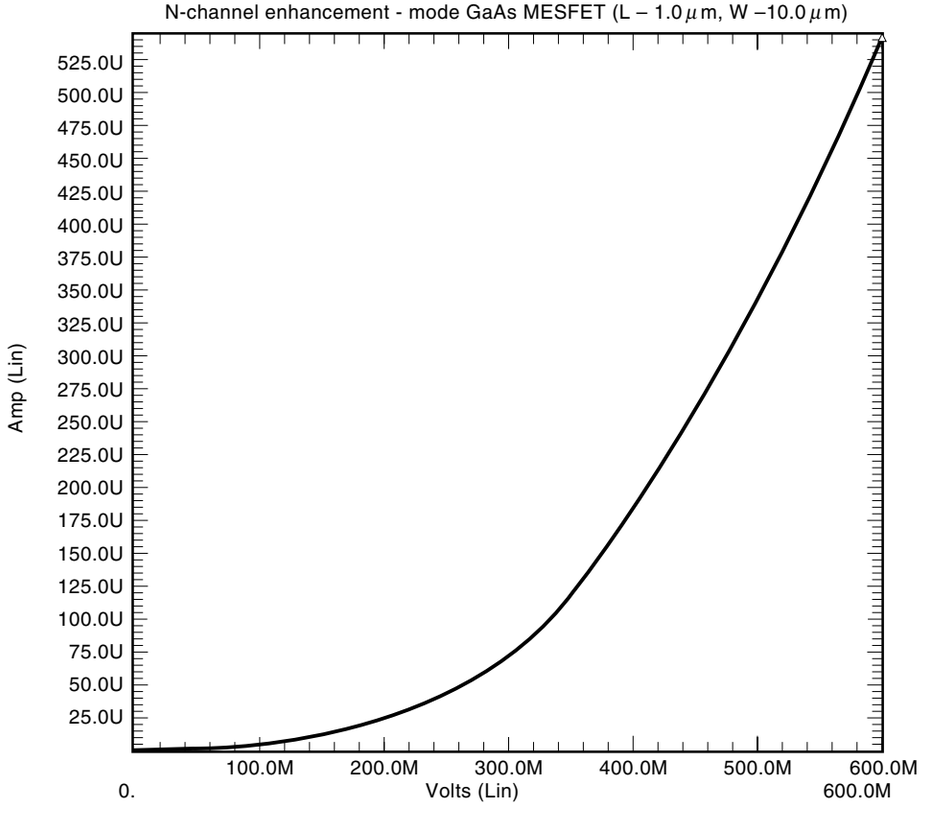

Figure 2. I_{DS} versus V_{GS} for $V_{DS} = +2.0$ V.

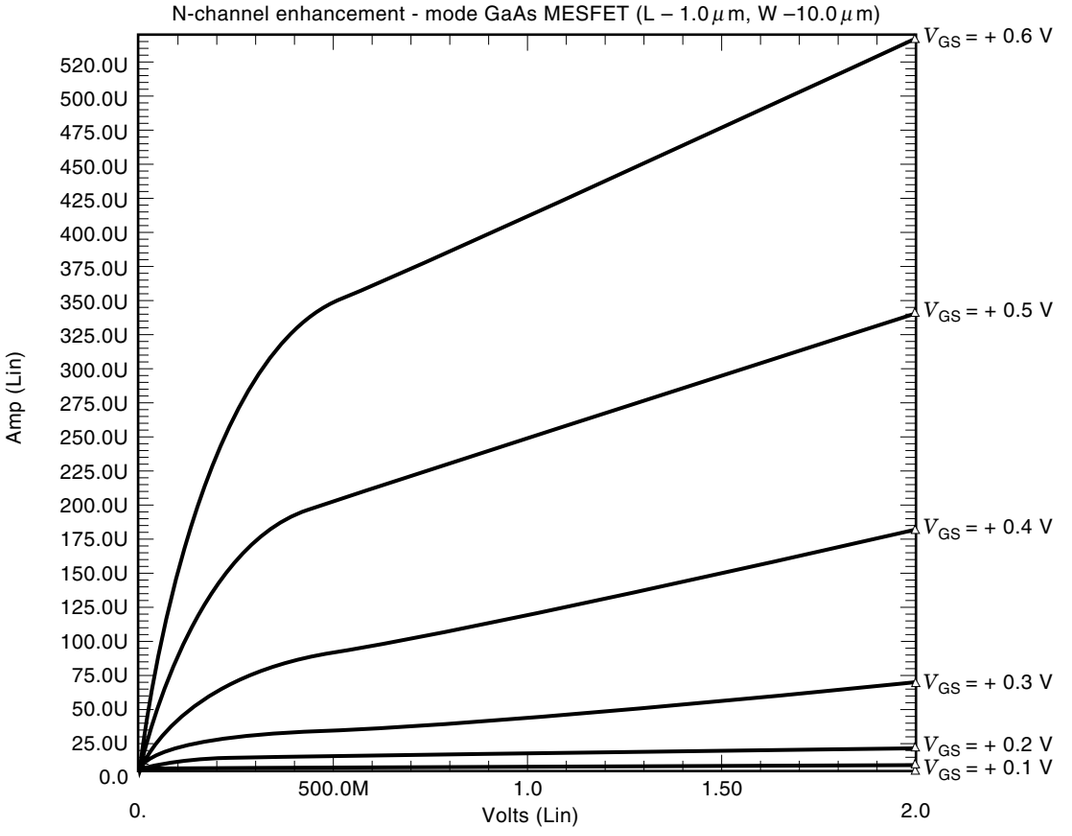

Figure 3. I_{DS} versus V_{DS} for different values of V_{GS}.

low V_T, a leakage current continues to flow from drain to source. This is known as subthreshold leakage current. Although Si FETs also have subthreshold leakage currents, they are not as pronounced as in GaAs MESFETs. In logic circuits, the leakage current causes reduced noise margins and fan out and can also negatively influence the speed of the logic gate, especially for logic circuits with a large number of inputs. However, for some circuits, the subthreshold leakage current is dominated by the gate current of the inputs to the next logic stage.

Another characteristic of the GaAs MESFET that can be observed in Fig. 2 is the transconductance of the device. Compared to a Si MOSFET of similar size, the transconductance is lower. This can also have a negative influence on circuit behavior, resulting in lower circuit gain. For logic circuits, the end result is a decrease in the logic swing, the noise margins, and also the speed. In Fig. 3, I_{DS} is plotted as a function of V_{DS} for various values of V_{GS}. In this figure, it can be seen that the first-order I–V characteristics of the MESFET are qualitatively similar to the first-order I–V characteristics of a Si MOSFET. The main differences between the two are in the second-order effects (15).

The I–V characteristics of depletion-mode GaAs MESFETs are not significantly different from those of enhancement-mode MESFETs. The main difference is that the curves are shifted because of the negative threshold voltage. Figure 4 is a plot of I_{DS} as a function of V_{GS} for $V_{DS} = +2.0$ V, for a depletion-mode, n-channel MESFET. The threshold voltage for this device is specified as -0.825 V. Figure 5 is a plot of I_{DS} as a function of V_{DS} for various different values of V_{GS}. From Figures 3 and 5 it can been seen that GaAs MESFETs have three regions of operation (15), as all Si and GaAs field effect transistors do. When V_{GS} is below V_T, the device is in the cut-off region. No drain-to-source current flows when the device is cut off, except for subthreshold leakage current. When V_{GS} is above V_T, the device can be either in the ohmic region, sometimes called the linear or triode region, or in the saturation region. As with Si n-channel FETs, GaAs n-channel MESFETs operate in the ohmic region when $V_{GS} \geq V_T$ and $V_{DS} < (V_{GS} - V_T)$. The transistors operate in the saturation region when $V_{GS} \geq V_T$ and $V_{DS} \geq (V_{GS} - V_T)$.

For circuit analysis, it is necessary to have a model for an active device such as a GaAs MESFET. For first-order approximations, the circuit model shown in Fig. 6 is usually sufficient. This model is similar to the SPICE Si JFET model (16). The associated equations for calculating the I–V relationships are based on the Shichman-Hodges model (17). Equation (1) can be

$$i_D = \beta[2(v_{GS} - v_T)v_{DS} - v_{DS}^2](1 + \lambda v_{DS}) \quad (1)$$

$$i_D = \beta(v_{GS} - v_T)^2(1 + \lambda v_{DS}) \quad (2)$$

used to calculate I_{DS} in the ohmic region and Eq. (2) can be used to calculate I_{DS} in the saturation region, where β is the transconductance and λ is the channel-length modulation parameter (15). It should be noted that significantly more complex and more accurate models and equations have been

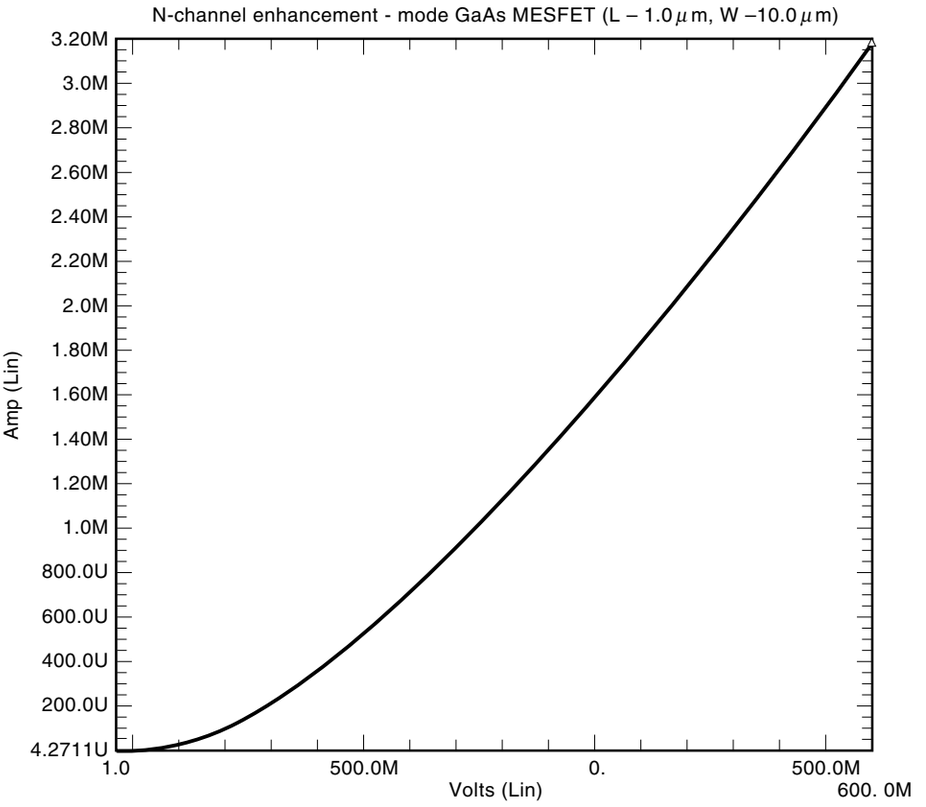

Figure 4. I_{DS} versus V_{GS} for $V_{DS} = +2.0$ V.

developed for describing and simulating the operation of GaAs MESFETs (18,19). For example, in submicron GaAs MESFETs, the velocity saturation effect has a major influence on I_{DS}.

GaAs DIRECTLY COUPLED FET LOGIC CIRCUITS

The most common form of static logic circuit for use with GaAs MESFETs is directly coupled FET logic (DCFL). A DCFL inverter is shown in Fig. 7 (20). It consists of a single enhancement-mode FET (EFET) and a single depletion-mode FET (DFET). The drain of the EFET is connected to the output node of the circuit, the gate is connected to the input node of the circuit, and the source is connected to ground. The EFET is sometimes called the pull-down transistor because its function is to pull the output-node voltage down to near ground potential when V_{GS} is greater than T. The drain of the DFET is connected to V_{DD} and the gate and source of the DFET are connected to the output node of the circuit. This configuration ensures that V_{GS} is always greater than V_T for the DFET because V_{GS} is always 0 V and V_T is less than 0 V. Thus, the DFET either operates in the ohmic region or the saturation region, depending on the value of V_{DS}, but it is never cut off. A DFET wired in this configuration is sometimes called an active load or an active pull-up because it serves to pull the output-node voltage high. For ease in understanding its operation, it can be thought of as a resistor although it does not have a constant value of V/I. The apparent DFET channel resistance is given by V_{DS}/I_{DS}, where $V_{DS} = V_{DD} - V_{OUT}$ and I_{DS} is determined from either Eq. (1) or Eq. (2), depending on the region of operation.

For the circuit in Fig. 7, when the input voltage is high, the EFET will be on and will pull the output voltage low against the current sourced by the DFET. The output low voltage of most DCFL logic gates approaches the value of V_{SS}. The exact voltage is highly dependent on the transconductance ratio of the EFET to the DFET. Thus, DCFL, like Si negative channel MOS (NMOS) logic, is known as a ratioed logic family. When the input voltage is low, the EFET will be cut off and the output voltage will be pulled high by the DFET. Thus, no current flows in the circuit when the input is low, except for leakage current. The output logic high voltage would approach the value of V_{DD} if nothing were connected to the output node. However, in practical applications, another DCFL logic gate is often connected to the output node. The input to this logic gate would most likely be the gate of an EFET which, as discussed previously, forms a Schottky-barrier diode with the channel. Therefore, the input of the logic gate connected to the output of the gate shown in Fig. 7 would clamp the output high voltage to a value between 0.6 and 0.7 V above the value of V_{SS}.

Figure 8 shows the dc transfer curve of a typical GaAs DCFL inverter. This inverter has a DFET pull-up with a 1.6 μm long by 2.0 μm wide gate. The EFET pull-down has a 0.8 μm long by 16.0 μm wide gate. These sizes are typical for modern fabrication processes. The output is loaded with two other inverters. For the plot in Fig. 8, V_{DD} is at ground potential (0.0 V) and V_{SS} is at -2.0 V. These are typical values for GaAs DCFL logic and provide compatibility with existing Si ECL ICs with respect to power supply voltages. Also, conversion of the on-chip DCFL logic swing to off-chip ECL logic levels is easier if the DCFL is operated between ground and

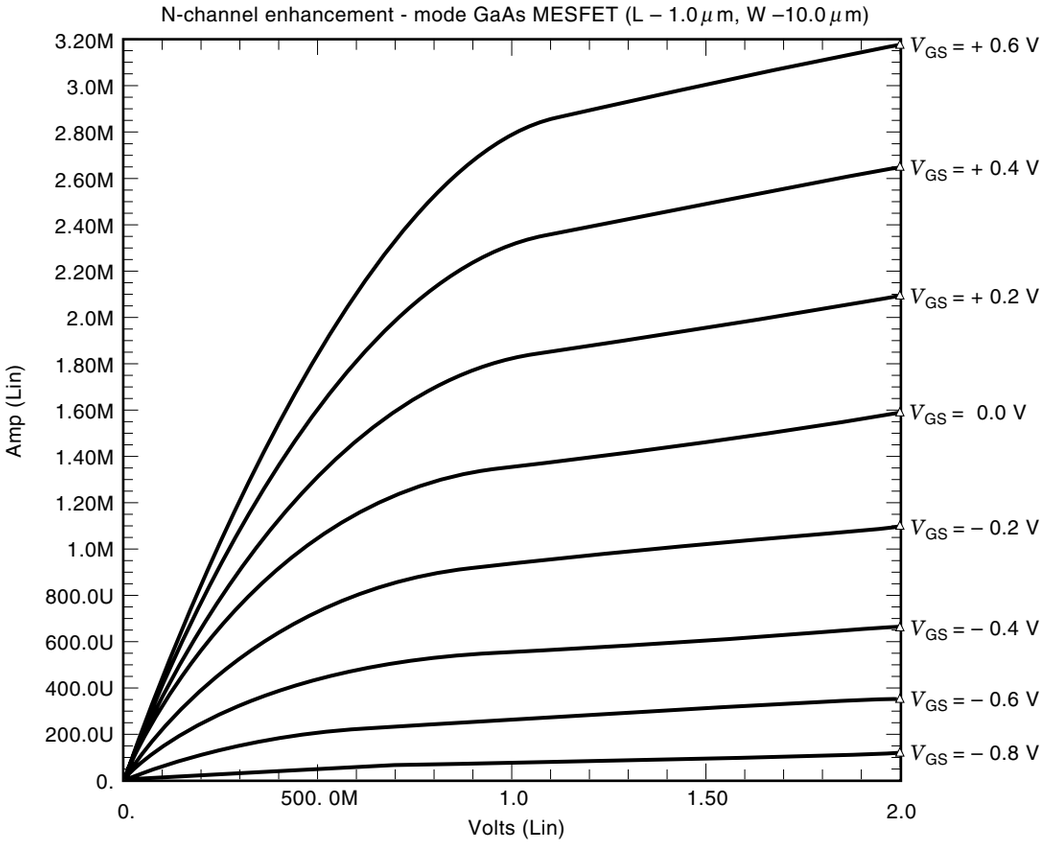

Figure 5. I_{DS} versus V_{DS} for different values of V_{GS}.

−2.0 V. This is an advantage if the GaAs DCFL ICs must interface to Si ECL ICs in a logic system.

Figure 8 can be used to explain how noise margins can be determined for GaAs DCFL and has been marked to show the minimum and maximum input high, input low, output high, and output low voltages. V_{OH}(max) is the highest possible output high voltage and V_{OL}(min) is the minimum possible output low voltage. V_{OH}(min) and V_{OL}(max) are the output voltages where the upper and lower parts of the dc transfer curve reach a slope of −1. V_{IL}(min) is the lowest possible logic low input voltage, and V_{IH}(max) is the highest possbile logic high input voltage. V_{IL}(max) and V_{IH}(min) are the input voltages where the upper and lower parts of the dc transfer curve reach a slope of −1. After these voltages are known, they can be used to calculate the noise margins according to Eqs. (3) and (4) (21). The noise margins calculated in Eqs. (3) and (4) are typical

$$\mathrm{NM_H} = |V_{\mathrm{OH}}(\min) - V_{\mathrm{IH}}(\min)| = |-1.335 - -1.54| = 0.205 \tag{3}$$

$$\mathrm{NM_L} = |V_{\mathrm{IL}}(\max) - V_{\mathrm{OL}}(\max)| = |-1.68 - -1.89| = 0.210 \tag{4}$$

values for this logic family. The method shown here for calculating noise margins is used frequently, but other methods do exist (22).

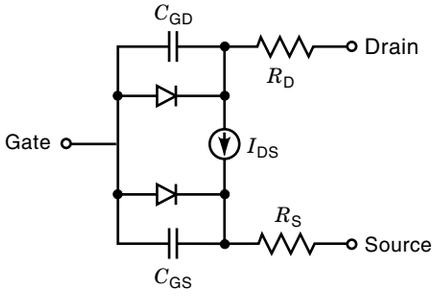

Figure 6. First-order circuit model for GaAs MESFET.

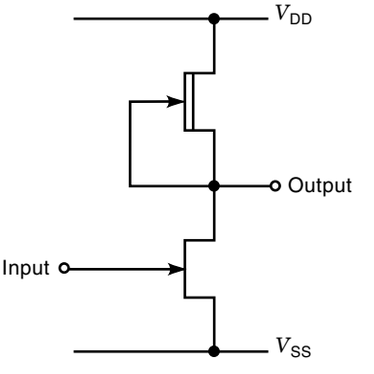

Figure 7. GaAs DCFL inverter.

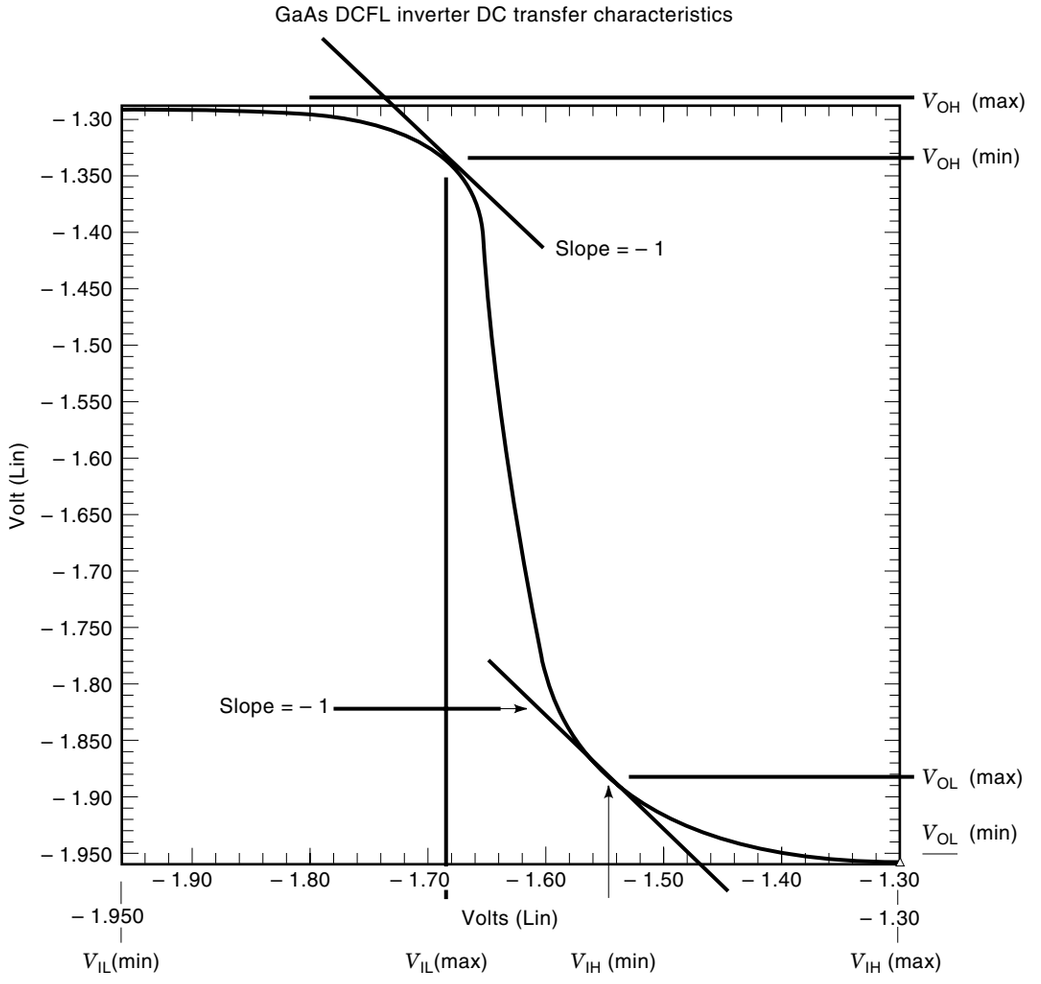

Figure 8. DC transfer curve of a GaAs DCFL inverter with two loads.

One of the major advantages of using GaAs logic over silicon logic is it's speed. Figure 9 shows a transient analysis of the logic gate shown in Fig. 7. Output loading on the gate is two inverters. Figure 9 can be used to explain how the output rise and fall times, T_R and T_F, are determined for GaAs logic (23). Initially, the output voltage swing is determined. Then, a horizontal line is drawn across the plot at the Y coordinate that is 10% of the voltage swing below the output high voltage. Another horizontal line is drawn across the plot at the y coordinate which is 10% of the voltage swing above the output low voltage. T_R is then defined as the time difference between when the rising output voltage crosses the 10% line and the 90% line. Similarly, T_F is defined as the time difference between when the falling output crosses the 90% line and the 10% line. Using 10–90% of the output voltage swing to determine T_R and T_F is somewhat arbitrary. However, it is the generally accepted practice. Sometimes, the 20–80% output voltage swing is used instead (22). This creates values for T_R and T_F that are noticeably shorter for the exact same circuit. Therefore, these values are difficult to compare against T_R and T_F values calculated using the 10–90% output voltage swing method. However, the 20–80% method is more useful for logic circuits that take a relatively long time to change from the steady state condition to the transition region. The purpose of determining T_R and T_F is to find out how fast the logic gate can slew the output node of the circuit. Thus, for circuits with a slow change from the steady state to the transition region, using the 20–80% method will give a more accurate indication of the ability of the circuit to slew a capacitive load connected to the output of the logic gate. Using the 10–90% method for the plot in Fig. 9, T_R is 150 ps and T_F is 50 ps. These are typical values for loaded DCFL circuits. It is interesting to note that T_F is significantly shorter than T_R. This is typical for GaAs DCFL circuits and is the result of the fact that the transconductance of the enhancement-mode pull-down FET is much greater than the transconductance of the depletion-mode pull-up FET. However, this high EFET-to-DFET transconductance ratio is necessary to maintain good dc noise margins.

Figure 9 can also be used to demonstrate how the low-to-high and high-to-low propagation delays, T_{PLH} and T_{PHL}, are determined for GaAs logic (23). Initially, a horizontal line is drawn at the midpoint of the output voltage swing. T_{PLH} is defined as the time difference between when the input voltage crosses the 50% point and when the rising output voltage crosses the 50% point. Similarly, T_{PHL} is defined as the time difference between when the input voltage crosses the 50% point and when the falling output voltage crosses the 50%

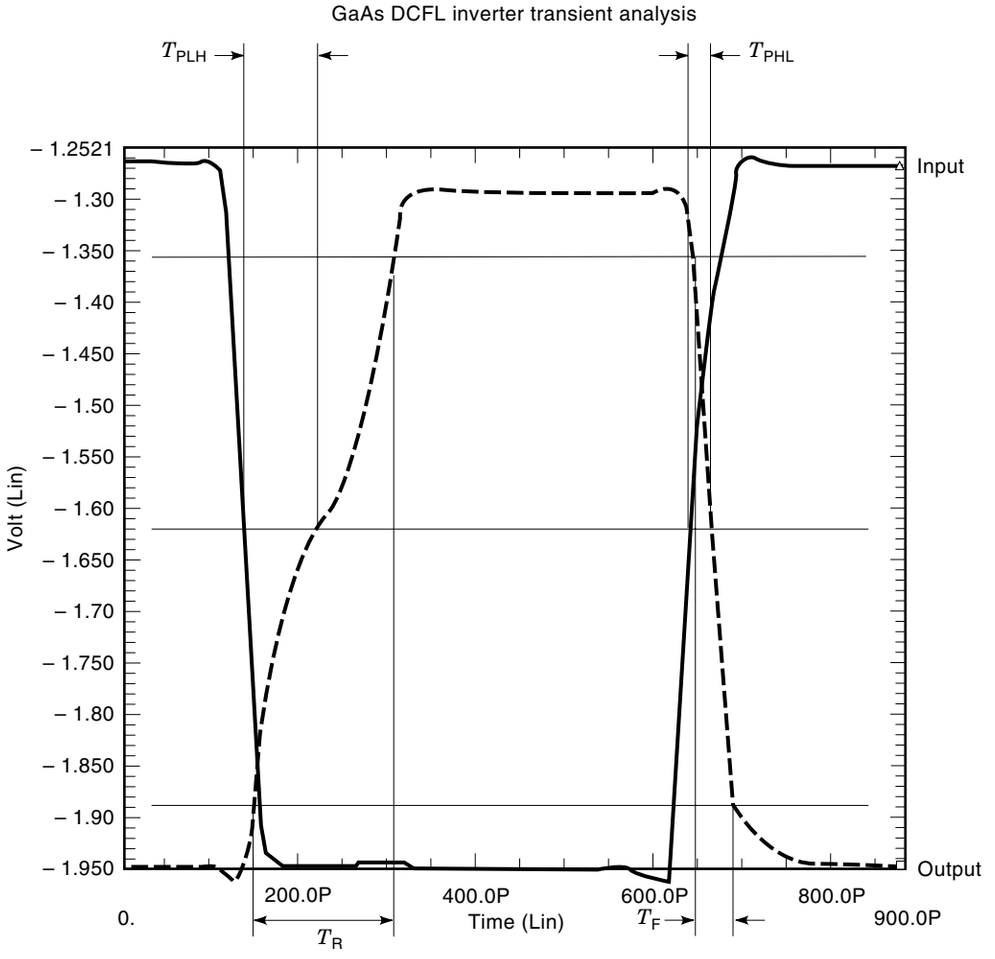

Figure 9. GaAs DCFL inverter transient analysis.

point. The 50% point is normally used for such calculations. For the plot in Fig. 9, T_{PLH} is 80 ps and T_{PHL} is 30 ps. These are also typical values. The significant difference between T_{PLH} and T_{PHL} is caused by the large difference between T_R and T_F.

Some of the more advanced Si ECL circuits are capable of producing the low values for T_R, T_F, T_{PLH}, and T_{PHL} described here. However, they do so at the expense of large amounts of power. The circuit discussed here consumes negligible current from the power supply when the output voltage is high and only 300 μA when the output is low. Assuming a 50% duty cycle, the average current consumption is 150 μA and the average power consumption is 300 μW, considerably less power than Si ECL requires at these speeds. It should be noted that DCFL can be fairly sensitive to output loading. To maintain high speed with high fan-out or when driving a high-capacitance load, a source-follower circuit can be appended to the output of the logic gate (20). Alternatively, a super-buffer logic circuit can also be used (24). These techniques have increased drive capability and maintain high switching speed but will increase the power consumption.

GaAs DCFL circuits other than inverters can be created by starting with the basic inverter design and adding additional EFET pull-down transistors to create NOR gates, NAND gates, and AND-OR-INVERT gates (20). A two-input NOR gate is shown in Fig. 10. Two EFET pull-downs are connected in parallel. If either of these transistors is turned on, then the output voltage of the gate will be pulled low. Both FETs must be turned off to allow the output voltage to be pulled high by

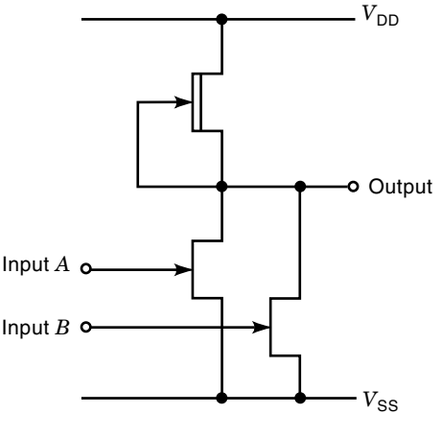

Figure 10. GaAs DCFL two-input NOR gate.

the DFET pull-up transistor, thus generating the Boolean NOR function. Three, four, and more input NOR gates can also be created. The practical limit on the number of inputs is determined by a combination of factors, including noise margins and speed. The more inputs that are added to the NOR gate, the more the noise margins become skewed because the total transconductance of all the EFETs becomes so much greater than the transconductance of the single DFET pull-up. Also, the addition of more EFETs to the output node increases the drain-to-source subthreshold leakage current, which will have an adverse effect on both the noise margins and the speed. The total parasitic capacitance on the output node also increases when the number of EFETs is increased, thus slowing down the output rise and fall times.

A two-input NAND gate is shown in Fig. 11. Two EFET pull-downs are connected in series. Both of these transistors must be turned on for the output voltage of the gate to be pulled low. If either FET is turned off, then the output voltage will be pulled high by the DFET pull-up transistor, thus generating the Boolean NAND function. Three, four, and more input NAND gates can also be created. The practical limit on the number of inputs is determined by both the noise margins and the speed. The more inputs that are added to the NAND gate, the more the noise margins become skewed because the total transconductance of all the series EFETs becomes too low to obtain the ratio of EFET transconductance to DFET transconductance required for good noise margins. Furthermore, the decrease in the total transconductance of all the series EFETs results in a decrease in the output fall time. In fact, the decrease in the total series EFET transconductance resulting from just two series EFETs is enough to make the two-input NAND gate slower than the two-input NOR gate. For this reason, NOR gates are generally preferred over NAND gates and product-of-sum logic design dominates in logic systems implemented with GaAs DCFL.

A four-input AND-OR-INVERT gate is shown in Fig. 12 that generates the logic function $f(A, B, C, D) = \overline{AB + CD}$. EFETs can be combined in a number of different circuit topologies to create almost any desired logic function. As with the NOR gates and NAND gates, the practical number of inputs is determined by a combination of the noise margins and the speed.

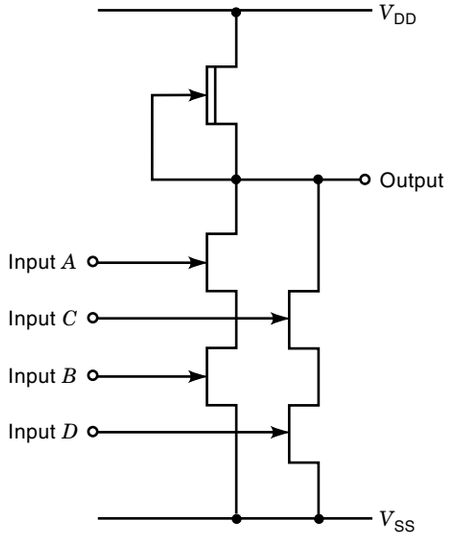

Figure 12. GaAs DCFL four-input AND-OR-INVERT gate.

ADDITIONAL LOGIC CIRCUITS FOR GaAs MESFET FABRICATION PROCESSES

In addition to their use in directly coupled FET logic circuits, GaAs EFETs can also be used as pass transistors to construct pass-gate logic, sometimes known as steering logic (20). A 2-to-1 multiplexer constructed from pass-gate logic is shown in Fig. 13. This circuit requires only two enhancement-mode transistors. The equivalent circuit constructed using DCFL would require 3 two-input NOR gates, a total of nine transistors. An inverter is needed for both designs to generate the complement of the select signal. The circuit shown in Fig. 13 is not a restoring logic circuit because it has no gain and the output voltage swing is slightly less than the input voltage swing. Therefore, it is not advisable to cascade multiple stages of pass-gate logic. Inputs and outputs should be connected to a form of restoring logic such as DCFL, which they can be directly connected to without any buffers or level-shifting circuits.

Despite the high speed of GaAs DCFL, some applications require even shorter logic propagation delays and/or shorter gate output rise and fall times. In such applications, GaAs

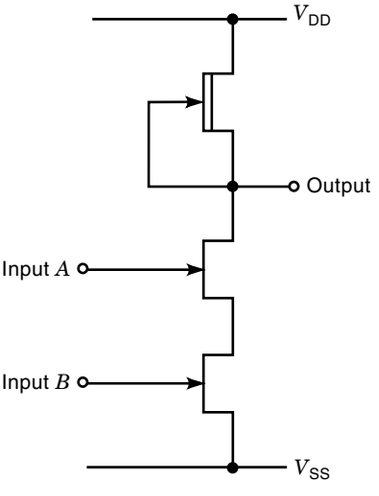

Figure 11. GaAs DCFL two-input NAND gate.

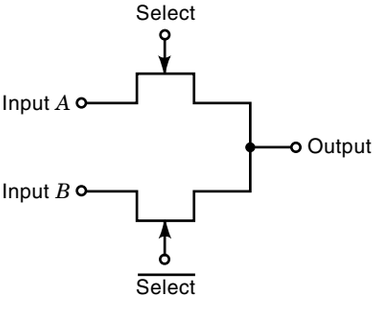

Figure 13. GaAs pass-gate 2-to-1 multiplexer.

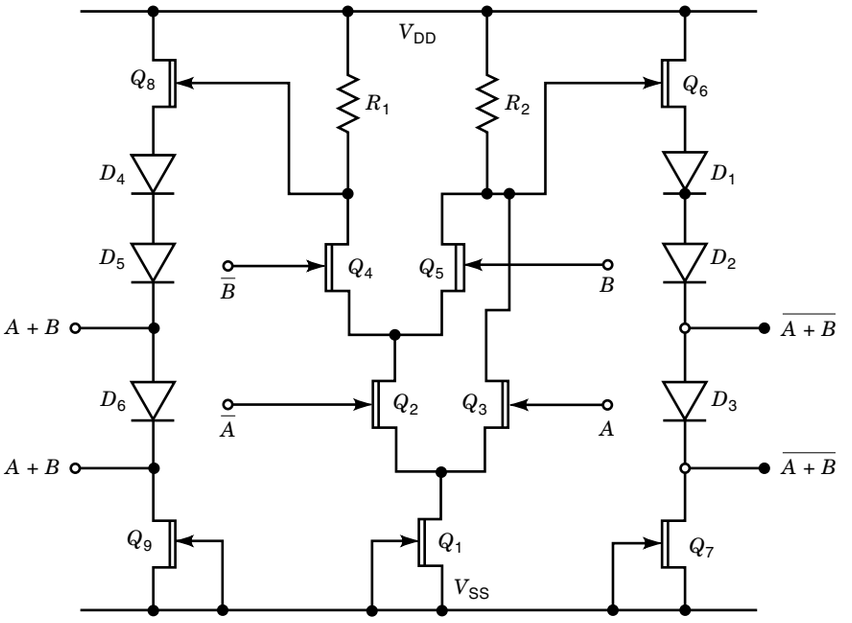

Figure 14. GaAs SCFL two-input OR/NOR gate.

source-coupled FET Logic (SCFL) can be used (25). The logic propagation delay of SCFL gates fabricated with commercial MESFET processes can be as low as 50 ps or less. The disadvantage of using SCFL is that it requires more transistors per logic function and has a higher power consumption-gate delay product than does DCFL. However, despite the higher power consumption, power and ground rail noise is less than with DCFL because SCFL generates logic functions using the principle of current steering. The total current consumed is always constant, regardless of the states of the inputs to the logic gate.

Figure 14 shows a SCFL two-input OR/NOR gate. The gate is constructed with all depletion-mode FETs because they have higher transconductance than EFETs of the same size and thus yield a higher-speed circuit. The part of the circuit that actually generates the logic function uses two differential pairs, Q_2 through Q_5. A SCFL inverter would require a single differential pair and a three-input OR/NOR gate would require three differential pairs. The A and $\overline{A}$ inputs are applied to differential pair Q_2/Q_3, and the B and $\overline{B}$ inputs are applied to differential pair Q_4/Q_5. The complements of all input signals are required to maintain dc balance, good noise margins, and high-speed operation. Thus, the use of SCFL in an integrated circuit can double the required interconnect area, compared to the use of DCFL. However, an advantage of using SCFL is that both the logic function and the complement of the function are generated at the same time. This ability is wasted if the complement is not required. However, if it is required, transistor counts are reduced.

In Fig. 14, Q_1 acts as a current source to bias the differential pairs. Although the internal impedance of this simple current-source is not usually high enough for analog differential amplifiers, it is usually sufficient for logic circuits and it uses fewer transistors than a current mirror. Q_7 and Q_9 are two more current sources that are used to bias the output source follower/level shifter stages. The source follower/level shifter output stages are composed of Q_6, D_1, D_2, D_3, and Q_7 for the NOR output and Q_8, D_4, D_5, D_6, and Q_9 for the OR output. These circuits have a positive gain that is slightly less than unity and they are required for two reasons. First, they reduce the loading on the differential pairs and improve the output drive capability, thus maintaining speed. Second, they are required for voltage shifting. The output voltage swing of the differential pairs is more positive than the input voltage swing. The source follower/voltage shifters shift down the output voltage swing to the point where it is compatible with the input voltage swing of the next stage. The number of diodes required in the voltage shifter varies depending on the bias points of the circuit and on which input is being driven in the next logic stage. For example, if inputs A and $\overline{A}$ of the next stage are being driven, then the outputs at the drains of Q_7 and Q_9 should be used. If inputs B and $\overline{B}$ are being driven, then the D_2/D_3 and D_5/D_6 outputs should be used.

Referring to Fig. 14, if both the A and B inputs are low, then the currents through Q_3 and Q_5 are reduced and the current through Q_2 and Q_4 increases. This decreases the voltage drop across R_2 and increases the voltage drop across R_1, which raises the voltage on the gate of Q_6 and lowers the voltage on the gate of Q_8. The voltages at the gates of Q_6 and Q_8 are shifted down the required amount by the previously described voltage shifting circuits. If input A is high and input B is low, then the current through Q_3 increases and the current through Q_2, Q_4, and Q_5 decreases. This increases the voltage drop across R_2 and decreases the voltage drop across R_1, which lowers the voltage at the gate of Q_6 and raises the voltage at the gate of Q_8. If input A is low and input B is high, then the currents through Q_3 and Q_4 decrease and the current through Q_2 and Q_5 increases. This increases the voltage drop across R_2 and decreases the voltage drop across R_1, which lowers the voltage at the gate of Q_6 and raises the voltage at the gate of Q_8. If inputs A and B are both high, then the current through Q_3 increases and the current through Q_2, Q_4, and Q_5 decreases. This increases the voltage drop across R_2 and decreases the voltage drop across R_1, which lowers the voltage at the gate of Q_6 and raises the voltage at the gate of Q_8. Thus the Boolean NOR function is implemented at the

gate of Q_6 and the Boolean OR function is implemented at the gate of Q_8.

The circuit in Fig. 14 can also be used to implement the AND/NAND function by applying DeMorgan's theorem (26). If the inputs to a NOR gate are inverted, the output of the NOR gate results in the AND operation. The use of SCFL requires that the complements of all input signals be applied to the complementary inputs. However, SCFL gates are balanced with respect to the dc operating point. Therefore, connecting the output of a gate to the complementary input of the next logic stage and the complementary output of a gate to the input of the next logic stage is permissible. Thus, the input to an SCFL logic gate can be logically inverted without any transistors. All that needs to be done is to cross the inputs to the gate. If this is accomplished, the NAND function will be available at the OR output, and the AND function will be available at the NOR output.

All the GaAs logic circuits discussed up to now are known as static logic circuits because they do not require a clock signal for proper operation (27). However, the use of a clock circuit can reduce the power consumption of a logic circuit because it can prevent the continuous flow of current from V_{DD} to V_{SS} when the input logic values are stable. With respect to the DCFL circuits previously discussed, up to 300 μA of output current per logic gate can flow from power to ground. With respect to the SCFL circuit previously discussed, power consumption is quite high because current is always flowing in the differential pairs and in the level-shifting circuits.

A popular dynamic logic circuit for use with GaAs E/D MESFET fabrication processes is two-phase dynamic FET logic (TDFL) (28). A TDFL two-input NOR gate is shown in Fig. 15. Two clock signals, Φ_1 and Φ_2, are required for proper operation. These two clocks must be opposite in phase and nonoverlapping during the clock high portions of both signals.

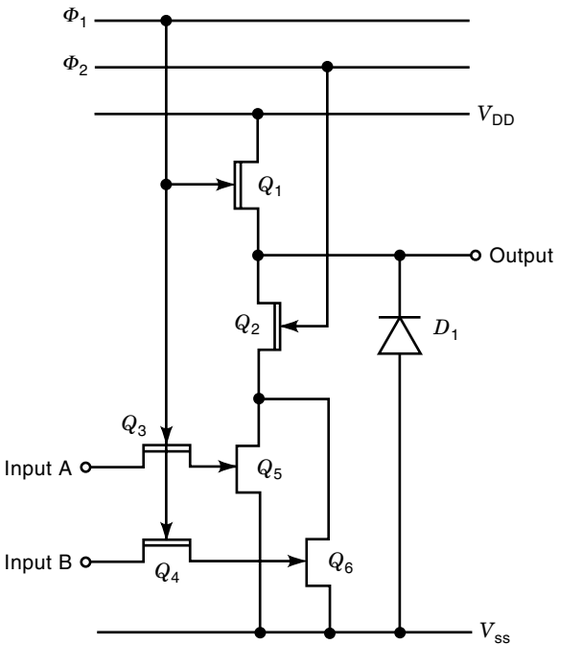

Figure 15. GaAs two-phase dynamic FET logic two-input NOR gate.

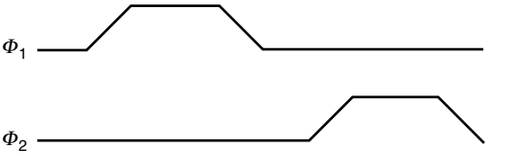

Figure 16. Timing of Φ_1 and Φ_2 clock signals for GaAs TDFL.

Figure 16 illustrates the required timing for the Φ_1 and Φ_2 clocks. Referring to Fig. 15, when Φ_1 is high, Q_1 is on and the output node charges through Q_1. The charge is stored in the reverse biased diode D_1, which is used only as a capacitor. At this point in time, Q_3 and Q_4 are also turned on and a logic high at either the A input, the B input, or both inputs will cause the gates of Q_5 and/or Q_6 to charge up to a logic high. If an input is low during this portion of the clock cycle, then any remaining charge on the gates of Q_5 and/or Q_6 from the previous cycle will be dissipated through Q_3 and/or Q_4. At this point in time, Φ_2 is low, Q_2 is off, and the output node is prevented from discharging. When Φ_1 goes low, the output node is isolated from both V_{DD} and V_{SS}. When Φ_2 goes high, Q_2 turns on. This allows the charge on the output node to discharge conditionally to ground through Q_2 and either Q_5 or Q_6, if either Q_5 or Q_6 are on. At this point in time, Q_5 and Q_6 will be on or off depending on whether a logic 1 or 0 was present at the appropriate input to the logic gate during the time period when Φ_1 was high. If input A is high, input B is high, or both inputs are high, then the output node will be discharged and pulled down to ground potential while Φ_2 is high. Thus, the Boolean NOR function is performed.

The output of the TDFL logic gate shown in Fig. 15 is valid only when clock Φ_2 is high. However, the inputs to this logic stage must be stable during the time period when Φ_1 is high. Therefore, cascaded TDFL logic stages must operate from opposite phases of the clock. An appropriate arrangement of clocks is shown in Fig. 17 for a cascade of four TDFL inverters. In Fig. 17, when the first and third inverters are precharging, the second and fourth inverters are evaluating. When the first and third inverters are evaluating, the second and fourth inverters are precharging. The actual waveforms are shown in Fig. 18. In this figure, a logic low output is represented by approximately 0 V and a logic high output is represented by approximately +500 mV. During precharge, the output node voltage reaches approximately 1 V. It should be noted that these logic level are 100% compatible with GaAs DCFL. If a logic system containing both DCFL and TDFL is desired, DCFL gate outputs can be directly connected to TDFL gate inputs. When connecting a TDFL gate output to a DCFL gate input, a dynamic latch is required because the output of the TDFL gate is not valid during the precharge portion of the clock cycle.

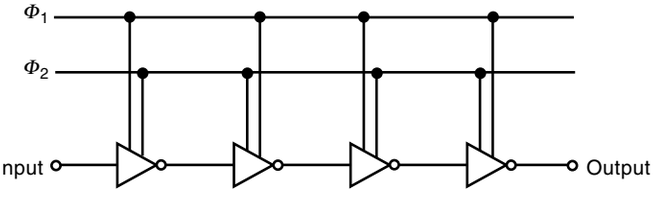

Figure 17. Cascaded GaAs TDFL inverters.

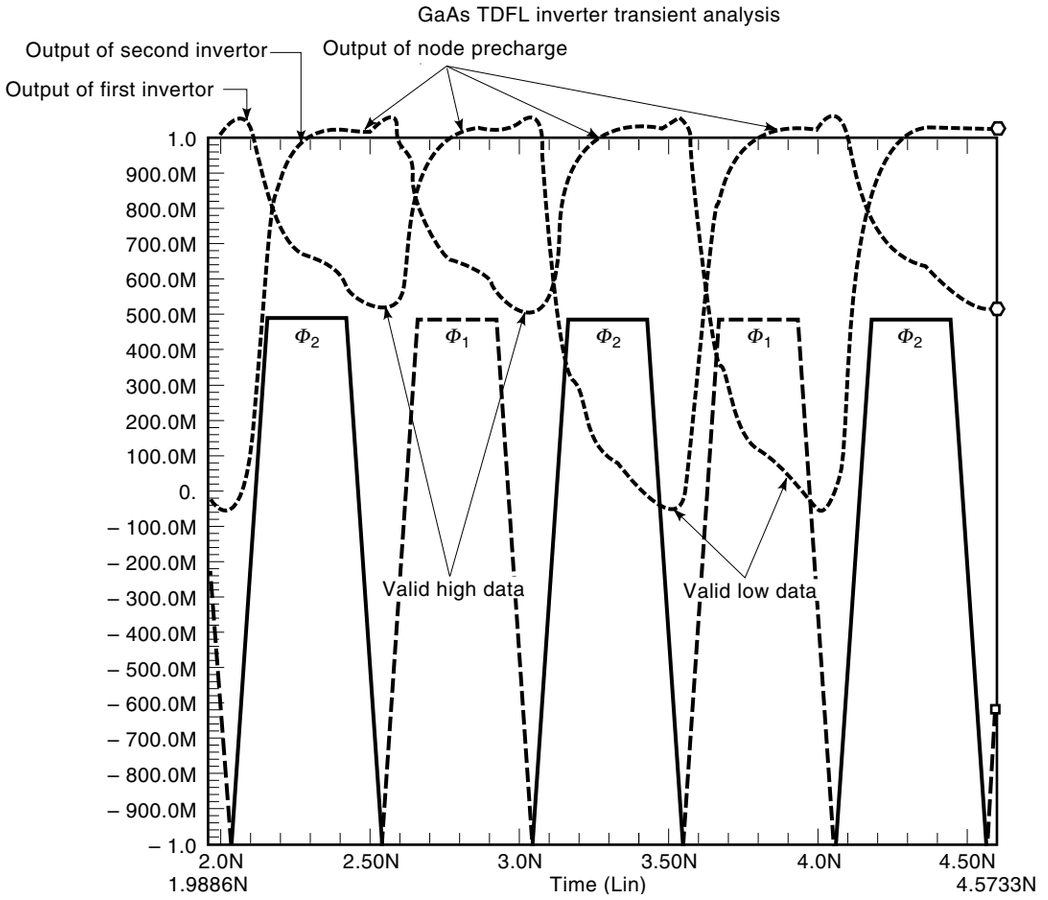

Figure 18. Operation of GaAs TDFL inverter cascade.

Referring to Fig. 18, the logic high that appears at the output of the first inverter during the first Φ_2 cycle appears at the output of the second inverter during the first Φ_1 cycle. The logic low that appears at the output of the first inverter during the second Φ_2 cycle appears at the output of the second inverter during the second Φ_1 cycle. The inherent ability to pass data along on every clock edge makes TDFL ideal for pipelined applications such as high-speed digital filters, data encoders, etc. No pipeline registers are required and thus no additional delays are incurred from flip flop internal propagation delays and set up and hold times. In addition to the high speed and inherent pipelining capability, TDFL also has the advantage of extremely low power consumption, as previously mentioned. It can be seen from the schematic diagram in Fig. 15 that at no time is there ever a conduction path directly from V_{DD} to V_{SS}. When operating with a clock frequency of 1000 MHz, the inverter in Fig. 14 consumes 31 μW, an order of magnitude less than GaAs DCFL. For pipelined systems, power is reduced even more because of the elimination of the pipeline registers.

GALLIUM ARSENIDE HETEROSTRUCTURE ISOLATED GATE FIELD EFFECT TRANSISTORS

Another popular type of gallium arsenide field effect transistor that is used in high-speed logic circuits is the heterostructure isolated gate field effect transistor (HIGFET). HIGFETs have a significantly different physical structure than do MESFETs and thus the fabrication process is also very different (29). Cross sections of GaAs n-channel and p-channel HIGFETs are shown in Fig. 19. The basic structure for these devices is a heterostructure that consists of layers of intrinsic GaAs (i-GaAs), intrinsic aluminum GaAs (i-AlGaAs), intrinsic indium gallium arsenide (i-InGaAs), i-GaAs, delta-doped silicon, and i-GaAs, all on a GaAs substrate. The source and drain regions are implanted all the way through the heterostructure with n-type dopant for n-channel transistors or p-type dopant for p-channel transistors. It can be seen by comparing Fig. 19 with Fig. 1 that the HIGFET is much more complex than the MESFET. It is also more expensive to manufacture. However, there are applications where the added cost is worthwhile, especially in low-power systems such as portable computers and satellite electronics.

Despite the significantly different structure and fabrication process, the terminal I–V relationships of the n-channel HIGFET are similar to those of the n-channel MESFET (30). Parameters such as V_T and the transconductance are different, but the basic shape of the I–V curves are the same. From the perspective of the logic circuit designer, one of the major differences is the value of the gate current as a function of the gate voltage. As mentioned previously, the Schottky-barrier diode that forms between the gate and the channel of the

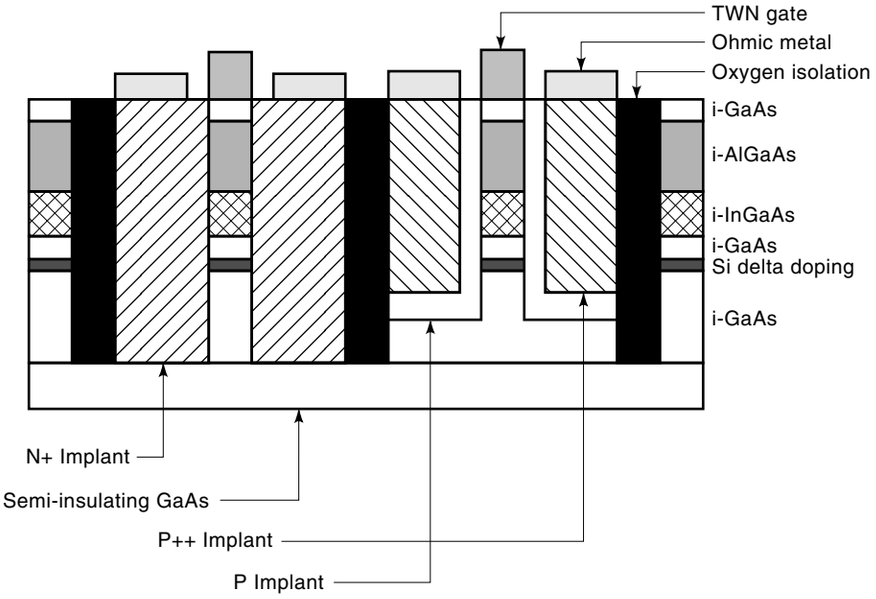

Figure 19. Structure of GaAs n-channel and p-channel HIGFETs.

MESFET allows a current to flow from gate to source when V_{GS} exceeds the turn-on voltage of the diode, which is normally in the range of 0.6 to 0.7 V. With the HIGFET, the gate is isolated from the channel. Although the gate is not insulated from the channel as is the case in the Si MOSFET, the isolated gate in the GaAs HIGFET results in significantly reduced gate current compared to the GaAs MESFET, especially for higher values of V_{GS} (31). Figure 20 shows a plot of I_G vs. V_{GS} for both an enhancement-mode n-channel MESFET and an enhancement-mode n-channel HIGFET. The MESFET has a gate length of 1.0 μm and a gate width of 10.0 μm, and V_T is 0.23 V. The HIGFET has a gate length of 0.7 μm and a gate width of 10.0 μm, and V_T is 0.61 V. The reduced value of I_G at high values of V_{GS} for the HIGFET is plainly evident. From the perspective of the logic circuit designer, this results in reduced power consumption, improved noise

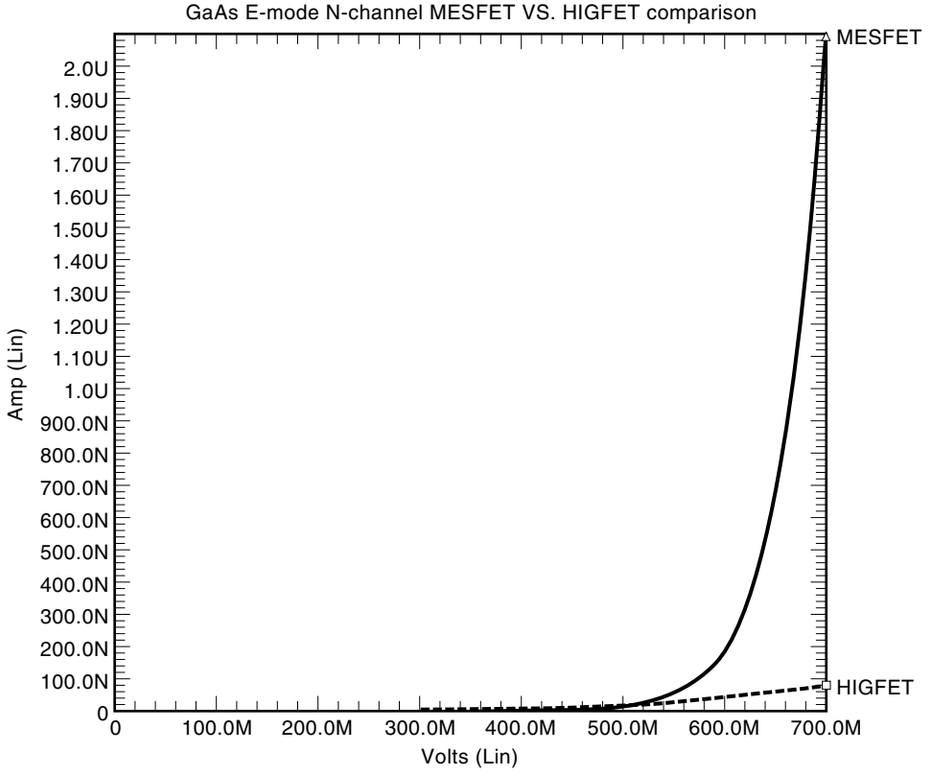

Figure 20. I_G as a function of V_{GS}.

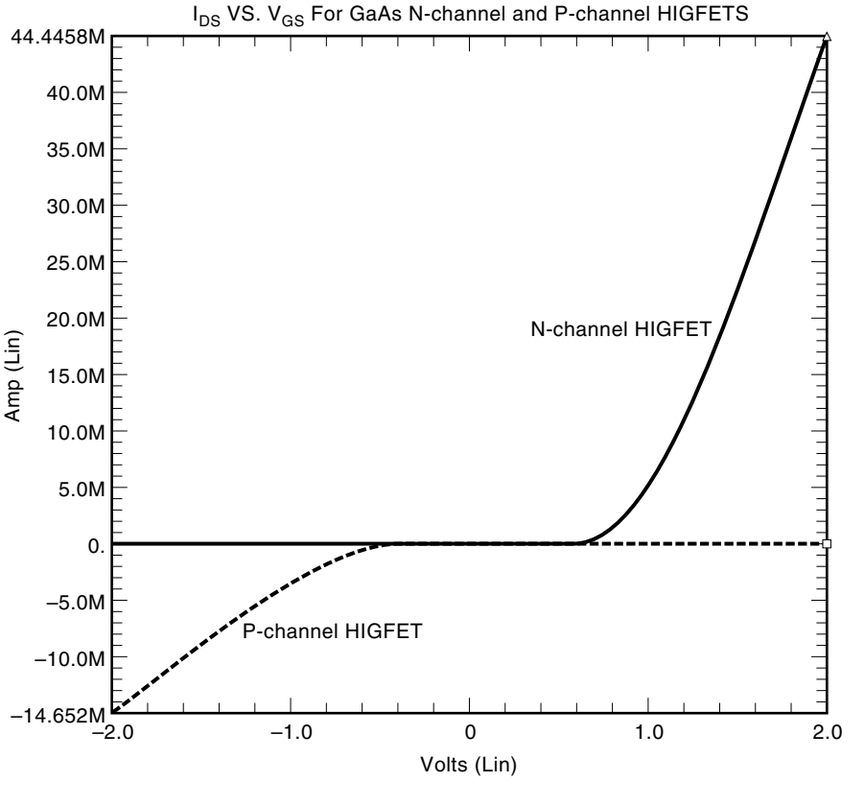

Figure 21. I_{DS} versus V_{GS} for n-channel and p-channel HIGFETs.

margins, and ease of design for both dynamic and static logic circuits (31).

As mentioned previously, with GaAs HIGFET fabrication processes, p-channel devices are much more practical than in GaAs MESFET processes. p-channel HIGFETs are still somewhat slower than n-channel devices, but they are desirable in certain circuits. The terminal I–V characteristics of a p-channel HIGFET are similar to those of the n-channel device, although the V_T, transconductance, and the signs of the voltages and currents are different. Figure 21 shows a plot of I_{DS} as a function of V_{GS} for both a p-channel HIGFET and an n-channel HIGFET. In Fig. 21, both devices have a gate length of 0.7 μm and a gate width of 10.0 μm. The V_T of the n-channel device is +0.61 V and the V_T of the p-channel device is −0.38 V. V_{DS} for the n-channel device is +2.0 V and V_{DS} for the p-channel device is −2.0 V. The differences between the polarities of the two devices is obvious. However, the difference between the absolute value of I_{DS} for a specific absolute value of V_{GS} should also be noted. The transconductance of the n-channel device is significantly greater than the transconductance of the p-channel device. The differences between the polarities and the transconductances of the n-channel and p-channel HIGFET can also be seen from the plots in Figs. 22 and 23. Figure 22 is a plot of I_{DS} versus V_{DS} for various different values of V_{GS} for a p-channel HIGFET.

GaAs STATIC COMPLEMENTARY LOGIC CIRCUITS

The availability of the p-channel device in GaAs HIGFET fabrication processes makes it possible to use the complementary static logic circuits that are so popular with silicon CMOS (13). A schematic diagram of an inverter is shown in Fig. 24 (13). In this circuit, the NFET and PFET turn on and off at opposite times. When the input is high, the NFET pulls the output low and the PFET turns off. When the input is low, the PFET pulls the output high and the NFET turns off. The dc transfer curve for such an inverter is shown in Fig. 25. The plot in Fig. 25 was obtained with V_{DD} = +1.5 V, a typical value for V_{DD} for this technology, which is capable of operating with a V_{DD} in the range of 1.0–2.0 V. The logic swing for this family of logic is usually from V_{SS} to V_{DD}. Gate length for both transistors is 0.7 μm and gate width is 2.0 μm. These are typical values of gate length and width for current fabrication technology. The output of the circuit used to obtain Fig. 25 was loaded with two inverters that are identical to the one analyzed. Noise margins for complementary static HIGFET logic can be calculated using the same equations as for a DCFL circuit fabricated with GaAs MESFETs. For the circuit shown, $NM_L = 0.66 - 0.065 = 0.595$ V and $NM_H = 1.46 - 0.85 = 0.610$ V. These values are typical.

Figure 26 shows a transient analysis of the inverter shown in Fig. 24. The value of V_{DD}, the input logic swing, and the output loading are the same as for the plot in Fig. 25. Figure 26 can be used to determine the output rise and fall times and logic propagation delays of static HIGFET logic for comparison against DCFL. From Fig. 26, T_R = 400 ps, T_F = 150 ps, T_{PLH} = 190 ps, and T_{PHL} = 110 ps. These values are typical. The output rise time is significantly greater than the fall time because, as mentioned previously, the transconductance of the PFET is significantly less than the transconductance of the NFET. The PFET gate could be widened to compensate for this. However, widening the gate would increase the capacitive loading at the input of the logic gate, which would reduce the speed of the previous logic stage for both low-to-

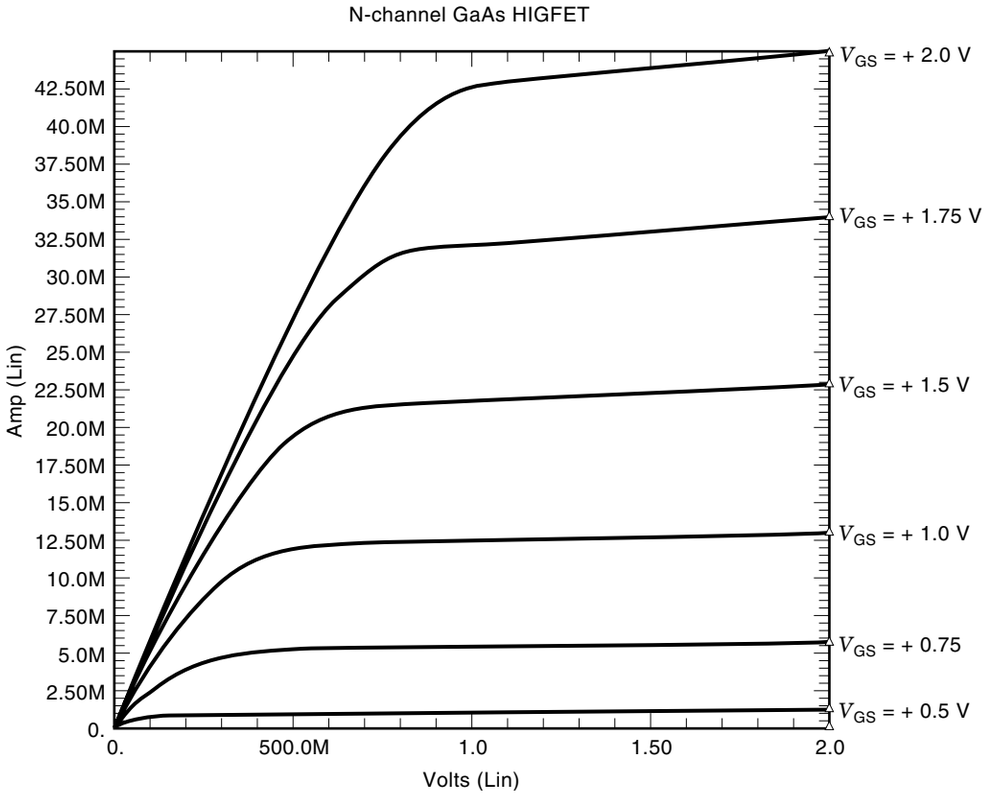

Figure 22. I_{DS} versus V_{DS} curves for GaAs n-channel HIGFET.

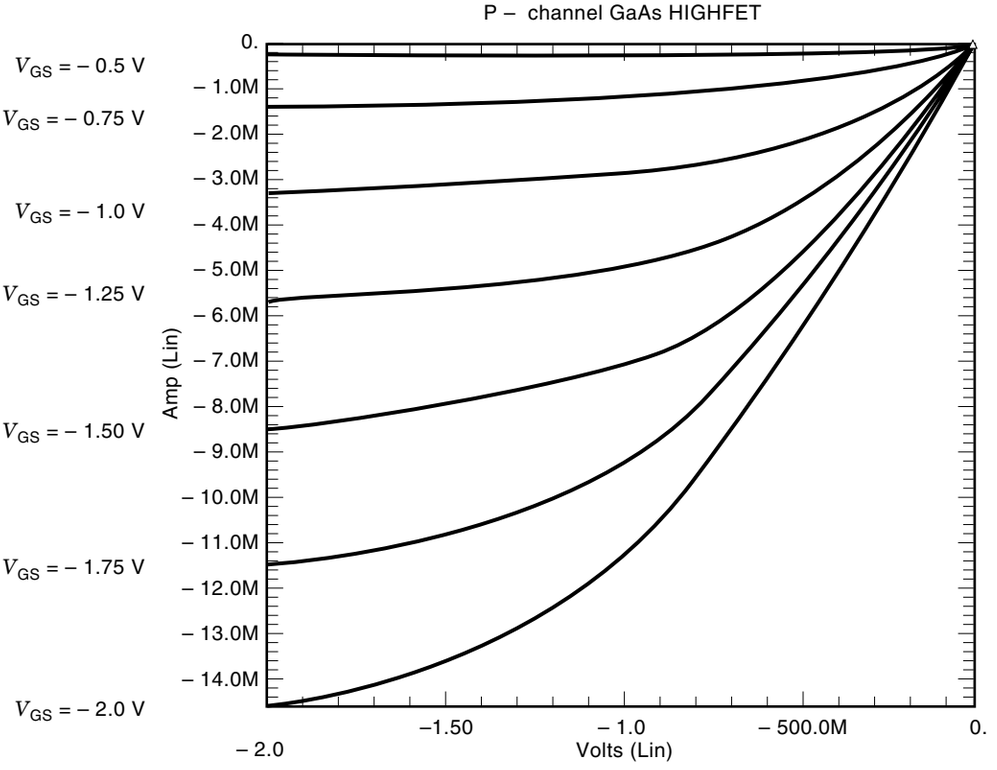

Figure 23. I_{DS} versus V_{DS} curves for GaAs p-channel HIGFET.

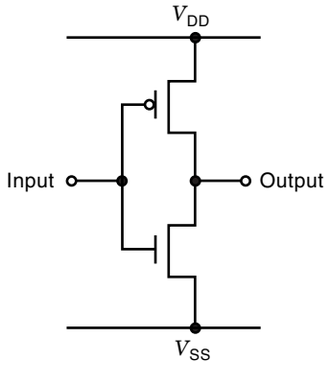

Figure 24. GaAs HIGFET inverter.

high and high-to-low transitions. In general, balancing T_R and T_F or balancing T_{PLH} and T_{PHL} is not as critical as the overall speed of operation. Comparing the transient analysis in Fig. 26 with the transient analysis in Fig. 9 illustrates the difference in speed between GaAs DCFL implemented with MESFETs and GaAs static complementary logic implemented with HIGFETs. For the DCFL inverter, T_R is 150 ps (250 ps faster), T_F is 50 ps (100 ps faster), T_{PLH} is 80 ps (110 ps faster), and T_{PHL} is 30 ps (80 ps faster). Thus, static complementary HIGFET logic is not as fast as DCFL implemented with GaAs MESFETs. However, with the exception of a small amount of leakage current, no power is consumed by the complementary HIGFET logic when the inputs are not changing. Power is consumed only when the inputs change states. Thus, power consumption for complementary HIGFET logic is normally lower than for MESFET DCFL. This makes complementary HIGFET logic preferable for portable, mobile, aeronautical, space-based, and other low-power applications. It will also work with lower power supply voltages than will MESFET logic circuits. For example, it operates correctly with a 1.2 V power supply, the output voltage of a rechargeable, single-cell, nickel-cadmium battery.

Other Boolean functions can be implemented with static complementary logic by using different circuit topologies (29,31). Figure 27 is a schematic diagram of a two-input NOR gate. In this circuit, if either of the two inputs is high, then at least one of the two NFETs will be turned on and the output will be pulled down to V_{SS}. Furthermore, the output will be isolated from V_{DD} because at least one of the PFETs will

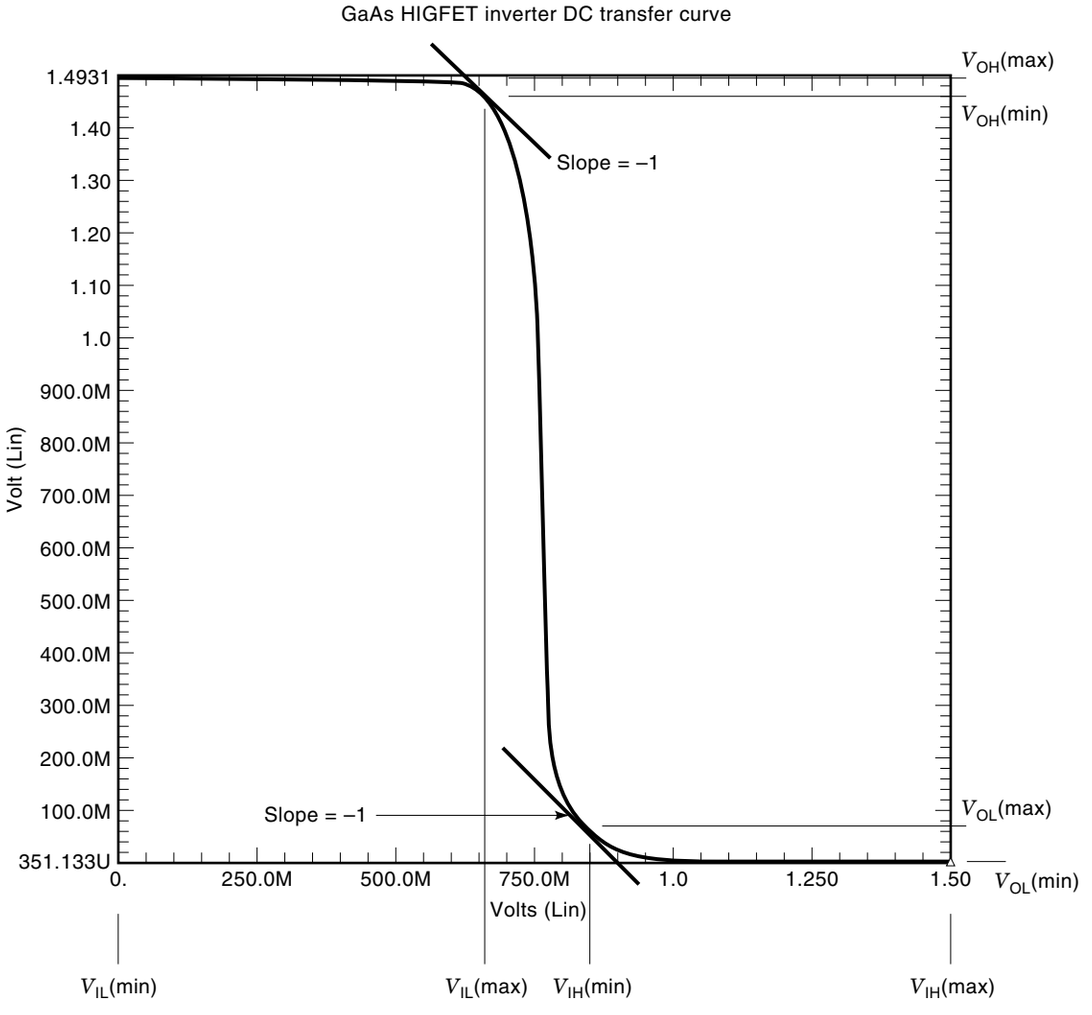

Figure 25. GaAs HIGFET inverter dc transfer curve.

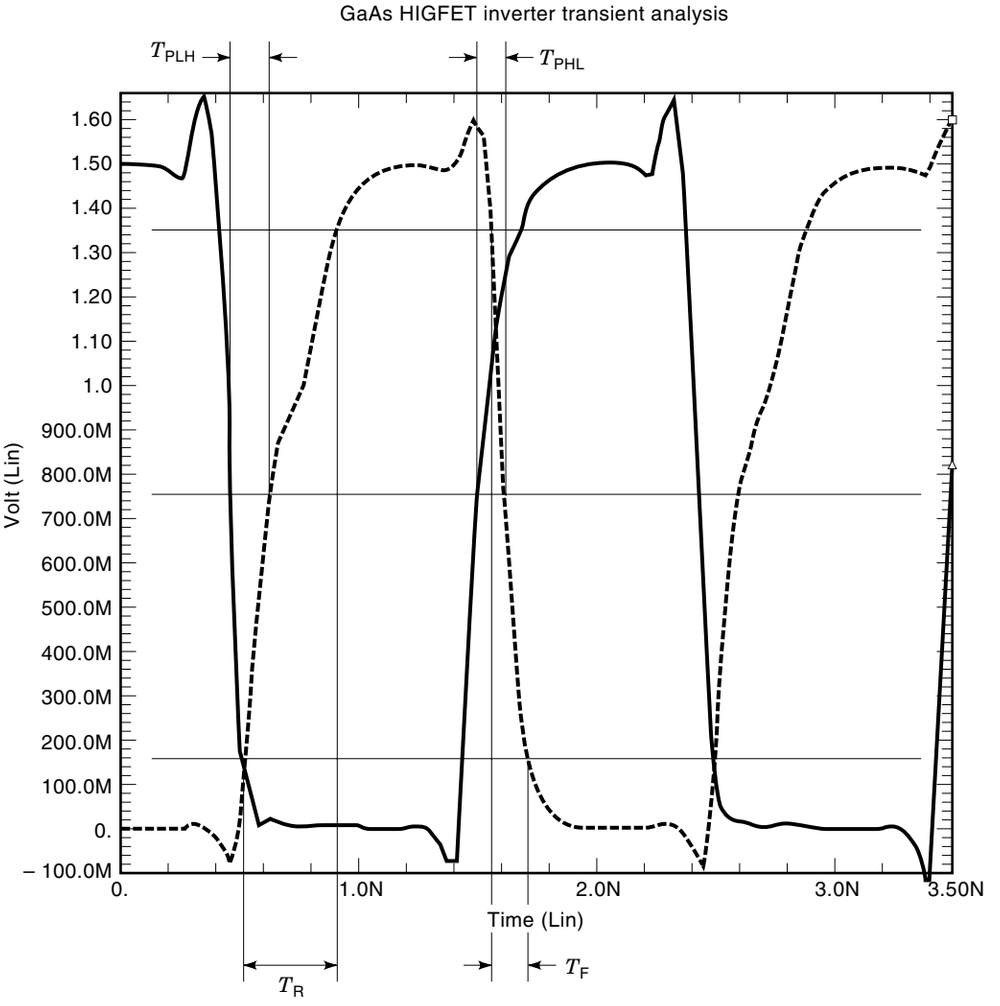

Figure 26. GaAs HIGFET inverter transient analysis.

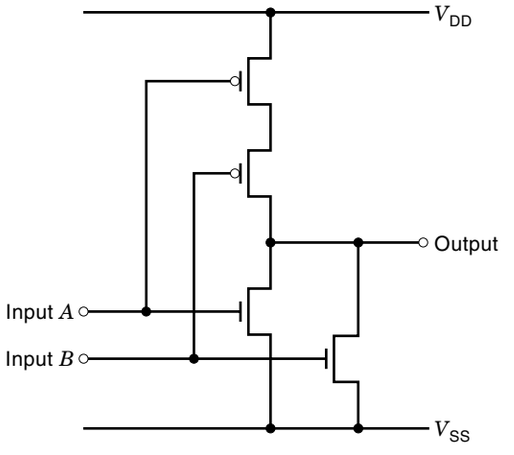

Figure 27. GaAs static two-input NOR gate using complementary HIGFETs.

be turned off. The output can be pulled high only if both inputs are low. For this combination of inputs, both PFETs will be on and both NFETs will be off. Thus, the Boolean NOR function is generated by the circuit in Fig. 27.

Figure 28 is a schematic diagram of a two-input NAND gate. In this circuit, both inputs must be high to turn on both NFETs and pull the output down to V_{SS}. Furthermore, if both input are high, then both PFETs will be off and the output node will be isolated from V_{DD}. If either input is high, then one of the NFETs will be turned off and the output will be isolated from V_{SS}. In this case, at least one of the PFETs will be on, and the output will be pulled high. Thus, the Boolean NAND function is implemented by this circuit.

With complementary static logic, multiple Boolean functions can be combined into a single logic gate. A four-input AND-OR-INVERT gate is shown in Fig. 29 that generates the logic function $f(A, B, C, D) = \overline{AB + CD}$. NFETs and PFETs can be combined in a number of different circuit topologies to create almost any desired logic function.

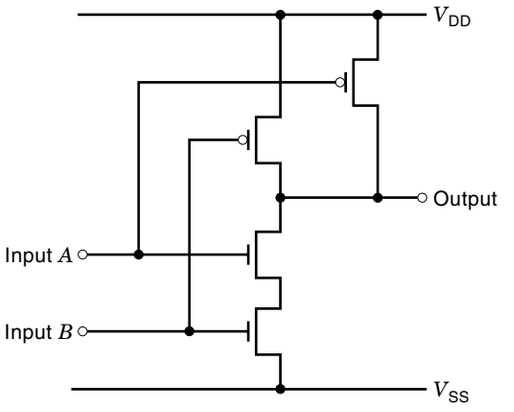

Figure 28. GaAs 2-input NAND gate using complementary HIGFETs.

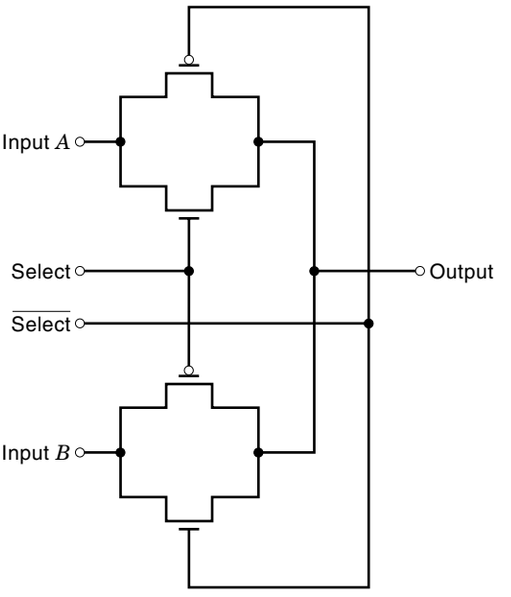

Figure 30. GaAs HIGFET pass-gate two-input multiplexer.

ADDITIONAL LOGIC CIRCUITS FOR GaAs HIGFET FABRICATION PROCESSES

Logic circuits other than static complementary logic are possible with GaAs HIGFET fabrication processes. One very useful type of logic, which is completely compatible with static complementary logic, is pass-gate logic. Pass-gate logic implemented with GaAs MESFETs has been previously discussed. However, when implementing pass-gate logic circuits with HIGFETs, NFETs must be paralleled with PFETs in order to obtain reasonable noise margins and speed. Fig. 30 shows a schematic diagram of a pass-gate, two-input multiplexer that performs the same function as the MESFET circuit shown in Fig. 13. The advantages and disadvantages of using HIGFET pass-gate logic are similar to those of MESFET pass-gate logic—reduced component count, smaller layout area, and reduced power consumption—but it also offers reduced noise margins and speed.

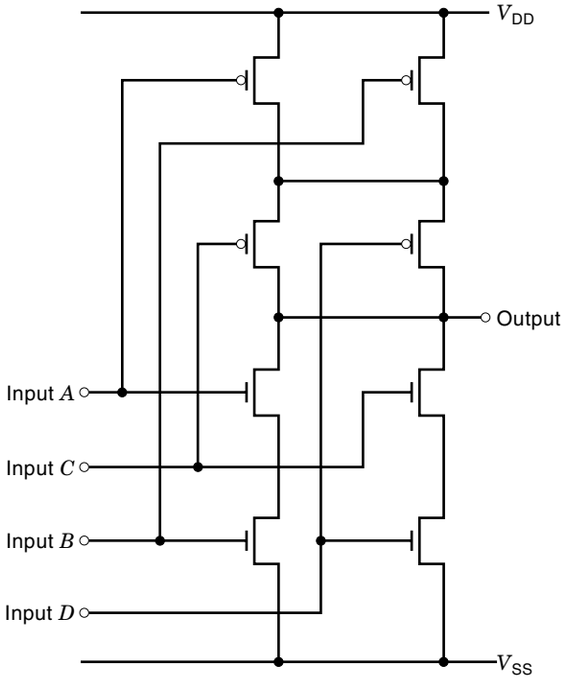

Figure 29. Four-input AND-OR-INVERT gate using GaAs complementary HIGFETs.

Another type of logic circuit that is popular to use with GaAs HIGFET fabrication processes is source-coupled FET logic (SCFL) (29). A SCFL two-input NOR gate, implemented with GaAs MESFETs, was shown in Fig. 14. The circuit topology shown in Fig. 14 can also be implemented with HIGFETs. The main difference between MESFET and HIGFET SCFL circuits is that n-channel depletion-mode FETs are not available in GaAs HIGFET fabrication processes. Therefore, n-channel enhancement-mode HIGFETs are used in place of the depletion-mode n-channel MESFETs shown in Fig. 14. This requires a change in the bias points of the differential part of the circuit and the level shifters. However, the basic circuit topology and operation stay the same. It should be noted that the use of PFETs is avoided in HIGFET SCFL circuits because they are not as fast as NFETs. The advantages and disadvantages of using HIGFET SCFL circuits are the same as for MESFET SCFL circuits—higher speed but increased power consumption, transistor count, and layout area.

Dynamic logic is also possible with HIGFET fabrication processes. A two-input NOR gate implemented with Two-Phase Dynamic Logic (TPDL) is shown in Fig. 31 (32,33). The operation of this circuit is similar to that of the TDFL circuit shown in Fig. 15. However, at the input to the circuit, parallel enhancement-mode n-channel and p-channel HIGFETs are used instead of a single, depletion-mode n-channel MESFET. Also, the gate is precharged through an enhancement-mode p-channel HIGFET rather than through a depletion-mode n-channel MESFET. This eliminates the need to distribute both

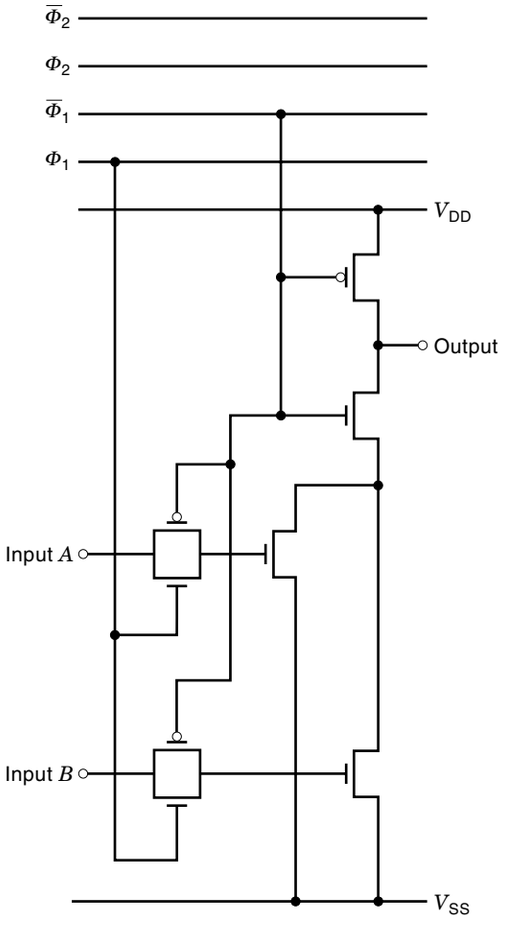

Figure 31. GaAs HIGFET TPDL two-input NOR gate.

the Φ_1 and Φ_2 clock signals to every logic stage. Only Φ_1 and $\overline{\Phi}_1$ or Φ_2 and $\overline{\Phi}_2$ need be routed to any single logic stage. Cascaded logic stages receive alternating clock signals: Φ_1 and $\overline{\Phi}_1$ for the first logic stage, Φ_2 and $\overline{\Phi}_2$ for the next logic stage, then Φ_1 and $\overline{\Phi}_1$ again, then Φ_2 and $\overline{\Phi}_2$ again, and so on. The logic swing of TPDL is compatible with static complementary HIGFET logic, which can directly drive TPDL. However, when the output of a TPDL gate drives a static complementary gate, a dynamic latch is necessary because the output of the TPDL gate is not valid during the precharge portion of the clock cycle. As with MESFET-implemented TDFL, the use of TPDL circuits in HIGFET fabrication processes reduces power consumption. However, an added benefit of using TPDL with HIGFET processes is a tremendous increase in speed. This is due to the fact that the slower PFETs are not used for generating logic functions, only for precharging the output node of the gate (32).

SUMMARY

The two most popular types of gallium arsenide field effect transistors for fabricating digital integrated circuits are MESFETs and HIGFETs. There are a number of different practical logic circuits for use with both types of FETs, including static logic, pass-gate logic, and dynamic logic. Design tradeoffs exist for all logic circuits with respect to noise margins, fan out, fan in, speed of operation, power consumption, logic function density, and ease of design.

GaAs logic circuits have very fast output rise and fall times and short logic propagation delays relative to silicon logic circuits. Although the power consumption of some GaAs logic circuits is high, comparisons between the power consumption-gate delay products for GaAs and silicon circuits indicate that GaAs circuits have an advantage over silicon circuits of four to five times in high-speed applications. However, silicon logic circuits are still preferred for low-speed and moderate-speed applications, or where the functional complexity of an IC requires over one million transistors. For space, military, and other applications requiring radiation tolerance, GaAs logic offers excellent hardness to total-dose and dose-rate effects. Furthermore, substantial progress has been made at reducing the sensitivity of GaAs logic to single-event upsets.

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