FIELD EFFECT TRANSISTOR MEMORY CIRCUITS

Although it is possible to realize any logical circuit using standard cells (single logic cells such as INVERTERS, NAND, NOR gates), memory circuits use specific topologies to increase the amount of bits stored per unit area. Memory circuits are composed of three blocks (see Fig. 1):

1. A storage matrix
2. An address decoder
3. An output multiplexer
4. I/O cells.

The storage matrix contains the cells that store the bits of information. These cells are arranged in rows and columns. For each row, a word line issued by the decoder allows access to all the cells of the row. When accessed, a cell copies its information to its bit line which runs along the corresponding column. In order to speed up the read operation, the bit lines are most generally precharged to a high voltage (close to or equal to V_{DD}) before the activation of the word line. The input–output (I/O) cells are placed at one end of the bit lines. For topological reasons, several words form a row, and the chosen word is sorted by the output multiplexer, which is commanded by some address bits. This arrangement is called *two-dimensional addressing.*

To obtain the highest storage density, the storage cells have the smallest possible area allowed by the process. For this reason, they have a poor current driving capability. This characteristic is at the origin of most of these important issues faced by the design of large memories:

1. *Bit-line capacitance.* The bit lines parasitic capacitance grows with the number of cells connected on it. This is the main factor limiting access time.
2. *Leakage currents.* In metal semiconductor field effect transistor (MESFET) technologies, the transistors often

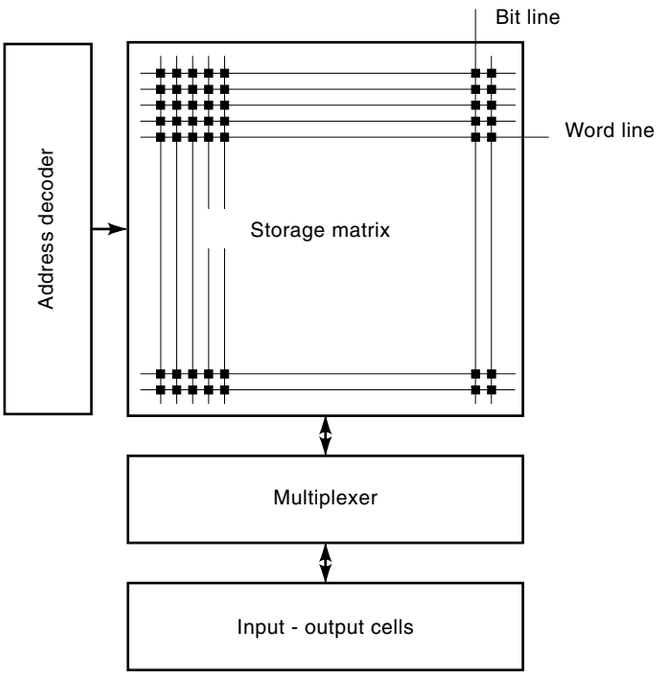

Figure 1. Basic organization of a memory circuits. The storage matrix contains the words of information, which are accessed through the output multiplexer and input–output I/O cells.

have a low threshold voltage, hence a nonnegligible subthreshold current, even when the transistor is supposed to be cut off. Depending on the type of memory, these leakage currents may induce a higher power dissipation or degrade the logic level on the bit lines, as in the case of ROMs.

3. *Power dissipation.* Power dissipation is an important issue of all MESFET based circuits. Solutions to reduce it are found either in circuit techniques or in process.
4. *Soft errors.* A soft error occurs when the information read in a cell is different from the information stored previously. Special process techniques or in some case special layout techniques allow a reduction of the soft-error rate.

In gallium arsenide, the most common processes are enhancement–depletion (EID). This means that the only transistors available are of the same type (generally *N*-type MESFETs), one with a positive threshold voltage (enhancement mode), the others with a negative threshold voltage (depletion mode). After a brief survey of the basic gates used in E/D processes, this chapter analyzes in detail the important issues faced by the design of large memories. Then, solutions to each problem are addressed in the case of read-only memory (ROM) and random access memory (RAM). Commercial circuits are presented. Finally, some results obtained with a complementary MESFET process are given.

DIRECT-COUPLED FIELD-EFFECT TRANSISTOR LOGIC

Direct Coupled FET Logic (DCFL) which looks like NMOS (n-channel Metal-oxide-semiconductor) logic in Silicon (Fig. 2), is the most compact and widely used logic family in gallium arsenide. The DCFL inverter uses both depletion and enhancement mode MESFETs (DMESFET and EMESFET, respectively). The DMESFET is used as the load by connecting its gate to its source while the EMESFET is used as the switching device. The inverter is simple and compact. However, it has a low noise margin since its logic swing is approximately 0.65V, the low logic swing is due to the fact that the logic high level is limited by the gate-to-source Schottky diode conduction. DCFL gates typically dissipate 0.2 to 1 mW per gate.

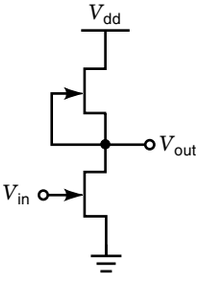

Figure 2. Schematic of a Direct Coupled FET Logic (DCFL) inverter. The bottom transistor is an enhancement mode MESFET ($Vt > 0$). The top transistor is a depletion mode MESFET ($Vt < 0$).

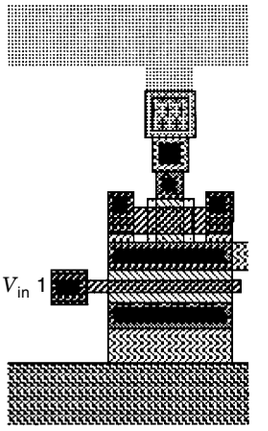

Figure 3. Layout of the DCFL inverter.

DCFL is a static ratioed logic family and then its performances depends on the sizing factor β, defined as

$$\beta = \frac{(W/L)_{pd}}{(W/L)_{pu}} \tag{1}$$

where W and L respectively represent the width and the length of the transistor and pu and pd the pull-up and the pull-down transistor.

Figure 3 shows the layout of a DCFL inverter, the cell dimensions including the power and ground busses are $15 \times 34\ \mu m^2$.

As DCFL gates are simple and compact and offer a relatively low power dissipation, those gates are generally used to build RAM and ROM circuits. However, when the temperature increases, the logic swing and the noise margin of DCFL gates is reduced, hence disturbing the memory operation. In order to overcome this problem, a source follower circuit as shown in Fig. 4 is used especially in RAM peripheral circuits to maintain enough swing even with temperature variations.

FIELD EFFECT MEMORY PROBLEMS ANALYSIS

Gallium arsenide technology is suited for high-speed systems; however, when designing regular structures such as ROM or

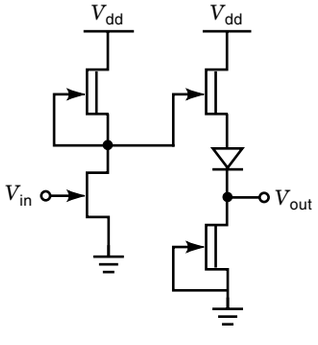

Figure 4. Schematic of the DCFL with source follower as used in RAM peripheral circuits. The low level output voltage V_{OL} is within millivolts of ground while that of DCFL is at least 100 mV. This guarantees a good output swing.

RAM, gallium arsenide presents some problems described in the sections that follow.

Leakage Currents

Subthreshold leakage currents in gallium arsenide that are five to six orders of magnitude larger than in silicon-MOSFET come from thermionic emission of carriers over the Schottky barrier and drain-source conduction through the substrate.

The subthreshold leakage current, which increases exponentially with the gate-source voltage V_{GS}, is primarily determined by process considerations (1) and is given by

$$I_D = I_0 \left(1 - \exp -\frac{cqV_{DS}}{kT}\right) \cdot \exp \frac{bqV_{DS}}{kT} \cdot \exp \frac{aqV_{GS}}{kT} \qquad (2)$$

where a, b, and c are empirical fitting parameters. I_0 is a saturation current factor. q, k, and T represent charge, Boltzmann's constant and temperature. kT/q is approximately 26 mV at room temperature. V_{DS} and V_{GS} are drain-source voltage and gate-source voltage.

Using HGaAs III technology from Vitesse Semiconductor (2), Figure 5 shows a dc HSPICE simulation of a running Statz model (3) at 25°C of the drain current versus a gate-source voltage of an EMESFET with W/L =10/0.6, for two different values of the drain-source voltage, v_{DS}, 0.1 V and 0.6 V. It can be seen clearly that even for $v_{GS} < v_T$ (where v_T is the threshold voltage in the order of 0.2 V) a current is flowing and the transistor is not completely cut off. The leakage current increases with temperature as we can see in Eq. (1). The subthreshold leakage current seriously affects the memories circuit operation.

In the ROM circuit, the parts that are strongly affected by the leakage current are the DCFL NOR gates in the programming matrix. The address decoder is made of DCFL logic, and its outputs are not at zero voltage when at low logic level. Thus, the transistors in the ROM matrix that receive these decoder outputs, have a nonnegligible drain current. This affects the circuit operation, by degrading the high level at the bit line outputs. The consequence is a limitation of the memory storage capacity.

In the RAM circuit, the subthreshold leakage current of the bit lines through the memory cells leads to an incorrect read operation, as shown in Fig. 6.

Assume a low logic level is stored on the left side. This low level corresponds to a voltage of approximately 0.1 V—the high level on the right side is represented by about 0.65 V. When the memory cell is not selected, a 0 V is applied on the gate of the two access transistors J1 and J2. However, as the bit lines are precharged at V_{DD}, a leakage current flows in J1 because its gate-source voltage V_{GS} equals 0, which is still too high to keep it blocked. On the other hand, J2 is fully blocked because its V_{GS} is negative (see Fig. 5). Consequently, the number of memory cells on a column is limited by these leakage currents occurring in all the cells which are not selected.

Power Dissipation

Because of the low noise margin, the NAND function obtained by a series connection of EMESFET transistor is seldom used. Thus, the DCFL inverter and NOR gates are selected for digi-

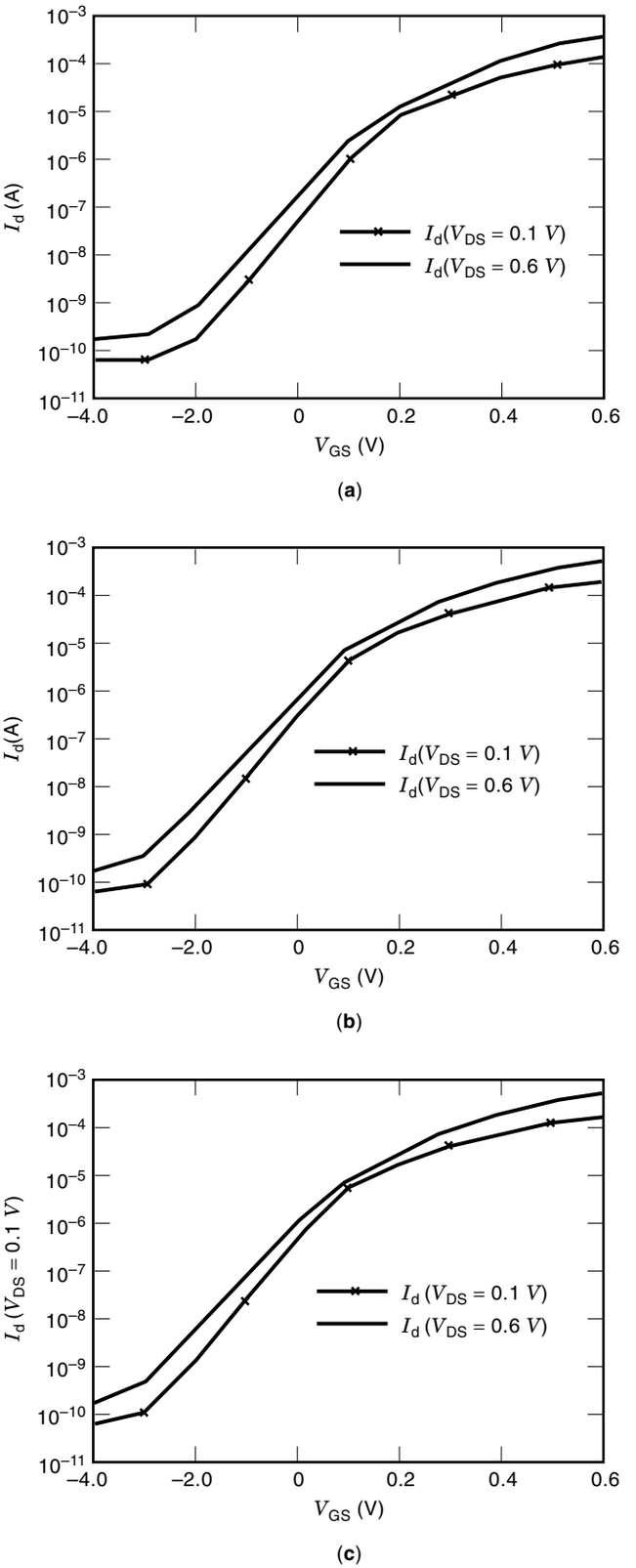

Figure 5. DC simulation of drain-current I_{DS} of an E-MESFET with W/L = 10/0.6. Conditions are: (a) 1 sigma slow; (b) typical; (c) 1 sigma fast process.

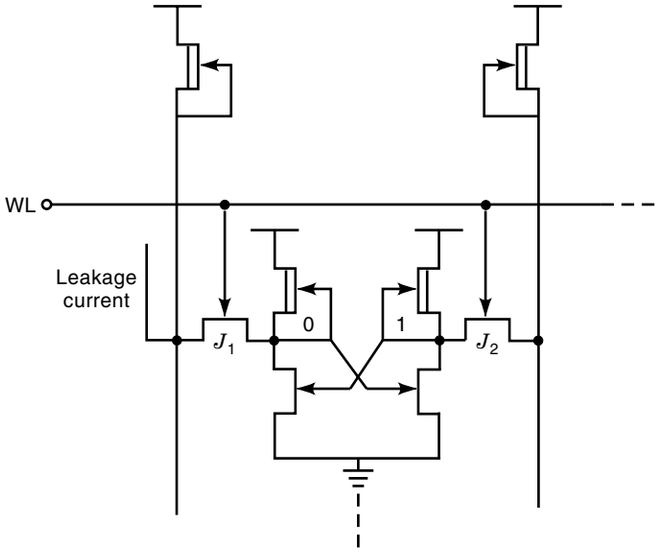

Figure 6. Leakage current path in the RAM cell. When the memory cell is unselected, a 0 V is applied on the gate of the two access transistors J1 and J2. Due to the gate-source voltage V_{GS} of the access transistor J1 which is not enough to block it, as well as its drain-source voltage, a leakage current flows at the low node of the memory cell.

tal design. For these circuits there are three sources of power dissipation summarized in the following equation:

$$P = P_{\text{static(average)}} + P_{\text{dynamic}} + P_{\text{leakage}} \tag{3}$$

$$P_{\text{static(average)}} = \eta P_{\text{sl}} + (1-\eta) P_{\text{sh}} \tag{4}$$

where η is the proportion of time when the gate output is low, where P_{sl} and P_{sh} are the static power dissipation at low level and at high level, respectively.

1. P_{sl}, *static power dissipation at low output level.* When one or all inputs of the DCFL NOR gate are at a high level, the output voltage is low, there is a conducting path from the supply to ground producing power dissipation.
2. P_{sh}, *static power dissipation at high output level.* Due to the presence of the parasitic gate-source Schottky diode, when output of the DCFL NOR gate switch to the high level and reaches the conduction level of the Schottky diode in the next stage, a current flows from the supply of the NOR gate to ground of the next stage through this diode.
3. P_{dynamic}, *dynamic power dissipation.* The instantaneous power is given by

$$P(t) = \frac{dE}{dt} = i_d \cdot V_{\text{dd}} \tag{5}$$

where i_d is the instantaneous current being drawn from the supply voltage V_{dd} and is equal to

$$i_d = C_{\text{L}} \cdot \frac{dV_{\text{out}}}{dt} \tag{6}$$

From Eqs. (5) and (6) the energy dissipated for a 0-to-1 transition (charge of the total load capacitance C_L) is equal to

$$\begin{aligned} E_{0\to1} &= \int_0^T P(t)\,dt = V_{\text{dd}} \int_0^T i_d(t) \\ &= V_{\text{dd}} \int_{V_{\text{ol}}}^{V_{\text{oh}}} C_L dV_{\text{out}} = V_{\text{dd}} \cdot C_{\text{L}} \cdot (V_{\text{oh}} - V_{\text{ol}}) \end{aligned} \tag{7}$$

Unlike complementary MOS (CMOS), the high output level V_{oh} is not equal to V_{dd} for the DCFL logic but to the the Schottky diode conduction level (0.65 V).

Finally the expression of dynamic power dissipation that is due to the charge of the total load capacitances can be given as follows:

$$\begin{aligned} P_{\text{dynamic}} &= \alpha_{0\to1} \cdot V_{\text{dd}} \cdot C_{\text{L}} \cdot (V_{\text{oh}} - V_{\text{ol}}) \cdot f_{\text{clk}} \\ &= \alpha_{0\to1} \cdot V_{\text{dd}} \cdot C_{\text{L}} \cdot \Delta V \cdot f_{\text{clk}} \end{aligned} \tag{8}$$

where $\alpha_{0\to1}$ is the node transition activity factor and ΔV is the voltage swing (approximately 0.6 V).

4. P_{leakage}. Another source of power dissipation is the subthreshold leakage current that occurs due to the conduction between the source and drain when the gate-source voltage, V_{GS}, is below the pinch-off voltage. The subthreshold leakage current is primarily determined by fabrication technology considerations and is given by Eq. (2).

The power dissipation due to the subthreshold leakage current is then given by

$$P_{\text{leakage}} = I_{\text{leakage}} V_{\text{dd}} \tag{9}$$

Thanks to the low power supply and small voltage swing, the dynamic component of power dissipation in Eq. (1) is always much less than the static component. For instance, with a voltage swing ΔV = 0.6 V, C_{L} = 30 fF and V_{dd} = 2 V, a gate dissipates less than 18 μW of dynamic power at a clock frequency of 500 MHz, whereas the average static power is typically 300 μW. The power dissipation due to the subthreshold current is also negligible in comparison to the static power. For an EMESFET (W =10 μ, L = 0.6 μm) the current simulated for V_{GS} = 0.1 V < V_{T} is in the order of 8 μA, which represents a twentieth of the total static currents.

Because of the high value of the static power compared to the other source of power dissipation, the aim of the gallium arsenide low-power designers is to eliminate first this source of power, (e.g., the case of CMOS developed because of the power consumption of NMOS). Using gallium arsenide, there has been some attempt to develop similar technologies. Unfortunately, in III–V materials, the hole mobility is low (10 times less than the electron mobility), so that the p-channel transistors have to be sized with a larger width than the n-channel transistors, hence increasing the gate input capacitance. Furthermore, because of the low Schottky barrier (0.3 to 0.4 V) on p-type gallium arsenide substrates, the p-FET gate forward conduction induces some static current consumption.

Finally, DCFL logic, which is considered a low-power logic family compared to other gallium arsenide logic families, con-

sumes significantly more than 0.2 mW per gate. This relatively high-power dissipation is another limiting factor of the storage capacity in the ROM and RAM circuits.

Yield

The physical properties of gallium arsenide are different from those of silicon; therefore, ion implementation is harder to control in gallium arsenide than in silicon. Material nonuniformities cause nonuniform transistor characteristics, which, in turn, cause threshold voltage variation across a wafer and between different wafers. This, when combined with the small noise margin from the low supply voltage and forward gate conduction clamping in MESFETs, leads to poor circuit yield, in our case memory circuits (4). In contrast, uniformity of device parameters seldom limits functional yield in silicon MOS thanks to the large noise margin due to the high supply voltage.

Short channel effects in gallium arsenide, such as threshold variation, is mainly due to the increase of the subthreshold current that flows in the semiinsulating substrate between the adjacent source/drain n^+-layers as the gate length becomes shorter, because of the high electric field between the two adjacent n^+-regions (5).

Soft-Error Immunity

Soft-errors due to the radiation effects of alpha particles is a serious problem in RAM circuits (6,7). Alpha particles, which are provided from the packages or material in the device itself, induce a noise current in the semiconductor devices flowing from the drain electrode. Furthermore, when the alpha particles hit a MESFET, electron–hole pairs are generated beneath the channel and lead to a redistribution of the electric field in the channel. As a consequence an injection of electrons from the source to the substate occurs resulting in a charge multiplication. In RAM circuits, the noise current decreases the voltage on the node storing the high level and then may cause an error on the stored data.

Access Time

Conventional sense amplifiers in silicon RAMs are based on voltage sensing, and yet this technique will be a reason for limiting high-speed operation because of speed dependency on the interconnection and the bit lines capacitances that increase with the increase of the memory capacity. As a result, in large silicon RAMs the output data swing is decreased, which leads to an extra delay and in the worst case to an incorrect readout operation.

These last years, the above problem was relieved using current sense amplifiers in large CMOS/BiCMOS SRAMs. In contrast, designing current sense amplifiers in gallium arsenide static RAMs is a challenge for designers because of some technological properties of gallium arsenide transistors.

To take advantage of high-speed gallium arsenide FETs, memory circuits designers have to decrease the output and interconnection capacitances and design a robust sense amplifier to sense current instead voltage, because the current sense amplifier is independant on the output capacitances of the bit lines.

PROPOSED SOLUTIONS TO MINIMIZE LEAKAGE CURRENT

RAM Circuits

To minimize the effect of the leakage current in the RAM circuits, some solutions have been proposed. One can mention the two ground shifting techniques proposed, respectively, by Makino et al. (8) and Chandna et al. (9). From Figure 5 we can see that when a transistor is reverse biased by at least 0.2 V the leakage currents are considerably reduced; therefore the idea is to reverse biasing the access transistors of the unselected memory cells. In the following sections each approach will be described

Technique 1. This technique shown in Fig. 7 achieves the reverse biasing of the access transistors by shifting the ground of the unselected memory cells (8). To do so, a transistor controlled by a row select signal and a diode are placed between the cell ground and the system ground. When a row is selected, the transistor J_1 is ON and the cells on this row are grounded. When the memory cell is not selected, the word line WL and the row select RS signals are in low level. Therefore the transistor J_1 is turned OFF and the ground of the memory cells is shifted by the Schottky diode voltage (0.6 V $\sim$0.7 V). As a result, the low and high stored data are raised to 0.6 V and 1.2 V, which leads to a reverse biasing of the access transistors of the unselected memory cells by at least 0.6 V.

Technique. Technique 1 reduces the leakage current in the unselected memory cells, but the cost is an increase in area and power consumption. The power is increased because an extra circuit is needed to shift the cell ground with the same speed as the circuit without using any leakage current com-

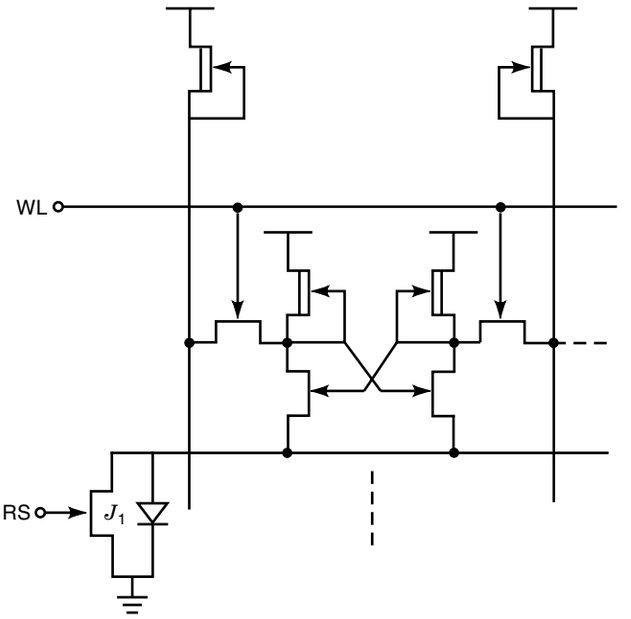

Figure 7. Technique 1 proposed by Makino et al. (8) to minimize the leakage current in the RAM cell. Using a transistor controlled by a row select signal and a diode, the access transistors are reverse biased by shifting the ground of the unselected memory cells.

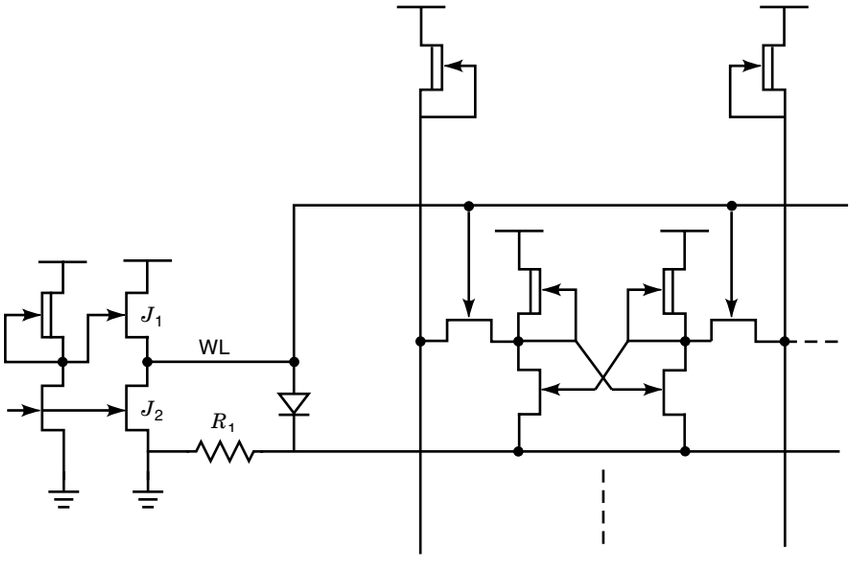

Figure 8. Technique 2 proposed by Chandna et al. (8) to minimize the leakage current in the RAM cell. The ground shifting is achieved in the memory cell by placing a resistor between cells ground and system ground.

pensation technique. In the case of a 32 kbit RAM, this power dissipation is estimated by Chandna et al. (9) to be at least 2 W. Therefore, to limit the leakage current with no extra power consumption, the same authors have proposed another technique shown in Figure 8. Another way to raise the ground of the unselected memory cells without increasing the power dissipation is to place directly a resistor between cells ground and system ground. The resistor is designed so that the voltage drop across it is at least 0.3 V, so the cells ground can rise from GND to 0.3 V. When a row is deselected, the word line WL is discharged to 0 V through the transistor J_2, and then the access transistors of the unselected cells is reverse biased by 0.3 V. Diode D_1 clamps the word line at one diode drop above the cells ground when the row is selected.

ROM Circuits

To minimize the problem of leakage currents in ROM circuits, several approaches have been proposed (10,11). One consists of modulating the aspect ratio β [Eq. (1)) with the fan in, so that the size of the pull-up transistors of the ROM bit lines increases (β decreases) with the number of word lines in order to compensate the leakage currents. The expression of modified β (i.e., β^*) is

$$\beta^* = \frac{I}{(1+p)\lambda + 1}\beta \tag{10}$$

where p represents the ratio between the absolute values of current to discharge and charge a load capacitance and λ represents the ratio between the total leakage current in the pull-down (V_{GS} in the order of 0.1 V)and the current through the transistor which is in the ON state (V_{GS} in the order of 0.65 V).

Of course, the β^* cannot be decreased too far, because it is then impossible to pull-down the bit lines. Practically, the fan in of the NOR gates must be kept lower than 32.

A second solution consists in modifying the storage cells to increase their source voltage when their input is low. The new storage cell called L2FC for Low Leakage FET Circuit is shown in Fig. 9. When V_{in} is at high logic level, L2FC operates normally like a DCFL inverter, and, when V_{in} goes low, a current I_d flows from the source current through the diode D_1 producing a voltage drop, so the source voltage of transistor J_2 becomes higher than its gate voltage. Therefore, transistor J_2 operates with a negative gate-source voltage which reduces considerably the leakage current. The cost is an increase in area and power consumption.

PROPOSED SOLUTIONS TO IMPROVE YIELD

To overcome yield problems associated with device variation, gallium arsenide digital circuits manufacturers such as Vitesse Semiconductor, ITT, and Mitsubishi use ion-implanted buried p-type (beryllium or magnesium) for their self-

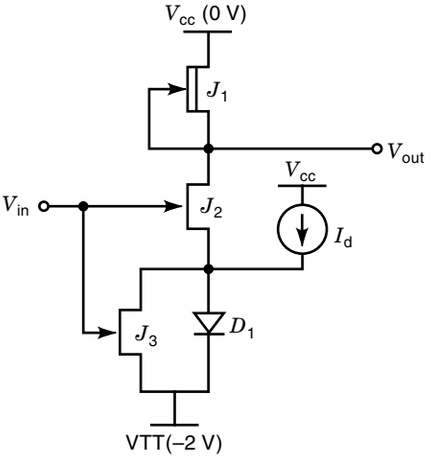

Figure 9. Schematic of the Low Leakage FET Circuit (L2FC) developed by Lopez et al. (11). To minimize the leakage current in the ROM memory cell, a source current and a diode are added to produce a negative gate source voltage in the transistor J2 when the word line voltage V_{in} is low.

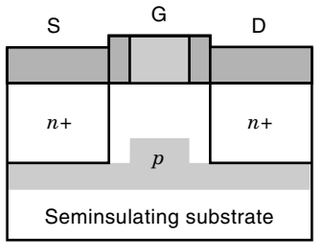

Figure 10. Structure of buried p-type (BP) self-aligned MESFET used to achieve high yield memory circuits. The buried p-layer acts as an energy barrier for electrons thanks to the $p-n$ junction. As a result, a good threshold voltage uniformity is obtained.

aligned gate E/D process (4,12). The use of a ion-implanted buried p-layer was proposed by Yamasaki and Hirayama in 1983 (13). The buried p-layer, acts as energy barrier for electrons due to the $p-n$ junction. The structure of such a BP self-aligned MESFET is shown in Fig. 10.

The implant advantages are good threshold voltage uniformity, good manufacturing control, and an improvement of device performance (I_{DSS}, g_m, and β increase with increasing BP dose). However, higher implant doses lead to an increase in gate capacitance which results in a degradation of the circuit speed. Despite the speed degradation, this approach produces a more manufacturable process, which is encouraging for achieving high-yield memory circuits.

PROPOSED SOLUTION TO IMPROVE THE SOFT-ERROR IMMUNITY

Because soft-errors induced by the parasitic current when a MESFET is hit by alpha particles are a serious problem in RAM circuits, improving the soft-error immunity has been an important task for designers. In addition to yield improvement, the p-type layer beneath the channel improves the soft-error immunity (14) by decreasing the collected charge. The high barrier of the $p-n$ junction reduces the charge multiplication induced by alpha particles, hence errors in storage nodes are reduced. To have good soft-error immunity, some techniques have been proposed to increase the critical charge in addition to the use of a MESFET with a p-type layer. We now describe briefly two such techniques.

Technique 1

For high-speed RAMs, a soft-error rate less than 100 FIT (1×10^{-7} error/device · h) is required. To decrease the soft-error rate, by increasing the capacitance of memory nodes, Hitachi has proposed to add two capacitances in the memory cell between gate and source of each pull-down transistor in the cross-coupled inverters, as shown in Fig. 11 (6). It has been found that the soft-error rate decreases from 10^6 FIT when using MESFETs with p-type layer to 100 FIT when capacitances are added to the memory cell. The disadvantage of this technique is the increase of the cell area because of the large area of the capacitances.

Technique 2

Mitsubishi has proposed another technique to add capacitances without a large increase in area (7). The capacitances

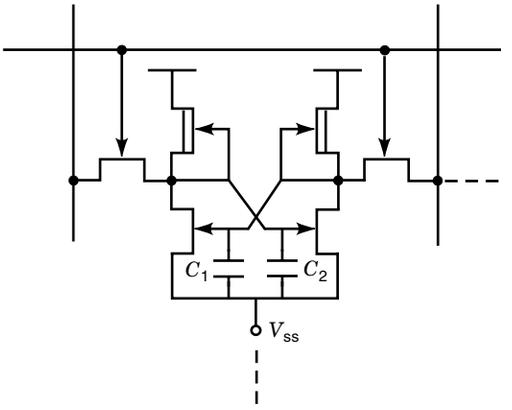

Figure 11. RAM cell with additional capacitances used to improve the soft-error immunity.

are effectively added by the use of two Schottky diodes connected between the gates of the two pull-down transistors in the memory cell and the drain of transistor J_0 as shown in Fig. 12. It has been shown that when using transistor J_0, the degradation of the high level is suppressed and then capacitances are effectively added to the storage nodes.

PROPOSED SOLUTIONS TO MINIMIZE THE POWER DISSIPATION

Power dissipation is a factor limiting the strorage capacity in memory circuits such as RAMs and ROMs. In 1983, Rockwell proposed the *power concentration* approach to save power dissipation in RAM circuits (15). With this approach, the RAM cell operates at a higher current level (provided by the column address demultiplexer) during readout than in the static mode. For this, a bit sense line is used. Because memory cells operate with little current in static mode, subthreshold current must be considered, and the minimum power dissipation

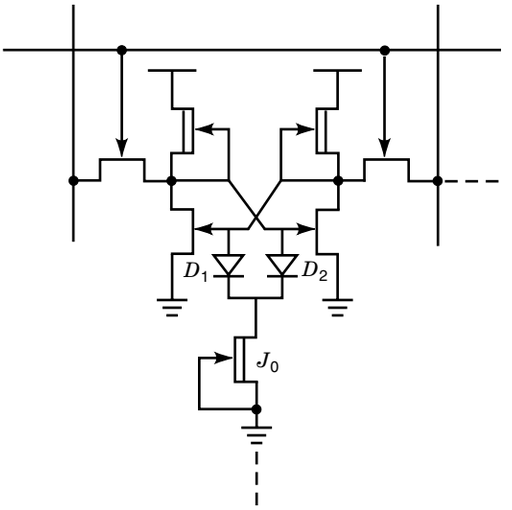

Figure 12. RAM cell with additional diodes used to improve the soft-error immunity. The two Schottky diodes increase the node capacity without a large increase in area.

is limited by the subthreshold current, which can be calculated using Eq. (2).

Four years later, a low-power 16 kbit RAM was fabricated by Rockwell (16). To achieve low-power dissipation, a powering-down approach was used. This approach consists in cutting off the power supply voltage of the peripheral circuits during standby through an on-chip power switch, while the supplies for the memory array are always ON. A power dissipation of 1 W and 200 mW during standby was measured with an access time of 20 ns.

In ROM circuits, an approach that overcomes the subthreshold currents and power dissipation at the same time was proposed. It is inspired by a divided word-line (DWL) technique, which has been proposed for CMOS RAMs (4). This technique allows the realization of both low-power and high storage capacity ROMs in gallium arsenide. In this technique, called divided decoder matrix (DDM), low-power operation is obtained by powering down the parts not situated in the addressing path, while high-storage capability is obtained by limiting the leakage currents in the ROM matrix (18). In addition, this approach improves the noise margin of the DCFL gate with the increase of the fan in (19).

As an application of the DDM technique, an 8 kbit MESFET ROM has been designed with a standard 0.6 μm gate MESFET process. The ROM has a typical access time of 1.2 ns and a power dissipation of 56 mW.

To increase the fan-in of the basic NOR gates in the ROM matrix, without complicating the ROM cells, one way is to pull the word lines as close as possible to zero. The DDM approach consists in dividing the address decoder and the ROM matrix memory into blocks and to power down the blocks not situated in the addressing path. As a side effect, the output voltage of the nonpowered decoder blocks is exactly equal to zero, hence reducing the leakage current of the bit lines.

Using the DDM approach, Eq. (10) becomes

$$\beta^{**} = \frac{\beta}{(1+p)[\lambda_1 N_1 + \lambda_2 (N_2 - 1)] + 1} \tag{11}$$

and the sizing parameters used are as follows:

1. $N_1 = 2^k - 2^j$. The total number of NOR gates in the nonpowered decoder blocks.
2. $N_2 = 2^j$. The number of NOR gates in each block of the address decoder.
3. $N = N_1 + N_2$. The total number of NOR gates in the address decoder.
4. λ_1. The ratio between the total leakage current in the pull-down transistors and the current through the transistor which is in the ON state related to the locked block ($V_{GS} = 0$ V).
5. λ_2. The ratio between the total leakage current in the pull-down transistors and the current through the transistor which is in the ON state related to the activated block ($V_{GS} = 0.1$ V).

In addition, the capacitance of the word line is composed of the gate-source capacitance C_{GS} of the EMESFETs connected to this line, and its interconnect capacitance. In gallium arsenide MESFETs, C_{GS} increases with the gate-source voltage V_{GS} as well as the drain-source voltage V_{DS} (3). As only one block is in the addressing path and the bit lines in the others are at 0 V, the address line capacitance (especially C_{GS}) is much smaller than in a conventional word line. Consequently, this approach allows us to reduce also the word line capacitance and then the word selection delay is reduced.

PROPOSED SOLUTION TO INCREASE THE SPEED

To achieve high-speed operation in the silicon RAMs, Hitachi proposed a current sense amplifier, which enhances the speed by about 25%. In addition, the use of bootstrap and common-mode data line feedback techniques leads to an improvement of 35% in the speed (6,20). These techniques, shown in Fig. 13, can be explained as follows:

1. The data line *bootstrap* circuit is realized using two DFET J_3 and J_4 (threshold voltage was -0.8 V in the used technology process) with the gate and source con-

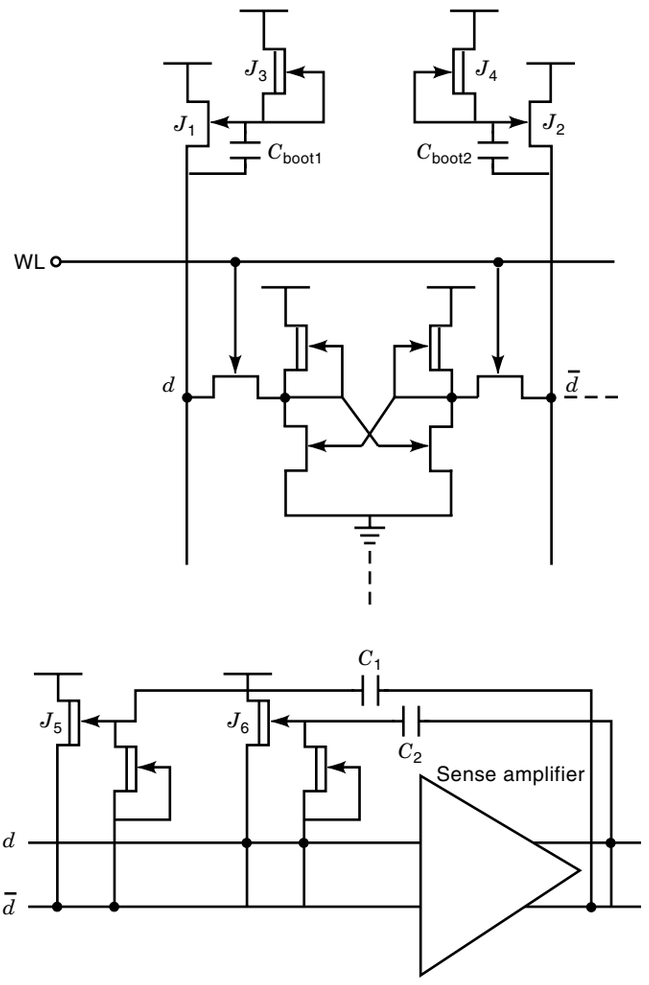

Figure 13. Bootstrap and common mode data line feedback circuit developed by Hitachi to achieve high speed operation in SRAMs. Bootstrap capacitances C_{boot1} and C_{boot2} in the data line circuit improve the swing voltage as well as the rise and fall times. In the common data-line feedback circuit, the access time is reduced still further, when the outputs of the sense amplifier are fed to the gate of J5 and J6 through the capacitances C_1 and C_2.

Table 1. Features of Silicon RAMs

Features	Mitsubishi 1.0 μm	Mitsubishi 0.7 μm	Gigabit Logic	Vitesse
Capacity, kbits	4	16	4	1
Chip size, mm^2	4.84 × 4.62	6.0 × 5.05	4.28 × 3.73	2.68 × 2.25
Cell size, μm^2	35 × 29	36 × 23	42.0 × 31.6	35.5 × 26
Access time, ns	7	5	2.25	2.5
Power dissipation, W	0.850	2	1.6	1.5

nected to the source of J_1 and J_2. When the read operation is selected, transient responses of data lines are transferred to the gate of J_1 and J_2 through the bootstrap capacitances C_{boot1} and C_{boot2}, hence the data line swing voltage is increased and faster fall and rise times are obtained.

2. Outputs of the sense amplifier are injected to the gate of J_5 and J_6 through the capacitance C_1 and C_2. By doing so, the access time is predicted to be reduced by 5%. This is called common-mode data line feedback circuit.

COMMERCIAL STATIC SRAMS

Some manufacturers, such as Mitsubishi, Gigabit Logic, and Vitesse Semiconductor Corp., have proposed some RAMs, the features of which are first summarized in Table 1, and presented briefly in the following sections.

Mitsubishi RAMs

Mitsubishi has proposed two RAMs, the first of 4 kbit (8) and the second of 16 kbit (21). These RAMs are constructed with DCFL gates and the peripheral circuits with DCFL and a source follower circuit to increase the swing and keep it constant with changing temperature. In this way, circuit operation becomes stable even at high temperatures. These RAMs are fabricated using Mitsubishi processes. The 4 kbit RAMs are fabricated using 1.0 μm self-aligned E/D MESFET and have an operating temperature range of 0° to 75°C. The 16 kbit use a 0.7 μm auto-aligned buried p-layer lightly doped drain (BPLDD) process and have an operating temperature range of 25°C to 100°C. As previously shown, Mitsubishi processes use a p-type layer beneath the channel to overcome the short-channel effect.

The size of the memory cell in the 4 kbit RAM that was enhanced by a ground shifting technique to limit leakage current is 35 × 29 μm^2, and 36 × 23 μm^2 in the 16 kbit. To increase soft-error immunity, effective capacitances have been added to storage nodes in the memory cell using diodes in 16 kbit RAM. Finally, chip size, access time, and power dissipation for 4 kbit and 16 kbit are respectively, 22.36 mm^2, 30.3 mm^2, 7 ns, 5 ns, 850 mW, and 2 W.

Gigabit Logic RAM

A 4 kbit RAM pin-for-pin compatible replacement for the industry standard 100474 ECL is available from Gigabit Logic (22). This RAM was fabricated using Gigabit Logic high-margin E/D process (HMED) with three levels of interconnect metallization. This explains the relatively small chip area of 16 mm^2. The wide operating temperature, which is from −55°C to 150°C has been achieved using a high-margin E/D RAM cell. The cost is an increase of the memory cell area (42.0 × 31.6 μm^2). Gigabit Logic RAM has a power dissipation of 1.6 W, a performant access time of 2.25 ns, and a best wafer yield of 39.5% (with an average of better than 20%).

Vitesse RAMs

Vitesse Semiconductor Corp. has proposed two 256 × 4 bit RAMs, one with transistor-transistor logic (TTL) input–output and the other with emitter-coupled logic (ECL) input–output (23). Vitesse RAMs are fabricated using an E/D 1.0 μm MESFET HGaAs II process and pin-for-pin compatible replacements for the industry standard 93422 and 100422 with an operating temperature range from −5°C to 85°C.

The memory cell is formed by two cross-coupled DCFL inverters and the cell size is 35.5 × 26 μm^2. These RAMs which have a total area of 2.68 × 2.25 mm^2 dissipate 1.5 W with a minimum access time of 2.5 ns. Finally, a functional yield greater than 50% on some wafers and an average lot yield of 30% have been obtained.

COMMERCIAL ROMS

The features of several commercially available ROMs are listed in Table 2 and described in the following sections.

NTT ROM

A gallium arsenide ROM of 512 word × 8 bit has been proposed by nippon telegraph and telephone (NTT) for the first time in 1987 (24). It was constructed with DCFL gates, peripheral circuits that used DCFL and a source-follower circuit, and a new memory cell. This cell is a single-transistor-type cell, with the gate and source of the transistor connected respectively to the word line and the bit line. The drain is tied to 1.5 V or GND according to the memory state (respectively 1 or 0). This ROM was fabricated using a NTT buried p-layer self-aligned implantation for n-type technology (BP-SAINT) process, which features 0.5 μm channel length.

The chip size is 2.64 × 2.86 mm^2 and the access time 1.2 ns. Measured power dissipation was 3.75 W including ECL

Table 2. Features of Commercial ROMs

Features	NTT	Gigabit Logic	Gigabit Logic
Capacity, kbits	4	4	8
Chip size, mm^2	2.64 × 2.86	2.44 × 3.55	5.09 × 4.80
Access time, ns	1.2	1.0	3
Power dissipation, W	3.75	2	3.5

compatible input–output buffers, with 97% dissipated in the peripheral circuit.

Gigabit Logic ROM

Gigabit Logic has proposed its first commercial ROM with a capacity of 4 kbits in 1988 with a reference 14GM048 and a chip size of 2.44×3.55 mm^2 (25). This ROM with an organization of 512 word $\times$ 8 bits is ECL compatible and has been fabricated using Gigabit Logic's three-level metal high-margin enhancement–depletion (HMED) process used also in the fabrication of the Gigabit Logic RAM discussed previously. Like NTT, Gigabit Logic uses a single FET as the ROM cell; hence an output current sensing amplifier is used to sense current instead of voltage because of the high capacitance of the bit lines. Measured access time and power dissipation at 25°C and 125°C were, respectively, 1.2 ns, 1.9 W and 1.1 ns, 2.2 W. This ROM has been used in a direct digital synthesizer (DDS) introduced on the market in July 1988.

Two years later, Gigabit Logic introduced an 8 kbit ROM with translation logic (26), using a 1.0 μm gate length E/D MESFET with 2 FETs, enhancement FET with a pinch-off voltage of 0.1 V, and depletion FET with a pinch-off voltage of -0.7 V. The circuit has been basically constructed with source coupled logic (SCL) similar to bipolar ECL. The chip size was 5.09×4.80 mm^2 and the access time 3.0 ns. As was used for the first 4 kbit ROM, a three supply voltage, GND -2.0 V and -5.2 V, was used, and a power consumption of 3.5 W was measured.

DESIGN OF SILICON RAMS USING COMPLEMENTARY GALLIUM ARSENIDE

Complementary logic circuits have been widely used in silicon (CMOS) for reducing static power dissipation. In a gallium arsenide MESFET, the contrast with silicon is not favorable for two reasons:

1. The hole mobility is disproportionately low. So, a complementary structure realization in the gallium arsenide MESFET needs a p and n transistor size ratio of 10/1 compared to 3/1 in silicon (CMOS), which is not practical.
2. The low-barrier high of the p-type gallium arsenide MESFET (0.45 eV) leads to a high leakage current for most circuit applications.

There have been some attempts to develop high-yield complementary gallium arsenide process. In 1993, Motorola Compound Semiconductor manufacturing line (CS-1) presented a complementary process (CGaAs) with two levels of interconnect metal for low-power digital circuits (27). The epitaxial wafer consists in AlGaAs/InGaAs/GaAs epilayers on gallium arsenide substrate.

To demonstrate low-power dissipation, a 4 kbit static RAM was fabricated by Motorola in 1995 as an experimental step using the complementary process CGaAs™ (28). Measured results have showed an access time of 5.3 ns and a power dissipation of 16.2 mW at a supply voltage of 1.5 V. Test was also performed at 0.9 V and measured access time and power dissipation were respectively 15 ns and 0.36 mW. Through this static RAM design, Motorola demonstrates a minimum power dissipation reported to date when using its complementary process compared to the noncomplementary gallium arsenide static RAMs.

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FIELD EFFECT TRANSISTORS. See MODULATION DOPED FETS.

FIELD EFFECT TRANSISTOR SWITCHES. See MICROWAVE SWITCHES.