JUNCTION FIELD EFFECT TRANSISTORS CIRCUITS

The basic operating principle of a field effect transistor (FET) has been known since J. E. Lilenfield's patent in 1925. In 1952, Schockley provided a theoretical description of a FET which led to the practical development of this electronic device. The junction field effect transistor (JFET) is a device in which the current flow between two terminals (drain and source) is controlled by the voltage applied to a third terminal called the gate. A cross section of a planar n-channel JFET is illustrated schematically in Fig. 1. The n-type channel is connected at either end through a heavily doped n^+ region to the source and the drain terminals. The p^+ region (gate) along with the n-channel forms a p^+n controlling junction. Let us suppose that a small positive voltage is applied to the drain and the source is grounded. Then a current flows between the drain and the source through the channel. Now if we apply a negative voltage to the gate, the p^+n junction is reverse-biased the depletion region widens and the channel narrows. As the channel narrows, its resistance increases and less current flows from the drain to the source. In this region of operation, called the linear region, the device behaves like a variable resistor whose value is controlled by the gate voltage. A further increase in the gate voltage extends the depletion zone more into the channel. When the channel is completely depleted of charge carriers, no current flows. The gate voltage at which this happens is called the pinch-off voltage. Now if

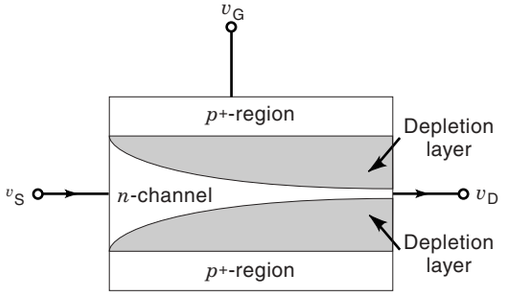

Figure 1. NJFET cross section.

we remove the restriction of small drain voltages, the width of depletion region and therefore of the channel vary with the x position. The voltage across the depletion region is higher near the drain than near the source. At large enough drain voltages, the channel at the drain edge is completely pinched off. This is the onset of the saturation region of operation in which a further increase in drain-top-source voltage does not increase the drain current. To a first approximation, the value of this current is a function of the gate-to-source voltage and of the geometry of the device. The output voltage characteristics are shown in Fig. 2 for an n-channel JFET with $W = 1800$ μm and $L = 5$ μm. The gate-to-source voltage is varied between 0 and 1.6 V with a voltage step of -0.2 V.

The current in the device is carried almost exclusively by majority carriers (electrons in n-type devices). This distinguishes field-effect transistors which are unipolar devices from bipolar junction transistors (BJTs). From a physical viewpoint the FET is a charge-controlled device, whereas the BJT is a current-controlled device. In MOSFET, JFET, and BJT, the current in the device is controlled, respectively, by the charge deposited onto the metal-oxide-semiconductor capacitor, the depletion region charge in the reverse-biased gate-channel junction, and the current of the forward-biased, base-emitter junction. The electrical characteristics are determined to a first approximation simply by the different physical control mechanism.

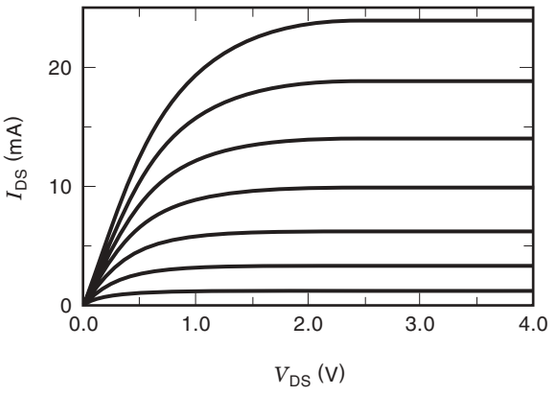

Figure 2. Measured output characteristics of a NJFET featuring $W = 1800$ μm and $L = 5$ μm. The gate-to-source voltage is varied between 0 and -1.6 V with a step of -0.2 V.

JFET APPLICATIONS

Hybrid and discrete circuit realizations make large use of JFETs. They are less common in VLSI circuits as the integration of JFETs on the same substrate with CMOS and/or bipolar devices requires some extra technological steps that lead to higher costs.

JFETs are widely used in operational amplifiers and buffers, high-frequency communication circuits, current sources, voltage-controlled resistors, and analog switches. In operational amplifiers where the base current and the finite imput impedance of BJTs limit the performance, FETs are used instead. FETs are essential when dealing with the high-impedance signal sources often encountered in measurement and instrumentation.

JFETs are used in operational amplifiers as input differential pairs, particularly in instrumentation applications where very weak signals must be accurately measured. Designs based on JFETs rely on low-noise performance and low offset. In fact the junction field effect transistor features very low noise especially at low frequency and, on the other hand, ion implantation accurately controls channel doping and its depth thus yielding a mismatch in the pinch-off voltage of the order of 1% to 2%. This results in amplifiers with offset voltages lower than those achievable with MOSFETs and comparable to those realizable with BJTs (1).

In small signal, high-frequency applications, such as TV, FM, auto radio, guided missiles, and radar, the FET has several inherent advantages over the bipolar transistor, such as a higher input voltage range for which the output spurious harmonics are suppressed, low noise in a wider frequency range, higher input impedance which can be useful to decouple high quality factor Q circuit loads (2).

JFETs, used as current sources, offer with unique advantage of self biasing, that is, they need no gate biasing. For example, a JFET with the source and the gate connected to ground is biased at its maximum current I_{DSS} when the drain voltage exceeds a couple of volts. JFETs are used in the linear region of operation as variable resistors in automatic gain control (AGC) amplifiers.

The field which has been taking full advantage of JFET characteristics is the amplification of signals coming from ionization detectors in nuclear physics and space applications. Depending on the specific application the front-end electronics must cope with radiation and must withstand low-temperature operation. The junction field-effect transistor is considered an intrinsically radiation hardened device. It is more tolerant to radiation than MOSFETs and BJTs. Moreover, because of the different conduction mechanism, FETs work properly at low temperature (well below 0°C) whereas BJTs do not.

Particle detectors are used to obtain information about energy, momentum, time of occurrence, or position of incidence of a particle impinging on the detector. Most detection methods use ionization in a detecting medium arising from particle interaction. In the simplest case, the charge in detectors is induced on a set of two electrodes for which ultimately only one parameter is important, their capacitance (3,4).

The signal charge delivered by an ionization detector is usually very small, ranging from few hundreds to thousands of electrons. Such a low signal needs to be processed by front-end electronics to insure the best measurement accuracy. In

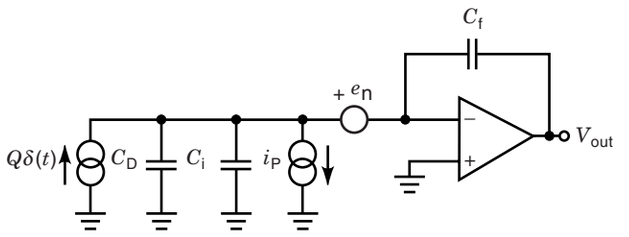

Figure 3. Capacitive-like detector and front-end charge preamplifier. The detector is represented by a dc current source and is followed by a charge-sensitive preamplifier with input referred noise sources.

most cases, the electronic noise limits the precision of the charge measurement. In Fig. 3 the particle detector is schematically represented by a delta-like current source of area Q in parallel to its capacitance C_D, followed by a charge amplifier. According to the two-port description (5), the charge amplifier is considered noiseless. The voltage and current sources represent, respectively, the series and parallel noise. In an ideal charge amplifier, the output voltage is proportional to the input charge Q through the feedback capacitor C_f, so that $v_o = Q/C_f$. Then this voltage signal is usually further processed to increase the signal-to-noise ratio and then digitized.

As mentioned before both the detector and the front-end electronics in space and nuclear physics applications operate in an extreme radiation environment, so that attention must be placed on radiation tolerance.

By characterizing silicon-based integrated electronic circuits from their amplifying elements (BJT, MOSFET and JFET), one can distinguish among different technologies. The sensitivity of these elements to bulk and surface radiation damage differs greatly. MOS transistors are affected mainly by oxide and interfacial damage, and bipolar transistors by bulk damage, whereas JFETs are in a certain sense "intrinsically radiation hard." The oxide and interfacial damage with its build-up of positive charges leads to a transistor threshold voltage shift that eventually renders a MOSFET-based circuit inoperable. Bipolar transistors suffer primarily from deterioration of carrier lifetime resulting in higher recombination in the base region and consequently a loss of current amplification (B) and an increase of the base current. Therefore, as far as radiation tolerance is concerned, JFETs are superior to both MOSFETs and bipolar transistors (6).

Noise Sources

It has been already emphasized that one of the major reasons why the JFET is used in electronic circuits is that it features extremely low-noise performance. In the following, the physical mechanism responsible for noise in the device is discussed to arrive at an equivalent description in terms of the two input noise sources and their power spectral densities.

Thermal fluctuations among current carriers in a channel are one of the principal noise mechanisms. These fluctuations produce thermal noise in the drain current and also in the gate current because of the capacitive coupling between the gate and the channel.

A second important source of noise is carrier generation through charge traps located in the space charge region of the channel-gate junction. Under normal operating conditions, the junctions are reverse-biased and a trap in the depletion region alternatively generates a hole and an electron, which are immediately swept out of the region by the strong electric field. In silicon devices at room temperature, these generated carriers constitute the main part of the leakage current in the gate lead. Therefore, there is a shot-noise component in the gate current which, at low frequencies predominates over thermal noise components capacitively coupled to the gate by thermal fluctuation in the drain current.

The depletion region fluctuation also produces noise in the drain current. This is caused by centers continually changing their charge state, causing a variation in the depletion layer width, and then in the channel width, thereby producing a noise current.

A third mechanism of noise is the fluctuation of carrier concentration due to the presence of charge traps in the channel. This depends strongly on the absolute temperature, the position and, the activation energy of the trap (7).

To derive a quantitative relationship between the power spectral density of the thermal noise and the small signal parameters of the device, the channel is treated as a resistor whose value depends on its position along the channel. An interesting but lengthy mathematical treatment leads to the following expression for power spectral density S_{idth} in the channel current for the case of V_{DS} close to zero (linear region) (8,9):

$$S_{idth} = 4kTg \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, and g is the conductance of the channel.

In the saturation region, the expression of the power spectral density of the thermal noise in the channel current is related to the transconductance of the device and is given by

$$S_{idth} = 4kT\Gamma g_m \tag{2}$$

The parameter Γ can be more than unity because of field-dependent mobility and hot electron effects (10). In long channel devices, in which these effects are negligible, Γ equals 2/3.

The thermal motion of the carriers in the channel causes a random variation in the potential along the channel producing a fluctuation in the depletion layer width. In this way the total charge in the depletion region also fluctuates randomly and, through the capacitive coupling between the gate and the channel, a noise current $I_G(t)$ flows in the gate terminal. The power spectral density of the noise current induced in the gate (S_{igth}) is expressed by (11,12)

$$S_{igth} = \frac{kT\Gamma\omega^2C^2}{g_m} \tag{3}$$

It is worth noting that this spectral component is proportional to the square of the frequency and to the square of the gate to channel capacitance C. Because this noise has the same physical origin as the thermal noise in the drain current, some correlation exists between the two. In most cases, especially at low frequency, this noise is completely negligible compared to the shot noise of the reverse-biased gate-channel junction and therefore is neglected.

Shot noise is associated with current flow across a potential barrier. In JFETs the reverse-biased gate-channel junc-

tion contributes shot noise in the gate current whose power spectral density (S_{ig}) is given by

$$S_{ig} = 2qI_G \tag{4}$$

where q is the electron charge and I_G is the gate current.

The presence of traps in the depletion region and in the channel of the JFET are responsible for the so-called random-telegraph-signal (RTS) noise. This noise is also called popcorn or burst noise.

In the time domain, the RTS signal is a random jumping of the drain current between two or more levels. The RTS type modulation of the drain current caused by transitions of charge state at traps is the primary mechanism for all noise due to traps. The trap changes its charge by emission or capture of a carrier. The characteristic times (capture and emission) are related to the nature of the trap and its location relative to the channel (13,14) and affect the RTS current. If we consider a single trap, the power spectral density in the drain current caused by RTS noise (S_{idL}) is given by

$$S_{idL} = \frac{k_1 f_c}{(f^2 + f_c^2)} \tag{5}$$

in which f_c is the inverse of the trap characteristic time. This spectral noise density, which is constant up to a frequency f_c and then falls off as $1/f^2$, is called Lorentzian, and therefore this type of noise is also called Lorentzian noise. In JFETs the Lorentzian noise is responsible for the low frequency noise.

Unlike the MOSFETs, $1/f$ noise is virtually absent in JFETs. However, it is not surprising that the low frequency noise in measured spectra has a $1/f^{\alpha}$-like dependence. In fact a very large number of traps, each with a different characteristic time, produces a superposition of Lorentzian terms in the power spectral density. A $1/f^{\alpha}$ fall off above the cutoff frequency is caused by superposing these Lorentzian terms (15). The virtual absence of flicker noise in these devices distinguishes them from almost all other solid-state devices. It also leads naturally to the inference that $1/f$ noise is not a bulk effect but is a phenomenon associated with the semiconductor oxide interface. Interfacial effects are absent from the JFET because the channel is modulated by a depletion layer located in the bulk of the device (16).

An equivalent JFET noise representation is derived from the analysis of the physical sources discussed above. Figure 4 shows the JFET considered noiseless and its equivalent series voltage source e_n and parallel current source i_p. Their spectral densities are, respectively,

$$S_{e_n} = \frac{4kT\Gamma}{g_m} + \sum_i \frac{k_{Li} f_{ci}}{g_m^2 (f^2 + f_{ci}^2)} = \frac{4kT\Gamma}{g_m} + \sum_i \frac{a_{Li} f_{ci}}{(f^2 + f_{ci}^2)} \tag{6}$$

and

$$S_{i_p} = 2qI_G + \frac{kT\Gamma\omega^2 C^2}{g_m} \tag{7}$$

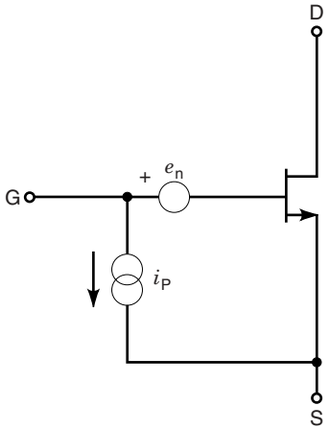

Figure 4. The JFET, considered noiseless, and its equivalent series voltage source e_n and parallel current source i_p.

The accuracy in measuring a small charge delivered by a capacitive source, such as ionization detectors, is generally limited by the noise in the front-end electronics for signal processing like that shown in Fig. 3. The noise introduced by the measurement system is usually expressed in terms of equivalent noise charge (ENC), which is the input charge that the detector should deliver to attain a signal-to-noise ratio at an output equal to 1. The processing channel is made up of a low-noise, charge-sensitive preamplifier followed by a noise-shaping filter. This filter enhances the signal-to-noise ratio. The choice of filter influences the ENC. All of the mathematical theory leading to an optimum filter choice has been deeply investigated in the literature and is not analyzed here (3,4,17,18). In what follows we indicate by T_m the peaking time of the filter output in response to a step voltage applied to the input.

The sources of noise previously described contribute differently to the ENC. The following quantities

$$\omega_T = \frac{g_m}{C_{in}} \quad \text{and} \quad H_{Li} = a_{Li} C_{in} \tag{8}$$

in which C_{in} is the device input capacitance, are characteristic of the JFET process. The white series noise, power spectral density contributes to the equivalent noise charge as

$$ENC_{th} = \sqrt{\frac{4kT\Gamma}{\omega_T}(m^{1/2} + m^{-1/2}) C_D \frac{A_1}{T_m}} \tag{9}$$

The parameter A_1 takes into account the noise transfer function, and it is characteristic of the filter. The parameter m is defined as C_D/C_{in}. From Eq. (9), it can be seen that the ENC_{th} attains a minimum when $m = 1$, that is, when C_{in} is equal to C_D, which is when the preamplifier is capacitively matched to the source. Moreover, the ENC_{th} is inversely proportional to the square root of $\omega_T T_m$, and this means that lower ENC_{th} values are achieved with faster technologies and longer measurement times.

The contribution to the equivalent noise charge from a Lorentzian term is expressed as

$$ENC_{lor} = \sqrt{H_{Li}(m^{1/2} + m^{-1/2}) C_D A_2} \tag{10}$$

The parameter A_2 depends on both the measurement time and the characteristic frequency of the trap. Knowing that a_{Li} is inversely proportional to the device gate area, we can

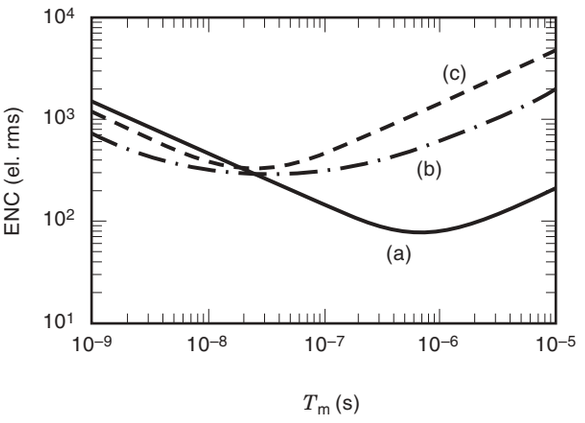

Figure 5. ENC vs measurement time for (a) a JFET (NJ26 InterFET Co.), (b) an HEMT (ATF35076 AvanTEK), and (c) a BJT (AT41435 AvanTEK). The three devices have the same C_{in} (1 pF) and are biased at 100 μA current.

state that H_{Li} is independent of the device dimension and is characteristic of a given process (13,19).

If the noise power spectral density has a $1/f$-like behavior, it contributes to the equivalent noise charge with a term analogous to that of Eq. (10), but independent of the measurement time. Finally, the shot noise in the leakage current contributes to the total ENC with a term given by

$$\mathrm{ENC_p} = \sqrt{2qI_G A_3 T_m} \tag{11}$$

where A_3 is being a constant dependent on the filter used. It is worth noting, from Eq. (11), that the contribution to the equivalent noise charge from the white parallel noise is proportional to the square root of the measurement time T_m.

A general concluding remark should be made on the basis of Eqs. (9), (10), (11). Although the ENC contributions due to thermal and Lorentzian spectral density components depend on the detector capacitance C_D, the contributions arising from parallel noise do not. The ENC is a useful tool for front-end electronics design in ionization detector applications.

At short measurement times, where the white series noise dominates, the ENC is inversely proportional to the square root of the cutoff frequency ω_T. From this viewpoint, heterostructural FETs like HEMTs are the best candidates (20). In fact they are the highest bandwidth transistors readily available today. Although the cutoff frequency of typical silicon JFETs used in preamplifiers for radiation detection is of the order of hundreds of MHz, cutoff frequencies of the order of 50 GHz to 100 GHz are available with HEMTs and MESFETs. The cutoff frequency of silicon BJT also reaches several tens of GHz but it suffers from the noise contribution added by the base spreading resistance. On the other hand, although leakage current is virtually absent in MOSFET and is usually less than 1 pA in JFETs, the gate current of MESFET and HEMT ranges around nanoamperes and makes a sizeable noise contribution. The BJT base current reaches microamps. Finally, although $1/f$ noise in MOSFET, MESFETs, and HEMTs sets a limit in the maximum possible resolution, $1/f$ noise in the JFET is of no concern. As an example, the ENC curves as a function of the measurement time for a junction field-effect transistor (NJ26 InterFET Co.), a HEMT (ATF35076 AvantTEK) and a BJT (AT41435 AvantTEK), labelled respectively (a), (b) and (c), are compared in Fig. 5. The three devices have the same C_{in} = 1 pF and are biased at 100 μA standing current.

JFET-BASED CIRCUITS

Among JFET circuit applications are a charge-sensitive monolithic preamplifier for calorimeters, a differential voltage meter for very low-temperature operation in bolometers, an application of JFETs in high frequency communication circuits and an automatic gain controlled amplifier based on a JFET in the linear region will be discussed.

All-JFET Charge-Sensitive Preamplifier

The integration of JFET on a silicon substrate is attractive for many reasons. Whenever a large number of detectors needs to be processed by the electronic front-end, small area and low power consumption are mandatory. The integrated solution allows placing a very large number of electronic readout channels close to the detector elements. Moreover, the possibility of integrating JFETs together with other devices (bipolar and CMOS) takes advantage of the characteristics of both type of devices on the same chip.

An example of a N-JFET-only charge-sensitive monolith is shown in Fig. 6. J1 and J2 constitute a cascade structure. The JFETs J3, J4, and J5 realize a boot-strapped load to present a high impedance on the drain of J2. JFET J5 buffers this high-impedance point. JFET J8 is the output stage. The cascaded current generator J6, J7 keeps the gain of the buffer J5 close to 1. C_f is the integrating capacitance, and R_f provides a dc feedback. The quiescent current in the first and second branch are the I_{DSS} values of J3 and J7. This evidences the self-biasing of the JFET when used as a current source.

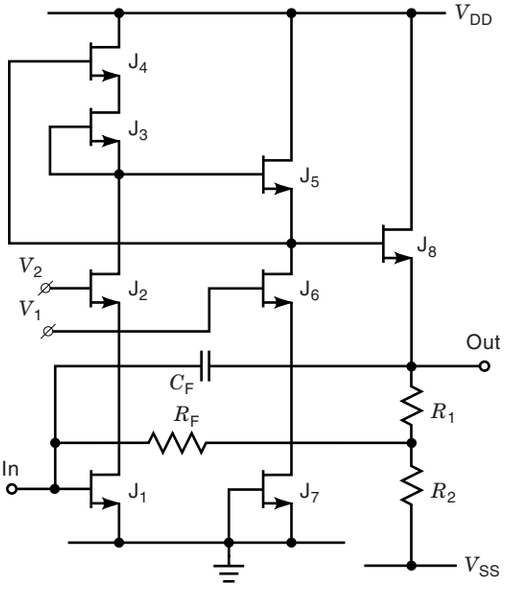

Figure 6. Charge preamplifier employing only N-JFETs.

The gate voltage of J1 and V_{SS} determine the voltage drop across R_2 and consequently the current trough J8 and the voltage on its source. The voltage of the high-impedance point on the drain of J2 is also determined. This preamplifier is designed for calorimetry. The input device area $W \cdot L$ is selected to satisfy the matching condition. The preamplifier noise spectral density is almost entirely due to that of the input device which is biased to achieve a white-noise spectral density of about 0.7 nV/$\sqrt{\text{Hz}}$, whereas the low-frequency noise spectral density does not exceed 2 nV/$\sqrt{\text{Hz}}$ at 10 Hz. A ENC = 1100 electrons (el). rms has been measured for a C_D = 240 pF at 1 μs shaping time (filter ORTEC 450) (21–23).

This design is an example of a monolithic solution based on only n-channel, junction field-effect transistors. This technology has been purposely developed with the aim of attaining noise behavior with the monolithic preamplifiers close to that of circuits employing discrete JFETs. A buried-layer approach was adopted to arrive at the coexistence on the same substrate of JFETs fabricated in the same way as discrete components. This circuit uses an interesting solution to realize the active load. The transistors J3, J4, and J5 are connected in a positive feedback loop, so that the impedance seen at the source of J3 is given by $r_{DS3}(g_{m4}r_{DS4})$. On the other hand, any variation in the pinch-off voltage causes a variation in the I_{DSS} proportional to the square of V_P, leading to a large uncertainty as to the working point and power consumption of the preamplifier.

JFET-Based Voltage-Sensitive Instrumentation Amplifier

JFETs are used in high-input-impedance, voltage-sensitive amplifiers for very high-resolution X-ray and γ-ray calorimeters, such as bolometers. In thermal detectors the energy released by the incident particle increases the temperature of the absorbing medium. Bolometers are termistors in which any temperature variation determines a corresponding change in the resistance. Very high resolution bolometers operate at very low temperatures ranging from tenths of a mK to a few K.

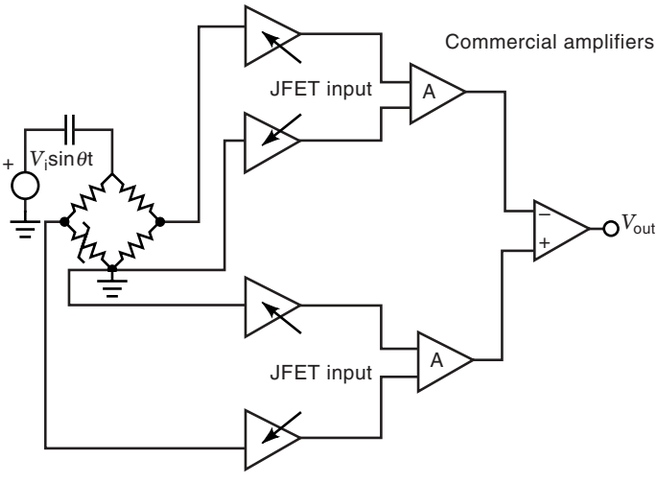

Figure 7. Voltage-sensitive instrumentation to detect the resistance variations of bolometers. A resistive bridge unbalance caused by a change in the resistance of the bolometers is detected by very low-noise, voltage-sensitive amplifiers. The commercial amplifiers give further gain and provide a voltage difference at the output.

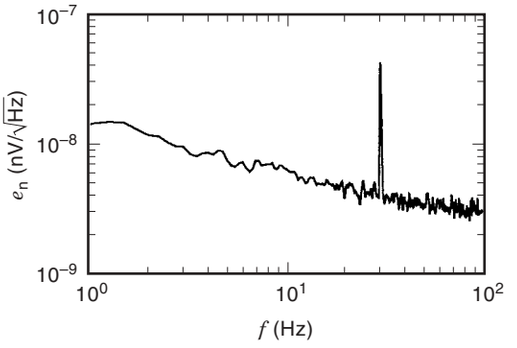

Figure 8. Spectral density measurement example. The 35 nV rms, emerging from the noise floor, corresponds to a 3.5 μK bolometer temperature variation.

The very low temperature and the extremely large number of phonons created by each event in this medium enables energy resolution lower than 1 eV if the electronic readout is noiseless (24). A resistive bridge is commonly used to detect the temperature variation. A sinusoidal voltage is applied to the input port of the bridge. Then the output voltage is amplified by a very low-noise voltage amplifier (see Fig. 7) which uses a JFET as a front-end device and is followed by an instrumentation amplifier. When a particle hits the detector, the temperature increases correspondingly changing the resistance. Therefore the output differential voltage across the bridge changes typically by tenths of a nV for each μK. It is clear that with such a low signal the noise should be as small as possible. Moreover any dc measurement would be impractical because offset voltage drift and $1/f$ noise of the front-end amplifier would deteriorate the measurement resolution. A low-frequency sinusoidal voltage signal is applied and a lock-in technique is used to eliminate the dc shift and increase the signal-to-noise ratio. The signal frequency must be chosen higher than the preamplifier noise corner frequency, that is higher than the frequency for which the $1/f$ and the white power spectral density are equal. On the other hand, the lock-in technique is based on coherent demodulation of the sinusoidal signal and low-pass filtering. Therefore, a low signal frequency is required to achieve low phase errors in the demodulator. JFET as a front-end device is the best choice because it features high input impedance along with very low corner frequency. As an example, Fig. 8 shows the input referred voltage spectrum in the frequency range 1 Hz to 100 Hz. A 35 nV rms sine wave, corresponding to a temperature variation of 3.5 μK, emerges clearly from the noise floor.

JFETs IN HIGH FREQUENCY COMMUNICATION CIRCUITS

The trend towards radio frequency highly integrated solutions demands for bipolar and BiCMOS based circuits. Nevertheless, in the medium to high frequency range (tens of Mhz) discrete circuits, JFETs are still widely used. As an example a LC voltage controlled oscillator based on a commercial JFET (2N3819) will be described. A VCO usually constitutes a

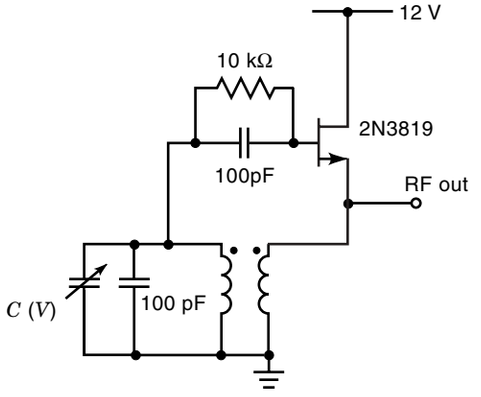

Figure 9. Coepits Voltage Controlled Oscillator (VCO). The frequency tuning is obtained thanks to a variable capacitor.

building block for Phase Locked Loop (PLL) circuits used to select frequencies in communication applications.

Fig. 9 shows the circuit diagram of a Colpitts VCO. The tuned LC is connected in an amplifier like circuit built around the JFET, to provide gain at resonance. Overall positive feedback is then used to cause a sustained oscillation to build up at the LC resonant frequency. The variable controlled by the applied voltage enables to select the frequency of the oscillator.

Automatic Gain Control (AGC)

As already mentioned JFETs are widely used as variable resistors. They find application for example as small signal attenuators, voltage-tunable filters, and automatic gain-controlled amplifiers. For example the voltage-controlled resistor is used to vary the voltage amplification of a multistage amplifier in the presence of a high-level input signal. A typical scheme of an AGC amplifier is shown in Fig. 10. The circuit uses a JFET as a VCR (voltage-controlled resistor). The output signal is rectified and filtered to obtain a dc signal proportional to the output ac amplitude. Then this voltage is applied to the control pin of the VCR. If the output voltage increases, the gain decreases accordingly, because the resistance of the VCR increases. The use of the blocking capacitor C_1 provides

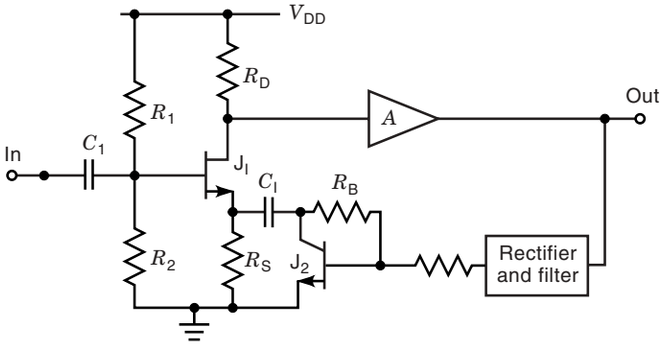

Figure 10. An automatic gain control (AGC) amplifier which uses a JFET in the linear region as a voltage-controlled resistor.

a gain control only for ac signals. Let us consider the I_D as a function of V_{DS} and V_{GS} in the linear region of operation

$$I_D = 2\frac{I_{DSS}}{V_P^2}V_{DS}\left(V_{GS} - V_P - \frac{1}{2}V_{DS}\right)$$

The drain-to-source resistance r_{DS} is thus given by

$$r_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{V_P^2}{2I_{DSS}\left(V_{GS} - V_P - \frac{1}{2}V_{DS}\right)}$$

For very low values of V_{DS} the resistance depends only on V_{GS} whereas a higher V_{DS} values the resistance depends also on the drain-to-source voltage. In the circuit proposed, the VCR is linearized using a negative feedback which sets $V_{GS} = V_C + V_{DS}/2$ thus eliminating, to a first approximation, the dependence of the variable resistor on the drain-to-source voltage (25).

PRECISE NOISE MEASUREMENTS

To evaluate the performance of an electronic system or compare different solutions in terms of noise, a very precise and reliable measurement equipment is mandatory. Several noise parameters have been introduced, such as the equivalent input noise voltage e_n, with its associated power spectral density S_{en}, the equivalent input noise current i_p, with associated power spectral density S_{ip}, the noise figure (NF), and the noise temperature T_S. According to the standard description in active two-ports, the noise is accounted for by the power spectral density $S_e(f)$ of a voltage source in series with the input port, the power spectral density $S_i(f)$ of a current source in parallel to the input port, and the cross-correlation density $S_{e,i}(f)$ between the two power spectral densities (5). Although these two voltage sources with related spectral densities completely describe the noise of any active two ports, other parameters may be used to characterize the noise of an electronic circuit. For example, the noise factor NF (usually expressed in decibels and called noise figure) is a figure of merit for a circuit or a single device with respect to noise. As given by the IEEE standards, the noise factor of a two-port device is the ratio of the available output noise power per unit bandwidth to the portion of that noise caused by the actual source connected to the input terminals of the device, measured at the standard temperature of 290 K. In other words, the noise figure is a measure of the noise degradation attributed to the two ports. The noise figure is usually used to compare the noise of different circuits in the context in which the impedance of the driving source is known. This is the case, for example, in microwave or radio-frequency applications. Another noise parameter, sometimes used, is the noise temperature T_S, which is the temperature of the source resistance that generates thermal noise equal to the amplifier noise. Noise is measured in much the same manner as other electrical quantities. But, because noise voltages are often in the nanovolt region, it is not possible to measure noise directly at its source. It is not possible, in other words, to put a sensitive voltmeter at the input of an amplifier and detect its noise. Often, the noise sources, contributing to the overall noise of a circuit, are distributed throughout it. The total noise is the sum of contributions coming from all noise generators. The

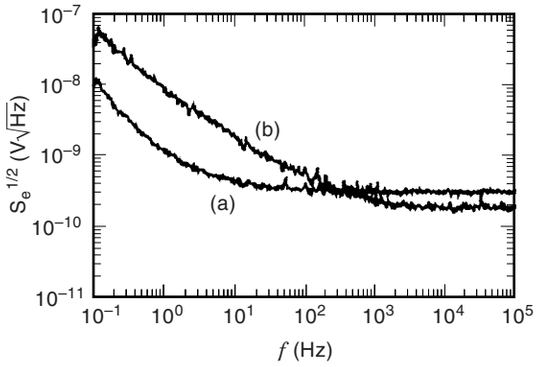

Figure 11. Measured noise power spectral density of a parallel combination of six matched large JFETs set to work at different current levels (2.5 mA and 28.5 mA, respectively, for curve (a) and (b)).

noise is usually measured at the output port where the level is highest (if the two-port is an amplifying circuit) and then referred back to the input. Two general techniques for noise measurement are the *sine wave method* and the *noise generator method.* In the former, we measure the rms noise at the output of the amplifier, measure the transfer voltage gain with a sine wave signal, and finally divide the output noise by the gain to obtain the equivalent input noise. In this way, both the noise and the output voltage are measured at higher levels. For the noise generator method, a calibrated broadband noise generator is placed at the amplifier input. With the noise generator set to zero noise, the total noise power at the output of the amplifier is measured. Then, the calibrated noise voltage is increased until the output noise is doubled. This means that the noise generator voltage is now equal to the equivalent input noise of the amplifier. The choice of the method depends on the application and the available instrumentation. The sine wave method lends itself to low-frequency measurement, while the noise generator method is usually preferred when high frequency mesurements are concerned. The former requires a two step measurement (that is a gain measurement along with the output noise one), but makes use of instrumentation usually available in a laboratory. The latter requires only one step measurement but also the availability of a calibrated noise source.

When investigating the fundamental noise mechanisms of single devices, the noise characterization often requires purposely designed and very accurate instrumentation. A single device can still be described by means of two noise generators (the voltage source can have values as low as 10^{-18} V²/Hz at 1 Hz and 10^{-20} V²/Hz above a few kHz, in the best silicon junction field-effect transistors). The commercially available spectrum analyzers feature intrinsic noise levels much higher than those to be measured. In fundamental noise studies, the need, then, arises for interfacing the device under test (referred as DUT in what follows) to the spectrum analyzer through an amplifier able to raise the noise under investigation well above the intrinsic limits of the instrument by add-

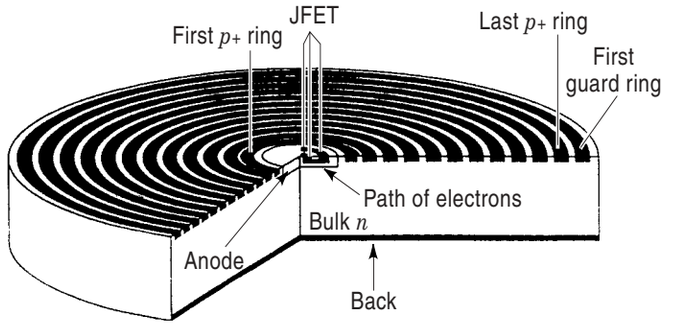

Figure 12. Schematic view of a silicon drift chamber (SDC) with integrated electronics. The top side has concentric p^+ rings 70 μm wide, separated by 40 μm of silicon dioxide. The rings are at different potential so that electrons, generated into the bulk, are collected at the n^+ anode. A JFET embedded in the anode is also schematically shown (Reprinted from Ref. 30 with kind permission from Elsevier Science - NL, Sara Burgerhartstraat 25, 1055 KV Amsterdam, The Netherlands.)

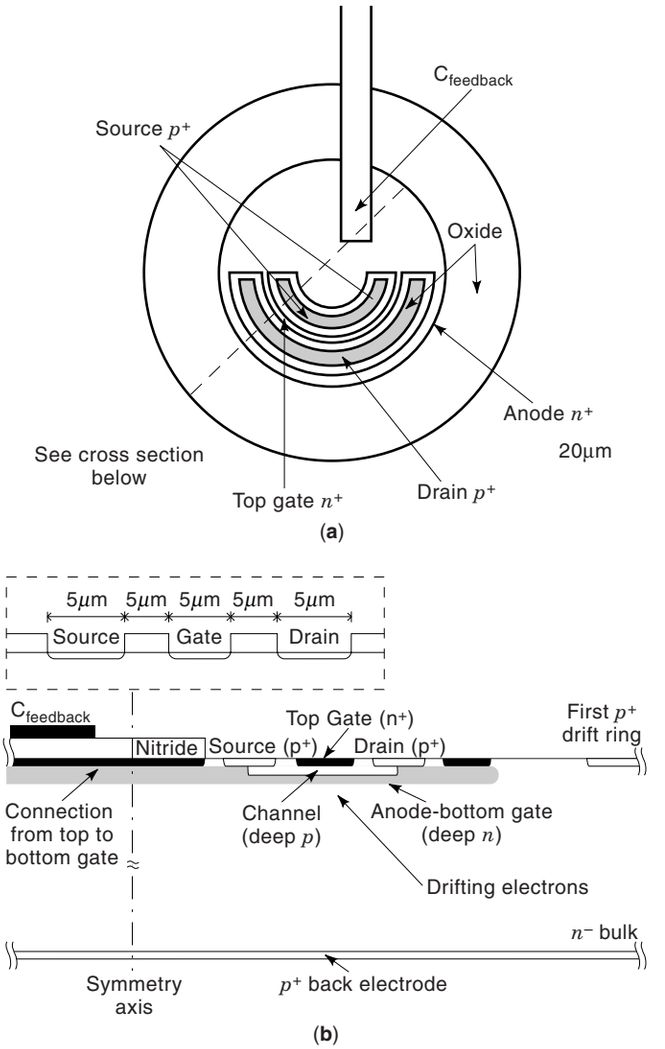

Figure 13. (a) Schematic top view of the anode of the SDC showing the integrated JFET and the feedback capacitance part of a charge-sensitive amplifier, (b) Cross section (not to scale) of the collecting anode. The inset shows the dimensions of the transistor. (Reprinted from Ref. 30 with kind permission from Elsevier Science - NL, Sara Burgerhartstraat 25, 1055 KV Amsterdam, The Netherlands.)

ing the smallest amount of noise on its own (26). Let us consider the problem of measuring the equivalent noise voltage source. The basic idea to amplify the device noise is to build up an amplifier in which the DUT constitutes the input device, and the noise contribution from other devices negligible. In this way, the amplifier output noise is the DUT noise multiplied by the amplifier gain. A transfer function calibration enables to refer the noise to the input dividing the output noise by the amplifier transfer function. Amplifiers based on this idea are designed to analyze the fundamental processes responsible for noise. The need for very precise control of the DUT biasing conditions, for a broad temperature range, and for eliminating background noise and noise coupling from the line has made this very low-noise interface a bench unit instrument with many features (27,28). As an example of ultra low-noise voltage detection, Fig. 11 shows the measured power spectral density for the parallel combination of six matched large JFETs (each gate width is $W = 9 \times 10^4$ μm, that is, the structure is equivalent to a single JFET featuring $W = 54 \times 10^4$ μm) set to work at two different current levels [2.5 mA and 28.5 mA respectively for curve (a) and (b)]. These devices have long channels ($L \sim 5$ μm), but still very large W/L and g_m and very small power density of the channel thermal noise. The theoretical values of the channel thermal noise agree well with the experimental densities of high frequency noise.

PERSPECTIVES IN JFETs

The very rapid growth of interest in silicon detectors for spectroscopy and positional measurement of ionizing radiation has been enhanced by the enormous improvement in silicon detector technology, in front-end electronics, and in signal processing. Because electronics and silicon detectors use the same substrate, it seems natural to integrate them on the same wafer. Based on this simple observation, many new detectors have been built which use a JFET as a front-end device integrated on the same substrate as the detector.

One of these detectors used for X-ray spectroscopy, is based on a silicon drift chamber (SDC) first proposed by Gatti and Rehak in 1983. SDCs are made on high-resistivity (2 to 10 kΩ) n-type wafers with rectifying p^+ junctions implanted on both sides of the detector. The volume of the detector is fully depleted of mobile electrons by a suitable potential applied to the electrodes on both sides of the wafer. A drifting field parallel to the detector surface is obtained by holding adjacent electrodes at a different potential so that electrons generated by the absorption of an X ray are focused into the central plane of the wafer and drift radially in this plane toward the small collecting anode placed in the center of the detector (see Fig. 12). The anode acts as a potential minimum for electrons. The peculiarity of this detector is that its capacitance is very small (less then 0.1 pF), independent of the detector size, and therefore the low value of ENC obtained allows very high energy resolution (29).

To take full advantage of the very low detector capacitance of silicon drift chambers, any stray capacitance should be eliminated and the first stage of amplification should capacitively match the detector itself. These features are obtained only by integrating the electronics on the detector wafer. Examples of this techniques employing n-channel JFET integrated on the high resistivity silicon substrate exists already. Also p-channel JFET has been proposed as amplifying device and this type of solution will be described hereafter. The p-JFET has been embedded in the n-doped anode of the detector as shown in Fig. 12.

The anode is also the top gate of the p-channel JFET used as the front-end device of a charge-sensitive preamplifier. A deep phosphorus implantation of circular shape acts as the collecting anode and bottom gate. The p-channel is made by a boron implantation whose projected range is between the two n-type implants. This JFET constitutes the front-end device of a charge-sensitive amplifier realized externally. The feedback capacitance is also integrated into the device and is shown in Fig. 13. One plate of this capacitance is the top gate of the device. The other is the metallization whose size determines the capacitance value. The thick nitride layer provides dielectric isolation. Using a 7 mm^2 large device, a ^{55}Fe spectrum at -50°C has been recorded which shows a resolution of 165 eV corresponding to a ENC = 13 el. rms at a shaping time of 0.5 μs (30).

Another very interesting detector which uses an on-chip JFET as a front-end device is the pn-CCD. In the pn-CCD the high resistive n-type bulk material is also completely depleted

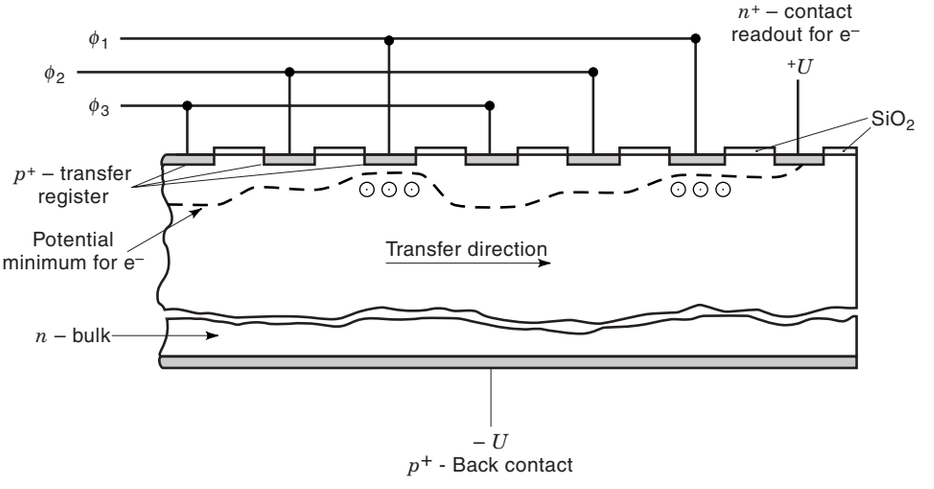

Figure 14. Functional principle of a fully depleted pn-CCD. The potential minimum for electrons is varied by a suitable potential applied to the shift register. Charge packets are collected and shifted to the read-out anode. (Reprinted from L. Strüder et al., "Device modelling of fully depletable CCDs". Nucl. Inst. Meth. Phys. Res., A253: 387, 1987, with kind permission from Elsevier Science - NL, Sara Burgerhartstraat 25, 1055 KV Amsterdam, The Netherlands.)

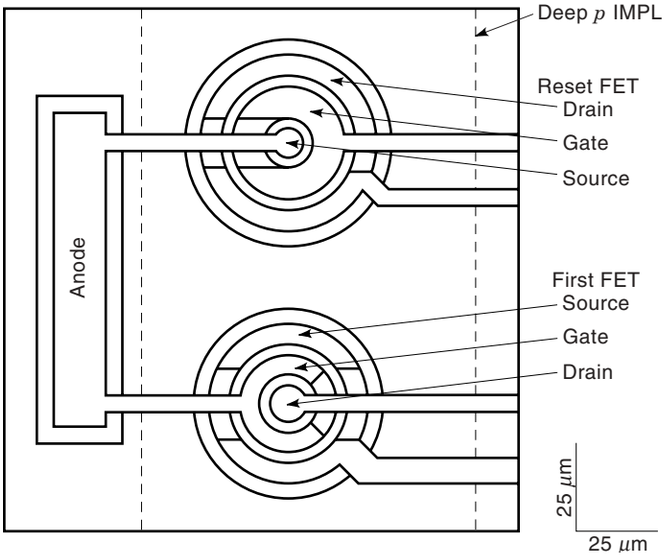

Figure 15. Schematic top view of the anode of the *pn*-CCD showing the integrated JFETs. The first FET has its gate connected to the anode and reads out the collected charge. The Reset FET has its source connected to the anode and is in normal operation in pinch-off. When the read-out is completed, it is switched in conduction, resetting the charge and establishing a fixed potential at the anode. (Reprinted from Ref. 32 with kind permission from Elsevier Science - NL, Sara Burgerhartstraat 25, 1055 KV Amsterdam, The Netherlands.)

of free carriers by a negative voltage applied to the large rectifying p^+ back contact (see Fig. 14). On the front side, p^+ implantations define the transfer registers. By an appropriate choice of voltages at p^+ transfer registers, it is possible to create local potential minima for electrons generated in the bulk by the impinging radiation. An adequate change in time of the register voltage (as in MOS-CCDs) allows discrete shift of the signal charge toward the readout anode. The transversal confinement of the charge is provided by a deep *n*-implantation that forms a guiding channel for the electrons. Each anode, which features a capacitance as low as 30 fF, is connected to the on-chip's first stage electronics which is made up of two *n*-channel JFETs isolated from the bulk by a deep *p*-implantation. The structure of the on-chip electronics is shown in Fig. 15 (31). The first FET (FF) is employed in a source follower configuration to buffer the high impedance of the anode. Its gate-to-source capacitance is about 90 fF. Thus it has good capacitive matching with the anode and ensures better noise performance. During the CCD shifting and readout of the signal charge, the reset FET (RF) is in the pinch-off state and does not affect the operation of the device. When the readout is completed, the reset FET is switched in conduction to reset the signal charge on the anode. The measured ENC of this on-chip electronics is 8.8 el. rms at room temperature and 2.2 el. rms at the CCD operating temperature of 150 K. This extremely low noise allows the very high energy resolution needed in astrophysics research (32). One of the x-ray cameras of the X-ray Multimirror Satellite (XMM) of the European Space Agency (ESA) will be equipped with this type of detector, invented at the Semiconductor laboratory of the Max-Planck-Institute in Munich.

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