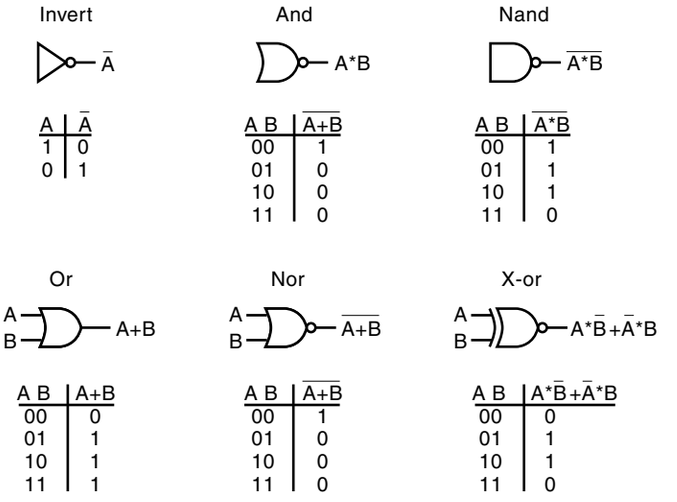

Figure 1. The notations of six basic logic gates, INVERT, AND, OR, NAND, NOR, and X-OR, where each logic function is described by a truth table.

NOR CIRCUITS

Any logic function can be expressed as the sum of products or the product of sums of all input logic variables. The state values of a binary logic variable, denoted by "1" or "0," are represented in circuits by either voltage or current using their magnitude (high or low) or polarity (positive or negative). Logic gates are basic building units which can perform standard binary logic functions. Figure 1 shows the notations of six basic logic gates, INVERT, AND, OR, NAND, NOR, and X-OR, where each logic function is described by a truth table with correct outputs for all possible combinations of binary inputs. The notation "*" is used for the logic operation AND, "+" for OR, and a bar on top of the logic variable for INVERT. The NOR and NAND gates are functionally complete, since all logic functions can be realized by either NOR or NAND gates. For example, a NAND function with one input yields INVERT; a NAND function followed by an INVERT yields the AND function; the X-OR function is realized by INVERT, OR, and AND gates; and the X-OR followed by INVERT yields the OR function. The INVERT gate has only one input. All other basic logic gates can have two or more inputs. Refer to Ref. 1 for general logic circuit design.

Logic gates can be implemented by various types of logic families, such as Transistor-Transistor Logic (TTL), Emitter-Coupled Logic (ECL) or Current Mode Logic (CML), Inte-

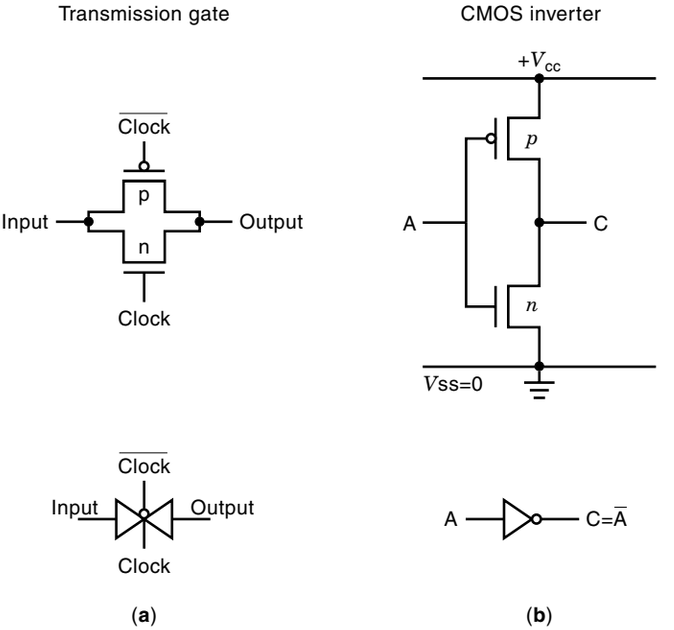

Figure 2. A transmission gate (a) is formed by a pair of *n*-MOS and *p*-MOS transistors connected in parallel. An inverter (b) is formed by a pair of *n*-MOS and one-*p*-MOS transistors connected in series.

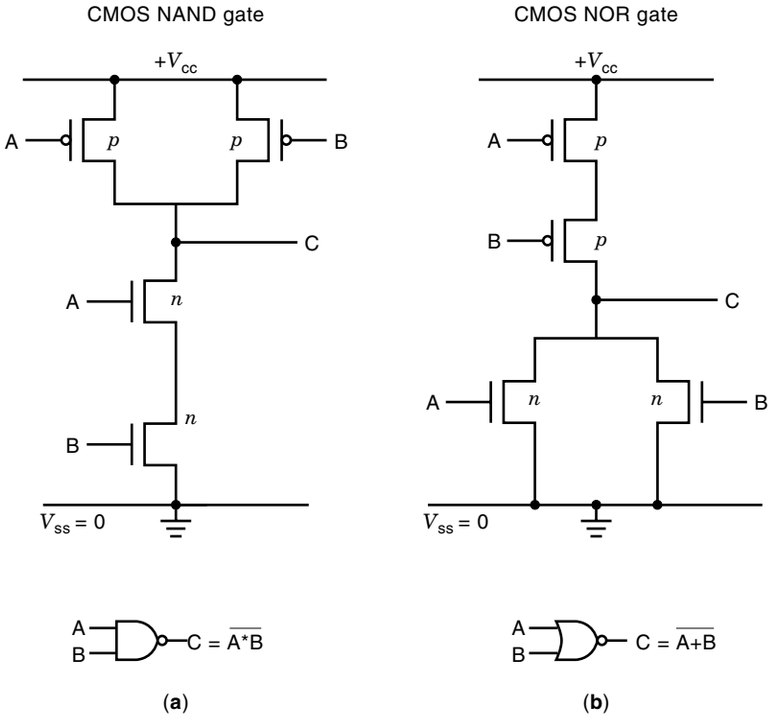

Figure 3. Static NAND gate (a) and NOR gate (b) with two inputs can be realized by CMOS technology, where each input is connected to a pair of *n*-MOS and *p*-MOS transistors.

grated-Injection Logic (I^2L), Metal-Oxide-Silicon Field Effect Transistors (MOSFET), Complementary MOSFETs (CMOS), Bipolar CMOS (BiCMOS) logic, and nonthreshold logic (NTL). Each logic family has certain characteristics in addition to their basic function for logic operations. The CMOS logic family has low power consumption, while bipolar logic families (ECL, TTL, I^2L) and BiCMOS logic are fast and flexible. The choice of logic families is based on considerations of power, speed, packing density, noise margin, supply voltage requirements, and cost. Logic gates and circuits can be implemented by discrete components or in monolithic integrated circuits. CMOS logic is by far the dominant technology in monolithic integrated circuits. Today's very large scale integration (VLSI) of logic circuits, for example, microprocessor, microcontroller, graphics processor, and so on, can perform complex logic functions using many logic gates and memories by integrating millions of MOS transistors on a single chip. Refer to Refs. 2 and 3 for digital CMOS VLSI design.

The logic gates are ideally designed for high speed (i.e., low delay time), low power dissipation, and small area. Consider a CMOS transistor. The propagation delay time (t_d) is approximately $C_L \cdot V_{dd}/I_{ds}$ or $C_L \cdot V_{dd}/[A(V_{dd} - V_t)^2]$; where C_L is the load capacitance, V_{dd} is the supply voltage, I_{ds} is the MOS transistor current, V_t is the threshold voltage, and A is proportional to transistor size (W/L) and carriers mobility. The switching power (P) is approximately $C_L \cdot V_{DD}^2 \cdot f$; where f is the operation frequency. The highest operation frequency of a circuit is determined by the total delay of critical paths and is inversely proportional to the delay time. The delay time can be reduced by using a larger transistor and applying higher supply voltage V_{dd}; however, in this case, the switching power increases. Therefore, the product of delay time and power (i.e., $t_d \cdot P$) is often used as a figure of merit for CMOS transistors as well as logic gates of various logic families.

In this article, the NOR gates implemented by various logic families are described first. Then, useful building blocks of logic circuits based on NOR circuits, such as NOR latch,

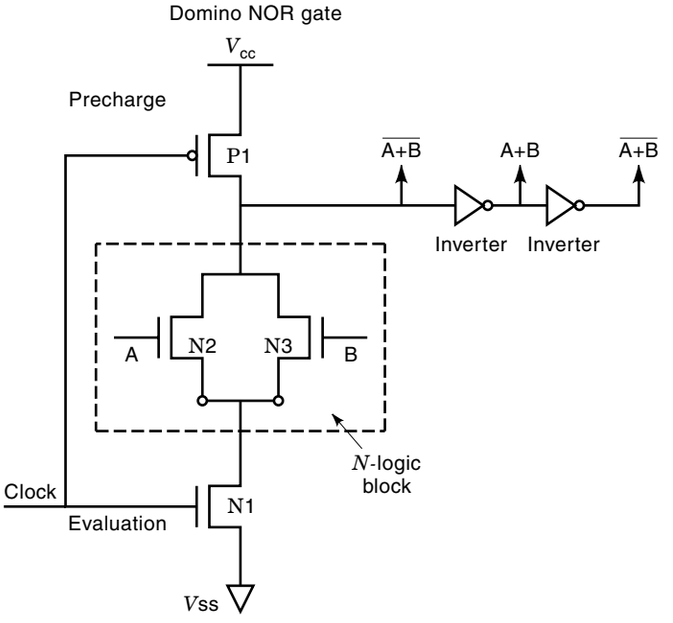

Figure 4. A domino CMOS NOR gate with two inputs is composed of a *p*-MOS transistor P1 (for precharge), an *n*-MOS transistor N1 (for evaluation), and an *N*-logic block.

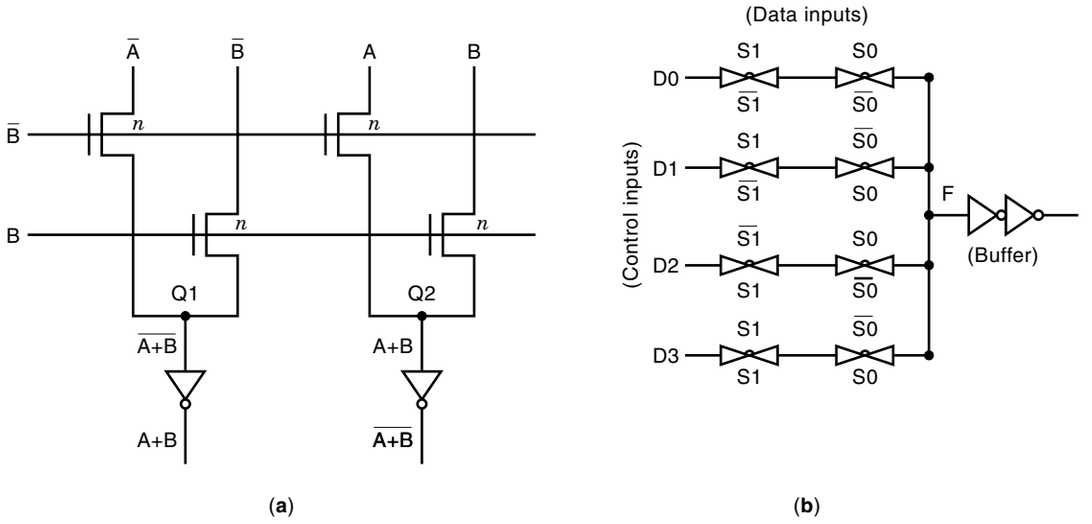

Figure 5. A logic NOR or logic OR can be realized by two n-MOS transistors as shown in (a). A multiplexer with four inputs from the drain (D0, D1, D2, and D3, used for reconfiguration) and two inputs from the gate (S0 and S1 used as data input) shown in (b) can be configured to any logic functions; for example, if D0 = 1, and D1 = D2 = D3 = 0, then the output F is the logic NOR of S0 and S1.

NOR programmable array, and NOR memory array (ROM, EPROM, and Flash memory) are described with emphasis on integrated circuits. Future trends of NOR gate devices and circuits are briefly mentioned. NAND circuits are equally useful as NOR circuits. NAND circuits are described in the article entitled NAND CIRCUITS.

NOR LOGIC GATES AND BUILDING BLOCKS

In CMOS technologies, the n-MOS and p-MOS transistors are simply electronic switches which can be turned on or off. A pair of n-MOS and p-MOS transistors can be connected in parallel to form a switch (referred to as a transmission gate),

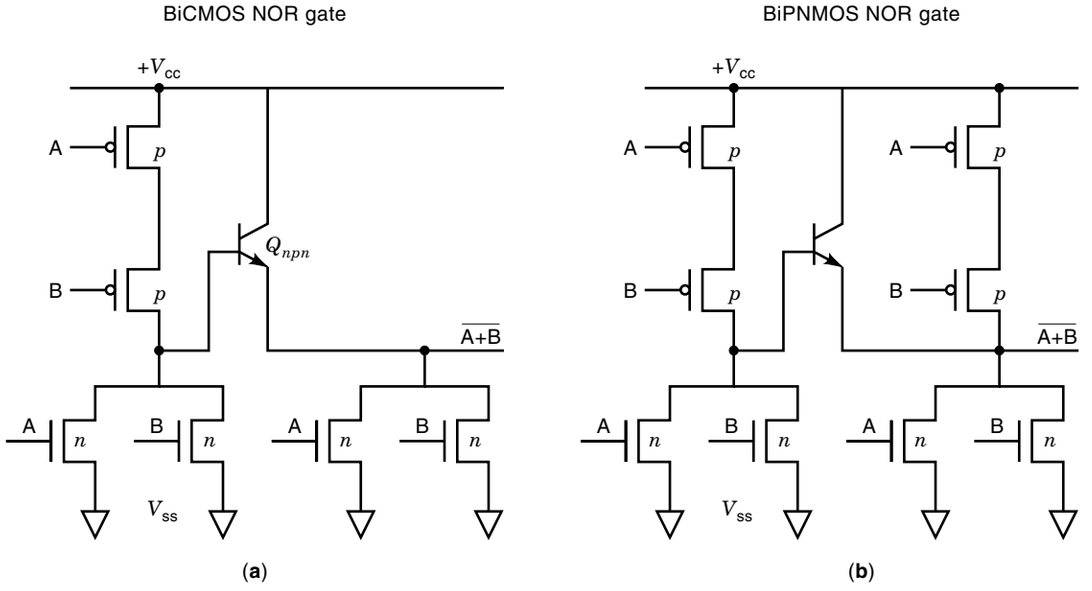

Figure 6. A BiCMOS NOR gate is shown in (a), where the npn bipolar is used as pull-up at the output stage. A BiCMOS NOR gate with p-MOS pull up at output stage as shown in (b) can restore a full V_{cc} swing at output node.

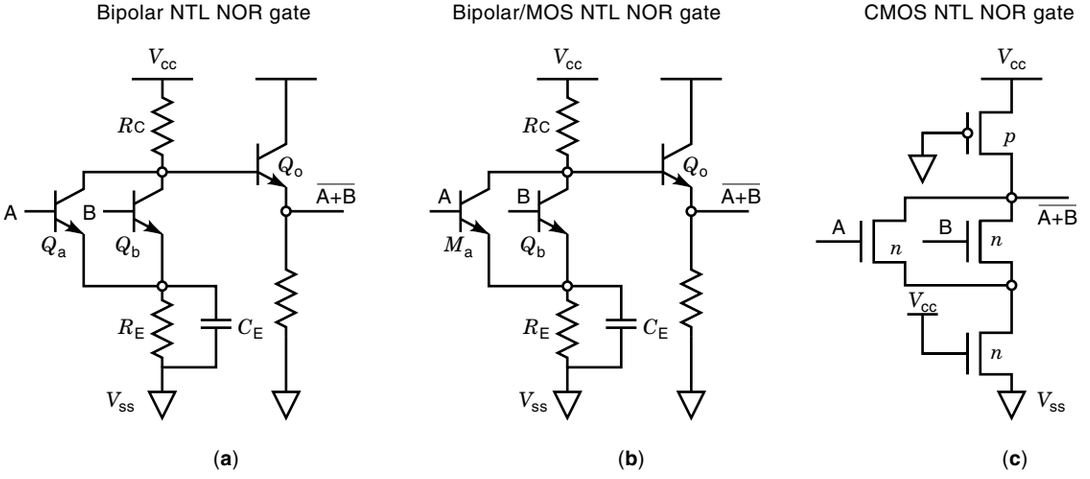

Figure 7. Nonthreshold logic gates. A NOR gate based on bipolar NTL is shown in (a). The negative feedback by R_E results in nonthreshold-like dc transfer characteristics. A hybrid MOS and bipolar input transistors as shown in (b) handles both input swing of CMOS (0 to V_{cc}) or bipolar (0 V to 0.5 V) without conversion. A NOR gate based on CMOS NTL as shown in (c) can have high speed performance but at a cost of higher power consumption than conventional CMOS gate.

as shown in Fig. 2(a), which can be turned on in a bidirectional manner regardless of the voltage polarity of the source and drain. A pair of *n*-MOS and *p*-MOS transistors can be connected in series to form an inverter as shown in Fig. 2(b). The *n*-MOS and *p*-MOS transistors and transmission gates are the basic elements forming various CMOS logic gates and circuits with several popular styles of implementation as described below. NOR gate implementations in this section are limited to 2 inputs for simplicity. High fan-in (i.e., greater than 2 inputs) NOR gates can be similarly implemented with trade-offs in output resistance and load capacitance.

NOR Gate in Static and Dynamic Logic

The static CMOS logic is the most widely used in applications. Figure 3 shows static two-input NAND and NOR logic gates as an example, where each input is connected to the gates of a pair of *n*-MOS and *p*-MOS transistors. The static CMOS logic circuits dissipate negligible static power unless the threshold voltages of *n*-MOS and *p*-MOS are too low. Static CMOS logic circuits require greater area (i.e., a pair of *n*-MOS and *p*-MOS transistors are required for each input of a logic gate) and are slower than other alternative implementations of CMOS logic circuits. Dynamic CMOS logic circuits, for example a domino logic, is an alternative implementation, where the logic circuits are activated in a dynamic manner. Figure 4 shows a domino CMOS NOR gate which is composed of a *p*-MOS P1 (for precharge), an *n*-MOS N1 (for evaluation), and an *N*-logic block. During the precharge phase (i.e., clock low), the P1 is on, and the output node is charged to V_{cc}. During the evaluation phase (i.e., clock high), P1 turns off and N1 is on, and the output node is discharged (if any one of the inputs is high and turns on N2 or N3 in the *N*-logic block) or remains at V_{cc} (if both inputs are low and, thus, both N2 and N3 are off). The output node, therefore, represents the output of NOR of the inputs, and the signal after the inverter represents the output of OR. Domino logic may also be imple-

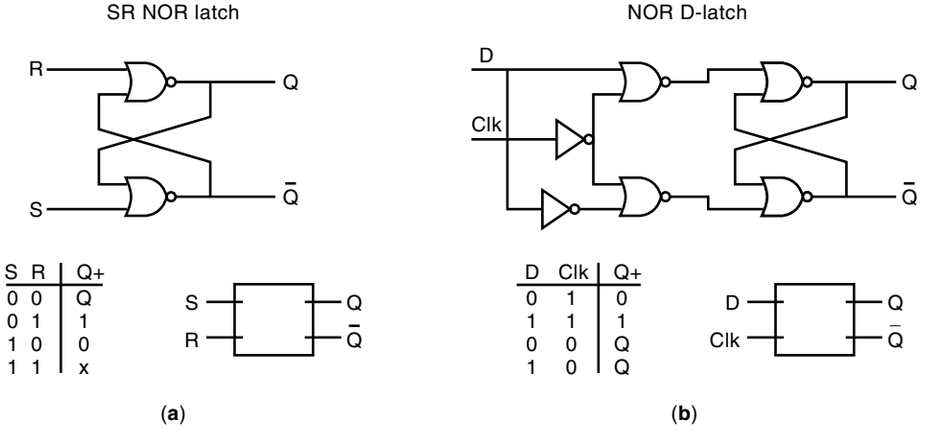

Figure 8. A pair of cross-coupled NOR gates forms a basic set-reset NOR latch in (a). NOR SR latches are often used as building blocks in practical design of flip-flops. By adding a synchronizing clock signal, as shown in (b), a NOR D-latch is formed.

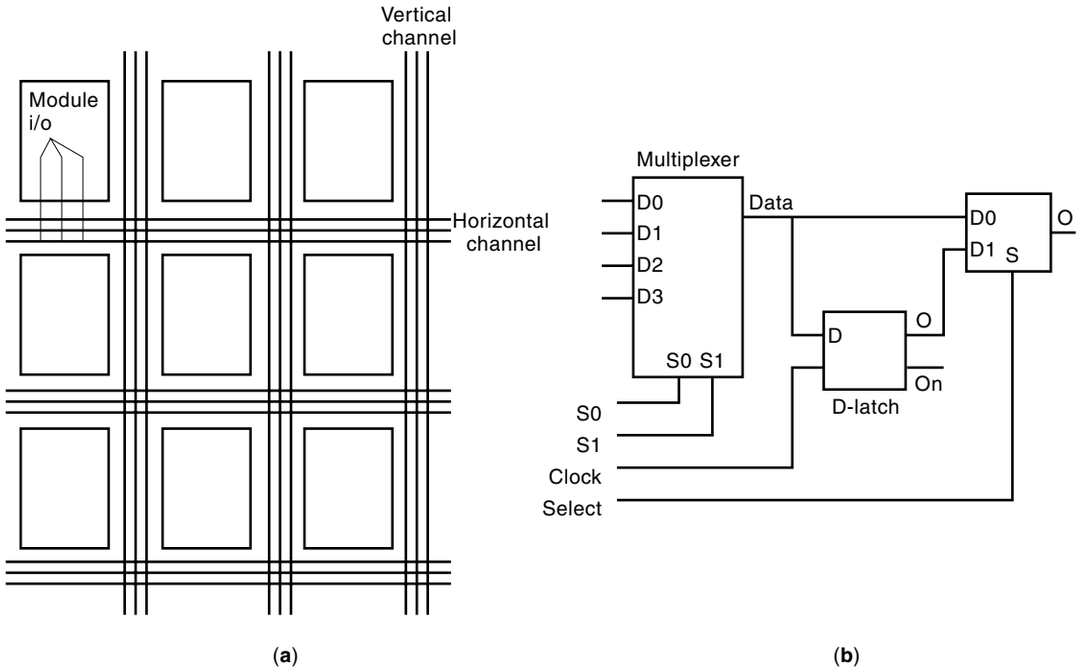

Figure 9. A general FPGA array, as shown in (a), consists of functionally complete and identical modules interconnected by programmable links in an array. The programmable links are used to interconnect modules and reconfigure the individual modules to perform any basic logic functions. One example of a module is shown in (b) with one multiplexer (with 2 inputs) and two D-latches.

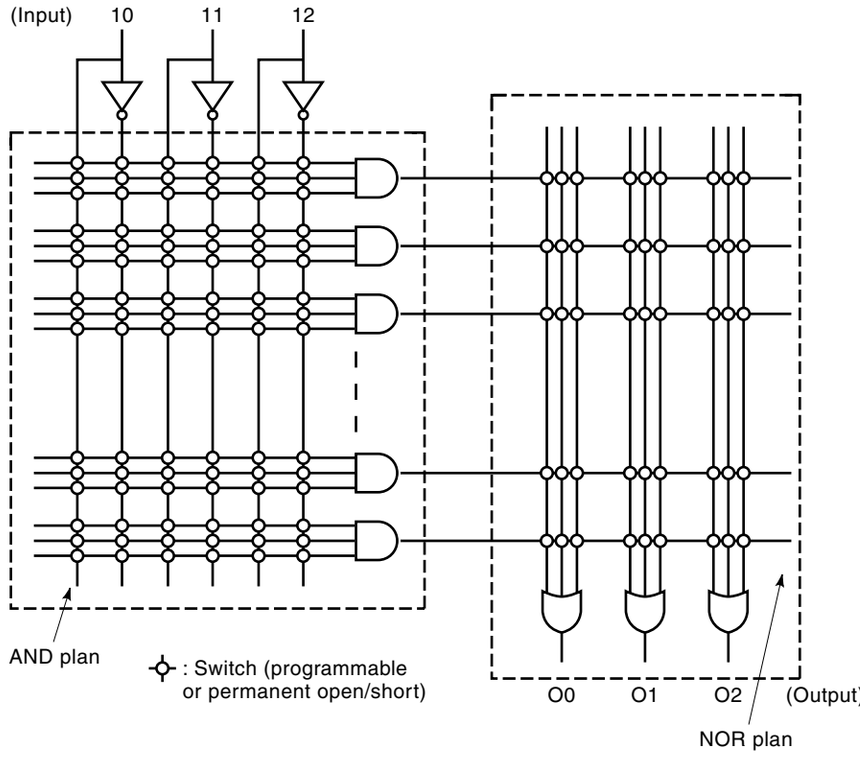

Figure 10. An AND-OR programmable logic device. The input variables are connected to AND gates through an "AND" switching array to form products of input variables, and then these products are connected to the OR gates through an "OR" switching array to form desirable outputs in terms of sum of products.

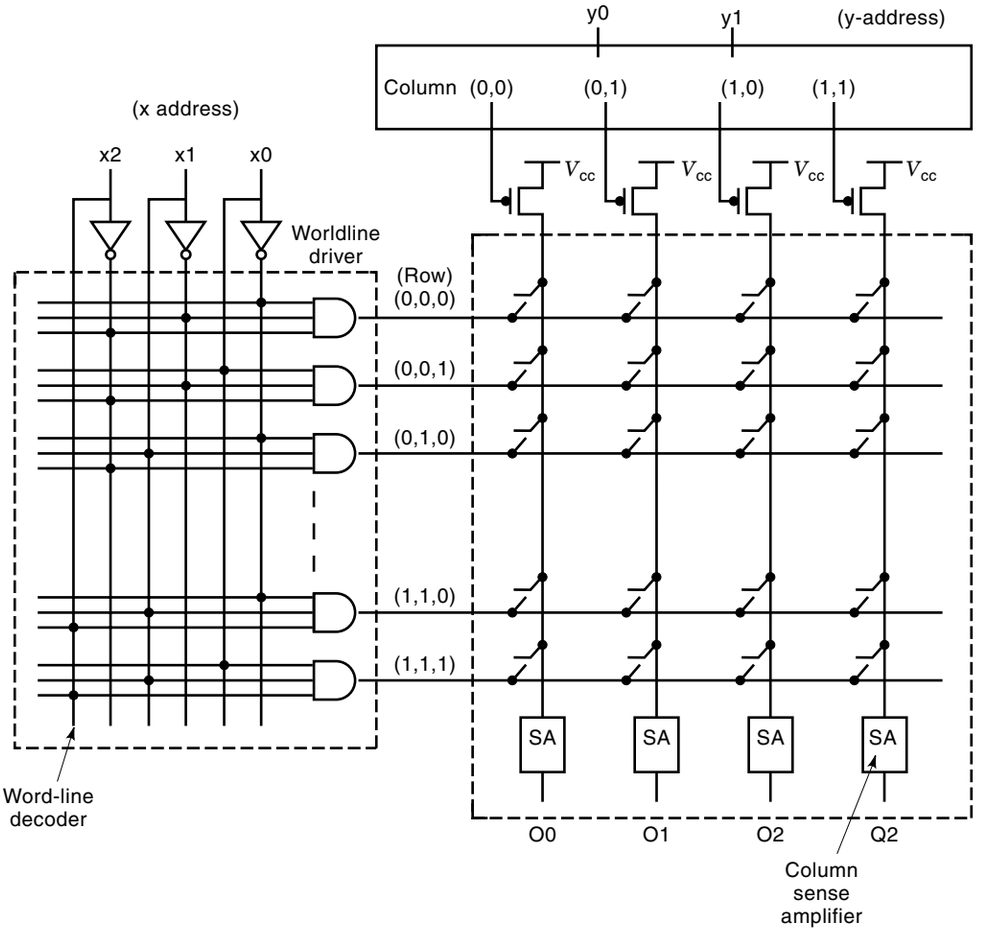

Figure 11. A NOR memory architecture is illustrated with 3 row-addresses (i.e., 8 rows) and 2 column-addresses (4 columns). The memory cells are represented by switches which can be programmed to open or short for storing the digital information of "1" or "0." Various memories are different in the actual structure of switches.

mented by using a *P*-logic block or both an *N*- and *P*-logic block in an alternating manner. In comparison to static CMOS logic circuits, the dynamic logic circuits are smaller in area and faster in speed at the cost of other performance measures (e.g., noise margin and power dissipation).

NOR Gate in Pass-Transistor Logic

Another useful implementation of CMOS logic gates is the pass-transistor logic based on MOS transistors used as switches. Both the drain and the gate of the transistor are used as inputs. Figure 5(a) shows that logic NOR or logic OR gates can be realized by two *n*-MOS transistors based on pass-transistor logic. The high value of the output at nodes Q1 and Q2 is $V_{cc} \cdot V_T$; therefore, these nodes can be connected to inverters or buffers to restore the output voltage to full swing. Figure 5(b) shows a multiplexer with four inputs from the drain (D0, D1, D2, and D3, used for reconfiguration) and two inputs from the gate (used as data input) based on transmission gates. By assigning the reconfiguration inputs, for example, if D0 = 1 and D1 = D2 = D3 = 0, then the output F is the logic NOR or S0 and S1. As another example, if D0 = 0, D1 = D2 = D3 = 1, then the output F is the logic OR. Similarly, logic AND, NAND, INVERT, and so on can be realized from the multiplexer by applying various combinations of bias to the reconfiguration inputs. Therefore, the multiplexer is also functionally complete and is very useful in a programmable logic array as discussed in more detail later in this article.

BiCMOS NOR Gate

BiCMOS logic circuits (4,5) have been widely used in high-speed digital applications, for example, in Static Random Access Memory (SRAM), digital signal processors (DSP), and so on. The BiCMOS gate is increased speed by merging bipolar transistors as a stronger pull-up or pull down at the cost of larger area and higher power dissipation than the corresponding CMOS gate. One example of a BiCMOS NOR gate (6) is shown in Fig. 6(a), where the *n*–*p*–*n* bipolar is used as a pull-up at the output stage. However, the output voltage can only swing to $V_{cc} - V_{BE}$, where V_{BE} is the base-emitter forward voltage drop. Figure 6(b) shows an improvement of a NOR gate (referred to as PBiNMOS NOR in Ref. 7) by adding

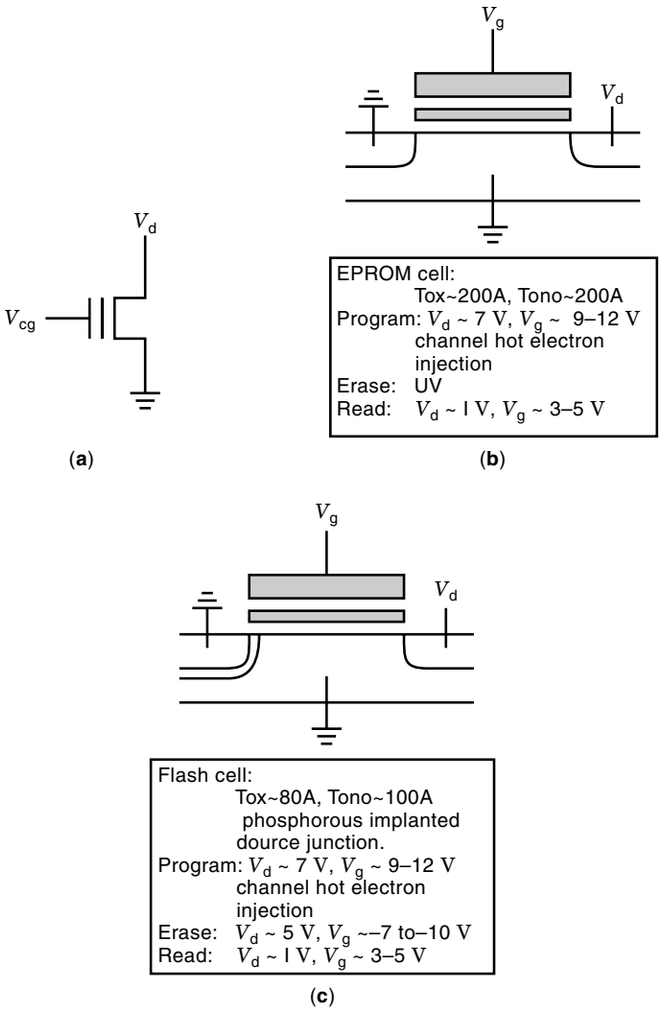

Figure 12. A notation of an n-MOS double-poly floating-gate cell is shown in (a). A sketch of an EPROM cell cross-section is shown in (b) with operation bias conditions. The memory cell of Flash memory as shown in (c) is similar to that of an EPROM cell except that the cell has thinner gate-oxide for electrical erase by a Fowler–Nordheim (FN) tunneling mechanism.

a p-MOS pull up so that a full V_{cc} swing at the output node is restored.

NOR Gate in Nonthreshold Logic

Nonthreshold logic (NTL) is attractive for its low power-delay product and is applicable to both bipolar and CMOS technologies. Figure 7(a) shows a NOR gate based on a bipolar NTL. The two resistors R_E and R_C can split the power supply voltage so that the output voltage swing is reduced. The negative feedback by R_E results in nonthreshold-like dc transfer characteristics. The shunting capacitor C_E is used to enhance the speed. Figure 7(b) shows a hybrid MOS and bipolar input transistors (8), so that the NOR gate can handle both the input swing of CMOS (0 to V_{cc}) or the bipolar (0 to 0.5 V) without conversion. Figure 7(c) shows a NOR gate based on CMOS NTL (9) with high speed performance but at a cost of higher power consumption than a conventional CMOS gate.

NOR Logic Blocks

The application of logic circuits is greatly enhanced if logic gates can be used as storage elements. Some basic flip-flops or latches for storage of one single bit (i.e., "1" or "0") are described in this section. A pair of cross-coupled NOR gates can form a basic latch (referred to as an asynchronous NOR SR latch) as shown in Fig. 8(a). When the set signal is "1," the output Q is set to "1." When the reset signal is "1," the output data are reset to "0." When both set and reset are "0," the data are latched and remain unchanged. Both set and reset signals are not allowed to be "1" simultaneously. A NOR SR latch is often used as building blocks in other practical designs of flip-flops. By adding a synchronizing clock signal, as shown in Fig. 8(b), a NOR D-latch is formed. When the clock is high, the data are latched into the D-latch output; when the clock is low, the D-latch output is not changed. Data latches are widely used in digital and mixed-signal circuits. There are many variations of flip-flop or latch design; interested readers are referred to related articles in this book. The logic circuits, including logic gates, as well as storage logic blocks can perform logic functions in a sequential manner (referred to as sequential logic), where the output data set is generated after the input data is stored. On the other hand, logic circuits including logic gates only (referred to as combinational logic circuits) can generate output data immediately (with a delay time in nanoseconds or less) from input data. Therefore, there are only two types of digital logic circuits, that is, combinational logic or sequential logic circuits.

NOR LOGIC ARRAYS

Some logic functions that may be hard to implement in random logic, such as those in the control units of VLSI microprocessors and finite-state machines, can be easily implemented using regular array structures. There are two main groups of such regular array structures for logic design, that is, the Field Programmable Gate Array (FPGA) (10,12) and Programmable Logic Devices (PLD) ().

Field Programmable Gate Array

A field programmable gate array utilizes identical modules interconnected in an array, as illustrated in Fig. 9(a). Each module is functionally complete and individually programmable to perform any basic logic function. At each intersection between the horizontal and vertical conductors is a programmable link (or switch). The programmable links are used to interconnect the modules and also to program the individual modules. One example of a module is shown in Fig. 9(b) with a two input multiplexer and two D-latches. Modules in practical design may have both combinational (e.g., multiplexers) and sequential logic gates (e.g., D-latches); or alternatively, there may be two types of modules in FPGA, one for combinational logic and one for sequential logic.

Programmable Logic Devices

The PLDs (13) are a two plane switching arrays. Figure 10 shows one typical PLD with AND-OR style, where the input variables are connected to AND gates through a switching array (i.e., AND plane) to form products of input variables, and then those products are connected to the OR gates

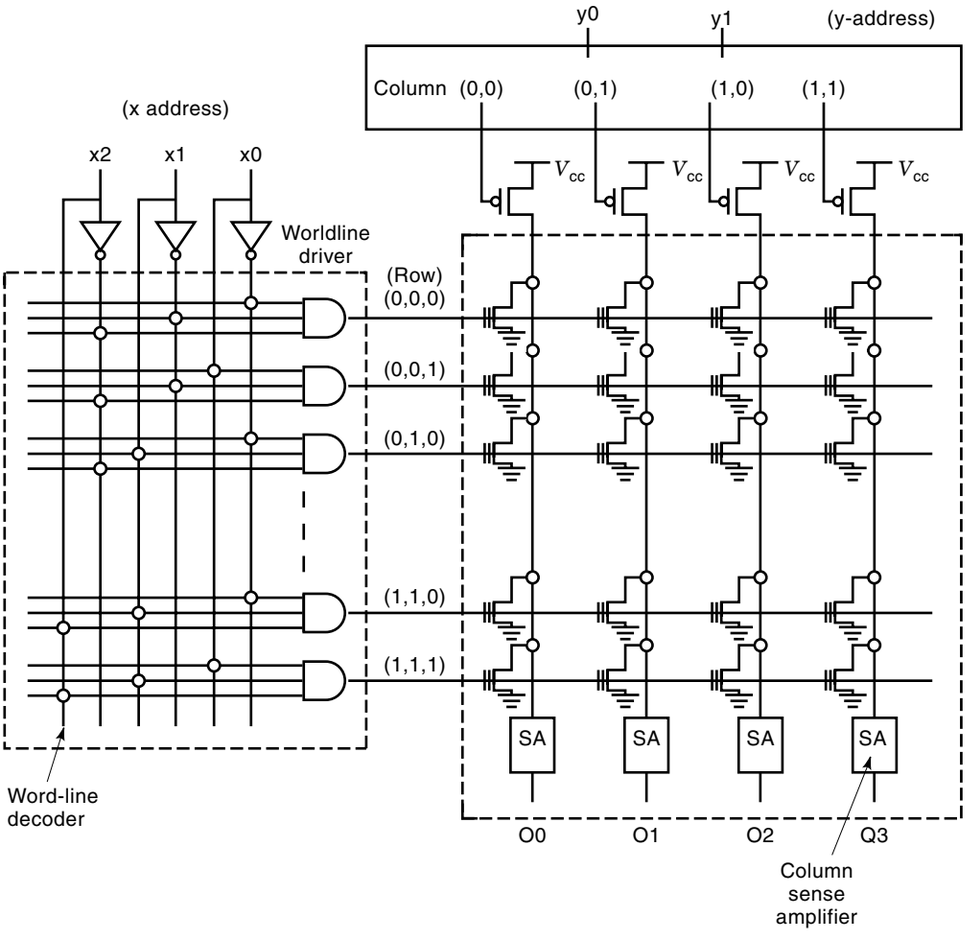

Figure 13. A simple 8 × 4 bit NOR array of EPROM or Flash memory is illustrated. Each column has a *p*-MOS transistor (as pull up) and 8 word-lines of cells connected in parallel as in a NOR gate with 8 inputs.

through a switching array (OR plane) to form desirable outputs in terms of a sum of products. The switches in the AND plane and OR plane can be either or both permanently connected or programmable as in many commercial products, for example, Programmable Logic Array (PLA) with both AND plane and OR plane programmable, Programmable Array Logic (PAL) with AND plane programmable only, and Programmable Read Only Memory (PROM) with OR plane programmable only. The AND gates and OR gates can be either static or dynamic gates. The PLDs can also have other styles, such as AND-NOR, NAND-OR, and NOR-NAND to realize logic functions based on either static gates or dynamic gates.

NOR MEMORY

The array architecture of programmable logic devices in Fig. 10 can be modified and used as nonvolatile memory (14). The information stored in nonvolatile memroy, as contrasted to dynamic memory, is in a permanent manner. The input variables can be used as x-address (i.e., row address) inputs. The AND plane as well as AND gates are used as row-address decoder and word-line driver. The OR plane is the memory array. The OR gates can be used as a column sense amplifier (SA) and selected by a y-address (i.e., column addresses) decoder. Figure 11 shows such a modified array architecture (commonly referred to as NOR array architecture) for a small memory with 3 row-addresses (i.e., 8 rows) and 2 column-addresses (4 columns) for illustration purposes. The memory cells are represented by switches in Fig. 11, which can be programmed to open or short for storing the digital information of "1" or "0." During read (or sensing), the selected word-line is biased to high by the word-line decoder, and the selected column is biased to V_{cc}; the SA output is low if the cell (i.e., switch) is open and high if short. Various memories are different in the actual structure of switches as discussed below. Today's nonvolatile memories have densities up to 64 megabits to 1 gigabit and have wide spread applications.

The memory cell has many different structures. A fuse link (fabricated by metal or poly-silicon), which can only be programmed once, is used for One-Time-Programming (OTP) memory. An *n*-MOS with floating-gate cell, as shown in Fig. 12(a), can be used for UV erased Electrically Programmable Read-Only-Memory (EPROM). Figure 12(b) shows a sketch of an EPROM cell cross-section and operation bias conditions. The EPROM cell can be programmed by channel hot electron

(CHE) injection from the high field region in the channel near the drain to the floating-gate so that the threshold-voltage (VT) of the cell is larger than V_{cc}. The digital information "1" or "0" is represented by the presence (i.e., high VT) or absence (i.e., low VT) of an electron charge on the floating-gate. The erase of an EPROM cell occurs by UV exposure. Electrons on the floating-gate become energetic after absorbing UV photons and can escape from the floating-gate. The memory cell of Flash memory as shown in Fig. 11(c) is similar to that of an EPROM cell except that the cell has thinner gate-oxide underneath the floating-gate, so that it can be electrically erased by a Fowler–Nordheim (FN) tunneling mechanism. Under the bias of erase (e.g., $V_d \sim 5$ V, $V_g \sim -10$ V), the electrons on the floating-gate are injected from the floating-gate toward the drain, so that the cell VT is lowered. The source junction is different from an EPROM cell in that it is dual implanted by both As and Phosphorous, so that the junction can sustain high voltage and reduce Gate-Induced Drain Leakage (GIDL) currents (15). Fig. 13 shows a simple 8×4 bit EPROM or Flash memory for illustration.

FUTURE LOGIC DEVICES AND CIRCUITS

CMOS devices will be continuously scaled into the nanometer regime (16) with improved device performance and lower power before running into fundamental limits of physics. A 50 nm channel length MOSFET will have a 20 A gate oxide operating at a 1 V power supply. The fabrication of such devices may have challenges in X-ray lithography, nanometer-scale inspection, and metrology tools. The clock frequencies of chips can be well into the gigahertz regime. Low-cost cooling of VLSI chips and packages are necessary.

Alternative nonMOSFET device structures (17) in nanometer regime were proposed by utilizing quantum effects of discrete charge (single- or few-electrons) interaction between semiconductor or metallic dots (~50 nm in diameter), such as the Resonant Tunneling Diode (RTD). Novel logic circuit architecture for nanometer scale device (18) is feasible in the form of a two-dimensional array of RTD. The RTDs are interconnected with each other by resistive links, and to the input and outputs by diodes at the 4-sides of the array. The RTDs inside the array collectively will have a bistable state (representing digital information "1" and "0") depending on the inputs and the connection between arrays. Each array can perform a simple logic function such as AND, OR, and so on. More details are shown in Refs. 17 and 18.

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NOTEBOOK COMPUTERS. See LAPTOP COMPUTERS.

NOTEBOOKS, ENGINEERING. See ENGINEERING NOTEBOOKS.

NUCLEAR ENERGY. See NUCLEAR ENGINEERING.