THIN FILM CAPACITORS

A capacitor, which stores electrical energy, blocks the flow of dc current, and allows the passage of ac current, consists simply of two parallel conducting electrodes separated by a dielectric material. For many applications, the capacitors need to be small in volume, lightweight, and reliable. Thin film capacitors, which offer significant advantages in size, reliability, uniformity, density, frequency, and performance, play an important role in electronic circuits. High performance thin film capacitors should exhibit low leakage, low dissipation, low temperature and voltage coefficients of capacitance, high breakdown voltage, and high capacitance per unit area.

CAPACITOR PARAMETERS

The ideal dielectric material for high-capacitance thin film capacitors should have a high dielectric constant, a low dielectric loss, a high dielectric strength (breakdown voltage), and a low dc leakage current density. The following parameters have been used to characterize the electric and dielectric properties of dielectric materials and/or capacitors.

Dielectric Constant

The dielectric constant or relative permittivity of a dielectric material determines the electrostatic energy that may be stored in that material per unit volume for a given voltage. Many insulating materials, depending on the applications, can be used as dielectric media for thin film capacitors. For most dielectric materials, the dielectric constant is a function of both temperature and frequency. One should note that some dielectric materials, such as ferroelectric materials which exhibit electric dipole moment in the absence of an external electric field, have nonlinear dielectric constant against the bias electric field. This nonlinear dielectric property of the materials can be a problem for some applications of thin film capacitors although this property can be purposely utilized for other applications such as electrically tunable microwave devices.

Capacitance per Unit Area

Geometrically, the capacitance per unit area for a thin film capacitor consisting of two parallel electrodes with common surface area A, separated by a dielectric layer of thickness t with a relative dielectric constant ϵ_r, is given by

$$C/A = \epsilon_r \epsilon_0 / t \tag{1}$$

where $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm is the permittivity of vacuum. The capacitance contribution from the edges of the dielectric film is neglected if the dielectric thickness is much smaller compared to the other dimensions of the dielectric.

From Eq. (1), one can see that two approaches can be used to increase the value of capacitance per unit area: (1) reducing the dielectric thickness, and (2) using a higher-dielectric-constant material as the dielectric. However, to maintain the reliability of the capacitors, the dielectric cannot be too thin. In other words, there is a maximum value of capacitance per unit area achievable for a given dielectric material.

Dissipation Factor

The dissipation factor of a thin film capacitor, which refers to the power losses resulting from the phase difference between the applied ac voltage and current, includes mainly the loss from the dielectric media and the loss from the leakage current of the capacitor. One model, namely, parallel in which a resistor (R_p) is connected in parallel with an ideal capacitor (C_p), is often used in circuit analysis. Series model, in which the capacitor is represented by an equivalent circuit composed of an ideal capacitor with a capacitance (C_s) and a resistor (R_s) connected in series, is also often used for circuit analysis. The dissipation factor, $\tan\delta$, is defined as the ratio of the conductance to the capacitive reactance of a capacitor and expressed as

$$\tan\delta = (2\pi f C_p R_p)^{-1} \tag{2}$$

$$\tan\delta = 2\pi f C_s R_s \tag{3}$$

for the parallel and series model, respectively. Here δ is the loss angle and f the frequency. A smaller dissipation factor gives higher performance.

In a planar thin film capacitor structure, electrode resistance contributes to the total losses of the capacitor as series resistance. Figure 1(a) shows a cross-sectional view of a generic thin film capacitor. The equivalent circuit of the thin film capacitor including both parallel and series resistance is shown in Fig. 1(b). The series resistance over here represents the combination of sheet resistance from conducting elec-

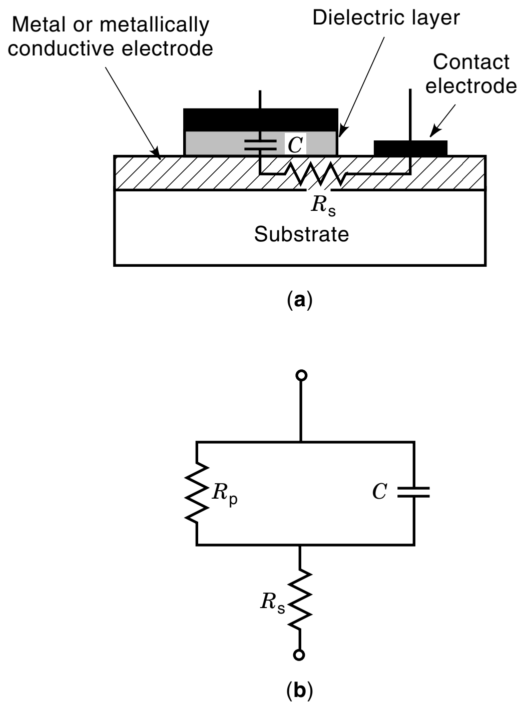

Figure 1. (a) Cross-sectional view of a generic structure of a thin film capacitor, and (b) the equivalent circuit of the thin film capacitor. A shunt resistance (R_p) is introduced when there is a dielectric leakage under bias. The series resistance (R_s) represents the combination of sheet resistance from conducting electrodes and the connection.

trodes and the connecting wiring. At high frequencies, the loss from the series resistance can be quite significant since the high frequency resistance of a conductor can be much higher than its dc resistance value. Thus, it is desirable to use highly conductive materials for electrodes in high frequency applications. It should also be noted that a large capacitance is seriously modified by series resistance as shown in Fig. 2(a). This effect can be more pronounced at high frequencies as shown in Fig. 2(b).

Dielectric Strength and Dielectric Breakdown Voltage

The dielectric strength of a thin film capacitor determines the maximum voltage that can be applied before its dielectric breakdown. The dielectric strength is expressed as

$$E_D = V_{BD}/t \tag{4}$$

where V_{BD} is the dielectric breakdown voltage. Dielectric breakdown of a capacitor results in a high current flowing though it and is a serious reliability concern. The breakdown often depends on defects in the dielectric layer instead of on the intrinsic properties of the material, since many techniques of depositing such layers produce their own characteristic defects. For example, pinholes, grain boundaries, microstructural and crystallographic imperfections, inclusions, second phases, and chemical composition inhomogeneity in the dielectric layer can all reduce the breakdown voltage. The electrode material and the interface between the electrode and the dielectric can also have some influence. For most dielectric thin films grown by physical vapor deposition techniques, the dielectric strength is around 10^6 V/cm. It should also be noted that electric breakdown is nondestructive and occurs at lower voltage. However, electric breakdown can precede destructive dielectric breakdown in dielectric materials.

Leakage Current Density

In many cases, the dielectric used for thin film capacitors is not an ideal insulating material. A small current can flow through it under an applied dc voltage. Such a current is called *leakage current.* The leakage current density, in amperes per square centimeter, is defined as the leakage current per unit area. It is often a function of the bias field, temperature, and physical geometry of the capacitor. One should be very careful in measuring the leakage current density in ferroelectric thin films in view of the relaxation processes in such materials. Similar to the dielectric strength, the leakage current density of a thin film capacitor is strongly related to the microstructural defects in the dielectrics. It should be noted that leakage current density could be heavily controlled by the Schottky barrier formed at the interface between the dielectric film and the electrode. This is often found when using high dielectric constant materials as dielectrics.

Electrical conduction or transport in dielectric films under an applied electrical field can be divided into barrier- and bulk-limited. Schottky emission and tunneling are the most important conduction mechanism for barrier-limited because it is an interface effect. On the other hand, Pool–Frenkel and intrinsic conduction are the most important bulk-limited conduction mechanisms. One can investigate the specific electri-

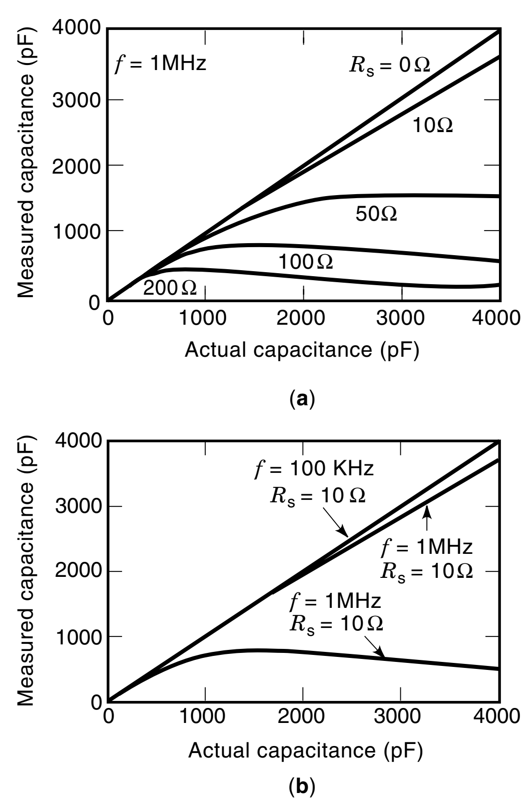

Figure 2. The relationship between the measured capacitance and the actual capacitance for thin film capacitors with different values of (a) series resistance and (b) measurement frequencies.

cal conduction mechanism of a thin dielectric film through the study of its current–voltage characteristics at different temperatures (1).

Temperature Coefficient of Capacitance

The temperature coefficient of capacitance (TCC), which is a measure of the rate at which the capacitance of a thin film capacitor varies with temperature, is expressed as

$$\text{TCC (ppm/}^\circ\text{C)} = \frac{C_2 - C_1}{C_1(T_2 - T_1)} \times 10^6 \quad (5)$$

where C_1 and C_2 are the capacitances of the capacitor at operating temperatures T_1 and T_2, respectively. For stable operation, the TCC should be as small as possible. A commercial thin film capacitor network on a silicon substrate using silicon dioxide and/or silicon dioxide–silicon nitride as a dielectric layer has a TCC around 50 ± 50 ppm/°C at operating temperatures between −55° and 150°C.

Voltage Coefficient of Capacitance

The voltage coefficient of capacitance (VCC), which is a measure of the rate at which the capacitance of a capacitor varies with bias voltage, is expressed as

$$\text{VCC (ppm/V)} = \frac{C_2 - C_1}{C_1(V_2 - V_1)} \times 10^6 \quad (6)$$

where C_1 and C_2 are the capacitances of a capacitor at operating voltages V_1 and V_2, respectively. For most applications, the VCC should be as small as possible. A commercial thin film capacitor network on silicon substrates using silicon dioxide and/or silicon dioxide–silicon nitride as a dielectric layer has a VCC less than 50 ppm/V at operating temperatures between −55° and 150°C.

THIN FILM DIELECTRIC MATERIALS

Many dielectric materials can be used for thin film capacitors. In the following, the most commonly used dielectric materials are discussed.

Low-Dielectric-Constant ($\epsilon_r < 10$) Materials

SiO_2. Silicon dioxide (SiO_2) is one of the most widely used dielectric materials in integrated circuits. It has an amorphous structure with an energy gap of 9 eV. The dielectric constant of SiO_2 is around 3.9. It has a dielectric strength of 10^7 V/cm and a dc resistivity of 10^{15} $\Omega \cdot$cm at room temperature (2). High-quality SiO_2 thin films can be grown or deposited in an extremely controllable and reproducible manner, so that they are an excellent choice for many applications. For example, SiO_2 can be used as a gate oxide for metal–oxide–semiconductor (MOS) transistors, as a surface passivation layer for devices, as an insulating material for isolating the devices, as a mask for ion implantation and/or diffusion, and as a dielectric layer for thin film capacitors. In low-density dynamic random access memory (DRAM) products, SiO_2 is mostly used for the dielectric layer in storage capacitor cells. With the development of 256-kbit and higher density DRAMs, multilayer and/or stacked SiO_2–Si_3N_4 dielectric structures are used to increase the charge capacity in order to prevent soft errors caused by alpha-rays (3), which come from the trace radioactive impurities in packaging materials and/or cosmic rays. These particles can generate carriers in semiconductor, which in turn can change the memory states.

Many deposition techniques can be used to deposit or grow SiO_2 films. Thermal oxidation of Si, either using conventional furnace or rapid thermal techniques, has resulted in the highest-quality SiO_2 films on Si with regard to low trap density. Other deposition techniques include plasma-enhanced chemical vapor deposition (PECVD), electron cyclotron resonance (ECR) CVD, photon-induced CVD, and reactive sputtering. The deposition technique, temperature, and environment can have an important influence on the dielectric and electric properties of the SiO_2 films.

Si_3N_4. Silicon nitride, Si_3N_4, is another very important dielectric material used in microelectronic devices and circuitries. It has an amorphous structure with an energy gap of 5 eV. The dielectric constant of Si_3N_4 is around 7.5. It shows a dielectric strength of 10^7 V/cm and a dc resistivity of 10^{14} $\Omega \cdot$cm at room-temperature (2).

Si_3N_4 has been used as a passivation layer for integrated circuits and as a mask for selective oxidation of silicon. Its high dielectric constant compared to SiO_2 makes it very attractive as a gate dielectric material for MOS devices and as a dielectric medium for thin film capacitors. Higher capacitance per unit area can be obtained with Si_3N_4, for the same dielectric thickness, than with SiO_2. High-quality Si_3N_4 thin films are mostly prepared by PECVD and low-pressure (LP) CVD techniques. Sputtering can be also used to deposit Si_3N_4 thin films.

SiO_2/Si_3N_4. For increased charge storage capacity in 256-kbit DRAMs, the reduction of dielectric thickness for SiO_2 has been accomplished with the use of three-dimensional structures. The required increase in storage charge density can be accomplished by using oxide–nitride–oxide sandwich dielectrics. Such a multilayer dielectric exhibits higher effective dielectric constant than SiO_2. Importantly, it also shows very good dielectric reliability. The TCC of the bilayer SiO_2–Si_3N_4 is typically in the range of 100 ppm/°C. Time-dependent dielectric breakdown data have shown that such a sandwich structure has longer lifetime than thermal SiO_2 of equivalent thickness (4).

Multilayer structures of SiO_2–Si_3N_4–SiO_2, SiO_2–Si_3N_4–native-SiO_2, SiO_2–Si_3N_4–SiON–RTN–Si_3N_4, and SiO_2–Si_3N_4–RTN–Si_3N_4 have been proposed for gate dielectrics (here RTN means rapid thermal nitridation). The structure of SiO_2–Si_3N_4–RTN–Si_3N_4 yields a lower leakage current than that of SiO_2–Si_3N_4–SiO_2. The former also shows superior time-dependent dielectric breakdown lifetime (5). A very thin SiO_2 layer is required for these multilayer structures in order to preserve the interface characteristics. SiO_2–Si_3N_4 can be used both for storage capacitor cells in DRAMs and for thin film capacitors in integrated resistor–capacitor thin film networks.

Intermediate-Dielectric-Constant ($10 < \epsilon_r < 100$) Materials

Ta_2O_5. Development of high-density DRAMs requires very thin dielectric films in three-dimensional stacked or trenched capacitors. Tantalum pentoxide (Ta_2O_5) is one of the most promising dielectrics for the next generation of DRAMs. It has an energy gap of 4 eV. The dielectric constant of Ta_2O_5 is around 20 to 35. Its dielectric loss is in the range of 0.003 in the kHz range. It has a dielectric strength of $\sim 3 \times 10^6$ V/cm at room temperature. It has a TCC of around 170 ppm/°C. Importantly, conventional semiconductor processes can prepare good quality Ta_2O_5 thin films.

Many deposition techniques can be used to deposit Ta_2O_5 thin films. The reported techniques include photo-CVD, LPCVD, metal–organic CVD (MOCVD), ECR PECVD, excimer-laser-induced CVD, reactive sputtering, pulsed laser deposition (PLD), spin coating and dip coating, and sol–gel. The most commonly used techniques are PECVD (6), LPCVD (7), and ECR PECVD (8).

It has been reported that the leakage current of Ta_2O_5 depends greatly on processing conditions and techniques. As-deposited Ta_2O_5 films tend to be leaky. The high leakage current is attributed to oxygen deficiency. A variety of postannealing techniques have been used to reduce it. During the annealing, oxygen diffuses into the Ta_2O_5 films. This process leads to the repair of oxygen vacancies, elimination of organic inclusions, and reduction of weak spots (9). A remarkable reduction in the leakage current of as-deposited Ta_2O_5 films has been demonstrated by using rapid thermal N_2O annealing. A leakage current density of 10^{-8} A/cm^2 at 3 MV/cm has been reported (10).

As dielectrics for storage capacitor cells, single layer Ta_2O_5 provides the simplest capacitor structure in use. Other capacitor structures proposed include SiO_2–Ta_2O_5–SiO_2, Si_3N_4–Ta_2O_5–SiO_2, and Ta_2O_5–SiO_2 (11). However, it should be noted that the inclusion of SiO_2 or Si_3N_4 in the capacitors will reduce the effective dielectric constant of the multilayers. One should also pay attention to the electrode materials for Ta_2O_5 capacitors, since the leakage current depends on the electrode material and varies with the annealing temperature. It has been reported that the leakage current is mainly determined by the work function of the electrode before and after low-temperature annealing (400°C). On the other hand, after high-temperature annealing (800°C), the leakage current is also affected by the reaction between Ta_2O_5 and the electrode. From the viewpoint of the leakage current, TiN and Mo (or MoN) are optimum electrode materials (12).

TiO_2. Titanium dioxide (TiO_2) is an alternative dielectric for thin film capacitors. The optical bandgap of amorphous TiO_2 films is about 3.44 eV, but increases to 3.98 eV for polycrystalline TiO_2 films (13). A bandgap as large as 4.85 eV for as-deposited TiO_2 has also been reported (14). The dielectric constant of TiO_2 films varies over a wide range from 4 to 86, depending on the processing conditions. A dielectric loss in the range of 0.003 in the kHz range can be achieved for TiO_2 thin films. The TCC of TiO_2 is typically in the range of -720 ppm/°C. A breakdown voltage of over 3×10^6 V/cm and leakage current density of 5×10^{-8} A/cm^2 at an electric field of 10^6 V/cm have been reported for TiO_2 films on Si with a film thickness of 19 nm (15).

Oxygen annealing of as-deposited TiO_2 can reduce the leakage current of TiO_2 films without decreasing the effective dielectric constant. The leakage current through the films is also related to the gate electrodes. It is especially low when Pt is used for the gate electrode. Polysilicon is found to suffer from high leakage current, particularly after subsequent thermal cycles (15).

The following deposition techniques have been used to deposit TiO_2 films on different substrates: electron-beam evaporation, LPCVD, PECVD, LP-MOCVD, reactive sputtering, and thermal oxidation of Ti. LP-MOCVD is the most-used technique and produces good TiO_2 films at relatively low processing temperatures.

High-Dielectric-Constant ($\epsilon_r > 100$) Materials

High-dielectric-constant materials such as perovskite oxides can achieve much greater capacitance per unit area at reasonable film thickness than traditonal SiO_2–Si_3N_4 or Ta_2O_5. The following discusses the electric and dielectric properties of the most promising high-dielectric-constant materials under investigation.

$SrTiO_3$. Strontium titanate ($SrTiO_3$) has an energy gap around 3.1 eV at room temperature. Its paraelectric nature at room temperature avoids the problems associated with ferroelectric materials. The dielectric constant of $SrTiO_3$ thin films is sensitive to the film thickness, the microstructure of the film, and the electrode material. The electrode materials can be Pt, Pt–Ti, Pt–Ta, TiN, RuO_2, and $SrRuO_3$. $SrTiO_3$ thin films are mostly deposited by sputtering, PLD, MOCVD, and molecular beam epitaxy (MBE).

Figure 3 shows the relationship between the dielectric constant and the electric field for various film thicknesses with different microstructures (16). The thickness dependence of the dielectric constant may be due to the resident stresses, grain size variations, dominance of surface layers at the grain boundaries with decreasing thickness, and/or the presence of a barrier layer at the electrode interfaces (17). As for the microstructure-dependent dielectric constant, the interface between the dielectric and electrode, as well as the grain boundary, may lower the dielectric constant (16). A decrease of the dielectric constant with increase of the applied field for $SrTiO_3$ thin films is observed at temperatures between 4.2 K and 300 K, and it is the strongest at the lowest temperatures. At higher bias, the measured capacitance of the $SrTiO_3$ film behaves according to $C \propto V^{-2/3}$ (18).

The dielectric loss of $SrTiO_3$ thin films is in the range of 0.01 to 0.03 at kilohertz to megahertz frequencies. Defects, stress, and oxygen deficiency in the film can all increase dielectric loss of thin films. The breakdown of a $SrTiO_3$ film is in the range of 10^5 to 10^6 V/cm, depending on the film thickness, the electrode material, and the microstructure of the films. The breakdown is most likely associated with the oxygen stoichiometry, defect density, and grain boundary structures. The leakage current of $SrTiO_3$ thin films is related to the work function of electrode materials. The current–voltage characteristics are influenced by the Schottky effect (19). Grain boundaries and oxygen deficiency in the film can also influence the leakage current.

$BaTiO_3$. Barium titanate ($BaTiO_3$) has found wide application in the electrical and electronics industries because of its very high dielectric constant. The bandgap of the $BaTiO_3$ film is about 3.9 eV. The refractive index of the $BaTiO_3$ thin films at wavelength 500 nm is 2.00, 2.07, and 2.51 for amorphous, microcrystalline, and crystalline, respectively (20). Crystal-

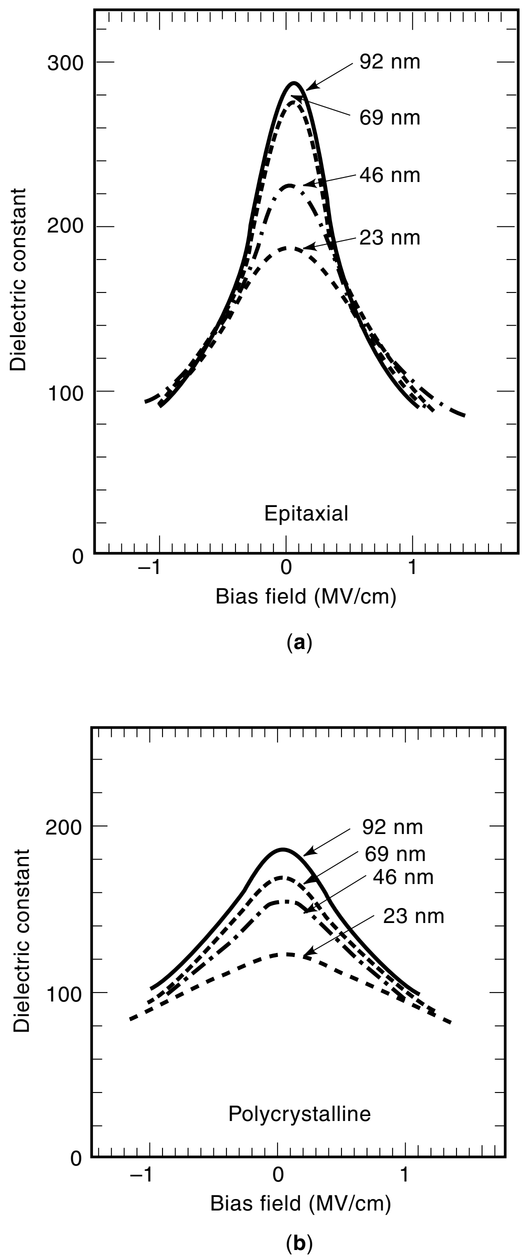

Figure 3. The dielectric-constant-versus-field characteristics for (a) epitaxially grown $SrTiO_3$ films and (b) polycrystalline $SrTiO_3$ films with various film thicknesses (from Ref. 16).

line $BaTiO_3$ shows a large anisotropy in dielectric properties. For example, the dielectric constants at room temperature along *c* and *a* axes are 160 and 4000, respectively (21).

Depending on the preparative conditions used, $BaTiO_3$ thin films are known to display a wide range of dielectric behavior. A dielectric constant as low as 12 is obtained when the $BaTiO_3$ is deposited at a substrate temperature of 23°C (22). However, a value greater than 1000 is achieved when it is deposited at a substrate temperature of 1000°C (23). The dielectric constant can be as high as 7000 if the film is deposited at a substrate temperature higher than 580°C and postannealed in air at a temperature of 1200°C for several hours (24). The value of the dielectric constant is found to be directly related to the grain size of the $BaTiO_3$ films. An amorphous film tends to have a lower dielectric constant than a polycrystalline one.

In practice, several problems have hindered the use of $BaTiO_3$ in thin film hybrid and integrated circuit applications. One of the major problems is the tendency to high electrical conductivity for high-dielectric-constant films. An increase in dielectric constant from 16 to 400 is accompanied by an increase in leakage current density from 10^{-13} A/cm^2 to 10^{-3} A/cm^2 at a bias voltage of 5 V for a dielectric thickness of near 600 nm (25).

Capacitor structures have been proposed that may retain the high dielectric constant of polycrystalline $BaTiO_3$ but also the low leakage current of amorphous $BaTiO_3$ (26,27). Figure 4 shows cross-sectional views of various capacitor structures: (a) a bilayer structure with amorphous on polycrystalline, (b) a bilayer structure with polycrystalline on microcrystalline, (c) a trilayer structure with amorphous on graded polycrystalline on polycrystalline, and (d) a nanolayer structure with amorphous on a number of stacked cycles of polycrystalline on microcrystalline layers. Capacitors with these structures hold promise for electrical and electronic applications because they provide electrical parameters such as breakdown voltage and conductivity comparable to amorphous $BaTiO_3$, but the high dielectric constant of polycrystalline $BaTiO_3$. These structures also promise the feasibility of designer control of the dielectric constant of the capacitors through the choice of each layer thickness of the multilayer thin film dielectric materials.

Compared with bulk single crystal $BaTiO_3$, thin film $BaTiO_3$ usually shows large coercive field, small remanent polarization, low dielectric constant, and a broad paraelectric–ferroelectric transition as seen from the dielectric constant measured as a function of temperature. Microstructural inhomogeneity, imperfect crystal quality, stresses imposed on the film by the substrate, grain size effects, and film orientation can all influence the dielectric and electrical properties of the $BaTiO_3$ thin films. It has been shown that $BaTiO_3$ films with

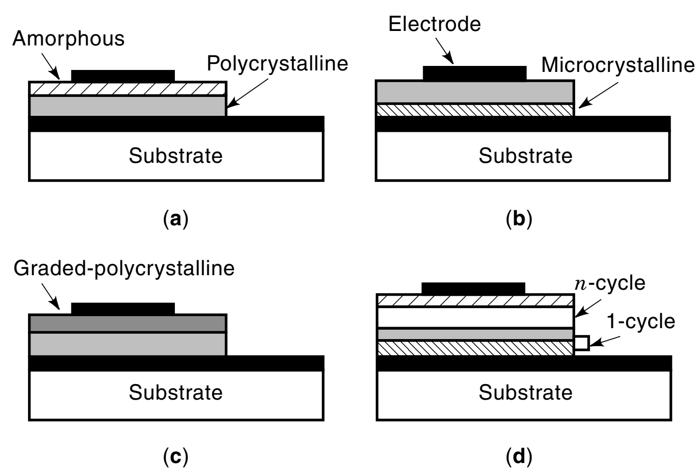

Figure 4. Cross sections of different capacitor structures: (a) bilayer structure with amorphous on polycrystalline; (b) bilayer structure with polycrystalline on microcrystalline; (c) trilayer structure with amorphous on graded polycrystalline on polycrystalline; and (d) nanolayer structure with amorphous on a number of stacked cycles of polycrystalline on microcrystalline layers (from Refs. 26 and 27).

high compressive stresses have higher refractive index and lower optical bandgap than films with low stresses. The Curie point and coercive fields are increased, while the remanent polarization is decreased with increasing compressive stress (28). By proper choice of deposition conditions, $BaTiO_3$ films having low intrinsic stresses and properties close to those of single crystals can be obtained. For example, thin film $BaTiO_3$ having refractive index 2.37 at 700 nm, bandgap 3.13 eV, remanent polarization 15.0 $\mu C/cm^2$, coercive field 10.2 kV/cm, and Curie temperature 129°C has been demonstrated (28).

More effort is needed to deposit high-quality $BaTiO_3$ on Si. The deposition of high-dielectric-constant $BaTiO_3$ thin films at temperatures above 600°C or annealed after deposition at a temperature near 1000°C can be successful as long as a good bottom electrode is used. However, the deposition of $BaTiO_3$ thin films directly on Si as gate dielectric at high temperature causes problems due to the interaction or interdiffusion between $BaTiO_3$ and Si. It has been found that the $BaTiO_3$–Si interface is not abrupt, but consists of a continuous region of varying chemical composition. The thickness of the intermediate layer between $BaTiO_3$ and Si is increased for $BaTiO_3$ films formed at higher substrate temperatures (29,30,31). It is apparent that an optimized processing condition must be developed to maintain the high dielectric constant of the $BaTiO_3$ film and to preserve the Si substrate surface. The latter becomes more important if $BaTiO_3$ is to be integrated with active devices on Si substrates. A low density of interface states or traps is one of the prerequisites for the fabrication of high-performance ferroelectric field-effect transistors (FEFETs) where a ferroelectric material is deposited on Si as the gate dielectric.

Many techniques can be used to deposit $BaTiO_3$ thin films. The most widely used techniques include reactive sputtering, reactive partially ionized beam deposition, activated reactive evaporation, PLD, MBE, photoenhanced CVD, MOCVD, plasma-enhanced MOCVD, and sol–gel. The electrodes for $BaTiO_3$ thin film capacitors can be Pt, Pd, RuO_2, $SrRuO_3$, $La_{0.5}Sr_{0.5}CoO_3$, or combinations thereof.

$Ba_{1-x}Sr_xTiO_3$. It is known that $BaTiO_3$ and $SrTiO_3$ can form solid solutions with each other at all compositions due to their similar crystal structures and the comparable ionic radii of Ba^{2+} and Sr^{2+} (32). Solid-solution quaternary $Ba_{1-x}Sr_xTiO_3$, which offers the advantages of the high dielectric constant of $BaTiO_3$ and the structural stability of $SrTiO_3$, provides superior dielectric and electric properties for thin film capacitors due to its paraelectric phase ($x < 0.7$) at room temperature and a lack of aging and fatigue effects from ferroelectric domain switching (33).

The energy gap of $Ba_{1-x}Sr_xTiO_3$ is in the range of 3.2 ± 0.1 eV. The ferroelectric to paraelectric phase transition temperature of $Ba_{1-x}Sr_xTiO_3$ can be described by the following (34):

$$T_c(^\circ C) = 131.5 - 295x \quad (7)$$

The dielectric constant is also a function of the x value, which can be varied from 0 to 1. Figure 5 shows the relationship between the dielectric constant of bulk $Ba_{1-x}Sr_xTiO_3$ and the temperature as a function of x (35).

Solid solutions of $Ba_{0.5}Sr_{0.5}TiO_3$, $Ba_{0.6}Sr_{0.4}TiO_3$, and/or bulk $Ba_{0.7}Sr_{0.3}TiO_3$ are the most widely investigated phases for thin film capacitors, since they provide not only reasonably good dielectric but also electrical properties at room temperature. For example, ceramic $Ba_{0.7}Sr_{0.3}TiO_3$ has a dielectric constant of 2510, a dielectric loss of 0.006, and an electrical resistivity of $1.45 \times 10^{10}\ \Omega \cdot cm$ (36). For thin films with the above chemical compositions, the dielectric constant at room temperature is around 200 to 600, depending on the deposition technique, the processing temperature, the film thickness, and the electrode used. Many thin film deposition techniques, such as sputtering, PLD, sol–gel, metal–organic decomposition (MOD), and MOCVD, have been used to deposit $Ba_{1-x}Sr_xTiO_3$ thin films on different substrates. The bottom electrode can be Pt, Pt/Ti, Pd, RuO_2, $YBa_2Cu_3O_{7-x}$, indium tin oxide, or $SrRuO_3$.

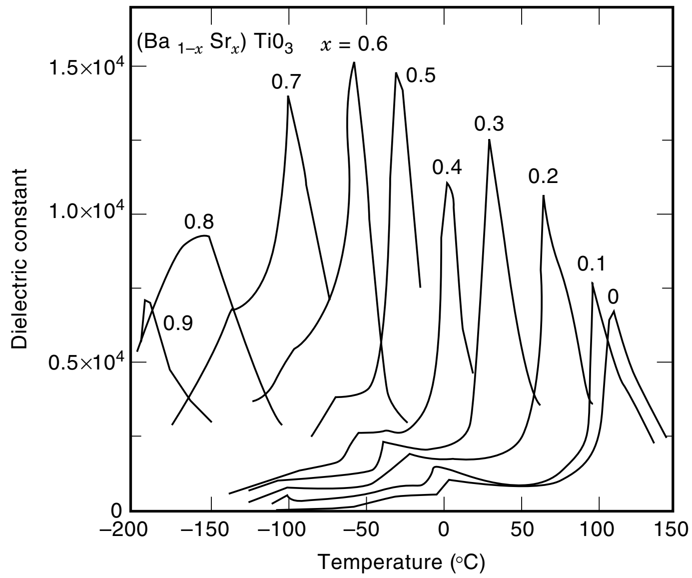

Figure 5. Relationship between the dielectric constant of $Ba_{1-x}Sr_xTiO_3$ and the temperature as a function of x (from Ref. 35).

$PbZr_xTi_{1-x}O_3$. Ferroelectric materials, such as $BaTiO_3$, $PbTiO_3$, $Bi_4Ti_3O_{12}$, $LiNbO_3$, $LiTaO_3$, $KNbO_3$, $Sr_xBa_{1-x}Nb_2O_6$, and $PbZr_xTi_{1-x}O_3$ (PZT), which have been processed as thin film forms, offer the possibility of achieving very high-capacitance thin film capacitors due to their extremely high dielectric constant. PZT, lanthanum-modified lead zirconate titanate (PLZT), and Nb-modified lead zirconate titanate (PNZT) are the most widely investigated ferroelectric thin films for nonvolatile ferroelectric RAMs. PZT provides the advantages of high remanent polarization, composition flexibility, and relatively low processing temperatures.

PZT has an energy gap in the range of 3.4 ± 0.1 eV. It has a Curie temperature of around 410°C. The dielectric constant is in the range of 200 to 1000. The remanent polarization is around 15 to 50 $\mu C/cm^2$. The coercive field is in the range of 10 to 25 kV/cm. The dielectric loss of PZT varies over a wide range from 0.1 to 0.03. As a candidate for use in nonvolatile memories, PZT has problems regarding reliability, such as *fatigue* (loss of switchable polarization of the capacitor as a result of repeated polarization reversals), *aging* (loss of switchable polarization with time or static storage), and *imprint* (the tendency for a capacitor to prefer one logic state over the other).

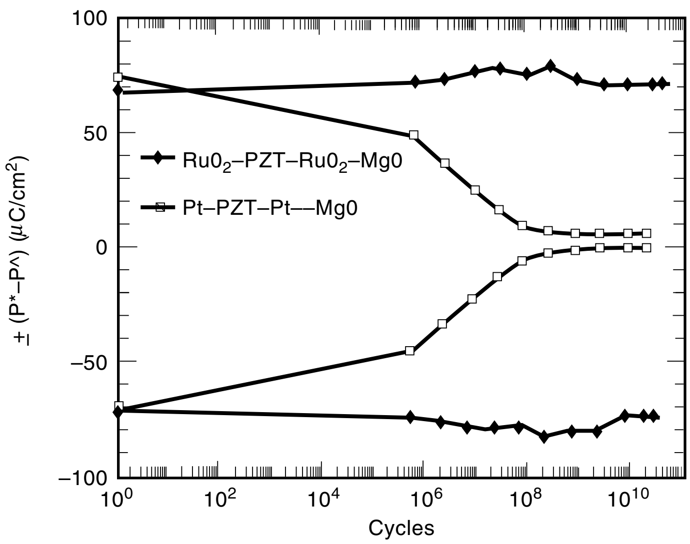

Figure 6. Fatigue curves of Pt–PZT–Pt–MgO and RuO_2–PZT–RuO_2–MgO capacitors. The fatigue tests are performed at 500 kHz on 100 $\mu m^2 \times 100$ μm^2 contacts (from Ref. 37).

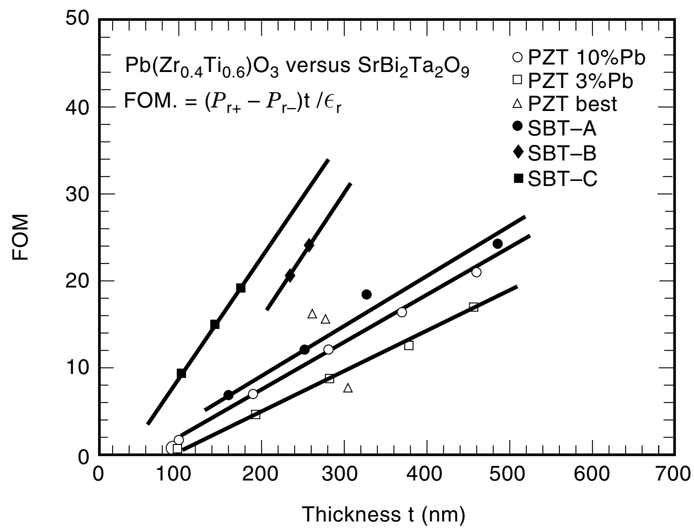

Figure 7. Figure of merit (FOM) for PZT and SBT thin films as a function of thickness. The FOM of SBT is much larger than that of PZT below 200 nm (from Ref. 43).

Fatigue-free PZT capacitors are obtained by using conductive oxide electrodes such as RuO_2, IrO_2, $La_{0.5}Sr_{0.5}CoO_3$, $YBa_2Cu_3O_{7-x}$, and $SrRuO_3$. Figure 6 shows a comparison of PZT capacitors with different electrode materials (37). Similar results have been obtained for PLZT and PNZT thin film capacitors by using $La_{0.5}Sr_{0.5}CoO_3$ as electrodes (38,39).

The most successful techniques for preparing PZT and its modified thin films are sol–gel, MOD, MOCVD, sputtering, and PLD. It should be noted that the crystal structure of the PZT films is very sensitive to the processing conditions. Thin films with a mixture of pyrochlore and perovskite structure are obtained at lower substrate temperature, say below 640°C. Films having a perovskite structure are obtained at a processing temperature above 640°C. On the other hand, very high processing temperature, say above 720°C, results in a second phase of $PbTi_3O_7$ due to the high Pb vapor pressure (40).

$SrBi_2Ta_2O_9$. A layered perovskite $SrBi_2Ta_2O_9$ (SBT) has been investigated for use in nonvolatile ferroelectric memories (41). It has an energy gap of 4.1 ± 0.1 eV and a Curie temperature of around 310°C. The dielectric constant is in the range of 100 to 600. It is not a strong function of film thickness, suggesting that the film is controlled by the bulk instead of the interface/surface. The dielectric loss is typically in the range of 0.05. Since SBT is structurally anisotropic, its ferroelectric properties are strongly dependent on the orientation of the films. The polarization and coercive field values decrease systematically with increasing degree of *c*-axis orientation. The *c*-axis-oriented films have an extremely low polarization value (≈1 $\mu C/cm^2$) and coercive field (≈22 kV/cm). The polarization vector most likely lies close to the *ab* plane (42).

Compared with PZT thin films, SBT exhibits many characteristics that are important for nonvolatile memories, such as negligible polarization fatigue when subjected to electric field cycling even with Pt electrodes, low-voltage operation, long data retention, little surface effect, superior imprint properties, and low leakage current. The main disadvantage of SBT is its small remanent polarization, about 10 $\mu C/cm^2$. However, the figure of merit (FOM), defined as $(P_{r+} - P_{r-})t/\epsilon_r$ with ϵ_r the zero-bias dielectric constant, of SBT is much larger than that of PZT at a film thickness of less than 200 nm, as shown in Fig. 7 (43).

ELECTRODE MATERIALS

The electrode material should be highly conductive, especially for high-frequency applications. It should not interact chemically with the dielectric material or form a low-permittivity compound at the interface between the dielectric layer and the electrode. In many applications, it should also not interact with the barrier layer that is in contact with the electrode. It must be stable enough at elevated processing temperature. In addition, one should consider the following in choosing the electrode materials: their work function, their ability to be patterned either by conventional chemical wet etching or dry etching methods, the stability of their surfaces, and their processing compatibility and suitability.

Metals

The elemental materials most commonly used for electrodes are Pt, Pd, Pd–Ti, Pt–Ti, and Pt–Ta (44). Pd and Pt have work functions of 5.0 eV and 5.3 eV, respectively. The typical electrode layer thickness for Pd or Pt is around 50 nm to 100 nm. The barrier (or adhesion) layer, Ti or Ta, usually has a thickness in the range of 10 nm to 50 nm. When using Pd and Pt for electrodes, the surface stability with regard to surface roughening may be a problem. For example, improper preparation of electrodes can result in Pt hillocks, which can electrically short the capacitors. These electrode materials can also deteriorate in oxygen environments at high temperatures.

Conductive Oxides

Many conductive oxides, such as $YBa_2Cu_3O_{7-x}$ (45), IrO_2 (46), RuO_2 (37), $SrRuO_3$ (47), and $La_{0.5}Sr_{0.5}CoO_3$ (38), have been studied recently as electrode materials for thin film capacitors in which ferroelectric and paraelectric materials are used as dielectrics. RuO_2, $SrRuO_3$, and $La_{0.5}Sr_{0.5}CoO_3$ are more attractive in terms of their electrical resistivity, thermal stability, processing compatibility, structural and chemical compatibility with high-dielectric-constant materials, and patterning capability. Improved electric and dielectric properties of PZT, PLZT, $BaTiO_3$, $SrTiO_3$, and $Ba_{1-x}Sr_xTiO_3$ have been observed on using RuO_2, $SrRuO_3$, and $La_{0.5}Sr_{0.5}CoO_3$ as electrodes, compared to the use of the conventional Pt. The improvement of the electric and dielectric properties of thin film capacitors achieved by using these conductive oxides as electrodes has been mostly attributed to their better structural and chemical compatibility and the cleaner interfaces (fewer charged defects) between the conductive oxides and the dielectric materials.

RuO_2. Ruthenium oxide (RuO_2), which crystallizes in tetragonal rutile structure ($a = b = 0.44902$ nm, $c = 0.31059$ nm), has a room temperature resistivity of 35 $\mu\Omega \cdot$cm for epitaxial thin films but in the range of 100 $\mu\Omega \cdot$cm for most polycrystalline thin films. The electrical and structural properties of RuO_2 can be found in Ref. 48. It exhibits excellent diffusion barrier properties, good thermal stability, and high chemical corrosion resistance. It is resistant to attack by strong acids, including aqua regia, and is thermally stable at temperatures as high as 800°C (49). The residual resistance ratio (RRR), which is a direct measure of film perfection and defined as RRR = $R_{300\,K}/R_{4.2\,K}$, of the RuO_2 thin films is in the range of 1 to 8, compared with values of 20 to 800 for bulk single crystal RuO_2.

RuO_2 thin films can be deposited by sputtering, PLD, CVD, and MOCVD. Polycrystalline RuO_2 thin films can be routinely deposited on different substrates such as Si, SiO_2–Si, MgO, quartz, and glass substrates at a temperature in the range of 500° to 575°C. For many applications, highly oriented RuO_2 is preferable. Recently, epitaxial RuO_2 thin films with a room temperature resistivity of 35 $\mu\Omega \cdot$cm and a RRR above 5 have been deposited on single crystal yittria-stabilized zirconia (YSZ), $LaAlO_3$, and YSZ–Si (50,51,52) substrates by PLD. Figure 8 shows the RRR of RuO_2 thin films on Si as a function of deposition temperatures (52).

Reactive ion etching employing CF_4 or O_2 plasma is effective in forming RuO_2 fine patterns. The etching rate of employing CF_4 or O_2 plasma is 2 to 5 times higher than that obtained by sputtering (53). RuO_2 can be also etched by reactive ion etching in O_2–CF_3CFH_2 using SiO_2 for the etch masks. The etched profiles are anisotropic and smooth. An etch rate of 160 nm/min has been achieved (54).

$SrRuO_3$. Strontium ruthenate ($SrRuO_3$), which crystallizes in the $GdFeO_3$-type orthorhombic distorted perovskite structure with lattice constants of $a = 0.5573$ nm, $b = 0.5538$ nm, and $c = 0.7856$ nm, has a room temperature resistivity in the vicinity of 280 $\mu\Omega \cdot$cm. Its thermal and chemical stability, high electrical conductivity, and structural compatibility with ferroelectric or high-dielectric-constant materials make $SrRuO_3$ very attractive as a bottom electrode for capacitors.

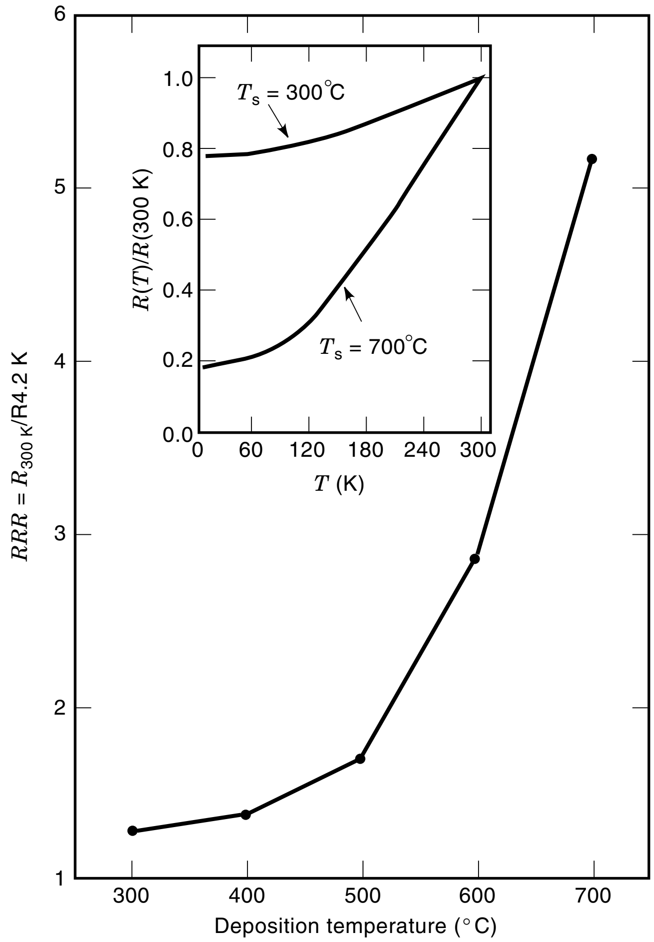

Figure 8. Residual resistance ratio of RuO_2 thin films as a function of deposition temperatures. The inset shows the typical normalized-resistance-versus-temperature characteristic of RuO_2 on YSZ-buffered Si (from Ref. 52).

Because of its extremely high thermal stability it is unaffected by dielectric thin film deposition. It has been shown that the $SrRuO_3$ surface keeps its as-deposited microstructure even after BSTO thin film deposition at 680°C (47).

Crystalline $SrRuO_3$ thin films have been successfully grown on many substrates, such as $SrTiO_3$, $LaAlO_3$, MgO with Pt or $BaTiO_3$ buffer layers, and Si with YSZ buffer layer. The $SrRuO_3$ thin films are smooth and almost particle-free. For example, epitaxial $SrRuO_3$ films (deposited at 650°C) show rms roughness less than 1 nm on a test area of either 0.1×0.1 μm^2 or 1.0×1.0 μm^2 (55). Such smooth films, deposited under optimized conditions, are extremely important for use as electrodes of high-dielectric-constant thin film capacitors, because particles can create problems in the devices, such as reduced breakdown voltage and enhanced leakage current density due to the decrease of effective dielectric thickness. Big particles can even kill the devices if they short the top and bottom electrodes.

The successfully employed deposition techniques to deposit $SrRuO_3$ are off-axis sputtering and pulsed laser deposition. The resistivity of $SrRuO_3$ is a strong function of substrate temperature during film deposition. Polycrystalline $SrRuO_3$ shows much higher resistivity than crystalline

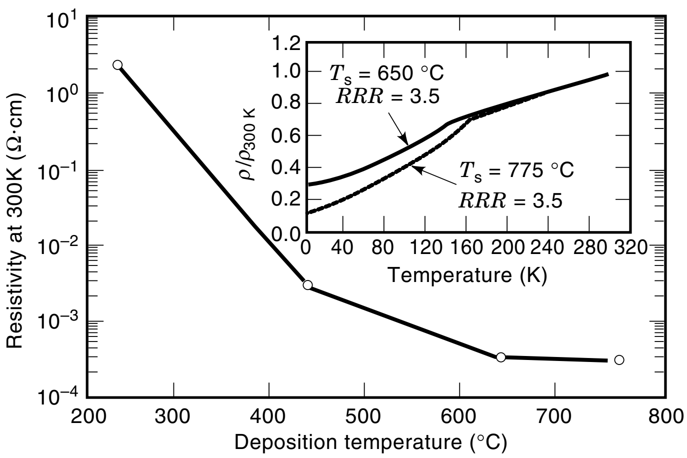

Figure 9. Room temperature resistivity of $SrRuO_3$ thin films as a function of deposition temperature. The inset shows the normalized resistivity of $SrRuO_3$ thin films deposited at 650° and 775°C, respectively, as a function of testing temperature (from Ref. 56).

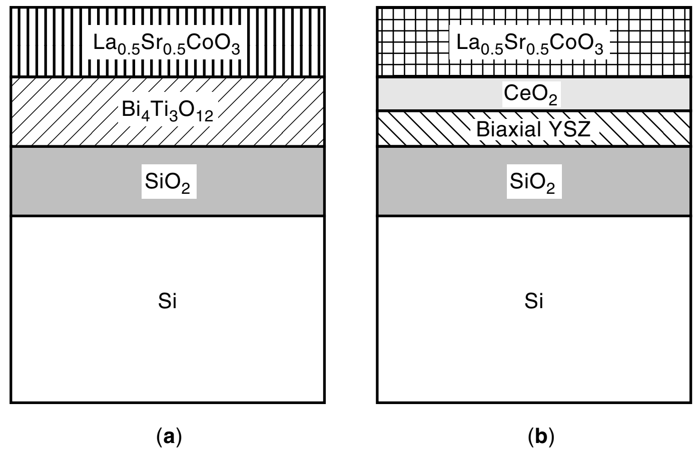

Figure 10. Schematic of the multilayer structures used to produce highly oriented $La_{0.5}Sr_{0.5}CoO_3$ on SiO_2–Si, (a) using $Bi_4Ti_3O_{12}$ as a template to produce $La_{0.5}Sr_{0.5}CoO_3$ with uniaxial normal alignment, and (b) using biaxially oriented YSZ as a seed layer to produce $La_{0.5}Sr_{0.5}CoO_3$ with alignment both normal to and in the film plane (from Refs. 38 and 58).

$SrRuO_3$. Figure 9 shows the room temperature resistivity of $SrRuO_3$ thin films as a function of deposition temperature (56).

$La_{0.5}Sr_{0.5}CoO_3$. The conductive oxide $La_{0.5}Sr_{0.5}CoO_3$, which has a psuedocubic lattice constant of 0.3835 nm and a room temperature resistivity of 90 $\mu\Omega \cdot cm$, has been extensively studied as an electrode material for ferroelectric thin film capacitors.

For applications of $La_{0.5}Sr_{0.5}CoO_3$ films as electrodes for nonvolatile ferroelectric RAMs, epitaxial and/or well-textured $La_{0.5}Sr_{0.5}CoO_3$ films are preferable. The reduced grain-boundary scattering from an epitaxial $La_{0.5}Sr_{0.5}CoO_3$ film leads to low resistivity of the film, which is a prerequisite for high-frequency applications. As a bottom electrode and/or seed layer for ferroelectric thin film capacitors, well-textured $La_{0.5}Sr_{0.5}CoO_3$ also induces epitaxial or preferential oriented growth in subsequently deposited ferroelectric films. This is important in that a highly oriented ferroelectric layer can produce a larger remanent polarization than a randomly oriented one (38,57).

Epitaxial and/or well-textured $La_{0.5}Sr_{0.5}CoO_3$ films have been grown on $SrTiO_3$, MgO, $LaAlO_3$, and YSZ. The growth of well-textured $La_{0.5}Sr_{0.5}CoO_3$ on the technically important material SiO_2–Si is more relevant in microelectronic devices, since SiO_2 is almost exclusively used as a field oxide, a passivation layer, and/or an isolation material in Si-based circuitry. Figure 10 shows the generic structures used to construct highly oriented $La_{0.5}Sr_{0.5}CoO_3$ on SiO_2–Si. By using $Bi_4Ti_3O_{12}$ as a template shown in Fig. 10(a), $La_{0.5}Sr_{0.5}CoO_3$ film with a uniaxial normal alignment is obtained (38). By using a biaxially oriented YSZ seed layer and a structural template CeO_2 as shown in Fig. 10(b), $La_{0.5}Sr_{0.5}CoO_3$ with alignment both normal to and in the film plane is obtained (58). The biaxially oriented $La_{0.5}Sr_{0.5}CoO_3$ film deposited at 700°C on SiO_2–Si shows metallic resistivity-versus-temperature characteristics and has a room-temperature resistivity of around 110 $\mu\Omega \cdot cm$.

APPLICATION OF THIN FILM CAPACITORS

Capacitors have found many applications in filtering, coupling, decoupling, tuning, bypassing, shifting, isolating, etc. Figure 11 shows the most common applications of thin film capacitors in (a) thin film resistor–capacitor network in thin film planar circuits and (b) storage capacitor cell for DRAMs in semiconductor integrated circuits.

High capacity thin film capacitors are also widely used in advanced packages, such as multichip modules where the thin film capacitors are fully integrated into the packaging architecture (59). In this case, thin film decoupling capacitors are used instead of ceramic capacitors. This allows the reduction of package volume which, in return, improves the speed of the devices. In all cases, a high capacity and a small area are preferred for today's sophisticated electronic systems.

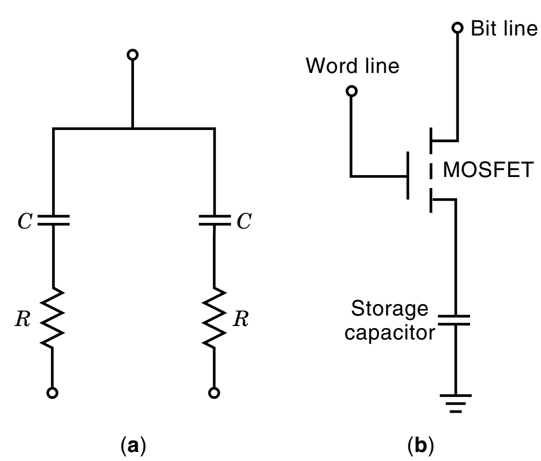

Figure 11. Applications of thin film capacitors: (a) thin film resistor–capacitor network in thin film planar circuits; (b) storage capacitor cell for DRAM devices in integrated circuits.

CONCLUDING REMARKS

The demand for high-capacitance and reliable thin film capacitors for integrated circuits and resistor–capacitor thin film networks will continue to grow. As dielectric materials, SiO_2, Si_3N_4, and SiO_2–Si_3N_4 will continue to be the widely used for low-capacitance thin film capacitors. The main candidates for a dielectric material to replace SiO_2–Si_3N_4 in the near future seem to be Ta_2O_5 and TiO_2. The potential advantages of using high-dielectric-constant materials such as $Ba_{1-x}Sr_xTiO_3$ and other ferroelectric materials as dielectrics for thin film capacitors are tremendous. However, more time and effort are needed before ferroelectric and/or paraelectric materials can be as widely used as conventional SiO_2–Si_3N_4 is today. In particular, for high-capacitance thin film capacitors using high-dielectric-constant materials, reproducible and robust processes such as CVD need to be developed in order to produce highly conformal thin films. For fabrication of very stable high-capacitance thin film capacitors, the thermal budget and stress should be also further investigated. Barrier-layer and electrode formation are also very important for processing integration to fabricate high-capacitance thin film capacitors.

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THIN FILM DEPOSITION. See SPUTTER DEPOSITION.