THIN FILM TRANSISTORS

A thin film transistor (TFT) is a three-terminal device, based on the metal–insulator–semiconductor structure, the components of which (gate insulator, semiconductor active layer, and metal contacts) are films with thicknesses normally below 1 μm, deposited on an insulating substrate. In a TFT the current flowing through the semiconductor active layer, injected by the source and drain contacts, is controlled by the potential applied to the electrode formed on the insulator, called the gate. Different device configurations have been

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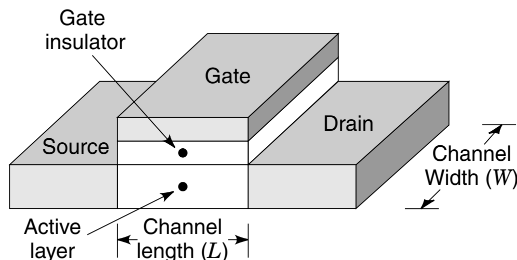

Figure 1. Schematic of the TFT structure.

used; Fig. 1 shows a basic device structure and illustrates the different components of the TFT. Normally TFTs are operated like enhancement-mode metal–oxide–semiconductor field-effect transistors (MOSFETs). When the gate voltage is low, very little current flows between the source and drain because of the high resistance of the active layer. When the gate voltage is high, charge is induced in the semiconductor active layer near the insulator–semiconductor interface, forming a conductive path (channel) between source and drain. Thus, the TFT operates as a switch controlled by the gate voltage.

The TFT was invented in 1930 by Lilienfeld (1), who proposed control of the electrical conductivity of a thin semiconducting film by modulating the semiconductor charges through a capacitively coupled metal electrode (field effect). Due to technological difficulties (poor insulator quality, control of semiconductor/insulator interfaces, and so forth) the field-effect transistor, had to wait until the work of Khang and Atalla in 1960 to be reconsidered. In 1961 Weimer described the first TFT using a vacuum-deposited thin film of CdS as the active layer. Since then a number of authors have reported on TFTs that employ different semiconductor active layers, including CdS, CdSe, and Te, and insulators. However, the development of TFTs was completely overshadowed by the rapidly growing technology of Si–SiO_2 MOSFETs. A new era for TFTs started at the end of 1970s, when in 1979 LeComber and coworkers (2) demonstrated the first hydrogenated amorphous silicon (a-Si:H) TFT and proposed its application in active-matrix liquid-crystal displays (AMLCDs). The unique characteristics of a-Si:H, to be deposited over large areas (up to 1 m^2) and at relatively low temperatures (<300°C) on cheap glass substrates, have allowed the application of a-Si:H TFTs to a new class of large-area products including an active matrix for LCDs, image sensors, and printer arrays. This new field of microelectronics is currently called large-area electronics (LAE). From the mid-1980s, due to performance limitations shown by a-Si:H TFTs (the field-effect mobility around 1 $cm^2/V \cdot s$ for n-channel transistors and very poor p-channel performances), increasing interest was devoted to low-temperature (<600°C) polycrystalline silicon (polysilicon) TFTs. Since then, dramatic development in the field of polysilicon TFT technology has followed, representing the most advanced technology for TFTs. Both n- and p-channel polysilicon TFTs can be made with field-effect mobilities exceeding 100 $cm^2/V \cdot s$, allowing circuit application of such devices. Demonstration of AMLCD with integrated driving circuitry based on polysilicon TFTs has opened new market possibilities. In the future, due to the potentialities of polysilicon TFTs to provide complex circuitry, new products based on the "system on glass" concept could be fabricated, such as an interactive portable computer.

In this article, the two main technologies for TFT fabrication, based on a-Si:H and low-temperature polysilicon active layers, will be discussed in some detail.

AMORPHOUS SILICON THIN FILM TRANSISTORS

Properties of Amorphous Silicon

The interest in amorphous silicon (a-Si) was merely academic until the introduction, in the late 1960s, of the plasma-deposition technique, in which silane (SiH_4) is decomposed by a radio frequency (RF) glow discharge. In fact, when depositing a-Si by conventional evaporation or sputtering, the material properties are very poor as a consequence of the large number of defects and microvoids.

The presence of distorted bonds as well as dangling bonds leads to localized states being energetically distributed within the semiconductor band gap. Therefore, strictly speaking, there is no longer an energy gap for the electronic states between conduction- and valence-band states in a-Si. However, due to the very low mobility of carriers occupying localized states, electric conduction in an amorphous semiconductor is primarily related to electrons and holes occupying delocalized states inside the conduction and valence bands, respectively. The energies E_c and E_v, respectively, that separate the extended from localized states in conduction and valence bond define the so-called mobility gap (see Fig. 2). The presence of a mobility gap induces classical semiconducting transport properties. The electronic properties of a-Si depend upon the density and energy distribution of the localized gap states [$N(E)$]. The density of states (DOS) determines the doping efficiency, transport properties, and recombination kinetics and, in device application, controls the potential profiles, influencing the semiconductor space charge. Figure 2 shows a schematic of the DOS for a-Si. Band tail states arise from potential fluctuations due to disorder (deviations in bond lengths and bond angles), and deep states are related to structural defects such as dangling bonds. Dangling bonds represent the main defect in a-Si and, in agreement with the Pauli exclusion principle, up to two electrons can be accommodated in each quantum level associated with the defect. This implies that dangling bonds exist in three charge states: posi-

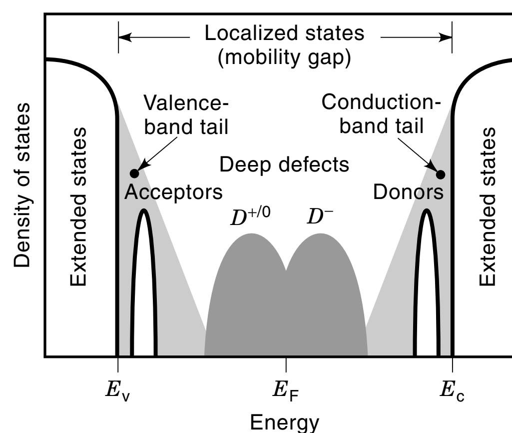

Figure 2. Schematic of the density of states in amorphous silicon.

tively charged (D^+), neutral (D^0), and negatively charged (D^-), when occupied by zero, one, and two electrons. The energies of the two electronic states, associated with the defect, are not same, due to the Coulomb interaction occurring when two electrons occupy the dangling bond. The energy levels are split by the correlation energy, which in a-Si is around 0.4 eV.

The neutral dangling bonds behave as paramagnetic centers and their density can be determined by electron spin resonance. Values in the range of 10^{19} centers/cm^3 to 10^{20} centers/cm^3 have been reported for evaporated or sputtered a-Si. The presence of such high defect densities in this material clearly inhibits any possible device application. The incorporation of H in the a-Si films, occurring, for instance, during plasma enhanced chemical vapor deposition (PECVD) or by plasma hydrogenation of evaporated or sputtered a-Si, produces a dramatic reduction of the electron spin resonance (ESR) signal. In fact, in the best quality hydrogenated a-Si (a-Si : H) films a density of paramagnetic centers below 10^{16} cm^{-3} has been measured. This can be explained by the saturation of most dangling bonds with the formation of Si–H bonds, whose bonding and antibonding states lie in the continuum of the valence and conduction bands, respectively.

Due to a number of advantages, including the possibility to deposit at low substrate temperatures (<300°C) and on large areas (up to 1 m^2), the PECVD technique is used the most to deposit a-Si : H films. Silane gas dissociation is achieved in the plasma induced by a radio frequency, usually capacitively coupled to two parallel electrodes, at low pressures (0.1 Torr to 1 Torr). The growth of films is related to the adsorption of SiH_n radicals ($n < 4$) formed in the plasma and to the release of atoms or molecules occurring at the growing surface. Although there is still some doubt about the exact deposition kinetics, the common view is that SiH_3 is the radical controlling the deposition. The best films show a dense structure, contain about 10% hydrogen, and are obtained at low deposition rates (0.1 nm/s to 1 nm/s) at a substrate temperature around 250°C and a low RF-power density (around 20 mW/cm^2). These materials have a mobility gap $E_c - E_v \sim$ 1.7 eV, a value close to the optical gap value. The thermal activation energy of dark conductivity ranges from 0.7 eV to 0.85 eV. Consequently the Fermi level (E_F) is close to the midgap (intrinsic material) and the dark resistivity is very high ($\sim$10 GΩ · cm).

Doping of a-Si : H deposited by PECVD can be obtained simply adding to the silane either phosphine (PH_3) or diborane (B_2H_6) for *n*- or *p*-type doping, respectively. Controlling the conductivity with this doping process was first demonstrated by Spear and LeComber in 1975, opening the doors to device applications of PECVD a-Si : H. Although substitutional doping is familiar to anyone working with semiconductors, this result was significant for an amorphous semiconductor. In fact, according to the principle that in an amorphous network the atoms adopt a coordination that minimizes the total energy by arranging as many electrons as possible in the bonding orbitals, both P and B are expected to be threefold coordinated and therefore not electrically active. The observed substitutional doping can be explained with the formation of pairs of fourfold-coordinated ionized impurities and compensating deep defects, such as Si dangling bonds. The pairing reduces the formation energy for a fourfold-coordinated impurity by the transfer of the electron from the impurity to the dangling bond. However, the formation energy of such pairs still remains higher than that required for the threefold-coordinated configuration and therefore only a low fraction of the incorporated dopants is in the electrically active configuration.

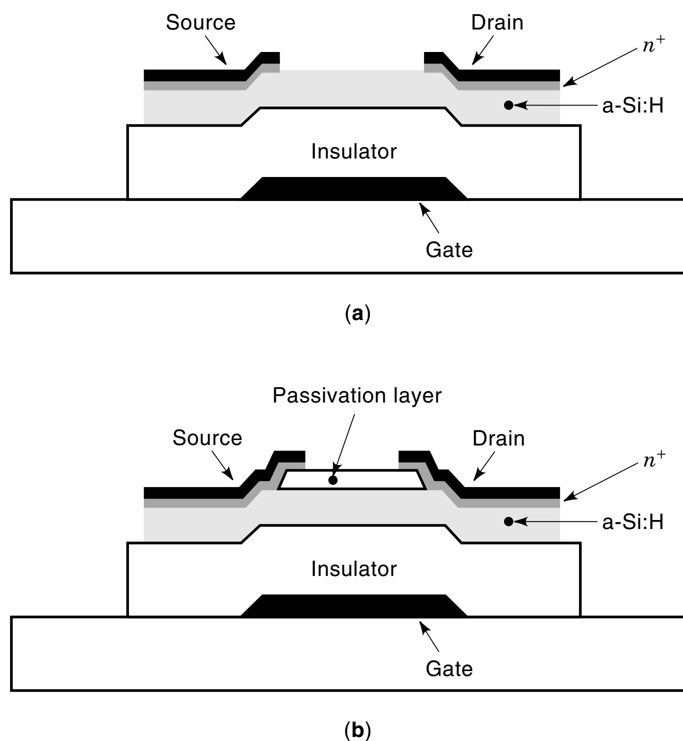

Figure 3. Schematic of inverted staggered bottom-gate a-Si : H TFTs: (a) channel-etch process, in which the channel region is defined by removing the n^+ a-Si : H from the back-channel by plasma etching; (b) channel-passivation process, in which a channel-passivation layer is deposited after a-Si : H active layer and then patterned and removed from the source/drain region before n^+-layer deposition.

The concentration of active donors (or acceptors) is observed to be proportional to the square root of the gas-phase concentration of dopant species. These considerations explain the low doping efficiency in a-Si : H, which decreases for increasing doping level. In particular, for a gas-phase concentration of 1% of PH_3, less than 1% of the incorporated P atoms are fourfold coordinated and of these active donors about 90% are compensated by the Si dangling bonds. Only about 10% of the electrons related to the remaining 10% of the active donors are in the conducting states above E_c, giving a value for the doping efficiency, measured in terms of free-electron concentration, as low as 10^{-4}. As a consequence, in these *n*-doped films the distance between the conduction-band edge, E_c, and the Fermi level is about 0.2 eV and the resistivity results quite high ($\sim$1 kΩ · cm). More details about the physical properties of a-Si : H can be found in Refs. 3 and 4.

Device Structure

In Fig. 3 the most popular device structures used for a-Si : H thin-film transistors are shown. Both types are *bottom-gate* inverted staggered transistors, that is, the gate and source/drain electrodes are on different planes of the device. The two structures differ for the step relative to the definition of the channel. According to Fig. 3(a), the device fabrication starts

with the deposition and patterning of the gate electrode. Typical gate metals used include Cr, Ta, and MoTa or MoW alloys, with resistitvity around 20 m$\Omega \cdot$cm. Then the gate insulator, the a-Si:H active layer, and the n^+ a-Si:H layer are sequentially deposited by PECVD in a single pump-down. The gate insulator is usually silicon nitride, deposited from a gas mixture of SiH_4 and NH_3, with thicknesses between 100 nm and 300 nm. However, silicon dioxide, deposited from He-diluted N_2O and SiH_4 gas mixtures, or oxynitride, deposited from NH_3, N_2O, and SiH_4 gas mixtures, have been also employed as gate insulators. The a-Si:H active-layer thickness is around 300 nm while the n^+ layer is about 50 nm thick. Finally, a metal layer (Al or Cr) is deposited to form the source/drain metal contacts.

After defining the source/drain metal, the n^+ a-Si:H is removed from the back channel by plasma etching, and for this reason the structure is often referred to as *channel-etch.* The channel-etch process is quite critical, as etching of the n^+ layer is not selective and therefore must be carefully timed. In order to allow sufficient tolerance a relatively thick a-Si:H layer is used (300 nm), with the disadvantage, however, of making the TFT relatively light sensitive.

The other structure [see Fig. 3(b)] offers in this respect a larger process window than the channel-etch, by introducing a channel passivation layer. After gate deposition and patterning, three layers, consisting of a gate insulator (a-SiN_x), an active layer (a-Si:H), and a channel-passivation layer (usually a-SiN_x), are PECVD deposited. The top passivating layer is then patterned and removed from the source/drain region with a proper selective etching technique. The n^+ a-Si:H is then deposited in a second PECVD deposition run. The *channel-passivation* process presents other disadvantages and requires an extra mask to define the channel and an extra PECVD deposition compared to the channel-etch structure. In addition, the formation of the a-Si:H/n^+ interface requires great care, due to the thin oxide and impurities that can be present between the two layers deposited in separate growth runs.

Devices with the *top-gate* inverted staggered configuration, where the layer deposition sequence is inverted compared with bottom-gate structure, have been also fabricated. These devices, due to a high defect density at the a-S:H/a-SiN_x interface when growing a-SiN_x on top of a-Si:H, show worse performance than the bottom-gate structure.

Furthermore, p-channel transistors, obtained by using p^+-doped layers as source–drain contacts, show very low field-effect mobilities, the hole-band mobility in a-Si:H being nearly 2 orders of magnitude lower than the electron-band mobility. As a consequence p-channel transistors have no practical use, preventing any complementary MOS (CMOS) technology based on a-Si:H TFTs.

Field Effect in Amorphous Semiconductor TFTs

To analyze the field-effect in a-Si:H TFTs, we can refer to the band diagram in Fig. 4, which describes the band-energy variation for positive gate voltage along the direction normal to the gate oxide. The band bending $\psi(x)$ is defined as $\psi(x) = [E_c(\infty) - E_c(x)]/q$, where $E_c(x)$ is the conduction-band edge in the space-charge region, assuming $E_c(\infty)$ in the neutral bulk, and ψ_s is the bond bending at the semiconductor/insulator interface, defined as $\psi_s = \psi(x = 0)$.

In the analyses of the field effect, it must be considered that, in the case of amorphous silicon TFTs, the active layer is usually undoped and the induced charge in the semiconductor is composed of free carriers and charged localized states (see the grey area in Fig. 4).

To find the band-bending profile in the surface space-charge layer of the amorphous semiconductor, Poisson's equation must be solved:

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{1}$$

where ϵ_s is the semiconductor dielectric constant, with the condition

$$\psi_s = (V_g - V_{fb}) - \frac{d_i}{\epsilon_i}(\epsilon_s F_s - Q_s) \tag{2}$$

where V_g is the gate voltage, F_s is the surface electric field, V_{fb} is the flat-band voltage, ϵ_i and d_i are the insulator dielectric constant and thickness, respectively, and Q_s is the interface charge density.

For an amorphous semiconductors the charge density $\rho(x)$ can be expressed as a function of $\psi(x)$, as the sum of trapped charge in localized states and free carrier density $\rho_{free}(\psi(x))$:

$$\rho(\psi(x)) = -q\int_{E_v}^{E_c} N(E)[f(E, E_F + q\psi(x)) - f(E, E_F)]\,dE + \rho_{free}(\psi(x)) \tag{3}$$

where $f(E, E_F)$ is the Fermi–Dirac distribution function

$$f(E, E_F) = \left[1 + \exp\left(\frac{E - E_F}{kT}\right)\right]^{-1} \tag{4}$$

where E_F denotes the position of the Fermi energy in the neutral bulk.

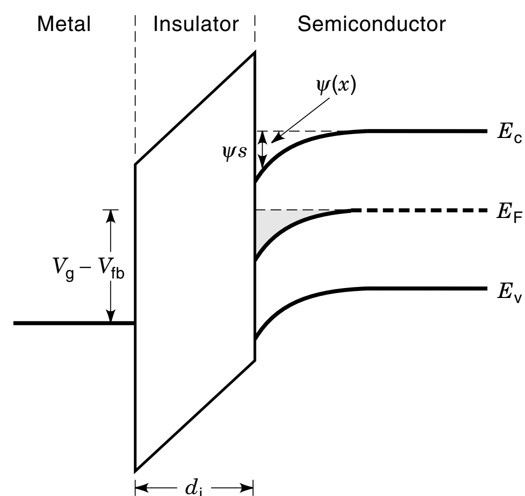

Figure 4. Band diagram for a metal/insulator/a-Si:H structure in the direction orthogonal to the semiconductor/insulator interface. The positive gate voltage V_g induces a charge of C_iV_g in a-Si:H, which is mainly localized in deep-state defects (grey area).

In the calculation of induced charge, a good approximation is to neglect the contribution of free carrier. In fact, due to the high defect density near the conduction and valence bands, surface band bending ψ_s in a-Si : H TFTs is not usually higher than 0.5 eV to 0.6 eV and, for these ψ_s values the trapped charge density exceeds the free-carrier density more than one order of magnitude (5).

Assuming a spatially uniform $N(E)$, Poisson's equation can be simplified by a transformation of the independent variable from x to ψ:

$$\left(\frac{d\psi}{dx}\right)^2 = F^2 = \frac{2}{\epsilon_s}\int_0^{\psi} \rho(\psi')\,d\psi' \tag{5}$$

where it has been assumed that $\psi = 0$ far into the semiconductor bulk. This form can be used to relate the surface electric field F_s to the surface band bending ψ_s when these quantities are changed through the application of a gate voltage V_g.

Finally the potential profile $\psi(x)$ can be found by considering

$$x = -\int_{\psi_s}^{\psi} \frac{d\psi'}{F(\psi')} \tag{6}$$

Once the band bending is known, the sheet conductance can be calculated from the relation

$$\frac{G - G_0}{G_0} = \frac{1}{d_s}\int_0^{\psi_s} \frac{\exp\left(\dfrac{q\psi}{kT}\right) - 1}{F_s}\,d\psi \tag{7}$$

where G_0 is the flat-band sheet conductance and d_s is the active layer thickness.

In the case of an exponential distribution of the localized state density in the upper half of the gap:

$$N(E) = N_0 \exp\left(\frac{E - E_c}{kT_0}\right) \tag{8}$$

where N_0 is the density of gap states at the conduction-band edge and kT_0 is the characteristic energy of the exponential band tail, the following analytical expression for the sheet conductance can be evaluated (6):

$$G - G_0 = K_0(V_g - V_{fb})^{(2T_0/T-1)} \tag{9}$$

where K_0 is constant for fixed temperature and depends on the DOS parameters (6). This simple expression can be quite useful when analyzing transfer characteristics in a-Si : H TFTs. From the sheet conductance the drain current I_d can be evaluated, in a fashion similar to the case of crystalline devices, by using the gradual channel approximation:

$$I_d = \frac{W}{L}\int_{V_d}^{0} G(V_g - V)\,dV \tag{10}$$

For small values of source–drain voltage, V_{ds}, this relation is approximated by

$$I_d = \frac{W}{l}G\left(V_g - \frac{V_{ds}}{2}\right)V_{ds} \tag{11}$$

while for $V_{ds} > V_g - V_{th}$, where V_{th} is the threshold voltage, the current is independent of V_{ds} because the contribution to the integral of $G(V_g - V)$ for $V > V_g - V_{th}$ is negligible. This saturated current is given by

$$I_{dsat} = \frac{W}{l}C_i\frac{\mu_{FE}}{2}(V_g - V_{th})^2 \tag{12}$$

where C_i is the gate oxide capacitance per unit area and μ_{FE} is the field-effect mobility. From the analysis just described, once the sheet conductance is experimentally measured, the density of localized states can be evaluated. The field-effect method was the first applied to determine $N(E)$ in amorphous silicon, and several authors have presented refined analyses (7,8). To understand the basic procedure, a low-temperature approximation can be considered. Thus the induced charge is given by

$$\rho(\psi) = -q\int_{E_F}^{E_F+q\psi} N(E)\,dE \tag{13}$$

and the density of states can be directly expressed by the following simplified expression:

$$N(E_F + q\psi_s) = \frac{\epsilon_s}{2}\frac{d^2}{d(q\psi_s)}(F_s^2) \tag{14}$$

It should be pointed out that the field-effect analysis requires the independent determination of V_{fb} to obtain the G_0 value.

Typical $N(E)$ calculated by the field-effect method appears to be U-shaped with a deep minimum (10^{16} states/cm$^3 \cdot$ eV to 10^{17} states/cm$^3 \cdot$ eV) near midgap with rapidly rising band tails. However, even in the more sophisticated field-effect analyses a number of assumptions are required, for example, a uniform density of states throughout the amorphous semiconductor layer. Field-effect methods provide a tool for routine determination of material quality in a-Si : H TFTs, retaining a reasonable degree of accuracy.

Electrical Characteristics

Figures 5 and 6 show typical output and transfer characteristics of amorphous silicon TFTs. The output characteristics show good saturation, although for small channel lengths (<3 μm) finite output resistances in the saturation region have

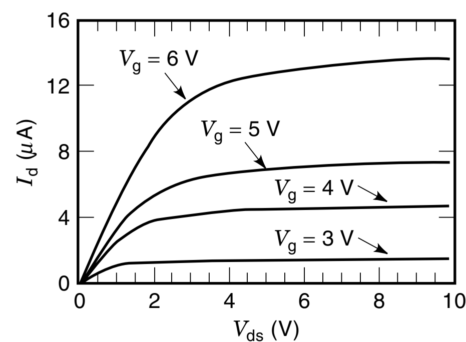

Figure 5. Output characteristics of a-Si : H TFT with $L = 10$ μm and $W = 200$ μm and with a 180 nm thick PECVD-deposited gate oxide.

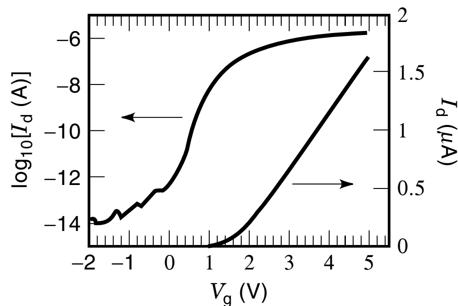

Figure 6. Transfer characteristics of a-Si : H TFT with $L = 20$ μm and $W = 200$ μm, measured at $V_{ds} = 0.5$ V, with a 180 nm thick PECVD-deposited gate oxide. The on/off ratio exceeds 7 orders of magnitude and from the linear region $V_{th} = 1.8$ V and $\mu_{FE} = 0.5$ $cm^2/V \cdot s$ can be evaluated.

been reported, related to space-charge-limited current effects in the pinch-off region near drain contact.

For transfer characteristics three different regions can be distinguished.

For $V_g < V_{fb}$ the devices are in an off condition and currents less than 1 pA flow in the channel. This low off-current level is a key characteristic for application of devices such as switching elements, for example, in AMLCDs.

For $V_{fb} < V_g < V_{th}$ an approximately exponential increase of I_d is observed. The exponential slope is related to the localized state density $N(E)$ in the gap. Material with low defect densities produces higher subthreshold slopes and, as a consequence, lower threshold voltages. In fact V_{th} can be expressed by

$$V_{th} = V_{fb} + f(N(E)) \tag{15}$$

where $f(N(E))$ is an opportune function of $N(E)$.

For $V_g > V_{th}$ and low V_{ds}, as in the case of crystalline silicon devices, a reasonably well-defined linear region can be observed, which allows one to define the threshold voltage (as the intercept of a linear fit for $I_d = 0$) and the field-effect mobility $\mu_{FE} = (d_i L)/(\epsilon V_{ds} W) S_l$, where S_l is the slope of the linear fit.

The evaluation of real μ_{FE} can be precluded by the influence of the contact series resistance that, reducing the I_d, results in a lower field-effect mobility (9). The reduction becomes more important for short-channel-length TFTs, and by fitting the experimental μ_{FE} as a function of channel length, the following relation has been verified:

$$\mu^*_{FE} = \mu_{FE} \frac{L}{L + \delta L} \tag{16}$$

where μ_{FE} is the intrinsic mobility and $L + \delta L$ is the effective channel length. To study the intrinsic performance of TFTs, excluding the contact contribution, a gated four-probe (GPB) structure has been used (9). In this device two narrow probes are placed between the source and drain electrodes to sense the voltage difference along the conducting channel. This structure allows one to measure to intrinsic characteristics such as μ_{FE} and V_{th} without the influence of source/drain series resistance.

Typical values of μ_{FE} are in the range of 0.5 $cm^2/V \cdot s$ to 1.5 $cm^2/V \cdot s$, much lower values than electron band mobility, due to the high localized state density in the gap. In fact, it can be shown (5) that $\mu_{FE} = n_{free}/(n_{loc} + n_{free})\ \mu_e$, where n_{loc} and n_{free} are the charge densities in the localized states and the free-carrier density, respectively, and μ_e is the electron band mobility. Considering that a good estimate for μ_e is 10 $cm^2/V \cdot s$ to 20 $cm^2/V \cdot s$ and that $n_{free} \approx 0.1 n_{loc}$ in the on regime, the field-effect mobilities reported are close to the maximum that can be achieved in such devices.

This limits a-Si : H TFTs to low-frequency applications only. In fact, the maximum operating frequency f_m for a device is given by

$$f_m = \frac{\mu_{FE}(V_g - V_{th})}{2\pi L^2} \tag{17}$$

in the saturation regime.

In principle, to increase the operation speed the channel length of the device can be reduced, and short-channel TFTs with different geometries have been proposed. In Fig. 7 the output characteristics of a TFT with $L = 0.2$ μm are shown (10). For this particular device $f_m \cong 250$ MHz has been evaluated. However, it can be seen that, at high V_{ds} an anomalous increase of I_d is observed. A similar avalanche current has been already observed in silicon-on-insulator (SOI) MOSFETs and in polycrystalline silicon (poly-Si) TFTs. Numerical analyses (11) show that in short-channel a-Si : H TFTs, when operated at high drain voltages, high electric fields are formed near the drain junction that induce impact ionization with an increase of the current until an avalanche breakdown of device occurs.

Instability Mechanisms

A phenomenon commonly observed in amorphous silicon TFTs is a slow drift of the threshold voltage when operated in the dc mode at relatively low gate voltages (see Fig. 8). Several studies (12–14) have been carried out on a-Si : H TFTs, both n and p channels, with different gate dielectrics. Although there are discrepancies among the different reported results, the main common features can be summarized as follows. The effect of positive bias stress on n-channel TFTs

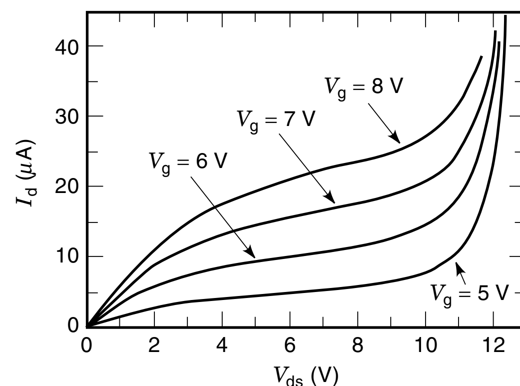

Figure 7. Output characteristics of a short-channel ($L = 200$ nm) a-Si : H TFT, made by direct writing electron-beam lithography (10). An anomalous current increase induced by impact ionization near the drain region is evident at high drain voltages.

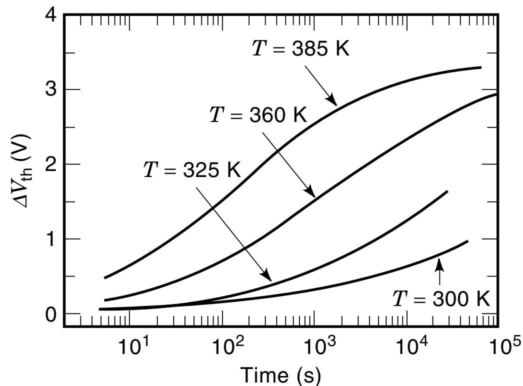

Figure 8. Threshold voltage variation ΔV_{th} versus time for a fixed stress voltage (4 V) at different temperatures for the devices shown in Fig. 6.

is to shift the transfer characteristics rigidly towards higher V_g, while negative bias stresses reduce V_{th} but, as the gate bias value increases in modulus, a progressive degradation of subthreshold slope appears. The behavior of p-channel transistors is the opposite: indeed positive bias stresses decrease V_{th} while moderate negative bias stresses increase it.

Two main mechanisms have been considered to explain this instability: charge injection into the gate insulator (13,14) and creation of metastable defects (12). Bias-stress experiments performed on both n-channel and p-channel devices with the same a-Si : H active layer and gate insulator or on ambipolar TFTs could, in principle, help distinguish between the two different mechanisms. In fact, charge trapping produces a rigid shift of electrical characteristics, while defect creation changes both V_{th} and subthreshold slope, depending on the energy of new localized states. In practice, p-channel devices have been shown to be critically dependent upon parasitic resistance effects, which can modify the results of bias-stress experiments (15).

The microscopic origin of the localized state creation mechanism has been related to the charge-induced breaking of Si–Si strained or weak bonds that form two dangling bonds. These two dangling bonds are prevented from recombining by a hydrogen atom that moves in to passivate one of the two dangling-bond defects. The result is a negligible decrease in the density of states near the conduction or valence band and an increase in the density of deep states. The model is consistent with a stretched exponential form for the V_{th} variation with time, shown by experimental data:

$$\Delta V_{\text{th}}(t) = \Delta V_0 \left\{ 1 - \exp\left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right\} \tag{18}$$

where t is the bias-stressing time and the characteristic time τ and the β parameter are related to the dispersive hydrogen diffusion. The energy location of the new defects has been described in terms of the concept of the defect pool model for dangling bonds in a-Si : H (12). According to this model, the density-of-state distribution in the energy gap for an equilibrated material depends on the Fermi energy position during equilibration. In particular, if E_F is closer to E_c as a result of applied positive gate voltage, dangling bonds will be formed deep in the energy gap, but if E_F is moved toward E_v, dangling bonds will be formed at higher energy, according to the experimental results for positive and negative bias stress on n-channel devices. The equilibration of the DOS is supposed to be related to the diffusive hydrogen motion. In addition, gate dielectrics influence the density of states of the active layer as the different fixed charge in the insulator results in a different Fermi level during a-Si : H deposition. This explains the different behavior after bias stress that is sometimes observed for TFTs with silicon nitride or silicon dioxide as the gate dielectric (12).

In contrast to the previous model, the threshold voltage shift could be interpreted to be the result of charge injection from the a-Si : H channel into traps located at the a-Si : H/insulator interface and in the gate insulator near the interface. In particular, a transitional region near the semiconductor/insulator interface is characterized by a higher density of energetically distributed localized states as compared to the bulk insulator. When a positive bias is applied to the gate electrode, the electron stored in the space-charge region of a-Si : H and residing in the gap states can relax into the empty states present in the transitional region and located at lower energy, via hopping through localized states. This process yields a V_{th} variation with time (13):

$$\Delta V_{\text{th}}(t) = (V_{\text{g}} - V_{\text{fb}}) \left(1 - \frac{1}{(t/\tau)^{\alpha} + 1} \right) \tag{19}$$

where V_g is the gate voltage applied during the bias stress experiment, the characteristic time τ and the α parameter are related to the dispersive charge injection in the gate insulator (13).

Photocapacitance experiments (14) and direct measurements of V_{fb} (15), measured during bias stress by the space-charge photomodulation technique, confirm the variation in the oxide fixed charge any stressing V_g. Following the charge-trapping theory, experimental data can be explained by a predominant charge injection at low and moderate stress biases while at high stress biases modifications in the density of states in a-Si : H or at semiconductor/insulator interface can also take place.

Recently, very stable a-Si : H TFTs have been reported (16). These devices do not show an appreciable V_{th} shift when high gate voltages are applied for several hours. The active layer of stable TFTs was deposited by the hot-wire deposition technique and contains ~8% of hydrogen, a slightly lower hydrogen content compared to conventionally PECVD deposited a-Si : H. It should be noted that active-layer deposition by the hot-wire technique avoids possible plasma damage of the underlying gate insulator.

These results suggest that instabilities in a-Si : H TFTs can critically depend upon the insulator/semiconductor interface formation, while metastable defect creation in the active layer appears not to be a general mechanism in a-Si : H TFTs.

Future Trends in a-Si : H TFTs

The low field-effect mobility of a-Si : H TFTs limits their application to high-definition large-area AMLCDs. Thus, there is an increasing need for high-performance a-Si : H TFTs. In addition, to increase the productivity and lower the cost of AMLCDs, there is a need for high throughput and operation up-time PECVD equipment. This enhancement in a-Si : H

TFT production should be achieved without sacrificing the device electrical performance.

Current research activities in a-Si : H TFTs are driven by the main requirements for higher values of the field-effect mobility and a higher deposition rate, a small parasitic capacitance due to gate/source overlap, and low-resistivity gate line materials.

The μ_{FE} of 0.3 cm^2/V · s to 0.7 cm^2/V · s are actually found in mass production. These values can be increased up to the μ_{FE} obtained for single devices (i.e., ~1.5 cm^2/V · s) to satisfy the requirement for large-size displays with high pixel density. On the other hand, field-effect mobility depends on PECVD process conditions and is limited by material properties. As a consequence, it has been reported that an increase in deposition rate and the need for high throughput result in a smaller field-effect mobility. This problem was very critical in the first-generation equipment based on batch treatment, where deposition rates were around 10 nm/min. The new generation of PECVD equipment, based on single substrate processing, allows the possibility to obtain μ_{FE} as high as 0.4 cm^2/V · s with a deposition rate of 350 cm^2/V · s.

The parasitic capacitance accompanied by gate pulse-off deteriorates the picture quality of AMLCDs, as flicker and afterimage are increased. A reduction in parasitic capacitance can be achieved by using a self-aligned TFT structure as well as reducing the channel length of TFTs. A fully self-aligned TFT has no overlap between gate and source/drain contacts, reducing the parasitic capacitance. This structure can be obtained by using ion-doped a-Si for source and drain regions. In addition, in this case the channel length can be also reduced and thus W can be reduced, keeping a constant W/L ratio. The smaller values of W and L result in a smaller value of the parasitic capacitance. Simulation results show that, with a field-effect mobility around 1 cm^2/V · s, only the fully self-aligned TFT will be applicable for 40 in. displays.

The fabrication of large-size AMLCDs will also require low-resistivity gate metals because of the problems of gate line delay. Typical gate metals (MoTa alloy, chromium, and α-tantalium) show too high a resistivity (~20 $\mu\Omega \cdot$ cm) for future applications. Al and Al alloy are now considered as low-resistivity gate materials, although Al can cause many process problems at relatively low process temperatures. These problems can be overcome by anodizing the Al gate or capping the Al contact with another metal.

POLYCRYSTALLINE SILICON THIN FILM TRANSISTORS

Since the early 1980s, polysilicon has attracted considerable attention for TFT application, due to its higher carrier mobility compared to a-Si. In particular, polysilicon technology is very attractive for future AMLCDs, since polysilicon TFTs can be applied not only as switching elements of the active matrix but also for the integrated driving circuitry. In fact, in contrast to a-Si technology, both n- and p-channel transistors can be fabricated, allowing CMOS circuits. Field-effect mobilities in n- and p-channel polysilicon TFTs greater than 100 cm^2/V · s have been reported, enabling a successful integration of row and column drive circuits on the active plate (17). These performances have been achieved through a dramatic improvement in polysilicon properties, obtained by a continuous evolution of the formation process of the polysilicon active layer.

In spite of the various techniques used for the polysilicon active-layer formation, a rather conservative approach to the TFT structure has been adopted over the last decade. In fact, the most widely used polysilicon TFT structure closely resembles the silicon-island polysilicon gate process employed in SOI devices, where self-aligned source and drain contacts are formed by ion implantation (see Fig. 1).

The simplest fabrication process usually requires only four masks for single-device definition. First the active layer (with a thickness between 50 nm and 100 nm) is deposited, crystallized (in the following the two main crystallization techniques will be discussed) and patterned into islands (first mask). Subsequently, a gate oxide is deposited to a thickness of 100 nm to 150 nm. Different deposition techniques have been employed to deposit the SiO_2 layer, including atmospheric pressure CVD from SiH_4 and O_2 at T = 400°C to 450°C, PECVD from He-diluted SiH_4 and N_2O, distributed electron cyclotron resonance (DECR) PECVD from SiH_4 and O_2, remote PECVD (RPECVD) from SiH_4 and O_2, and PECVD from tetraethylorthosilicate (TEOS). The polysilicon gate electrode is then deposited and patterned (second mask). Ion implantation of the source, drain, and polysilicon gate is then performed, followed by thermal annealing for doping activation. Next, deposition of the SiO_2 passivation layer (300 nm to 500 nm thick) and contact opening, via holes, are performed (third mask). Finally, Al contacts are deposited and patterned (fourth mask), followed by forming gas (N_2 + 5% H_2 gas mixture) annealing. Normally, the completed devices are subjected to a post-hydrogenation treatment, performed in a hydrogen plasma, to further passivate the Si dangling bonds.

Polysilicon Active-Layer Formation

The main technological effort has been devoted to the optimization of the properties of the polysilicon active layer, and the three main techniques applied to the polysilicon TFT process will be now discussed: low-pressure chemical vapor deposition (LPCVD), solid-phase crystallization (SPC) of a-Si, and excimer-laser crystallization (ELC) of a-Si.

Deposited Polysilicon. The first studies on polysilicon TFTs were based on the use of polysilicon active layers deposited by LPCVD from silane gas. Typical deposition parameters are silane pressure p = 10 Pa to 20 Pa; deposition temperature T_d = 580°C to 630°C; and growth rate 10 nm/min to 5 nm/min. In Fig. 9 a cross-sectional view of a film deposited at T_d = 630°C and p = 13 Pa is presented. As can be seen, the crystallites have a V appearance at the substrate interface and form a mean angle with the normal of 15° (18). The crystallites have, for these deposition conditions, a preferential ⟨110⟩ orientation (18) and contain a high density of thin laminar ⟨111⟩ microtwins (18). As a result of this structure, the thicker the film the larger will be the grain size at the top surface, where the channel is formed in a TFT. Consequently, the polysilicon TFTs show improved performance by increasing the active-layer thickness. On the other hand, the off current is also degraded by the thickness increase, limiting the benefits of this approach. The field-effect mobility values for n-channel TFTs with the deposited polysilicon and active-

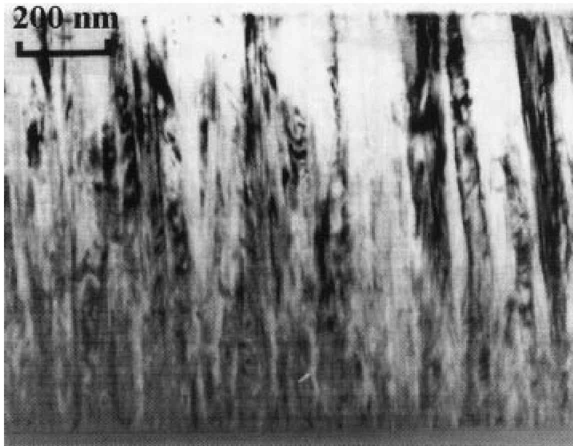

Figure 9. Cross-sectional view of a polysilicon film deposited by LPCVD at 630°C and with a silane pressure of 13 Pa (courtesy of J. Stoemenos).

layer thickness below 1 μm are around 5 $cm^2/V \cdot s$ to 10 $cm^2/V \cdot s$.

This is due to the high density of silicon dangling bonds and distorted bonds associated with structural defects such as incoherent microtwins that induce localized states in the band gap. In general, the polysilicon DOS is spatially nonuniform and, therefore, it is rather difficult to be determined precisely from transport properties. However, it has been shown that the characteristics of polysilicon TFTs can be adequately described by assuming a uniform effective DOS (19) and, therefore, reconstructing the problem to that already discussed for the field-effect analysis in amorphous semiconductor TFTs. The measurement of the DOS is an essential tool for material characterization and process control. The effective DOS can be determined by field-effect analysis of the transfer characteristics at fixed temperature or from the temperature dependence of the field-effect or, alternatively, by deep-level transient spectroscopy (DLTS) measurements. By combining the measurements on both n- and p-channel TFTs a continuous and U-shaped DOS has been determined, as shown in Fig. 10 (20). The DOS is reduced by increasing the active-layer thickness, in agreement with the structural properties of LPCVD-deposited polysilicon, and by plasma hydrogenation, due to the passivation of silicon dangling bonds.

Significant improvement in the grain size can be achieved by reducing the deposition pressure (0.1 Pa to 1 Pa) (18). However, the presence of large grains (up to 0.5 μm) is accompanied by a considerable surface roughness, which has been demonstrated to degrade carrier mobility as well as electrical stability. Although this work (18) has considerably increased the understanding of the grain growth mechanism, the film roughness has limited its application.

Solid-Phase Crystallization of a-Si. A remarkable improvement in polysilicon TFTs performance was achieved by the introduction of polysilicon active layers obtained by SPC of a-Si films, deposited by LPCVD (21). In fact, typical values of the field-effect mobility in n-channel TFTs using optimized SPC films were reported in the range of 30 $cm^2/V \cdot s$ to 40 $cm^2/V \cdot s$ (21).

The a-Si films, deposited by LPCVD at temperatures below 600°C from silane, can be converted into polysilicon by prolonged (10 h to 100 h) thermal annealing at temperatures between 530° and 600°C (22). The SPC takes place by nucleation of crystalline clusters that grow spontaneously when a critical size is reached. The growth progresses by displacement of atoms from the amorphous phase to the crystalline phase. The crystallization can be described by the Avrami–Johnson–Mehl equation (23):

$$c(t) = 1 - \exp[-(t - t_0)3/t_c^3] \tag{20}$$

where $c(t)$ is the crystalline fraction, t_0 is the so-called incubation time, that is, the time required for the formation of the first crystallites with a critical size, and t_c is the characteristic crystallization time. The grain size is in the range of 0.2 μm to 1 μm, much larger than that in deposited polysilicon films, and depends on both annealing temperature and deposition temperature (22). It has been also shown that field-effect mobilty in TFTs increases as the grain size increases (21). Further grain-size increase can be obtained by using a-Si deposited from disilane (24). For a-Si deposited at 460°C to 480°C from disilane and annealed for 65 h at 580°C to 600°C grain sizes up to 3 μm to 5 μm have been obtained (24). This is related to the formation of a few nuclei in a-Si, so that they can grow larger before impinging on their neighbors. A disadvantage of the SPC process of a-Si deposited from disilane is represented by the much longer incubation time and characteristic crystallization time compared to those for a-Si deposited from silane (24).

The grains resulting from the SPC process are generally elliptical in shape (see Fig. 11) and present a high density of microtwins. The generation of microtwins allows fast incorporation of the atoms in the crystal lattice during the SPC process, resulting in a fast reduction of the free energy of the

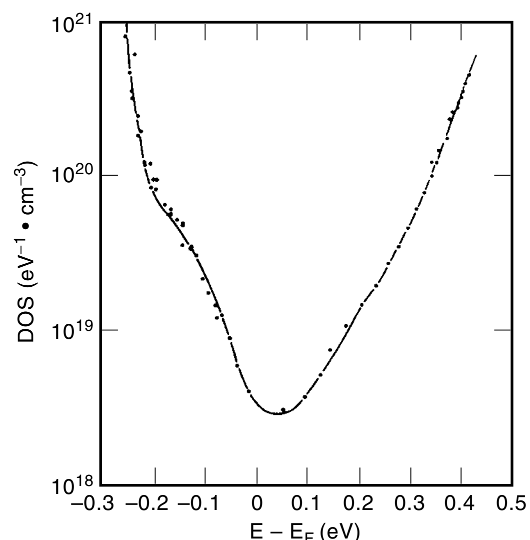

Figure 10. Polysilicon density of states in the forbidden gap deduced from the field-effect conductance of a TFT employing LPCVD-deposited polysilicon, 600 nm thick, as the active layer. The energy is referred to the Fermi-level position at flat-band conditions. Data for $E - E_F > 0$ and $E - E_F < 0$ were obtained by the field-effect method from n-channel and p-channel devices, respectively.

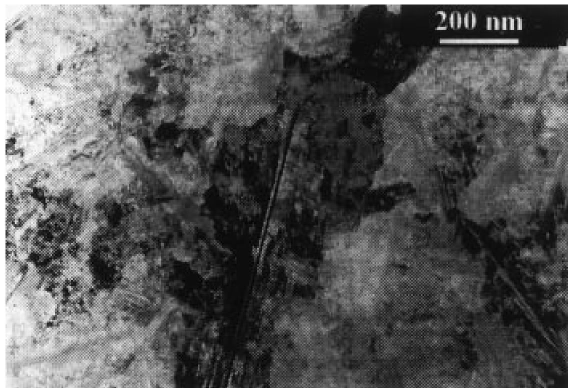

Figure 11. Transmission electron microscope (TEM) plane view of SPC polysilicon annealed at 600°C (courtesy of J. Stoemenos).

system by creating large and highly twinned grains. On the other hand, the presence of first-order twins (electrically inactive) is related to other defects, such as incoherent steps or second- and higher-order twins that are electrically active. This implies that a high density of localized states is expected not only at the grain boundaries but also within the grain. This explains how, even in large-grain (up to 5 μm) polysilicon TFTs, the electron field-effect mobility is limited to values of 40 $cm^2/V \cdot s$ to 70 $cm^2/V \cdot s$.

In Fig. 12 the transfer characteristics of polysilicon TFTs employing SPC material are shown. The device characteristic improvement of SPC polysilicon TFTs, if compared to LPCVD-deposited polysilicon TFTs, is related to a sensible reduction of the DOS, shown in Fig. 13, if compared to the data shown in Fig. 10. A further reduction of the DOS, especially in the so-called deep states associated with silicon dangling bonds, can be achieved by plasma hydrogenation (see Fig. 13).

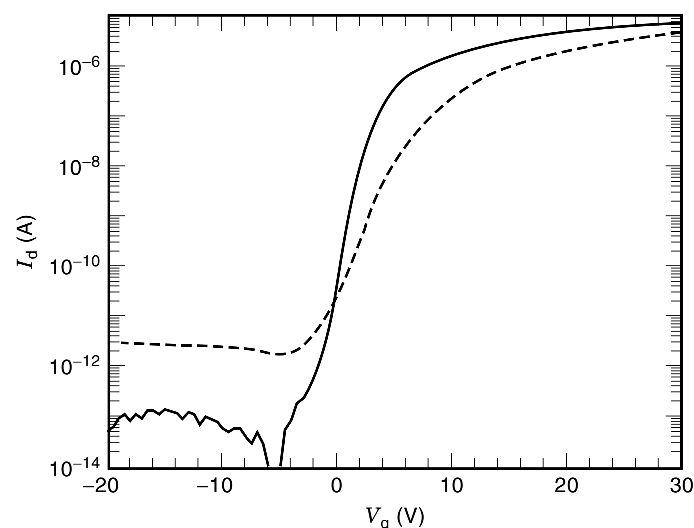

Figure 12. Transfer characteristics of TFTs using an SPC polysilicon active layer, deposited at 480°C and annealed at 580°C for 65 h before (dashed line) and after hydrogenation (solid line). From the linear plot threshold voltages of 11.5 V and 4 V were evaluated for nonhydrogenated and hydrogenated TFTs, respectively, while the value of field-effect mobility was found to be 50 $cm^2/V \cdot s$ for both cases.

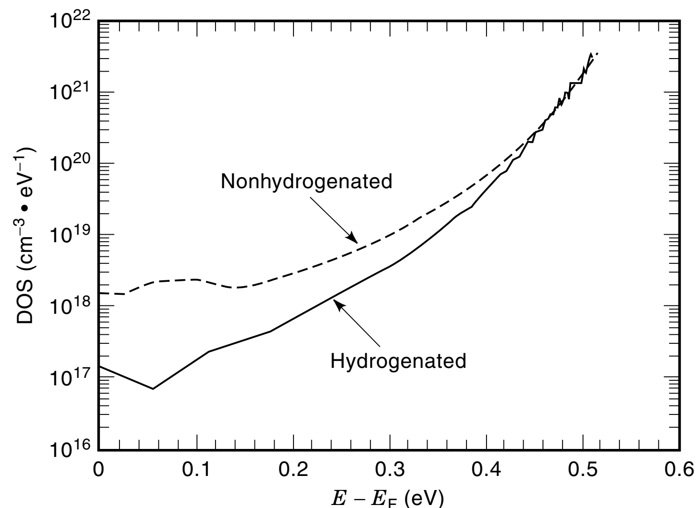

Figure 13. Density of states in the upper half of the polysilicon gap, deduced from the transfer characteristics shown in Fig. 5, before (dashed line) and after hydrogenation (solid line).

Excimer Laser Crystallization of a-Si. Further improvement in the polysilicon TFTs performance has been obtained by the introduction of ELC polysilicon active layers leading to electron field-effect mobilities greater than 100 $cm^2/V \cdot s$ (25,26). Excimer lasers emit in the UV region (output wavelengths 193 nm, 248 nm, and 308 nm for ArF, KrF, and XeCl gas mixtures, respectively) with a short pulse duration (from 10 ns to 30 ns). The combination in Si of strong optical absorption of the UV light ($\alpha > 10^6$ cm^{-1}) and small heat diffusion length during the laser pulse (~100 nm) implies that high temperatures can be developed in the Si surface region, causing melting without appreciable heating (<400°C) of the substrate. This makes the ELC process compatible with glass substrates, one of the major advantages of this technique. Another advantage is that the polysilicon obtained has good crystallinity (see Fig. 14) with very few in-grain defects due to the melt-regrowth process.

Depending upon the laser energy density, different transformations can occur. As the energy density is increased above the energy required to melt the surface of the Si film the amorphous layer undergoes partial melting. The resulting structure consists roughly of two layers: an upper, large-grained layer (whose thickness is related to the primary melt induced by the laser) and a lower, fine-grained layer (related to explosive crystallization) (27). As the energy density is increased the grain size increases (see Fig. 14), reaching a maximum when the Si film is almost totally melted and only few crystalline clusters, sparsely distributed, remain unmelted. When this condition occurs the grains grow laterally around the seeds, until they impinge on each other and until a grain size in excess of 1 μm can be reached [see Fig. 14(c)]. This particular condition is often referred to as superlateral growth (SLG) (28). At higher energy densities the film completely melts and substantial undercooling of the liquid occurs before solidification via homogeneous nucleation and growth can take place, resulting in a small grain structure (28).

Since in polysilicon TFTs electron field-effect mobility is found to increase with increasing grain size it is obvious that

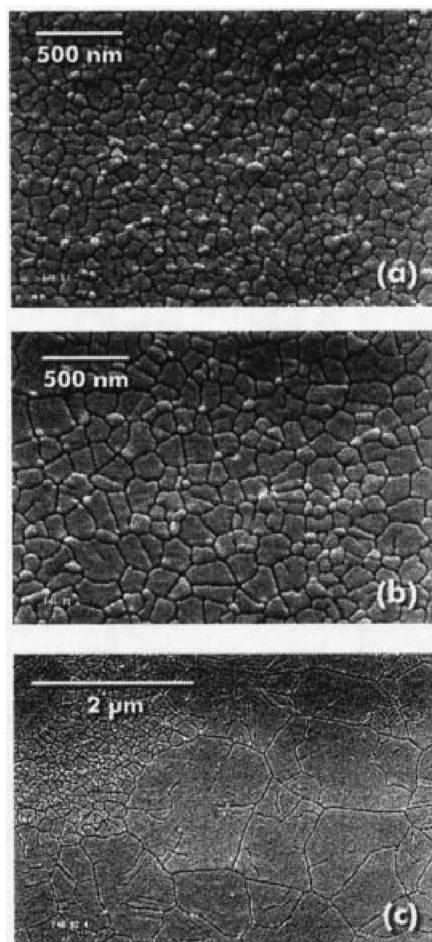

Figure 14. Scanning electron microscope (SEM) views of Secco etched 80 nm thick polysilicon films for different excimer-laser irradiation conditions: (a) 360 mJ/cm², (b) 460 mJ/cm², and (c) 520 mJ/cm². During laser irradiation the substrate temperature was kept at 340°C.

the most attractive regime is represented by the SLG. In fact, excellent performance in TFTs employing such material can be obtained, as shown in Fig. 15, with electron-field effect mobilities in the 300 cm²/V · s to 400 cm²/V · s range (29). However, due to its peculiar mechanism, the SLG regime corresponds to a narrow processing window, and large nonuniformities in the grain size distribution and, consequently, in the device performance are observed. In fact, when unmelted crystalline clusters are sufficiently separated, homogeneous nucleation will be triggered between the grains leading to a situation depicted in Fig. 14(c) with a mixture of very large grains and small grains.

Several approaches to control the lateral solidification by inducing lateral thermal gradients (30) or by sequential lateral solidification (31) have been recently reported. These techniques, although giving further insight on the SLG process, are still far from representing practical solutions for large-area fabrication.

Another very promising approach is the combined use of SPC and ELC techniques (32). When very large and highly defected grains obtained by SPC are partially melted by excimer laser irradiation, the bottom unmelted layer will act as

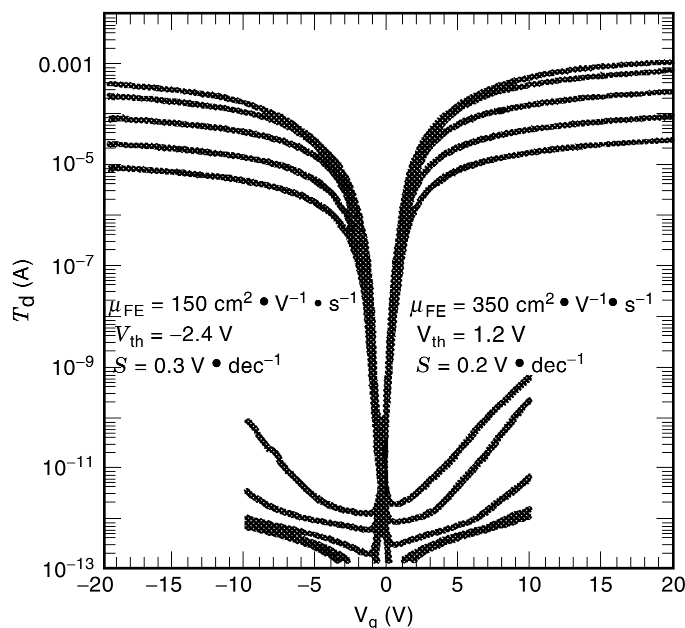

Figure 15. Transfer characteristics of both *n*- and *p*-channel TFTs fabricated on polysilicon film obtained by ELC in the SLG regime (*S* is the subthreshold slope).

seed during the regrowth process. Most of the in-grain defects are eliminated in the melted region by the melt-regrowth process, as shown in Fig. 16, while the grain size remains unaffected. In this way large grains with good crystallinity, extending from the free surface down to the melt depth, can be obtained, as shown in Fig. 16, combining the beneficial aspects of the two techniques. Note also that, since in field-effect devices the channel region is confined within a few nanometers beneath the insulator/semiconductor interface, the two-step annealing process appears to be a very robust process for TFT fabrication. In fact, as long as the melt depth is larger than a few nanometers and smaller than the film thickness, the top surface structure and defect density of the polysilicon film should be the same and therefore insensitive to pulse-to-pulse fluctuations or beam nonuniformities. This allows a large process window for the excimer-laser crystallization process, as demonstrated by the very uniform electrical characteristics shown by TFTs fabricated according to this technique (32).

Some Relevant Electrical Characteristics of Polysilicon TFTs

When using polysilicon TFTs as switching elements, a high on/off ratio as well as a low off current are required, while for

Figure 16. Cross-sectional view of a 160 nm thick polysilicon film sequentially annealed by SPC at 600°C for 12 h and subsequently by ELC at 350 mJ/cm². It is evident that in the upper part of the film (where the primary melt induced by the laser irradiation occurs) a much lower defect density is present (courtesy of J. Stoemenos).

circuit application there is strong demand for high field-effect mobility, high stability, and low-noise devices. We have already discussed in the preceding section how material properties can influence the device characteristics as well as the technological aspects to achieve high performance. As previously anticipated, the electrical characteristics can be analyzed in terms of an effective DOS, thus leading to similar expressions for the current–voltage relationships as deduced in the case of a-Si : H TFTs. Some specific aspects of the electrical characteristics of the polysilicon TFTs will be presented in this section. The experimental results that will be shown are relative to TFTs made at Thomson-CSF, Labretoire Central de Recherches (Orsay) where SPC polysilicon was used as the active layer.

Leakage Current. When polysilicon TFTs are used as switching elements in active matrices, the off current has to be low, since it limits the time the video information can remain on a pixel before refreshing. The off current (commonly called "leakage current" in polysilicon TFTs) depends on the generation–recombination (GR) mechanisms occurring in the depletion region at the drain junction. Figure 17 shows the drain current at negative V_g (off regime, for n-channel TFTs) for different source/drain voltages. As can be seen, at low V_{ds} the off current is independent of V_g and increases superlinearly with V_{ds}, becoming sensitive at high V_{ds}, to V_g. At low V_{ds} the leakage current is dominated by thermal generation occurring in the depletion layer close to the drain. Since the gate voltage modulates the depletion volume only in a region extending 10 nm to 20 nm from the insulator/semiconductor interface, the off current is almost constant with V_g for thick (>100 nm) active-layer devices, as shown in Fig. 17. The off current decreases with decreasing V_g for thin (<100 nm) active-layer devices. Since thermal generation occurs over the entire depletion volume, thin active layers minimize the leakage current due to thermal emission. At high V_{ds}, high electric fields are present at the drain junction, and field-enhanced generation mechanisms dominate the leakage current. Several mechanisms have been proposed, including field-enhanced thermal emission (Frenkel–Poole emission), trap-assisted tunneling, thermionic field emission (phonon-assisted tunneling) and band-to-band tunneling. However, strong evidence that the off current in polysilicon TFTs is dominated by the phonon-assisted tunneling mechanism has been reported (33,34). This process includes, in the case of electron excitation, the thermal emission from the Fermi level to an empty localized state at higher energy followed by tunneling from the localized state to the conduction band.

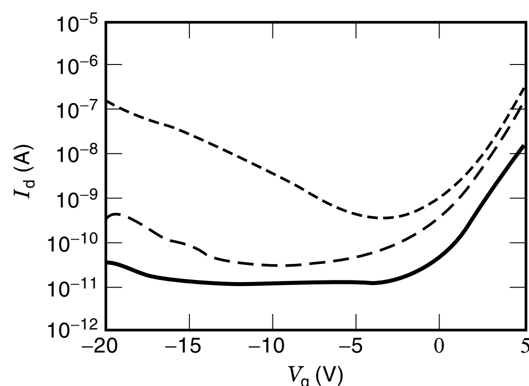

Figure 17. Drain current in the off regime for n-channel TFT, employing a 100 nm thick SPC polysilicon active layer, for different source/drain voltages [V_{ds} = 0.1 V (solid line), V_{ds} = 1 V (dashed line), V_{ds} = 10 V (dotted line)]. At low V_{ds} the off current is V_g-independent but becomes sensitive to V_g at high V_{ds}.

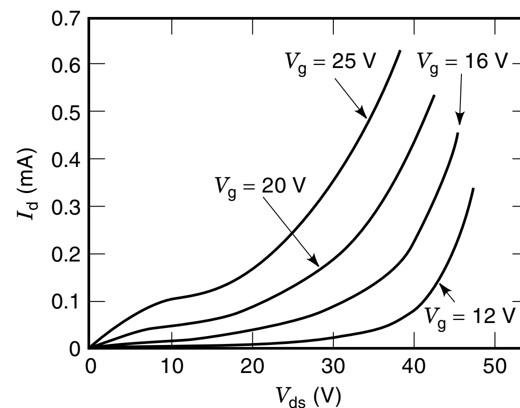

Figure 18. Output characteristics, measured at different V_g, for a SPC polysilicon TFT with L = 10 μm. It is evident, for high V_{ds}, that the drain-current increase (kink effect) is induced by impact ionization and enhanced by the parasitic bipolar transistor (PBT) action.

More recently, it has been shown by refined two-dimensional numerical simulations (34) that band-to-band tunneling is predominant at low temperatures (<200 K) while around room temperature Frenkel–Poole emission, phonon assisted tunneling, and band-to-band tunneling all play a role with phonon-assisted tunneling and Frenkel–Poole emission predominant at low electric fields and band-to-band tunneling at high electric fields. At higher temperatures (>300 K), phonon-assisted tunneling and Frenkel–Poole mechanisms dominate the off current.

Kink Effect. The output characteristics of polysilicon TFTs show, at high V_{ds}, an anomalous current increase, often called the kink effect (35) in analogy with SOI devices (36), as shown in Fig. 18. This effect results in an increase of the output conductance and therefore increases, in digital circuits, the power dissipation and slightly degrades the switching characteristics. In analog circuit applications, the kink effect reduces the maximum attainable gain as well as the common mode rejection ratio.

Two-dimensional numerical simulations have been shown to be particularly useful in the analysis of the kink effect in polysilicon TFTs (37). In particular, kink effect is originated by impact ionization at the drain end of the channel, where the electric field is larger. Indeed, when polysilicon TFTs are biased in the saturation region at large drain voltages, the electric field at the drain end is rather large, and generation of electron–hole pairs by impact ionization occurs. In addition, the kink effect is also enhanced by a parasitic bipolar transistors (PBT) action (37), similar to that in SOI devices. In fact, impact-ionization-generated holes are injected into the floating body (base), forcing further electron injection from the source (emitter), and then are collected by the drain (collector). This added drain current augments the impact

ionization, which in turn drives the floating body harder, thereby causing a regenerative action leading to a premature breakdown. The presence of the PBT effect can be clearly evidenced by the potential barrier lowering at the source junction, as shown in Fig. 19, induced by the impact-ionization-generated holes flowing towards the source region. Also, from the numerical analysis, the PBT action is strongly influenced by the recombination kinetics, which in turn is controlled by the gap state density and capture cross sections (37). In fact, as holes flow towards the source, they experience a recombination process via the energetically distributed gap states. The higher the recombination rate (i.e., high density of states or capture cross sections) the lower the hole concentration at the source.

Hot-Carrier Effects. Since supply voltages applied to circuits employing polysilicon TFTs tend to be relatively high (10 V to 30 V), the presence of high electric fields can induce hot-carrier effects (HCE). The HCE in polysilicon TFTs have been recently investigated, both in n-channel (38,39) and p-channel devices (40), and appear to be the predominant mechanism for device degradation. In view of the application of such devices in active matrix LCD driving circuitry or static random-access memory (SRAM), the stability of the electrical characteristics becomes an important issue. Therefore, HCE have been widely investigated in order to determine the long-term reliability of polysilicon TFTs. Indeed, the application of prolonged bias stress in n-channel TFTs, operated at a high source/drain voltage V_{ds} and different gate voltage V_g, can greatly affect the transconductance, g_m, as well as the off current (38). Transconductance degradation is commonly related, in n-channel MOSFETs, to a negative effective oxide charge, controlled by the generation of acceptor-type interface states (38,41). On the other hand, the off current in polysilicon TFTs at high V_{ds}, depends on field-enhanced generation mechanisms. Therefore the off-current reduction (increase) has to be related to a reduction (increase) in the local electric field. The electric field variations, in turn, have to be related to the injected charge into the oxide near the drain region, where the electric field is higher and the carriers can gain enough energy to be injected into the oxide. In particular, in n-channel TFTs the presence of positive charges at the oxide/semiconductor interface will cause an off-current reduction (38), since oxide positive charges partially screen the negative charges on the gate electrode. By analogy, hot-electron injection (negative oxide charge) results in an off-current increase (38).

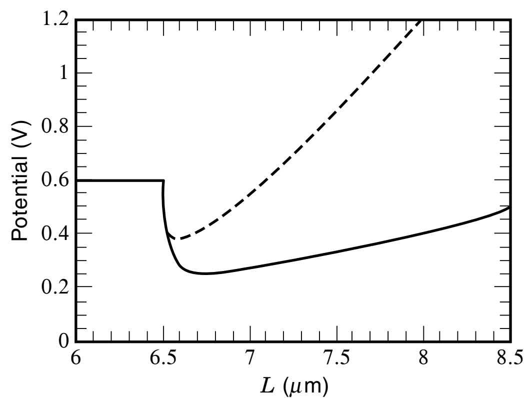

Figure 19. Numerically calculated potential at the source junction, with (dashed line) and without (solid line) impact ionization turn on in the simulations. The potential barrier lowering is induced by the impact-ionization-generated holes flowing towards the source region.

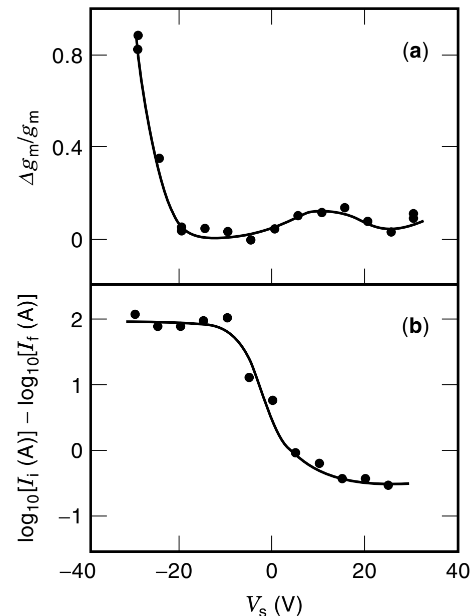

Figure 20. (a) Relative transconductance variation, $\Delta g_m/g_m$, versus stressing gate bias V_s, after stressing for 12 h at fixed source–drain voltage $V_{ds} = 20$ V (each point is relative to a different sample). (b) Variation of ($\log_{10} I_i - \log_{10} I_f$), versus stressing gate bias V_s, where I_i and I_f are the off currents measured at $V_g = -12$ V and $V_{ds} = 10$ V, before and after bias stressing for 12 h at $V_{ds} = 20$ V, respectively (each point is relative to a different sample).

In Figs. 20(a) and 20(b) the relative variation of the transconductance $\Delta g_m/g_m$ (where $\Delta g_m = g_m - g_f$, with g_m and g_f the before and after bias-stress transconductance, respectively) and the variation of the leakage current ΔI_{off} = (log I_i − log I_f) (where I_i and I_f are the off currents measured at V_g = 12 V and V_{ds} = 10 V before and after stress, respectively), after stressing for 12 h at V_{ds} = 20 V, are shown as a function of stressing gate bias V_s. From the data in Fig. 20(a) three regions can be distinguished:

1. $V_s > 0$ V. In this case the transconductance variations resemble those observed in n-channel crystalline Si (c-Si) MOSFETs with a maximum degradation around $V_s = V_{th}$ (41). Furthermore, as V_s increases in this region, the off current increases too, due to electron injection near the drain junction.
2. -20 V $< V_s < 0$ V. In this region the off current is significantly reduced due to hot-hole injection, as already discussed. This off-current reduction is accompanied by only a very small g_m degradation. This suggests that hot-hole injection mainly causes, in this bias regime, the formation of oxide hole traps that are charged positively during the bias stress. It is important to note that for -20 V $< V_s < -10$ V the off current after stress can be reduced up to 2 orders of magnitude without any appreciable degradation in g_m (<5%).
3. $V_s < -20$ V. For these bias-stress conditions a dramatic degradation in g_m occurs, along with off-current reduction. This implies that the formation of oxide hole traps

is now accompanied by the creation of interface states, responsible for the g_m degradation.

Noise Performance. Noise performance is a critical device parameter for analog circuits and it has been recently shown that polysilicon TFTs are characterized by a strong $1/f$ noise (42), commonly observed in c-Si MOSFETs (43,44).

The origin of the low-frequency noise in MOSFETs has been related to either carrier-number fluctuation or carrier-mobility fluctuation. In the carrier-number fluctuation model, based on the McWorther theory (43), the fluctuations of the drain current are induced by fluctuations of the interfacial oxide charge due to the dynamic trapping and detrapping of free carriers into slow oxide traps. In other words, due to the interface charge fluctuations, the flat-band voltage V_{fb} fluctuates and therefore the charge induced in the semiconductor also fluctuates. In the mobility fluctuation model, the fluctuations of the drain current arise from the fluctuations of the carrier mobility possibly through a fluctuation of the scattering cross section. This results in a $1/f$ noise whose intensity is inversely proportional to the total number of carriers in the system. From the shape of the plot of the normalized drain current spectral density, S_I/I_d^2, versus I_d, the noise in polysilicon TFTs can be ascribed to carrier-number fluctuations (42). The experimental data can be fitted to the theoretical expression for the S_I/I_d^2 in the case of carrier number fluctuations (44):

$$\frac{S_I}{I_d^2} = \left(1 + \frac{\alpha \mu_{eff} I_d}{g_m}\right)^2 \left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} \tag{21}$$

where a is a constant, μ_{eff} is the effective carrier mobility in the channel, g_m is the device transconductance (evaluated from the experimental data), and $S_{V_{fb}}$ is the flat-band voltage spectral density. The continuous lines shown in Fig. 21 represent the best fit of the data to Eq. (21) and, as can be easily recognized, a very good agreement is observed. The mean value of the fitting parameter a was found to be 1×10^4 V·s/C to 2×10^4 V·s/C, close to that reported for c-Si MOSFETs (10^4 V·s/C) (44), while the value of the fitting parameter $S_{V_{fb}}$ was around 1.2×10^{-8} V^2/Hz for $L = 20$ μm. The noise in polysilicon TFTs appears much higher than that in c-Si MOSFETs and such a higher noise level could be related to fluctuations of the barrier heights present at the polysilicon grain boundaries or to a higher density of traps in the oxide close to the interface.

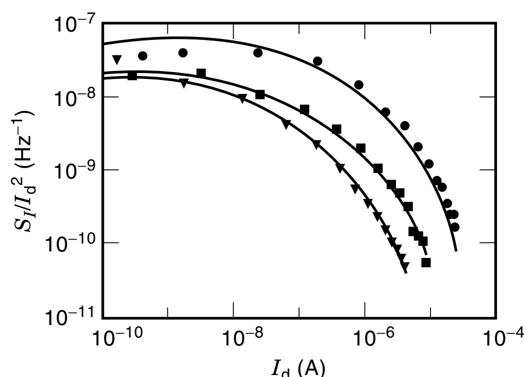

Figure 21. Normalized drain current spectral density, S_I/I_d^2, at 20 Hz versus the mean value of the drain current I_d, for SPC polysilicon TFTs with channel length $L = 5$ μm (circles), $L = 20$ μm (squares), and $L = 40$ μm (inverted triangles). Solid lines are the best fit to Eq. 21.

Future Trends in Polysilicon TFTs

Polysilicon TFT technology has been rapidly evolving over the last decade. Since the introduction of excimer-laser crystallization process, device performance has become attractive for a number of applications in LAE and in particular for the fabrication of integrated-driver AMLCD devices. Although a number of problems still remain to be solved with ELC, including uniformity, surface roughness, pulse-to-pulse reproducibility, and maintenence, there is no doubt that in the near future this technology will be suitably controlled and used in mass-production factories.

Concerning the electrical characteristics, most of the undesired effects, including leakage current, the kink effect, and hot-carrier effects, are related to the presence of high electric fields at the drain junction, mainly determined by the abruptness of the lateral doping profile in the drain. Therefore, the use of self-aligned structure appears inappropriate, and drain-field engineering is required to reduce the previously mentioned undesired effects. To this purpose, several different device configurations have been recently proposed including lightly doped drain (LDD), gate-overlapped LDD (GOLDD), drain-offset, active-gate, multiple-gate, and field-induced drain (FID) structures. Although most of these structures have shown substantial improvements of the electrical characteristics, at present it is not clear which structure is best. A strong effort will be devoted in the near future to optimize physical and geometrical parameters of the structures. Comparative studies of the different solutions will benefit two-dimensional numerical simulations, which have been proved to be a formidable tool in understanding transport properties of polysilicon TFTs.

Circuit application of polysilicon TFTs, which represents the main advantage over the competing a-Si technology, is also rapidly evolving. A variety of polysilicon-TFT-based circuits have been already demonstrated, including integrated drivers for AMLCDs (the current main application), linear image sensors, load devices in SRAMs, control logic in power devices, and operational amplifiers for neural networks. As device characteristics will improve by the introduction of drain-field relief structures, a consistent improvement in the circuit performance and reliability is expected. At that time, polysilicon circuits will easily find applications in different areas, and the local signal amplification and/or processing in smart sensors could be of particular interest. However, for further progress in design architecture, in analogy to c-Si circuit design, the development of refined circuit simulators of polysilicon-TFT-based circuits is of strategic importance. In fact, currently available circuit simulators, such as those developed at Cambridge University or at Virginia University, do not take into account all the different field-enhanced effects, such as the leakage current or kink effect.

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