POWER INTEGRATED CIRCUITS

Power integrated circuits (PICs), also called intelligent power devices (IPDs), are integrated circuit devices capable of withstanding high voltages and/or high currents. In addition they have features associated with mixed-signal integrated circuits, such as thermal detection, short circuit protection and digital interface. Power handling capability is typically greater than 5 W. The first PICs were bipolar voltage regulators and motor drivers. In 1978 Murario (1) described a 4 A bipolar integrated circuit with some of the protection schemes of modern IPDs. The major problem with the device was high thermal dissipation. As power requirements and device complexity have increased, this problem has remained despite packaging advances.

Increased PIC complexity and digital integration requirements have forced a change from bipolar to mostly MOS-based processes. Power IC technology inevitably lags behind conventional mixed-signal technology by about three to six years because of additional difficulty in integrating higher voltage components, the development of power outputs, and economic factors. Power outputs are typically lateral D-well metal oxide semiconductor (LDMOS) devices (2), usually available in a variety of voltage options.

APPLICATIONS FOR POWER ICs

The automotive market is the major consumer of PICs. Here applications range from 0.1 to 30 A in low-side drive (LSD), high-side drive (HSD) and H-bridge configurations (Table 1). PICs have become increasingly popular to implement complete or partial system functions, resulting in improved performance, reduced size, and lower cost. The automotive industry has used power ICs effectively to offer improved safety, engine management systems and, comfort features (3). Figure 1 is a photograph of a 60 V-rated four output (quad) fuel injector driver. The outputs are shown at the top of the chip, which

J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*.

Table 1. Automotive Intelligent Power Device Applications, Current Requirements, Configurations, and the Typical Quantities Found on a Vehicle

Application	Current, A	Configuration[a]	Quantity/ Vehicle
ABS	6–15	HSD	2–6
A/C	6–8	HSD/LSD	1
Fan	2–6	HSD/H	2–6
Fuel Injection	1–4	HSD/LSD	1–8
Headlamps	6	HSD	4–8
Heated mirror	2–4	HSD	2
Ignition	7	LSD	1–8
Instruments	0.1	$\frac{1}{2}$H	2–6
Mid-current lamps	2	HSD/LSD	10–20
Mirrors	0.5–2	H	2–4
Panel lamps	<0.5	HSD/LSD	10–40
Seats	10	H	3–6
Sun roof	10	H	1
Suspension	2–6	$\frac{1}{2}$H	4
Throttle/choke	6	H	1–2
Transmission	2–6	HSD/$\frac{1}{2}$H	2–8
Window heater	15–30	HSD	1–2
Windows	10	H	2–4
Windshield wiper	5–15	H	1–2

[a] H = H-bridge; HSD = High-side drive; LSD = Low-side drive.

is designed for packaging in a 15 pin single-in-line (SIP) power package.

Power ICs are also used in consumer and computer peripheral applications (4–6). Most printers have one or two PICs to drive voltage regulation and motor functions. Figure 2 is a photograph of a multifunctional printer driver IC. The chip has H-bridge and LSD motor control, together with switch-mode regulator controllers. It is controlled through a serial interface by a microcontroller. Numerous other applications include drivers for dc–dc converters, stepper motors, dc motors, solenoid drivers, flat panel display controls, printer head drivers, lamp drivers, and various uses in telecommunications.

POWER IC DESIGN CONSIDERATIONS

Voltage Supply

In automotive electronics the battery and alternator combination is normally the source of all electric power. In normal operation this combination supplies between about 6 V and 16 V. However, most automotive power ICs are designed to operate at or to withstand at least 24 V, which can be present during a double battery jump start. The power source for a PIC is often the automotive battery itself or a regulated voltage source from the battery. Engine management applications typically require operation from 6 V to 25 V. Body electronic applications, for example headlamp drivers, may

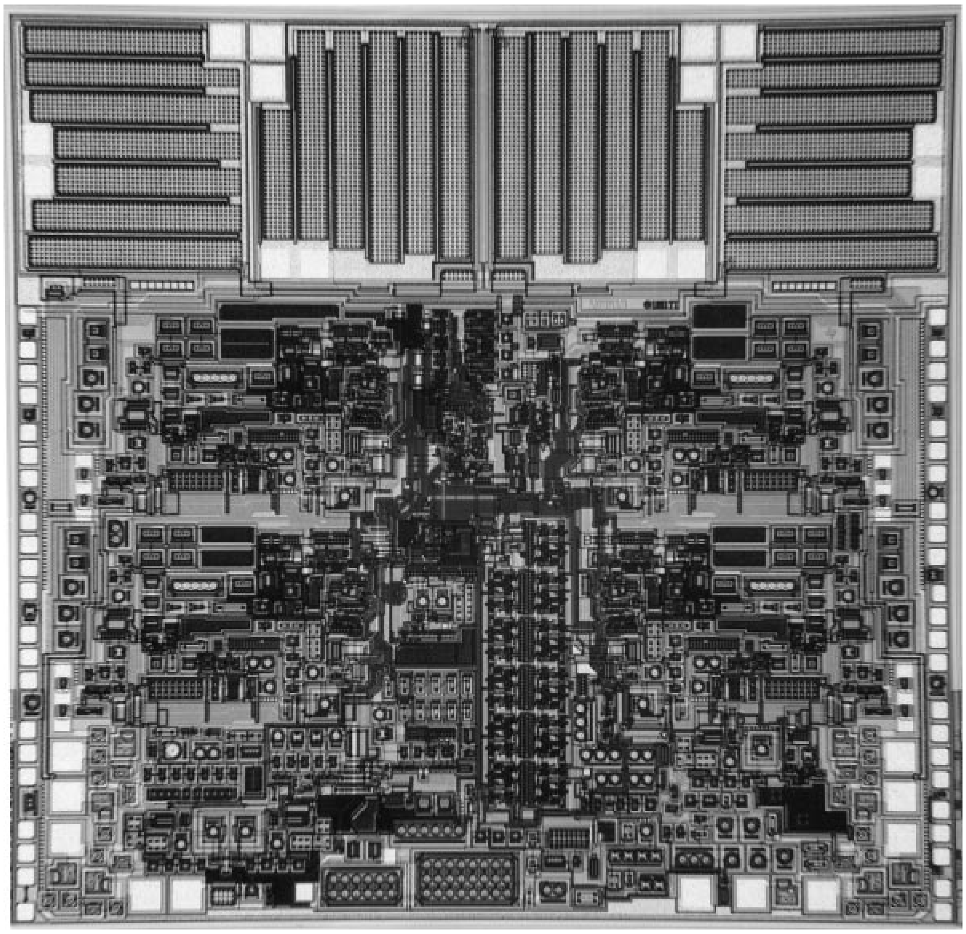

Figure 1. This chip photograph shows a quadruple fuel injector driver. The outputs are 60 V DMOS devices, rated at 1 Ω per output. The four output structures are placed at the top of the chip. The device is packaged in a 15 pin single-in-line power package.

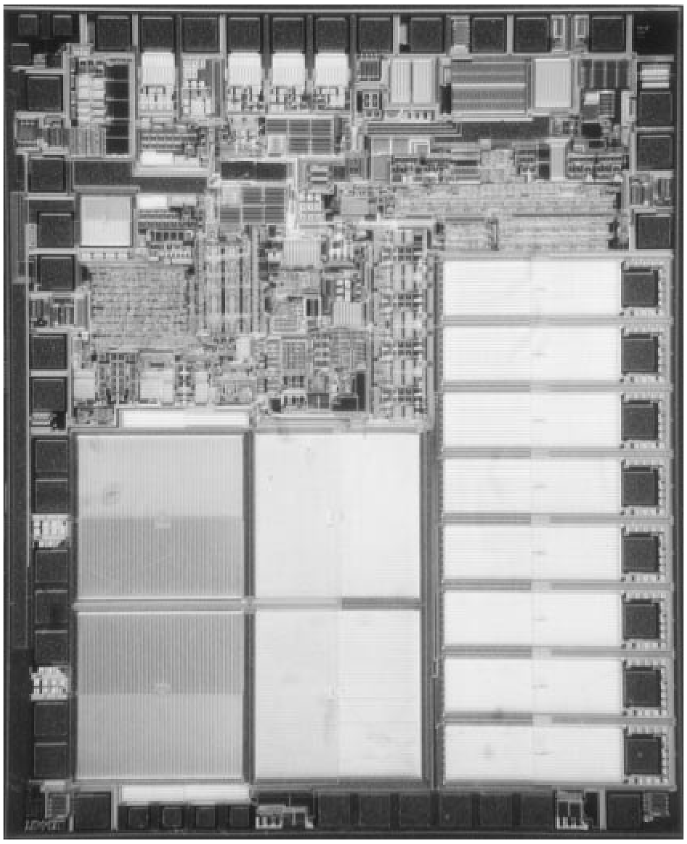

Figure 2. This chip photograph shows a multifunctional printer driver IC. The chip has an H-bridge (lower left), for driving a bidirectional dc motor and eight low-side drives for stepper motor control (right hand edge). Two switch-mode regulator controllers are part of the circuitry in the top portion of the chip.

require only an operating range of approximately 8 V to 16 V. In consumer products and computer peripherals a PIC often sees an input from a rectified, smoothed, but unregulated transformer output. The voltage may range between about 15 V and 60 V.

Output Power Limiting

Thermal constraints are a major consideration in defining power ICs. This is handled by a combination of packaging and high temperature circuit protection. For example, in the case of a shorted or partially shorted load at a power output, chip protection is required, which is often achieved with a dual analog and digital power limiter. An analog current limiter prevents large current spikes. This protects bond wires within the package and limits power to the load. A digital chopping circuit may be used to provide additional protection by limiting the on-time to a low duty cycle in over-current conditions. The duty cycle is chosen to maintain total power below the level which can cause overheating of the chip.

The analog current limit circuit shown in Fig. 3 uses a sense-FET approach to determine the current level in the LDMOS output structure. Sense current, I_s is derived from a small LDMOS structure integrated within the LDMOS output device. The sense-FET principle works by assuming that the source, gate, and drain voltages of the output device and sense-FET are approximately the same. Then both LDMOS devices have equivalent current densities. Hence the current in the sense-FET can be related to the output device area to determine current through the output. Current I_s is typically about one-thousandth the current in the output device. The current I_s causes a voltage V_s to be developed across resistor R_s. With increasing load the voltage across R_s rises. Under excessive load conditions, this may rise to the $V_{be(on)}$ voltage of transistor Q_1. At this point Q_1 turns on, pulling down on the gate voltage V_g. An equilibrium is reached as the gate voltage is reduced to the point where the increased resistance of the LDMOS limits the LDMOS current.

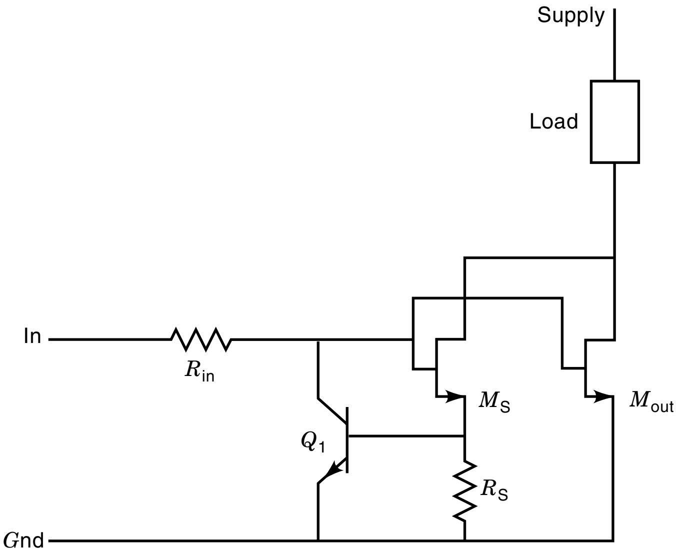

Figure 3. Circuitry for analog current limit, using a sense-FET approach. The load is outside the chip. All other components are integrated into the chip.

This circuit has a negative temperature coefficient (TC) defined by the temperature coefficients of $V_{be(on)}$, which is negative, and R_s, which is typically positive. This combined effect is shown graphically in Fig. 4. The current sense trip point

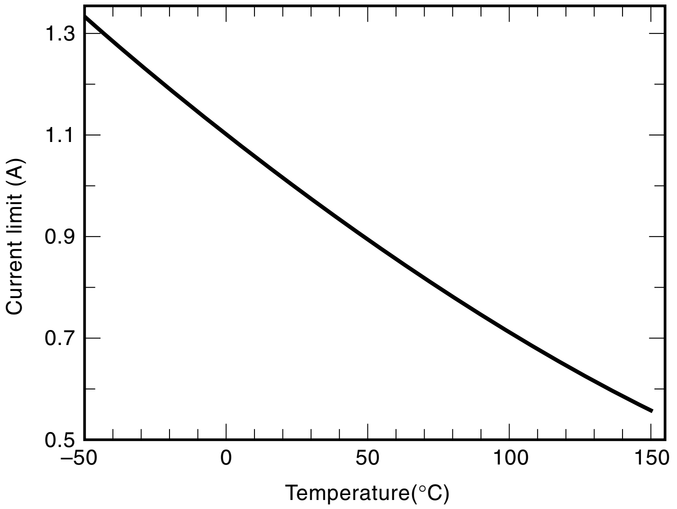

Figure 4. Normal current limit for the circuit shown in Fig. 3. The circuit has a marked negative temperature coefficient defined from the characteristics of Q_1 and R_1. It is seen that current limit with this type of circuit can vary by a factor of 2 between −50° and 150°C.

can be approximated by

$$I_{\text{trip}} = \frac{(R_{\text{dson(sense)}} + R1)}{R_{\text{dson(output)}}} {}^{*} \frac{V_{\text{be}(Q_1)}}{R1}$$

Typically, resistance $R1$ is much smaller than $R_{\text{dson(sense)}}$, thus

$$I_{\text{trip}} \approx \frac{\text{Area}_{\text{(out)}}}{\text{Area}_{\text{(sense)}}} {}^{*} \frac{V_{\text{be}}}{R_1}$$

If required from the thermal analysis, additional digital circuitry may be introduced to place the output in a low-duty cycle (typically 1% to 20%) during over-current conditions.

Voltage Spikes and Supply Transients

Possibly the most severe transient condition experienced by automotive power ICs is load dump (7). This occurs when the battery is disconnected while the alternator is generating. Then the alternator output voltage can rise as high as 120 V (depending on speed and load current). This voltage decays over several hundred milliseconds (Fig. 5). System-level clamping normally holds this below 40 V to 60 V.

Survivability is an obvious requirement of an IC during load-dump transients. In addition, power output transistors are often required to stay off (high impedance) or turn off independently of external logic input signals during load dump. This is straightforward if a high voltage process is used. However, such processes sacrifice IC size, performance, and cost (Fig. 6). Usually circuit techniques are employed to allow lower voltage, higher performance processes to withstand voltages greater than the design limits under dc conditions.

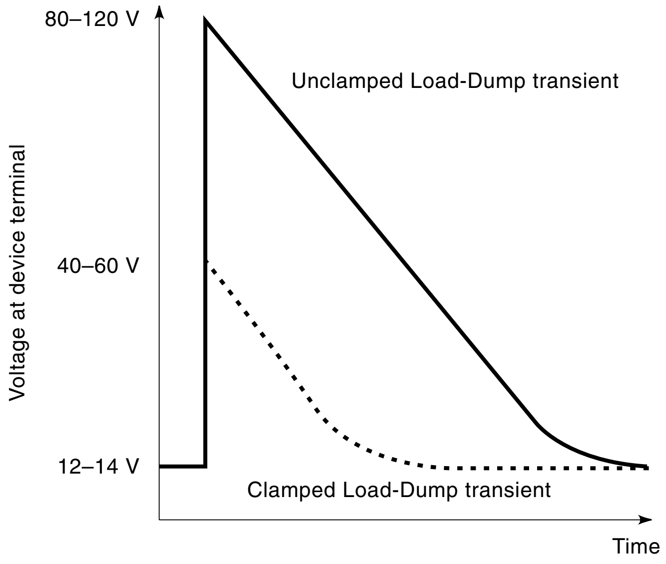

Figure 5. Waveform of the load-dump transient. The transient occurs in an automotive electrical system, when the battery is disconnected while the alternator is generating. Then the output voltage can rise as high as 80 V to 120 V, with voltage decay over several hundred milliseconds. System level clamping normally holds the transient below around 40 V to 60 V.

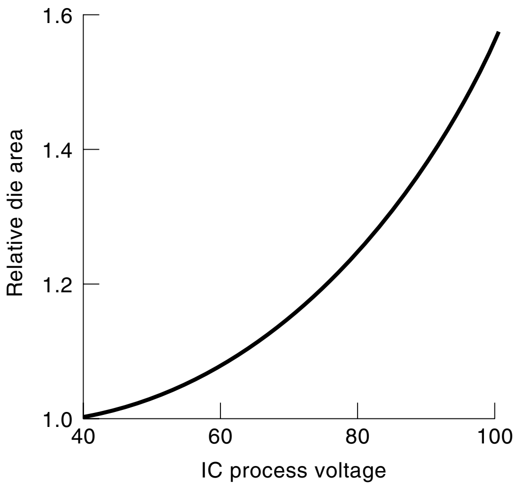

Figure 6. Graph showing the relative chip size of a typical IC, when designed with different voltage processes. This indicates the inefficiency of designing for dc blocking of a high-voltage transient, if that transient is significantly higher in voltage than the dc blocking required.

Safe Operating Areas

Even during supply transients, such as load dump, output transistors must operate within their safe operating area (SOA) (8). Power transistors conducting during a load-dump transient may be forced into regions outside their SOA Curve, resulting in device destruction. If protection is used, such as described in Ref. (9), SOA performance is increased substantially. Inductive loads may improve load-dump performance by delaying the current transient, thereby preventing simultaneous high-current and high-voltage conditions

Intermittent connection between load and PIC output, which is simulated by the “chatter test,” is another important automotive transient condition in which protection is often required. The chatter test requires repeated opening and closing of the circuit at the IC output or in some versions of the test, opening and closing a short circuit across the load while the output is in the “on” condition. Load inductance can cause short-duration positive and negative voltage spikes. Typical failure from this test is caused by device “latch-up,” due to parasitic thyristor activation within the silicon, as described in the layout techniques section of this article.

Electromagnetic Interference

The high currents switched by power ICs can generate electromagnetic interference (EMI). This can manifest itself on nearby entertainment systems. To reduce EMI to acceptable levels, it is often necessary to shape or slow down the switching characteristics of the output. A rapidly switched load has significant high-frequency components, a major cause of EMI. By contrast, slow switching reduces high-frequency power but dissipates more power in the PIC during switching (10). A tradeoff is usually made between acceptable switching power dissipation and radiated interference. In practice switching at the rate of 1 A/μs is normally as slow as required to maintain EMI within acceptable levels (Fig. 7).

High Temperature IC Design

The operating temperature of a chip is defined by the ambient plus any heating effects within the IC. A high ambient is found for applications in automotive engine management, where 125°C maximum module temperature is frequently quoted. Historically 150°C is the maximum allowable chip temperature. This leaves just 25°C for the temperature rise of the chip. Such a restriction causes design and packaging difficulties. Many ink-jet type printers have lower ambient temperature maximums, typically 50° to 75°C, but because of cost restrictions the chip is packaged in a more thermally resistive package, resulting in a higher temperature rise due to chip power. Methods of approaching these thermal problems include low θ_{jc} packaging, low resistance outputs, and higher acceptable junction temperatures.

For operation above 150°C, high temperature design and packaging considerations are necessary. Many high temperature reliability issues are the result of package and bond-related mechanisms. Standard IC gold bonding to aluminum die metal is prone to an intermetallic phenomenon known to cause "purple plague." This may be eliminated by using aluminum bond wires to the aluminum die bond pad. For operation above 150°C, the plastic mold compound may exceed its glass transition temperature T_g, which can cause high-stress reliability issues. This problem may be resolved by using a plastic with T_g greater than about 200°C.

Within the IC, component characteristics change markedly as temperature increases above 150°C. Care must be taken in design to prevent adverse circuit operation. For example, high temperatures can affect the operating thresholds of sensitive analog cells, such as band-gap voltage reference, and analog-to-digital (ADC) circuits. In most cases these effects may be minimized by ensuring that operating bias currents remain greater than about ten times the leakage. Between about 150° and 200°C bipolar devices may offer the best circuit design options because normal MOS device V_t variations can cause devices to become intrinsic at high temperatures (11). Operation above about 225°C is not possible with bipolar devices and requires specialized MOS circuit design techniques (12).

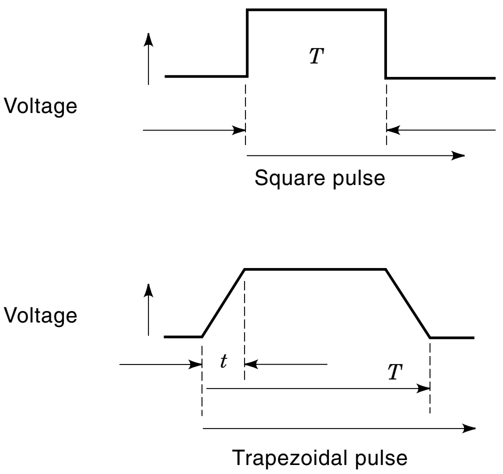

Figure 7. Switching options for EMI suppression. The top signal is a square wave pulse. If a high current is being switched, fast switching can generate substantial electromagnetic interference. To minimize this, the switching edges can be slowed down to form a trapezoidal pulse.

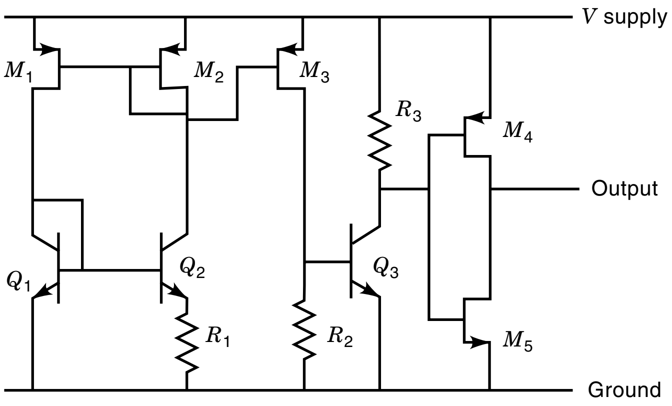

Figure 8. Simplified thermal detection circuit. A defined current is produced in the circuit comprising M_1, M_2, M_3, Q_1, Q_2, and R_1. This current passes through R_2 defining the voltage at the base of Q_3. At high temperatures the voltage at the base of Q_3 reaches the $V_{be(on)}$ threshold, allowing Q_3 to turn on. This threshold point is registered at the output when the inverter comprising M_4 and M_5 switches from 0 V to supply voltage.

Thermal Shutdown

Numerous thermal sensing circuits exist. Most are based on threshold voltage measurement of current through a resistor. The "threshold" voltage is often detected using the negative TC $V_{be(on)}$ of a bipolar transistor. The resistor current is typically generated by a band-gap type current source. The resistor type is matched to the resistor type used for the bandgap, although the values of the resistors may be different. This is to minimize thermal shutdown variation. Figure 8 illustrates a simplified over-temperature sensing configuration. A defined current is produced in the circuit comprising M_1, M_2, M_3, Q_1, Q_2, and R_1. This current passes through R_2 defining the voltage at the base of Q_3. At high temperatures, as the $V_{be(on)}$ of Q_3 reduces, the voltage at the base of Q_3 reaches the $V_{be(on)}$ threshold, allowing Q_3 to turn on. This threshold point is amplified through the circuit and is signaled at the output when the inverter comprising M_4 and M_5 switches from 0 V to supply voltage. The thermal sensing output can be used as an input to logic circuitry for thermally activated shutdown of high-current circuitry.

Electrostatic Discharge (ESD)

An important aspect of power IC design is the robustness to ESD and other transients. A technique used with drain-extended high voltage MOS (DEMOS) devices is the integration of a thyristor (SCR) in the high voltage MOS component (13). The SCR is designed such that it triggers below the breakdown voltage of the MOS, and thus provides protection to the MOS device and minimizes chip dissipation. This technique is described elsewhere in the encyclopedia (9).

LAYOUT TECHNIQUES

LDMOS power outputs operate at a high current density. Hence it is important to minimize voltage drop due to metal

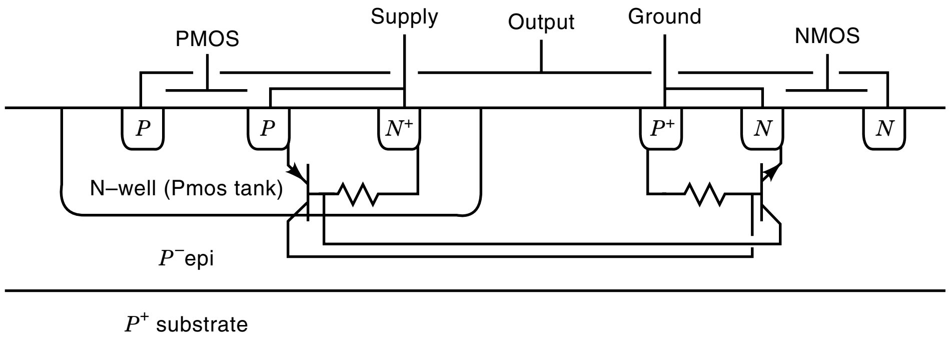

Figure 9. Cross section showing integrated circuit diffusion profile. A parasitic thyristor exists between supply and ground at many places on the chip. This may be triggered by rapid external transient voltages and currents. Layout techniques minimize the susceptibility of these devices to trigger, often by minimizing the resistor values.

bussing. If the metal bussing resistance is not optimized on the die layout, it can add significantly to the R_{dson} of the chip. To counteract this, it is normal practice to use a thick, low R_{sp} top level metal, and design the power outputs close to the bond pads to minimize metal resistance. It is normal practice to isolate DMOS outputs using guard rings to minimize electrical noise from affecting such sensitive analog circuits as ADCs. Particularly sensitive circuitry may have its own additional guard ringing.

Figure 9 shows how a parasitic thyristor can be formed between a supply and ground connection. Latch-up may be nondestructive, causing only loss of data or increased supply currents, or it may be destructive. Chatter-induced latch-up is prevented with appropriate layout techniques. One such technique involves placing guard rings around output structures. Guard rings prevent carriers (electrons or holes) injected by voltage spikes from reaching sensitive areas of the die (Fig. 10). Another latch-up prevention technique is through improved IC grounding. This prevents debiasing which may lead to thyristor turn on.

PACKAGING AND THERMAL MODELING

Packaging is often one of the main limitations of power IC capabilities. Power generated in the IC caused by controlling large loads must be dissipated to prevent the chip from overheating. Packaging technology for a PIC is often innovative, with the use of special plastics and lead frames. Thermal modeling software is used extensively to ensure that the chip (or portion of chip) does not exceed its thermal rating. If a thermal sensing circuit is positioned too close to a power output, it may trip prematurely during short current transients, such as occur at turn on. This is undesirable. Equally, if placed too far from a power output, the thermal sense may not trigger until the output has overheated and become damaged. Thus thermal modeling is considered essential in assisting in the placement of thermal sensing circuitry.

Packaging developments resulting from the heat dissipation requirements of PICs include heat-sinked, surface-mounted, and very low thermal resistance SIP packages. Packaging, such as the 15 pin single-in-line SIP, is available with a θ_{jc} of around 2°C/W, though cost and the requirement for heat sinking are drawbacks to this package type.

In cost-sensitive applications an alternative to SIP packaging is to design the PIC for a lower output resistance than would be required for the application itself. This reduces the power dissipation in the chip. This may be combined with a low-cost, moderate θ_{jc} package, developed specially for the power IC market. Such packages include low θ_{jc} versions of the 20 and 44 pin small outline, 80 and 100 pin chip carrier, and 20 pin dual-in-line packages, which have θ_{jc}s in the range of 10° to 30°C/W. Any increased die area required for the lower output resistance is typically more than offset by the reduced packaging costs over the use of expensive heat-sinked power packages with θ_{jc}s in the range of 2°W to 10°C/W.

Thermal Definitions for Packaging

Heat can be transferred through the mechanisms of conduction, convection, and radiation. Conduction and convection are of highest importance in assessing package thermal performance. Conduction is the primary mechanism of heat transfer within the package itself. This occurs within the chip, typically silicon, through the plastic of the package, and through the lead frame. Heat flow through a material is proportional to the temperature difference across the material and its cross-sectional area, but inversely proportional to material thickness.

In addition to conduction, convection becomes important for transferring heat from the outside of the package through air in contact with the package or lead-frame surface. Pack-

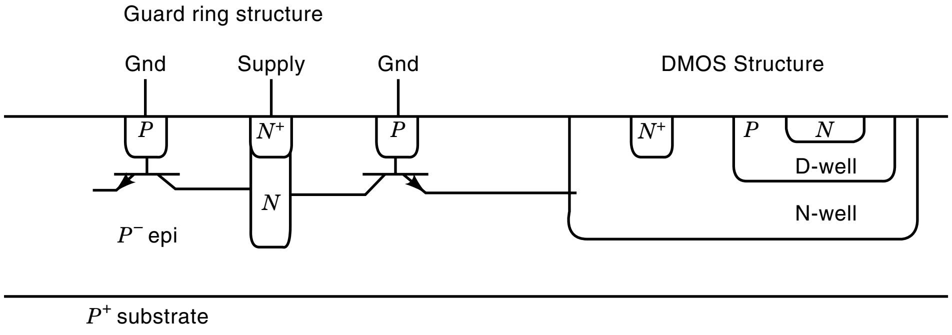

Figure 10. Guard ring structure used for latch-up prevention.

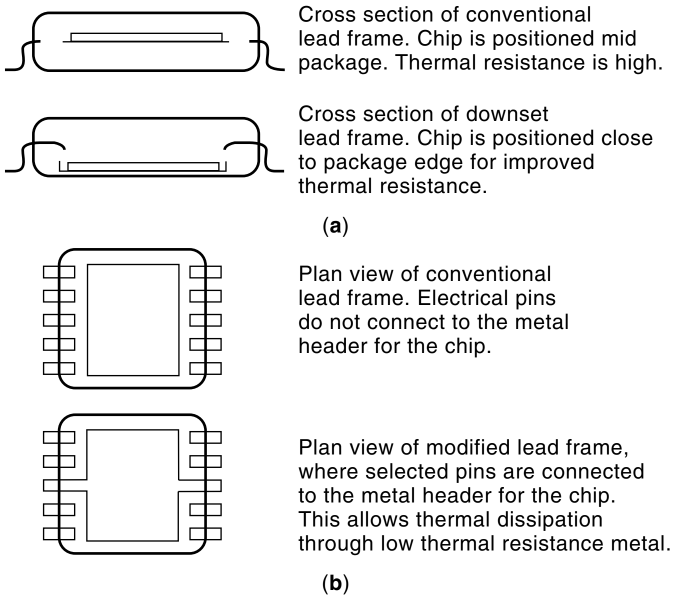

Figure 11. (a) A cross-sectional view of a conventional package and deep-downset lead frame. (b) A plan view of a conventional lead frame and one with pins connected to the lead-frame.

ages, which can get especially hot, are sometimes designed to be placed in a flow of forced air for improved heat loss via convection. Heat transfer by conduction is the most significant method of heat dissipation for most power devices. Typically, power packages are designed with deep-downset headers (onto which the IC is epoxied or soldered), or they have some pins connected to the header to give a low thermal resistance to the ambient conditions. Figure 11 shows conventional, deep-downset and header connected package representations.

When determining the thermal operating range, it is necessary to consider the dc and ac characteristics of the silicon and package. A thermal representation of a packaged die may be developed by analyzing the component stages (Fig. 12). Each section of the device has thermal time constant T_c. T_c of silicon is around 2 ms. The T_c of the lead-frame is about 100 ms, and for a packaged device in free air is around 10 s. Thermal constants between transistor junction and the case (θ_{jc}) or junction to pin (θ_{jp}) are used to represent thermal capabilities when a package is connected to an infinite heat sink. Thermal constants between junction and the air ambient (θ_{ja}) represent thermal capabilities when package heat dissipates only to a still air environment. If a power pulse is shorter than the time constant of the materials, the transient thermal constant is improved (Fig. 13).

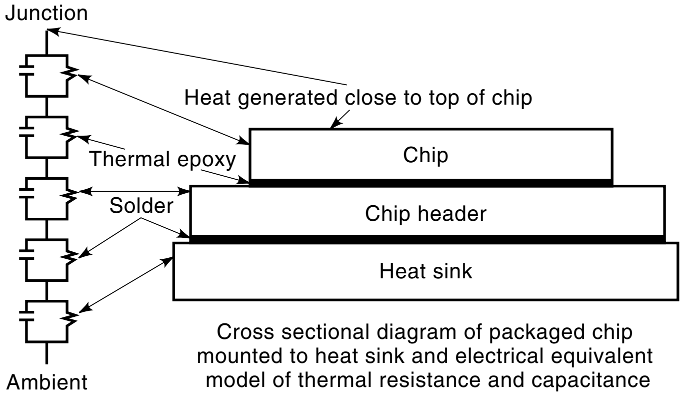

Figure 12. Thermal representation of a package, indicating thermal resistance and thermal capacity of the silicon and package.

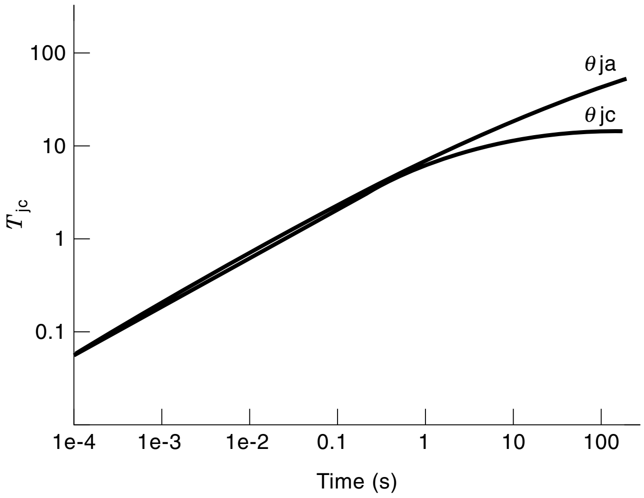

Figure 13. Thermal characteristics between transistor junction to case and transistor junction to ambient. If an applied power pulse is short, the thermal time constant is improved.

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ANDREW MARSHALL
Texas Instruments Incorporated